INTEGRATED CIRCUITS

RF/WIRELESS COMMUNICATIONS
DATA HANDBOOK

Philips
Semiconductors

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RF/WIRELESS COMMUNICATIONS

1995

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DATA HANDBOOK

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RF/Wireless Communications

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Preface

RF/Wireless Communications

Thank you for your interest in Radio Frequency (RF)/Wireless products from Philips Semiconductors. As a leading supplier to the RF/Wireless market, we offer a wide range of discrete and semiconductor RF/Wireless components.

This RF/Wireless Communications handbook includes information on current RF/Wireless integrated circuits from Philips Semiconductors. The products are used in a wide range of RF/Wireless transmitter and receiver electronics. These applications include: Cellular radio, cordless telephones, high performance receivers, two-way communications and LANs.

Selected products from this handbook can be used to build a complete cellular radio. The system diagrams located in the Cellular Section can help you determine which products are best suited for your application.

Philips Semiconductors also offers discrete RF/Wireless components through the Discrete Semiconductor Group. For information on this product line, please contact Philips Semiconductors–DSG at 401/762–3800.

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Ordering Information

LINEAR PRODUCTS PART NUMBERING SYSTEM

Example: NE XXXX N

Package Description:
A = Plastic Leaded Chip Carriers (PLCC)
D = Plastic SO
F = Ceramic Dual In-Line
G = Hermetic Chip Carriers – Leadless
H = Headers
N = Plastic Dual In-Line
P = Pin Grid Array – Hermetic
W = Hermetic Cerpac
Y = Ceramic Square Quad Flat Pack

Device Number

Device Family and Temperature Range Prefix
AU = -40°C to +125°C
NE = 0 to +70°C
SE = -55°C to +125°C
SA = -40°C to +80°C

PHILIPS PRODUCTS PART NUMBERING SYSTEM PREFIXES HE, PC, PN, SA, TD, TE, TS, UM

Example: TD A XXXX P N

Device Family
HEx = CMOS Circuit
PCx = CMOS Circuit
PNx = NMOS Circuit
SAx = Digital Circuit
TDx = Linear Circuit
TEx = Linear Circuit
TSx = Analog Circuit
UAx = Digital Circuit
UMx = Digital Circuit

Package Description:
N = Plastic Dual In-Line
D = Plastic SO
F = Ceramic Dual In-Line
U = Plastic Single In-Line

Package Marking on Part:
P = Plastic Dual In-Line
T = Plastic SO
D = Hermetic Cerdip

Device Number

Operating Temperatures:
A = Temperature range not specified (see data sheet)
B = 0 to +70°C
C = -55°C to +125°C
D = -25°C to +70°C
E = -25°C to +85°C
F = -40°C to +85°C

Product Status

RF/Wireless Communications

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data, and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

The Philips Family of High Performance Front-End Systems

	Description	V_{CC}	I_{CC}	Pins	Pkg	Input Frequency	Gain (Power)	Noise Figure	Input IP_3	1dB Comp.	Input Imped.	Output Imped.	Feature Highlights
Integrated Front-End Systems							f_{RF} = 900MHz						
NE/SA600	LNA + Mixer	4.5-5.5V	13mA/4.2mA* @5V	14	D	LNA 1.2GHz	16/-7.5dB*	2.2dB	-10/+26dBm*	-20dBm	50Ω	50Ω	— LNA Overload Mode — Excellent Noise Figure
						Mixer 1.2GHz	-2.6dB	14dB	+6dBm	-4dBm	50Ω	High	
SA601	LNA + Mixer	2.7-5.5V	7.4mA@3V	20	DK	LNA 1.2GHz	11.5dB	1.6dB	-2dBm	-16dBm	50Ω	50Ω	— Low Voltage — Excellent Noise Figure
						Mixer 1.2GHz	+6dB	10dB	-2dBm	-13dBm	50Ω	High	
SA620	LNA + Mixer + VCO	2.7-5.5V	10.4mA/7.2mA* @3V	20	DK	LNA 1.2GHz	11.5/-7.5dB*	1.6dB	-3/+25dBm*	-16dBm	50Ω	50Ω	— Low Voltage — Excellent Noise Figure — LNA Overload Mode — Internal VCO
						Mixer 1.2GHz	+3dB	9dB	-6dBm	-13dBm	50Ω	High	
UAA2072M	LNA + Image Reject Mixer	4.5-5.3V	31.5mA@5V	20	DK	LNA + IRM 960MHz	26dB	4dB	-15dBm	-24.5dBm	200Ω	High	— Image reject mixer (30dB min. reject) — Tx down-convert mixer
Mixer Systems							f_{RF} = 45MHz						
NE/SA602A	Mixer + Oscillator	4.5-8.0V	2.4mA@6V	8	N, D	500MHz	17dB	5.0dB	-13dBm	-25dBm	1.5kΩ	1.5kΩ	— Excellent Noise Figure — High Gain
NE/SA612A	Mixer + Oscillator	4.5-8.0V	2.4mA@6V	8	N, D	500MHz	17dB	5.0dB	-13dBm	-25dBm	1.5kΩ	1.5kΩ	— Excellent Noise Figure — High Gain
RF Amplifiers							f_{RF} = 900MHz (NE/SA5200), 100MHz (others)						
NE/SA5200	Dual Gain Stage	4.0-9.0V	4.2mA/95µA* @5V (per amplifier)	8	D	DC – 1.2GHz	7.5/-13.5dB* (per amplifier)	3.6dB	-1.8dBm	+3.2dBm	50Ω	50Ω	— DC to 1.2GHz Operation — Power-Down Mode
NE/SA5204A	Wideband Amp	5.0-8.0V	25mA@6V	8	N, D	DC – 350MHz	19dB	6.0dB (50Ω) 4.8dB (75Ω)	-2dBm	+4dBm	50Ω	50Ω	— DC to 350MHz Operation
NE/SA5205A	Wideband Amp	5.0-8.0V	25mA@6V	8	N, D	DC – 550MHz	19dB	6.0dB (50Ω) 4.8dB (75Ω)	-2dBm	+4dBm	50Ω	50Ω	— DC to 550MHz Operation
NE/SA5209	Variable Gain Amp	4.5-7.0V	43mA@5V	16	N, D	DC – 850MHz	25dB (voltage)	9.3dB	+13dBm (output)	-3dBm	1.2kΩ	60Ω	— DC to 850MHz Operation — Gain Control Pin
NE/SA5219	Variable Gain Amp	4.5-7.0V	43mA@5V	16	N, D	DC – 700MHz	25dB (voltage)	9.3dB	+13dBm (output)	-3dBm	1.2kΩ	60Ω	— DC to 700MHz Operation — Gain Control Pin

Temperature Range

NE: 0 to +70°C
SA: -40 to +85°C

Package Descriptions

D Small Outline – 14
Small Outline – 16
Small Outline – 20

DK: Shrink Small Outline Package (SSOP) – 20

N: Dual In-Line Plastic

*Amplifier: Enabled/Disabled

RF/Wireless Communications

RF AMPLIFIER FAMILY OVERVIEW

	NE/SA5200	NE/SA5204A	NE/SA5205A	NE/SA5209	NE/SA5219
Description	**Dual Gain Stage**	**Wideband Amp**	**Wideband Amp**	**Variable Gain Amp**	**Variable Gain Amp**
V_{CC}	4 – 9V	5 – 8V	5 – 8V	4.5 – 7.0V	4.5 – 7.0V
I_{CC}	4.2mA/95 µA*@5V (per amplifier)	25mA @ 6V	25mA @ 6V	43mA @ 5V	43mA @ 5V
Bandwidth (3dB)	DC - 1.2GHz	DC - 350MHz	DC - 550MHz	DC - 850MHz	700MHz
Gain (power)	7.5dB/–13.5dB* (per amplifier)	19dB	19dB	25dB (voltage)	25dB (voltage)
Noise Figure	3.6dB	6.0dB 50 Ω 4.8dB 75 Ω	6.0dB 50 Ω 4.8dB 75 Ω	9.3dB	9.3dB
1dB Compression	+3.2dBm	+4dBm	+4dBm	–3dBm	–3dBm
3rd Order Intercept (input)	–1.8dBm	–2dBm	–2dBm	+13dBm (output)	+13dBm (output)
Input Impedance	50 Ω	50 Ω	50 Ω	1.2k Ω	1.2k Ω
Output Impedance	50 Ω	50 Ω	50 Ω	60 Ω	60 Ω
Package	SO8	DIP8 SO8	DIP8 SO8	DIP16 SO16	DIP16 SO16
Features	+DC to 1.2GHz operation +Power-Down mode	+DC to 350MHz operation	+DC to 550MHz operation	+DC to 850MHz operation +Gain control pin	+DC to 700MHz operation +Gain control pin

*Amplifier: Enabled/Disabled

The Philips Family of High Performance IF Systems

	V_{CC}	I_{CC}	Pins	Package	Input Freq	IF Freq	f_{RF} = 45MHz			RSSI Range	Fast RSSI	Freq Check Pin	IF Filter Match	Output Op Amps	Feature Highlights
							Input Sensitivity	Mixer Gain	Input IP_3						
FM IF															
NE/SA604A	4.5-8V	3.3mA @ 6V	16	D,N	25MHz	25MHz	0.22μV[1]	–	–	90dB	–	–	455kHz	–	– High Sensitivity
NE/SA614A	4.5-8V	3.3mA @ 6V	16	D,N	25MHz	25MHz	0.22μV[1]	–	–	80dB	–	–	455kHz	–	– Wide IF BW
NE/SA624	4.5-8V	3.4mA @ 6V	16	D,N	25MHz	25MHz	0.22μV[1]	–	–	90dB	✓	–	455kHz	–	
Mixer/FM IF															
NE/SA605	4.5-8V	5.7mA @ 6V	20	D,DK,N	500MHz	25MHz	0.22μV	13dB	-10dBm	90dB	–	–	455kHz	–	– High Sensitivity
NE/SA615	4.5-8V	5.7mA @ 6V	20	D,DK,N	500MHz	25MHz	0.22μV	13dB	-10dBm	80dB	–	–	455kHz	–	– High Input Frequency
NE/SA625	4.5-8V	5.8mA @ 6V	20	D,DK,N	500MHz	25MHz	0.22μV	13dB	-10dBm	90dB	✓	–	455kHz	–	
NE/SA627	4.5-8V	5.8mA @ 6V	20	D,DK,N	500MHz	25MHz	0.22μV	13dB	-10dBm	90dB	✓	✓	455kHz	–	– Wide IF BW
Low Voltage Mixer/FM IF															
SA606	2.7-7V	3.5mA @ 3V	20	D,DK,N	150MHz	2MHz	0.31μV	17dB	-9dBm	90dB	–	–	455kHz	Audio Op Amp RSSI Op Amp	– High Sensitivity
SA616	2.7-7V	3.5mA @ 3V	20	D,DK,N	150MHz	2MHz	0.31μV	17dB	-9dBm	80dB	–	–	455kHz	Audio Op Amp RSSI Op Amp	– Low Power
SA607	2.7-7V	3.5mA @ 3V	20	D,DK,N	150MHz	2MHz	0.31μV	17dB	-9dBm	90dB	–	✓	455kHz	Audio Op Amp RSSI Buffered	– Audio/RSSI Output Op Amps
SA617	2.7-7V	3.5mA @ 3V	20	D,DK,N	150MHz	2MHz	0.31μV	17dB	-9dBm	80dB	–	✓	455kHz	Audio Op Amp RSSI Buffered	
SA608	2.7-7V	3.5mA @ 3V	20	D,DK,N	150MHz	2MHz	0.31μV	17dB	-9dBm	90dB	–	✓	455kHz	Audio Buffered RSSI Op Amp	– Power-Down Mode (SA626/636)
SA626	2.7-5.5V	6.5mA @ 3V	20	D,DK	500MHz	25MHz	0.54μV[2]	11dB[2]	-16dBm[2]	90dB	✓	–	10.7MHz	Audio Buffered RSSI Op Amp	
SA636	2.7-5.5V	6.5mA @ 3V	20	D,DK	500MHz	25MHz	0.54μV[2]	11dB[2]	-16dBm[2]	90dB	✓	–	10.7MHz	RSSI Op Amp	
SA676	2.7-5.5V	3.5mA @ 3V	20	D,DK	100MHz	2MHz	0.45μV	17dB	-10dBm	70dB	–	–	455kHz	Audio Op Amp RSSI Op Amp	
Low Voltage Mixer/Digital IF															
SA637	2.7-5.5V	3.5mA @ 3V	20	D,DK	200MHz	2MHz	-117dBm[3] 0.31μV	15dB	-10dBm	90dB	✓	–	455kHz	RSSI Op Amp	

Temperature Ranges
NE: 0 to + 70°C
SA: -40 to + 85°C

Package Descriptions
D: Small Outline - 16
Small Outline - 20
DK: Shrink Small Outline Package (SSOP) - 20
N: Dual In-Line Plastic - 16, 20

IF Filter Match
455kHz = 1.5kΩ
10.7MHz = 330Ω

NOTES:
1. Measured with a Philips NE/SA602A mixer prior to the IF input.
2. Measured at f_{RF} = 240MHz
3. Represents the -3dB Input Limiting point (dBm). Also shown in μV units into a 50Ω matching network.

Frequency Synthesizer Selector Guide

RF/Wireless Communications

The Philips Family of High Performance Frequency Synthesizers

	Vcc	Icc	Pins	Pkg	Max RF/Input Frequency	Channel Spacing	Fractional-N Divider	Auxiliary Synthesizer	Applications
Fractional-N Frequency Synthesizers									
SA7025DK	2.7 to 5.5V	7.5mA@3V	20	SSOP20	1.0GHz (main) 150MHz (aux) 40MHz (aux)	10-5000kHz (main) 40-20,000kHz (aux) 10-5000kHz (aux)	✓	✓	NADC (IS-54), PDC, GSM digital cellular
SA8025DK	2.7 to 5.5V	11mA@3V	20	SSOP20	1.8GHz (main) 150MHz (aux) 40MHz (aux)	10-5000kHz (main) 40-20,000kHz (aux) 10-5000kHz (aux)	✓	✓	PHS digital cordless, PDC digital cellular
UMA1005T	2.9 to 5.5V	5mA@3V	20	SSOP20	30MHz (main) 90MHz (aux) 30MHz (aux)	10-5000kHz (main) 40-20,000kHz (aux) 10-5000kHz (aux)	✓	✓	NADC (IS-54), PDC, GSM digital cellular
Frequency Synthesizers									
UMA 1014T	4.5 to 5.5V	13mA@5V	16	SO16	1.1GHz	5-100kHz			AMPS/TACS cellular, cordless
UMA1015M	2.7 to 5.5V	9.6mA@3V	20	SSOP20	1.1GHz 1.1GHz	8.5-375kHz		✓ (Dual)	CT1/CT1 + cordless AMPS/TACS NMT cellular
UMA1016xT	4.5 to 5.5V	10mA@5V	16	SO16	1.0GHz	100-1000kHz			cordless spread spectrum
UMA1017M	2.7 to 5.5V	8.5mA@3V	20	SSOP20	1200MHz	10-2000kHz			GSM digital cellular, spread spectrum
UMA1018M	2.7 to 5.5V	8.5mA@3V	20	SSOP20	1200MHz (main) 300MHz (aux)	10-2000kHz (main) 10-1000kHz (aux)		✓	GSM digital cellular
UMA1019AM	2.7 to 5.5V	12mA@3V	20	SSOP20	1750 MHz	10-2000kHz			DECT digital cordless, DCS 1800
UMA1020M	2.7 to 5.5V	12mA@3V	20	SSOP20	2400MHz (main) 300MHz (aux)	10-2000kHz (main) 10-2000kHz (aux)		✓	DECT digital cordless, DCS1800

	Vcc	Icc	Pins	Pkg	Max Input Frequency	Max Compare Frequency	Input Sensitivity	Divide Ratio
Prescalers								
SA701N, D	2.7 to 6V	4.5mA@3V	8	DIP, S08	1.1GHz	65kHz/270kHz	-35dBm	128/129, 64/65
SA702N, D	2.7 to 6V	4.5mA@3V	8	DIP, S08	1.1GHz	1000kHz	-35dBm	64/65/72
SA703N, D	2.7 to 6V	4.5mA@3V	8	DIP, S08	1.1GHz	335kHz	-35dBm	128/129/144

RF/Wireless Communications

Baseband Processors

PART TYPE		APPLICATION	V_{DD}	I_{DD}	PACKAGE
PCD5032	ADPCM Codec	DECT	2.7 - 6.0 2.7 - 6.0	7mA Typ. Active 20µA Typ. Stdby	28-Pin SO28 44-Pin QFP
PCD5040	BMC (Burst Mode Controller)	DECT	2.7 - 6.0	15mA Typ. Active	64-Pin QFP
PCD5081	Signal Processor – Mobile	GSM	5.0	— —	80-Pin QFP
PCD5082	Signal Processor – Base	GSM	5.0	— —	160-Pin QFP
PCD5071	Baseband Interface	GSM	5.0	31mA Typ. Rx 7mA Typ. Tx	44-Pin QFP 44-Pin QFP
NE/SA5750	Audio Companding Amplifier	AMPS TACS	5.0	8.4mA Typ. 1.8mA Stdby	24-Pin DIP 28-Pin SOL
NE/SA5751	Audio Filter and Control	AMPS TACS	5.0	2.7mA Typ. 0.9mA Stdby	24-Pin DIP 28-Pin SOL
SA5752	Audio Companding VOX and Amplifier	AMPS TACS	2.7	3.1mA Typ. 125µA Stdby	20-Pin SOL 20-Pin SSOP
SA5753	Audio Filter and Control	AMPS TACS	2.7	2.7mA Typ. 600µA Stdby	20-Pin SOL 20-Pin SSOP
PCF5001	POCSAG decoder	PAGERS	1.5 - 6.0	60µA Typ.	28-Pin Mini-Pack 32-Pin QFP
PCD5003	Advanced POCSAG paging decoder	GSM	1.5 - 6.0	50µA Typ. (ON) 25µA Typ. (OFF)	32-Pin TQFP
UMA1000LT	Data processor for cellular radio	AMPS TACS	3.0 - 5.5	2.5µA Typ.	28-Pin SOL

RF/Wireless Communications

The Philips Family of High Performance Compandors

	Vcc	Icc	Pins	Packages	ALC Voltage	Reference Gain	Unity Down	Power Features	Key	Applications
NE/SA570	6-24V	3.2mA	16	D, F, N	Both Channels	Fixed 1.8V	775mVrms	NO	-Excellent Unity Gain Tracking Error -Excellent THD	High Performance Audio Circuits "Hi-Fi Commercial Quality"
NE/SA571	6-18V	3.2mA	16	D, F, N	Both Channels	Fixed 1.8V	775mVrms	NO	-Excellent Unity Gain Tracking Error -Excellent THD	High Performance Audio Circuits "Hi-Fi Commercial Quality"
NE/SA572	6-22V	6mA	16	D, F, N	Both Channels	Fixed 2.5V	100mVrms	NO	-Independent Attack & Release Time -Good THD -Needs an Ext Summing Op Amp	High Performance Audio Circuits "Hi-Fi Studio Quality"
NE/SA575	3-7V	3-5.5mA*	20	D, DK, N	Right Channels	Vcc/2	100mVrms	NO	-2 Uncommitted On-Chip Op Amps Available -Low Voltage	Consumer Audio Audio Circuits "Commercial Quality"
NE/SA576	2-7V	1-3mA*	14	D, N	Right Channels	Vcc/2	100mVrms	NO	-Low Power -Low External Component Count	Battery Powered Systems "Commercial Quality"
NE/SA577	2-7V	1-2mA*	14	D, N	Right Channels	Vcc/2	10mV to 1V(rms)	NO	-Low Power -Programmable Unity Gain	Battery Powered Systems "Commercial Quality"
NE/SA578	2-7V	1-2mA*	16	D, N	Right	Vcc/2 Channel	10mV to 1V(rms)	YES (170µA)	-Low Power -Programmable Unity Gain -Power Down -Mute Function Summing Capability (DTMF) -600Ω Drive Capability	Battery Powered Systems "Commercial Quality"

NOTE: NE/SA5750/5751 & SA5752/5753are also Excellent Audio Processor Components for High Performance Cordless and Cellular Applications that include the Companding Function

* Icc varies with VCC

Packages include: NE: 0 to +70 C; SA: -40 to +85 C; N: Plastic DIP; D: Plastic SO; F: Cer DIP; DK: SSOP (Shrink Small Outline Package)

Applications include: Cordless Phones, Cellular Phones, Wireless Mics, Modems, Consumer Audio, and Two-way Communications

RF/Wireless Communications

System Standard — Product Selector Guide

● Recommended part-type / system solution
X Alternate solution

PRODUCTS			TARGET SYSTEMS										
Function	Type	Description	Cellular			Cordless					Wireless Data		
			(N)AMPS /(E)TACS	IS-54/ TDMA	GSM	CT0	CT1	SS	DECT	PHS	802.11	CDPD	PAGERS
RF Amplifiers	SA5200	Gain block – 1GHz			X		X	X					
RF Front-End	SA600	LNA/Mixer – 1GHz	X	X				X				X	
	SA601	LNA/Mixer – 1GHz	●	●			●	●				●	
	SA1620	Low voltage GSM RF transceiver			●								
	UAA2072M	Image reject GSM front-end			X								
	UAA2080T	Advanced pager receiver											X
	UAA2082	Advanced pager receiver											●
Synthesizers\ Prescalers	UMA1014T	Synthesizer – BIP – 1GHz	X				X					X	
	UMA1015M	Low-voltage, dual – 1GHz	●				●					●	
	UMA1017M	Low-voltage, single loop – 1GHz			X			X					
	UMA1018M	Low-voltage, low noise – 1GHz			●								
	UMA1019M	Low-voltage, single loop - 2GHz			●				●				
	UMA1020M	Low-voltage, low noise – 2.4GHz							●	X	●		
	UMA1005T	Synthesizer, Fractional-N		X	X								
	SA7025	Low-voltage, Fractional-N – 1GHz		●	X								
	SA8025	Low-voltage, Fractional-N – 2GHz								●	X		
Mixer / IF / Demod	SA605	High perf/wide BW mixer FM/IF	X	X	X			X	X	X	X	X	
	SA606/7/8	Low-voltage, high perf mixer FM/IF	●	●		●	●					●	
	SA626	Low-voltage/Wide BW/fast RSSI						●		●			
	SA636	SA626 with Wideband data output							X		●		
	SA637	SA626 with Digital IF		●									
	SA639	Low-voltage mixer FM/IF w/switch							●		●		
	SA1638	Low-voltage GSM IF transceiver			●								
Transmitter	SA900	I/Q transmit modulator		●									

System Standard Selector Guide (cont.)

RF/Wireless Communications

System Standard — Product Selector Guide

● Recommended part-type / system solution
X Alternate solution

PRODUCTS			TARGET SYSTEMS										
			Cellular			Cordless					Wireless Data		
Function	Type	Description	(N)AMPS /(E)TACS	IS-54/ TDMA	GSM	CT0	CT1	SS	DECT	PHS	802.11	CDPD	PAGERS
Audio Processing	SA5752	Audio processor system – 3V	●									●	
	SA5753	Audio processor system – 3V	●									●	
	NE576/77/78	Compandor	X			●	●						
Data Processing	UMA1000LT	Data processor – 3V	●									●	
	PCD5032	ADPCM – codec							●				
	PCD5040/41	Burst Mode controller							●				
	PCF5081/82	Digital signal processor			●								
	PCD5071	Baseband interface			●								
	PCF5001	POCSAG paging decoder											●
	PCF5003	Advanced POCSAG paging decoder											●
Control	89CE558	Microcontroller with flash memory	X									X	
	P90CL301	Low-voltage 16-bit microcontroller			●				X				
	P80CL51	Low-voltage 8-bit microcontroller				●	X						X
	P80CLxxx	Low-voltage 8-bit microcontroller							●				
	TDA8005	Smart card interface			●								
(IC20)	P83CL580	Microcontroller	●									●	
(IC20)	P83CL781/2	Microcontroller				X	●						X
(IC20)	P83CL410	Microcontroller											X
Misc.	PCA5075*	RF PA controller			●								
	TDA7050	Audio amplifier	●										
	TDA8781	Log amplifier			X								

Section 2
RF Front-Ends and Paging Receivers

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RF/Wireless Communications

The Philips Family of High Performance Front-End Systems

	Description	V_{CC}	I_{CC}	Pins	Pkg	Input Frequency	Gain (Power)	Noise Figure	Input IP_3	1dB Comp.	Input Imped.	Output Imped.	Feature Highlights
Integrated Front-End Systems							f_{RF} = 900MHz						
NE/SA600	LNA + Mixer	4.5-5.5V	13mA/4.2mA* @5V	14	D	LNA 1.2GHz	16/-7.5dB*	2.2dB	-10/+26dBm*	-20dBm	50Ω	50Ω	— LNA Overload Mode — Excellent Noise Figure
						Mixer 1.2GHz	-2.6dB	14dB	+6dBm	-4dBm	50Ω	High	
SA601	LNA + Mixer	2.7-5.5V	7.4mA@3V	20	DK	LNA 1.2GHz	11.5dB	1.6dB	-2dBm	-16dBm	50Ω	50Ω	— Low Voltage — Excellent Noise Figure
						Mixer 1.2GHz	+6dB	10dB	-2dBm	-13dBm	50Ω	High	
SA620	LNA + Mixer + VCO	2.7-5.5V	10.4mA/7.2mA* @3V	20	DK	LNA 1.2GHz	11.5/-7.5dB*	1.6dB	-3/+25dBm*	-16dBm	50Ω	50Ω	— Low Voltage — Excellent Noise Figure — LNA Overload Mode — Internal VCO
						Mixer 1.2GHz	+3dB	9dB	-6dBm	-13dBm	50Ω	High	
UAA2072M	LNA + Image Reject Mixer	4.5-5.3V	31.5mA@5V	20	DK	LNA + IRM 960MHz	26dB	4dB	-15dBm	-24.5dBm	200Ω	High	— Image reject mixer (30dB min. reject) — Tx down-convert mixer
Mixer Systems							f_{RF} = 45MHz						
NE/SA602A	Mixer + Oscillator	4.5-8.0V	2.4mA@6V	8	N, D	500MHz	17dB	5.0dB	-13dBm	-25dBm	1.5kΩ	1.5kΩ	— Excellent Noise Figure — High Gain
NE/SA612A	Mixer + Oscillator	4.5-8.0V	2.4mA@6V	8	N, D	500MHz	17dB	5.0dB	-13dBm	-25dBm	1.5kΩ	1.5kΩ	— Excellent Noise Figure — High Gain
RF Amplifiers							f_{RF} = 900MHz (NE/SA5200), 100MHz (others)						
NE/SA5200	Dual Gain Stage	4.0-9.0V	4.2mA/95μA* @5V (per amplifier)	8	D	DC – 1.2GHz	7.5/-13.5dB* (per amplifier)	3.6dB	-1.8dBm	+3.2dBm	50Ω	50Ω	— DC to 1.2GHz Operation — Power-Down Mode
NE/SA5204A	Wideband Amp	5.0-8.0V	25mA@6V	8	N, D	DC – 350MHz	19dB	6.0dB (50Ω) 4.8dB (75Ω)	-2dBm	+4dBm	50Ω	50Ω	— DC to 350MHz Operation
NE/SA5205A	Wideband Amp	5.0-8.0V	25mA@6V	8	N, D	DC – 550MHz	19dB	6.0dB (50Ω) 4.8dB (75Ω)	-2dBm	+4dBm	50Ω	50Ω	— DC to 550MHz Operation
NE/SA5209	Variable Gain Amp	4.5-7.0V	43mA@5V	16	N, D	DC – 850MHz	25dB (voltage)	9.3dB	+13dBm (output)	-3dBm	1.2kΩ	60Ω	— DC to 850MHz Operation — Gain Control Pin
NE/SA5219	Variable Gain Amp	4.5-7.0V	43mA@5V	16	N, D	DC – 700MHz	25dB (voltage)	9.3dB	+13dBm (output)	-3dBm	1.2kΩ	60Ω	— DC to 700MHz Operation — Gain Control Pin

Temperature Range

NE: 0 to +70°C
SA: -40 to +85°C

Package Descriptions

D Small Outline – 14
Small Outline – 16
Small Outline – 20

DK: Shrink Small Outline Package (SSOP) – 20

N: Dual In-Line Plastic

*Amplifier: Enabled/Disabled

Balanced modulator/demodulator

MC1496/MC1596

DESCRIPTION

The MC1496 is a monolithic double-balanced modulator/demodulator designed for use where the output voltage is a product of an input voltage (signal) and a switched function (carrier). The MC1596 will operate over the full military temperature range of -55 to +125°C. The MC1496 is intended for applications within the range of 0 to +70°C.

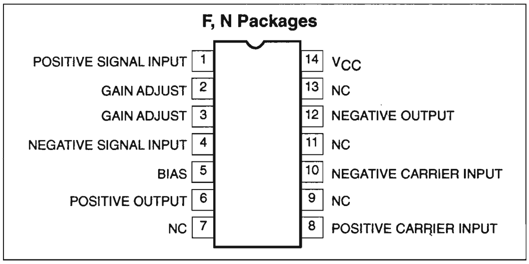
FEATURES

- Excellent carrier suppression
  65dB typ @ 0.5MHz
  50dB typ @ 10MHz
- Adjustable gain and signal handling
- Balanced inputs and outputs
- High common-mode rejection—85dB typ

APPLICATIONS

- Suppressed carrier and amplitude modulation
- Synchronous detection
- FM detection
- Phase detection
- Sampling
- Single sideband
- Frequency doubling

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Ceramic Dual In-Line Package Cerdip)	0 to +70°C	MC1496F	0581B
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	MC1496N	0405B
14-Pin Ceramic Dual In-Line Package Cerdip)	-55 to +125°C	MC1596F	0581B
14-Pin Plastic Dual In-Line Package (DIP)	-55 to +125°C	MC1596N	0405B

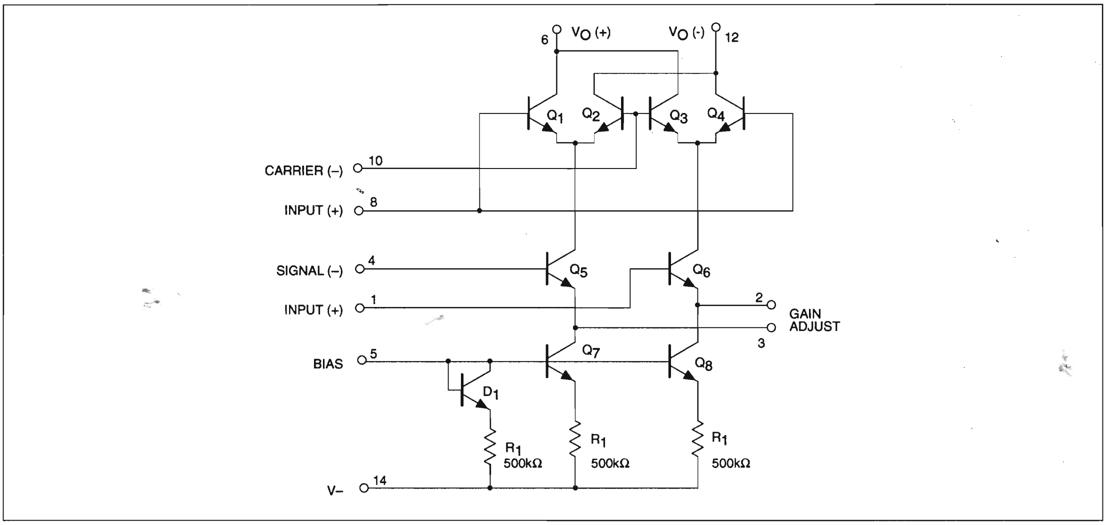
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Applied voltage	30	V
V_8-V_{10}	Differential input signal	±5.0	V
V_4-V_1	Differential input signal	$(5 \pm I_5 R_e)$	V
V_2-V_1, V_3-V_4	Input signal	5.0	V
I_5	Bias current	10	mA
P_D	Maximum power dissipation, T_A=25°C (still-air)[1] F package N package	 1190 1420	 mW mW
T_A	Operating temperature range MC1496 MC1596	 0 to +70 -55 to +125	 °C °C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:

1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.4mW/°C

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

V_{CC}=+12V_{DC}; V_{CC}=-8.0V_{DC}; I_5=1.0mADC; R_L=3.9kΩ; R_E=1.0kΩ; T_A=25°C, unless otherwise specified.

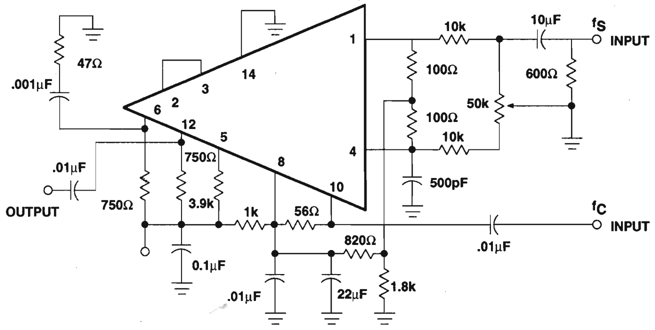
SYMBOL	PARAMETER	TEST CONDITIONS	MC1596			MC1496			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Single-ended input impedance	Signal port, f=5.0MHz							
R_{IP}	Parallel input resistance			200			200		kΩ
C_{IP}	Parallel input capacitance			2.0			2.0		pF
	Single-ended output impedance	f=10MHz							
R_{OP}	Parallel output resistance			40			40		kΩ
C_{OP}	Parallel output capacitance			5.0			5.0		pF
	Input bias current								μA
I_{BS}	I_{BS}=			12	25		12	30	
I_{BC}	I_{BC}=			12	25		12	30	μA
	Input offset current								μA
I_{IOS}	$I_{IOS}=I_1-I_4$			0.7	5.0		0.7	7.0	
I_{IOC}	$I_{IOC}=I_8-I_{10}$			0.7	5.0		0.7	7.0	μA
T_CI_{IO}	Average temperature coefficient of input offset current			2.0			2.0		nA/°C
	Output offset current								
I_{OO}	I_6-I_{12}			14	50		15	80	μA
T_CI_{OO}	Average temperature coefficient of output offset current			90			90		nA/°C
V_O	Common-mode quiescent output voltage (Pin 6 or Pin 12)			8.0			8.0		V_{DC}
	Power supply current								mA_{DC}
I_{D+}	I_6+I_{12}			2.0	3.0		2.0	4.0	
I_{D-}	I_{14}			3.0	4.0		3.0	5.0	
P_D	DC power dissipation			33			33		mW

AC ELECTRICAL CHARACTERISTICS

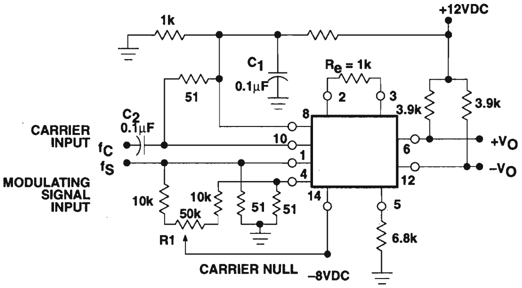
V_{CC}=+12$_{DC}$; V_{CC}=-9.0V_{DC}; I_5=1.0mA_{DC}; R_L=3.9kΩ; R_E=1.0kΩ; T_A=+25°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MC1596			MC1496			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CFT}	Carrier feedthrough	V_C=60mV_{RMS} sinewave and offset adjusted to zero							
		f_C=1.0kHz		40			40		μV_{RMS}
		f_C=10MHz		140			140		
		V_C=300m$V_{P\text{-}P}$ squarewave:							
		Offset adjusted to zero f_C=1.0kHz		0.04	0.2		0.04	0.4	mV_{RMS}
		Offset not adjusted f_C=1.0kHz		20	100		20	200	
V_{CS}	Carrier suppressions	f_S=10kHz, 300mV_{RMS} sinewave							
		f_C=500kHz, 60mV_{RMS} sinewave	50	65		40	65		dB
		f_C=10MHz, 60mV_{RMS} sinewave		50			50		
BW_{3dB}	Transadmittance bandwidth	Carrier input port, V_C=60mV_{RMS}		300			300		MHz
	(Magnitude) (R_L=50Ω)	sinewave f_S=1.0kHz,							
		300mV_{RMS} sinewave							
		Signal input port, V_S=300mV_{RMS}		80			80		MHz
		sinewave $\lvert V_C \rvert$ = 0.5V_{DC}							
A_{VS}	Signal gain	V_S=100mV_{RMS}; f=1.0kHz	2.5	3.5		2.5	3.5		V/V
		$\lvert V_C \rvert$ = 0.5V_{DC}							
CMV	Common-mode input swing	Signal port, f_S=1.0kHz		5.0			5.0		$V_{P\text{-}P}$
A_{CM}	Common-mode gain	Signal port, f_S=1.0kHz		-85			-85		dB
		$\lvert V_C \rvert$ = 0.5V_{DC}							
DV_{OUT}	Differential output voltage swing capability			8.0			8.0		$V_{P\text{-}P}$

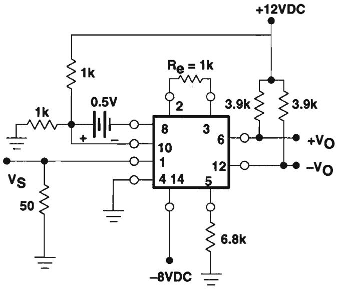
TEST CIRCUITS



Carrier Rejection and Suppression



Carrier Rejection and Suppression



Signal Gain and Output Swing

Balanced modulator/demodulator applications using the MC1496/1596

AN189

BALANCED MODULATOR/DEMODULATOR APPLICATIONS USING MC1496/MC1596

The MC1496 is a monolithic transistor array arranged as a balanced modulator-demodulator. The device takes advantage of the excellent matching qualities of monolithic devices to provide superior carrier and signal rejection. Carrier suppressions of 50dB at 10MHz are typical with no external balancing networks required.

Applications include AM and suppressed carrier modulators, AM and FM demodulators, and phase detectors.

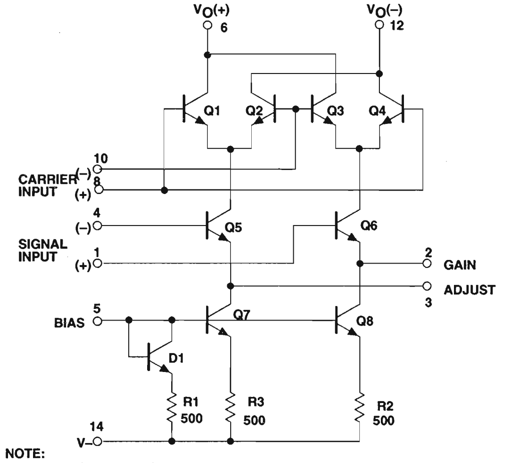
THEORY OF OPERATION

As Figure 1 suggests, the topography includes three differential amplifiers. Internal connections are made such that the output becomes a product of the two input signals V_C and V_S.

To accomplish this the differential pairs Q1-Q2 and Q3-Q4, with their cross-coupled collectors, are driven into saturation by the zero crossings of the carrier signal V_C. With a low level signal, V_S driving the third differential amplifier Q5-Q6, the output voltage will be full wave multiplication of V_C and V_S. Thus for sine wave signals, V_{OUT} becomes:

$$V_{OUT} = E_X E_Y \left[\cos(\omega x + \omega y)t + \cos(\omega x - \omega y)t\right] \quad (1)$$

As seen by equation (1) the output voltage will contain the sum and difference frequencies of the two original signals. In addition, with the carrier input ports being driven into saturation, the output will contain the odd harmonics of the carrier signals. (See Figure 4.)



NOTE:
All resistor values are in ohms

Figure 1. Balanced Modulator Schematic

Internally provided with the device are two current sources driven by a temperature-compensated bias network. Since the transistor geometries are the same and since V_{BE} matching in monolithic devices is excellent, the currents through Q_7 and Q_8 will be identical to the current set at Pin 5. Figures 2 and 3 illustrate typical biasing arrangements from split and single-ended supplies, respectively.

Of primary interest in beginning the bias circuitry design is relating available power supplies and desired output voltages to device requirements with a minimum of external components.

The transistors are connected in a cascode fashion. Therefore, sufficient collector voltage must be supplied to avoid saturation if linear operation is to be achieved. Voltages greater than 2V are sufficient in most applications.

Biasing is achieved with simple resistor divider networks as shown in Figure 3. This configuration assumes the presence of symmetrical supplies. Explaining the DC biasing technique is probably best accomplished by an example. Thus, the initial assumptions and criteria are set forth:

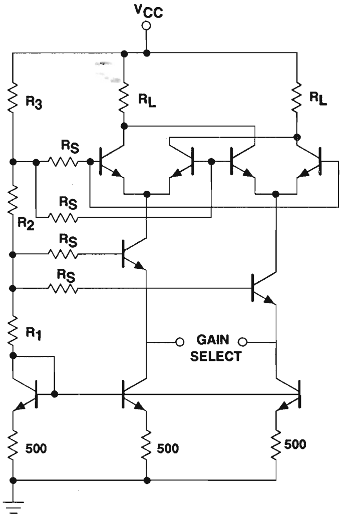
1. Output swing greater than $4V_{P-P}$.
2. Positive and negative supplies of 6V are available.
3. Collector current is 2mA. It should be noted here that the collector output current is equal to the current set in the current sources.

As a matter of convenience, the carrier signal ports are referenced to ground. If desired, the modulation signal ports could be ground referenced with slight changes in the bias arrangement. With the carrier inputs at DC ground, the quiescent operating point of the outputs should be at one-half the total positive voltage or 3V for this case. Thus, a collector load resistor is selected which drops 3V at 2mA or 1.5kΩ. A quick check at this point reveals that with these loads and current levels the peak-to-peak output swing will be greater than 4V. It remains to set the current source level and proper biasing of the signal ports.

The voltage at Pin 5 is expressed by

$$V_{BIAS} = V_{BE} = 500 \cdot I_S$$

where I_S is the current set in the current sources.



NOTE:
All resistor values are in ohms

Figure 2. Single-Supply Biasing

BIASING

Since the MC1496 was intended for a multitude of different functions as well as a myriad of supply voltages, the biasing techniques are specified by the individual application. This allows the user complete freedom to choose gain, current levels, and power supplies. The device can be operated with single-ended or dual supplies.

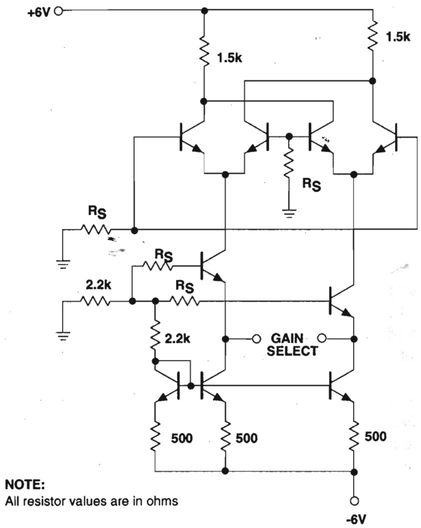


Figure 3. Dual Supply Biasing

$$V_{BIAS} = V_{BE} = 500 \times I_S$$

where I_S is the current set in the current sources.

For the example V_{BE} is 700mV at room temperature and the bias voltage at Pin 5 becomes 1.7V. Because of the cascode configuration, both the collectors of the current sources and the collectors of the signal transistors must have some voltage to operate properly. Hence, the remaining voltage of the negative supply (–6V+1.7V=–4.3V) is split between these transistors by biasing the signal transistor bases at –2.15V. Countless other bias arrangements can be used with other power supply voltages. The important thing to remember is that sufficient DC voltage is applied to each bias point to avoid collector saturation over the expected signal wings.

BALANCED MODULATOR

In the primary application of balanced modulation, generation of double sideband suppressed carrier modulation is accomplished. Due to the balance of both modulation and carrier inputs, the output, as mentioned, contains the sum and difference frequencies while attenuating the fundamentals. Upper and lower sideband signals are the strongest signals present with harmonic sidebands being of diminishing amplitudes as characterized by Figure 4.

Gain of the 1496 is set by including emitter degeneration resistance located as R_E in Figure 5. Degeneration also allows the maximum signal level of the modulation to be increased. In general, linear response defines the maximum input signal as

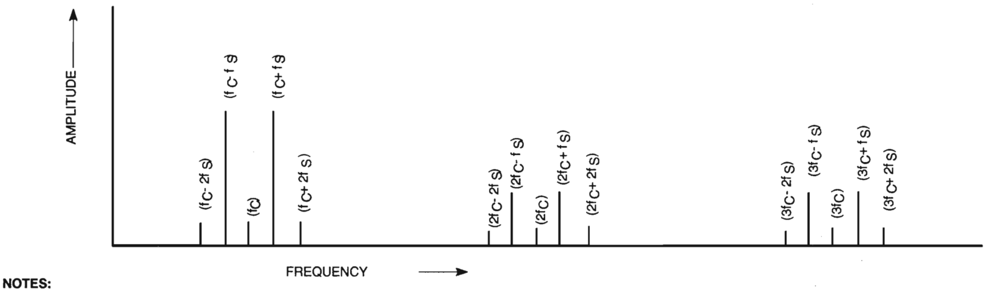
$$V_s \le 15 \bullet R_E \text{ (Peak)}$$

and the gain is given by

$$A_{VS} = \frac{R_L}{R_E + 2r_e} \qquad (2)$$

This approximation is good for high levels of carrier signals. Table 1 summarizes the gain for different carrier signals.

As seen from Table 1, the output spectrum suffers an amplitude increase of undesired sideband signals when either the modulation or carrier signals are high. Indeed, the modulation level can be increased if R_E is increased without significant consequence. However, large carrier signals cause odd harmonic sidebands (Figure 4) to increase. At the same time, due to imperfections of the carrier waveforms and small imbalances of the device, the second harmonic rejection will be seriously degraded. Output filtering is often used with high carrier levels to remove all but the desired sideband. The filter removes unwanted signals while the high carrier level guards against amplitude variations and maximizes gain. Broadband modulators, without benefit of filters, are implemented using low carrier and modulation signals to maximize linearity and minimize spurious sidebands.



NOTES:

f_C Carrier Fundamental

f_S Modulating Signal
$f_C \pm f_S$ Fundamental Carrier Sidebands

$f_C \pm nf_S$ Fundamental Carrier Sideband Harmonics

nf_C Carrier Harmonics
$nf_C \pm nf_S$ Carrier Harmonic Sidebands

Figure 4. Modulator Frequency Spectrum

AM MODULATOR

The basic current of Figure 5 allows no carrier to be present in the output. By adding offset to the carrier differential pairs, controlled amounts of carrier appear at the output whose amplitude becomes a function of the modulation signal or AM modulation. As shown, the carrier null circuit is changed from Figure 5 to have a wider range so that wider control is achieved. All connections are shown in Figure 6.

AM DEMODULATION

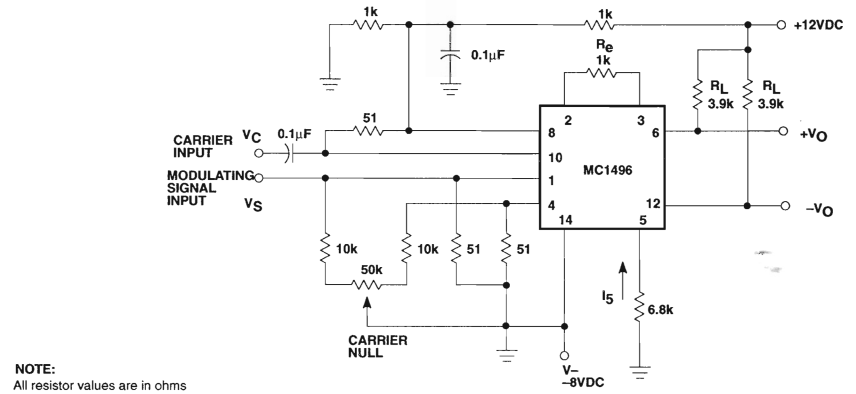
As pointed out in Equation 1, the output of the balanced mixer is a cosine function of the angle between signal and carrier inputs. Further, if the carrier input is driven hard enough to provide a switching action, the output becomes a function of the input amplitude. Thus the output amplitude is maximum when there is 0° phase difference as shown in Figure 7.

Amplifying and limiting of the AM carrier is accomplished by IF gain block providing 55dB of gain or higher with limiting of 400µV. The limited carrier is then applied to the detector at the carrier ports to provide the desired switching function. The signal is then demodulated by the synchronous AM demodulator (1496) where the carrier frequency is attenuated due to the balanced nature of the device. Care must be taken not to overdrive the signal input so that distortion does not appear in the recovered audio. Maximum conversion gain is reached when the carrier signals are in phase as indicated by the phase-gain relationship drawn in Figure 7.

Output filtering will also be necessary to remove high frequency sum components of the carrier from the audio signal.

PHASE DETECTOR

The versatility of the balanced modulator or multiplier also allows the device to be used as a phase detector. As mentioned, the output of the detector contains a term related to the cosine of the phase angle. Two signals of equal frequency are applied to the inputs as per Figure 8. The frequencies are multiplied together producing the sum and difference frequencies. Equal frequencies cause the difference component to become DC while the undesired sum component is filtered out. The DC component is related to the phase angle by the graph of Figure 9.

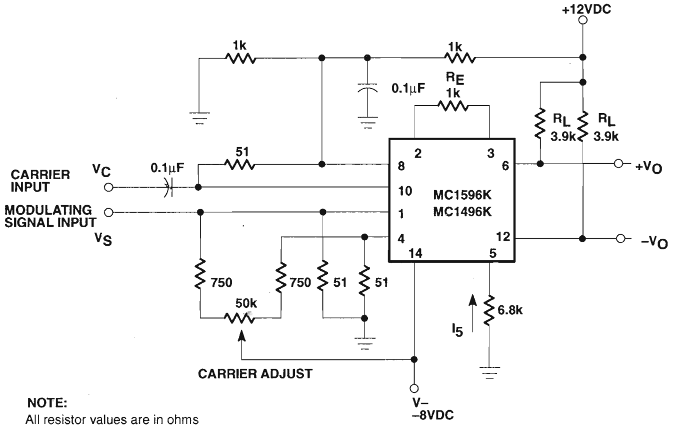


NOTE:
All resistor values are in ohms

Figure 5. Double Suppressed Carrier Modulator

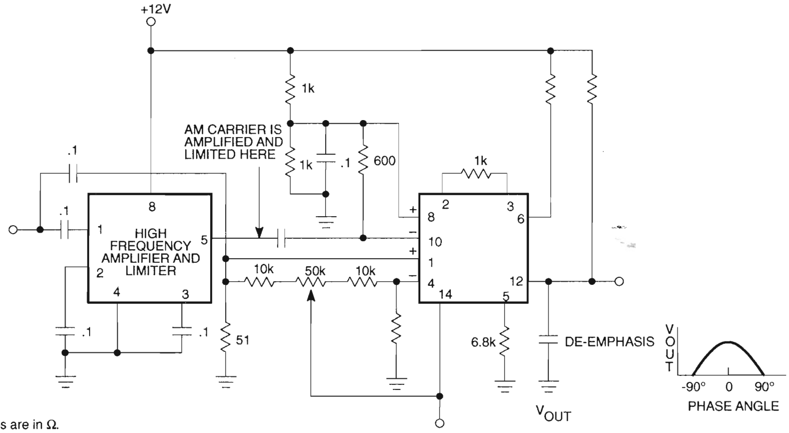
Table 1. Voltage Gain and Output vs Input Signal

CARRIER INPUT SIGNAL (V_C)	APPROXIMATE VOLTAGE GAIN	OUTPUT SIGNAL FREQUENCY(S)
Low-level DC	$\frac{R_L V_C}{2(R_E + 2r_E)\left(\frac{KT}{q}\right)}$	f_M
High-level DC	$\frac{R_L}{R + 2r_e}$	f_M
Low-level AC	$\frac{R_L V_C \text{ (rms)}}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C + f_M$
High-level AC	$\frac{0.637R_L}{R_E + 2r_e}$	$f_C + f_M$, $3f_C + f_M$. $5f_C + f_M$...



NOTE:
All resistor values are in ohms

Figure 6. AM Modulator



NOTE:
All resistor values are in Ω.

Figure 7. AM Demodulator

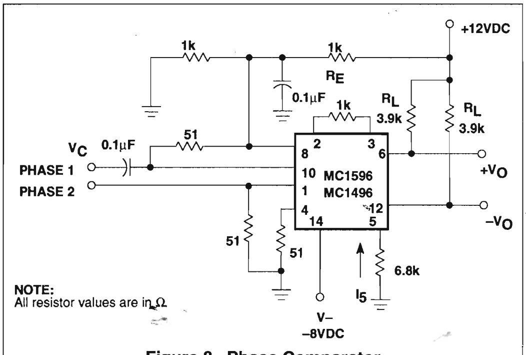


Figure 8. Phase Comparator

At 90° the cosine becomes zero, while being at maximum positive or maximum negative at 0° and 180°, respectively.

The advantage of using the balanced modulator over other types of phase comparators is the excellent linearity of conversion. This configuration also provides a conversion gain rather than a loss for greater resolution. Used in conjunction with a phase-locked loop, for instance, the balanced modulator provides a very low distortion FM demodulator.

FREQUENCY DOUBLER

Very similar to the phase detector of Figure 8, a frequency doubler schematic is shown in Figure 10. Departure from Figure 8 is primarily the removal of the low-pass filter. The output then contains the sum component which is twice the frequency of the input, since both input signals are the same frequency.

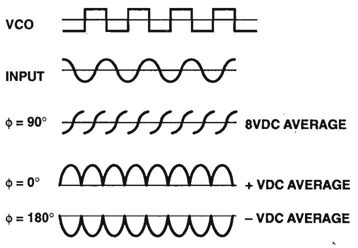


Figure 9. Phase Detector ± Voltages

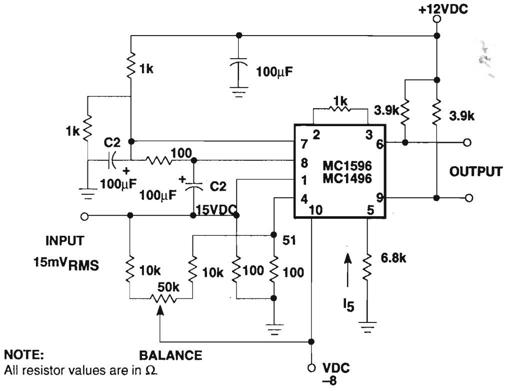


Figure 10. Low Frequency Doubler

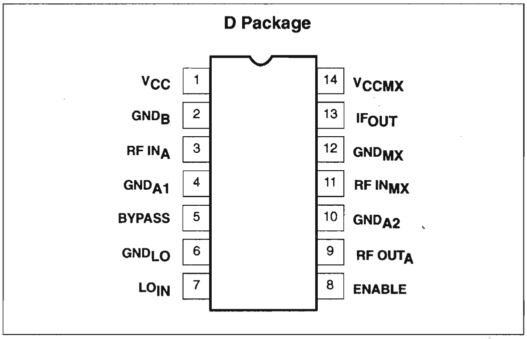
DESCRIPTION

The NE/SA600 is a combined low noise amplifier (LNA) and mixer designed for high-performance low-power communication systems from 800-1200MHz. The low-noise preamplifier has a 2dB noise figure at 900MHz with 16dB gain and an IM$_3$ intercept of -10dBm at the input. Input and output impedances are 50Ω and the gain is stabilized by on-chip compensation to vary less than ±0.5dB over the -40 to +85°C temperature range. The wide-dynamic-range mixer has a 14dB noise figure and IM$_3$ intercept of +6dBm at the input at 900MHz. Mixer input impedance is 50Ω with an open-collector output. The chip incorporates an option so the LNA can be disabled and replaced by a through connection. The amplifier IM$_3$ intercept increases to +26dBm in this mode; thus, large signals can be handled. The nominal current drawn from a single 5V supply is 13mA and 4.2mA in the LNA thru mode.

FEATURES

- Low current consumption: 13mA nominal, 4.2mA in the LNA thru mode
- Excellent noise figure: 2dB for the amplifier and 14dB for the mixer at 900MHz
- Excellent gain stability versus temperature
- Switchable overload capability
- Amplifier matched to 50Ω
- Mixer input matched to 50Ω
- Oscillator input matched to 50Ω

PIN CONFIGURATION



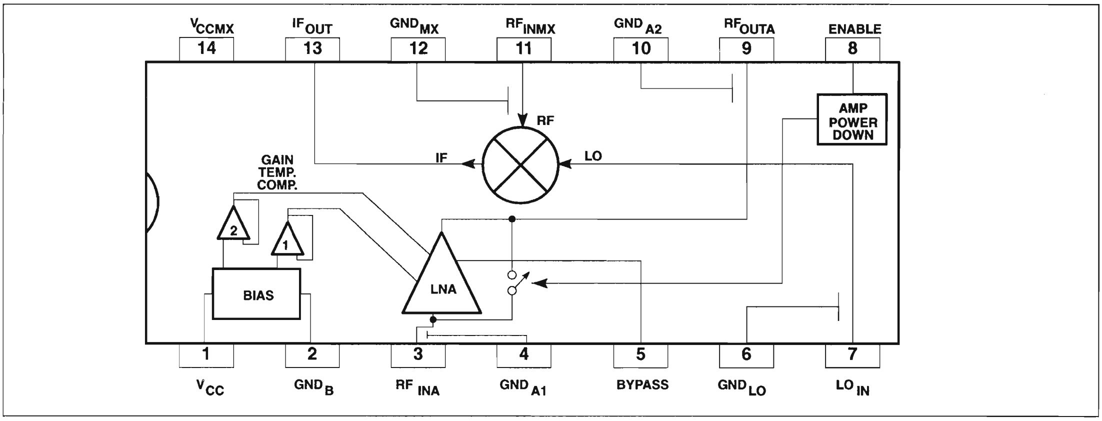
APPLICATIONS

- 900MHz front end for GSM/AMPS/TACS/ hand-held units
- RF data links
- UHF frequency conversion
- Portable radio
- Spread spectrum receivers
- 900MHz cordless phones

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Small Outline (SO) package (Surface-mount)	0 to +70°C	NE600D	0175D
14-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA600D	0175D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}, V_{CCMX}	Supply voltage[1]	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC}+0.3)	V
ΔV	V_{CC} to V_{CCMX}	-0.3 to +0.3	V
ΔG	Any GND pin to any other GND pin	-0.3 to +0.3	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 14-Pin Plastic SO	980	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 9V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   14-Pin SO: θ_{JA} = 125°C/W
3. CAUTION: The NE/SA600 is built on a BiCMOS process and is sensitive to electrostatic discharge.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}, V_{CCMX}	Supply voltage	4.5 to 5.5	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS[1,2]

V_{CC} = V_{CCMX} = +5V, T_A = 25°C; Test Figure 1, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	–3σ	TYP	+3σ	MAX	
I_{CC}	Supply current (Pin 1, 13, 14)	Enable input high	10	11	13.0	15	16	mA
		Enable input low	3.2	3.6	4.2	4.8	5.2	
V_T	Enable logic threshold voltage		1.12	1.17	1.27	1.37	1.42	V
V_{IH}	Logic 1 level: LNA gain mode		2.0				V_{CC}	V
V_{IL}	Logic 0 level: LNA thru mode		–0.3				0.8	V
I_{IL}	Enable input current	Enable = 0.4V	-1		0		1	µA
I_{IH}	Enable input current	Enable = 2.4V	-1		0		1	µA
V_{LNA-IN}	LNA input bias voltage	Enable input high			0.78			V
$V_{LNA-OUT}$	LNA output bias voltage	Enable input high			1.27			V
V_{BY}	LNA bypass bias voltage	Enable input high			1.05			V
V_{MX-IN}	Mixer RF input bias voltage				1.43			V
V_{LO-IN}	Mixer LO input bias voltage				3.35			V

NOTE:
1. The ENABLE input must be connected to a valid logic level for proper operation of the NE/SA600.
2. Standard deviations are estimated from design simulations to represent manufacturing variations over the life of the product.

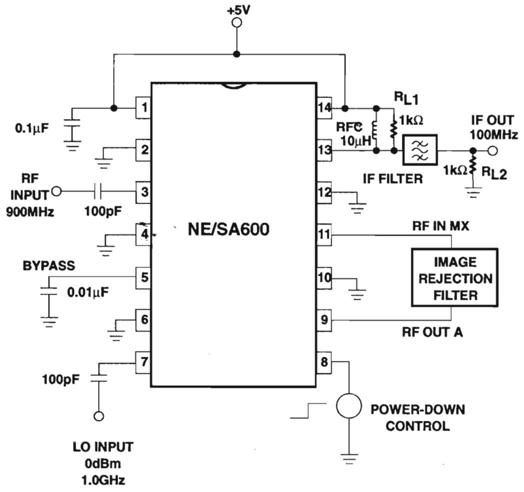
AC ELECTRICAL CHARACTERISTICS[1,2]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			–3σ	TYP	+3σ	
LNA ($V_{CC} = V_{CCMX}$ = +5V, T_A = 25°C; Enable = Hi, Test Figure 1, unless otherwise stated.)						
S_{21}	Amplifier gain	900MHz	14.9	16	17.1	dB
S_{21}	Amplifier gain in thru mode	Enable = LO, 900MHz	–9.0	-7.5	–6.0	dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity enabled	900MHz		-0.008		dB/°C
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity in thru mode	Enable = LO, 900MHz		-0.014		dB/°C
$\Delta S_{21}/\Delta f$	Gain frequency variation	800MHz - 1.2GHz		-0.014		dB/MHz
S_{12}	Amplifier reverse isolation	900MHz	–47	-42	–37	dB
S_{11}	Amplifier input match[3]	900MHz	–11	-10	–9	dB
S_{22}	Amplifier output match	900MHz	–16.8	-15	–13.2	dB
P_{-1dB}	Amplifier input 1dB gain compression	900MHz	–21.2	-20	–18.8	dBm
IP_3	Amp input 3rd-order intercept	Test Fig. 2, 900MHz	–11.6	-10	–8.6	dBm
	Amp input 3rd-order intercept (thru mode)	Test Fig. 2, 900MHz, Enable = LO		+26		dBm
NF	Amplifier noise figure	900MHz	1.9	2.2	2.5	dB
	Amp noise figure w/shunt 15nH inductor at input	900MHz	1.7	2.0	2.3	dB
t_{ON}	Amplifier turn-on time	Enable Lo → Hi, Coupling = 100pF		30		µs
		Coupling = 0.01µF		3		ms
t_{OFF}	Amplifier turn-off time	Enable Hi → Lo, Coupling = 100pF		10		µs
		Coupling = 0.01µF		1		ms
Mixer ($V_{CC} = V_{CCMX}$ = +5V, T_A = 25°C, Enable = Hi, f_{LO} = 1GHz @ 0dBm, f_{RF} = 900MHz, f_{IF} = 100MHz, Test Fig. 1, unless otherwise stated)						
VG_C	Mixer voltage conversion gain	$R_{L1} = R_{L2} = 1k\Omega$	9.5	10.4	11.3	dB
PG_C	Mixer power conversion gain	$R_{L1} = R_{L2} = 1k\Omega$	–3.05	-2.6	–2.15	dB
S_{11RF}	Mixer input match	900MHz	–23	-20	–17	dB
NF_M	Mixer SSB noise figure	Test Fig. 3, 900MHz, f_{IF} = 80MHz	12.2	14	15.8	dB
P_{-1dB}	Mixer input 1dB gain compression	900MHz	–5.3	-4	–2.7	dBm
IP_{3INT}	Mixer input third order intercept	900MHz	+5	+6	+7	dBm
IP_{2INT}	Mixer input second order intercept	900MHz	+18	+20	+22	dBm
$G_{RFM\text{-}IF}$	Mixer RF feedthrough	900MHz, C_{IF} = 3pF		–7		dB
$G_{LO\text{-}IF}$	Mixer LO feedthrough	900MHz, C_{IF} = 3pF		-10		dB
$G_{LO\text{-}RFM}$	Local oscillator to mixer input feedthrough	900MHz		-33		dB
S_{11LO}	LO input match	900MHz	–24	–20	–16	dB
$G_{LO\text{-}RF}$	Local oscillator to RF input feedthrough	900MHz		-46		dB
$G_{RFO\text{-}RFM}$	Filter feedthrough	900MHz		-39		dB
LNA + Mixer ($V_{CC}=V_{CCMX}$=+5V, T_A=25°C, Enable=Hi, f_{LO}=1GHz @ 0dBm, f_{RF} = 900MHz, f_{IF} = 100MHz, Test Fig. 1, unless otherwise stated)						
PG_C	Overall power conversion gain			13.4		dB
NF	Overall noise figure			3.5		dB
IP_3	Overall input 3rd-order intercept			–13		dBm

NOTE:

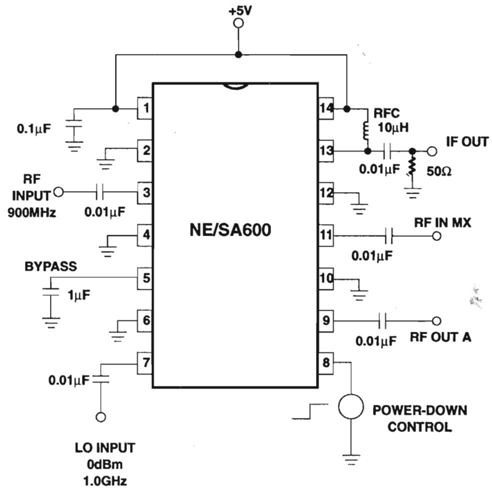
1. All meausrements include the effects of the NE/SA600 Evaluation Board (see Figure) unless otherwise noted. Measurement system impedance is 50Ω.
2. Standard deviations are estimated from design simulations to represent manufacturing variations over the life of the product.
3. With a shunt 15nH inductor at the input of the LNA, the value of S_{11} is typically –15dB.

TYPICAL APPLICATION

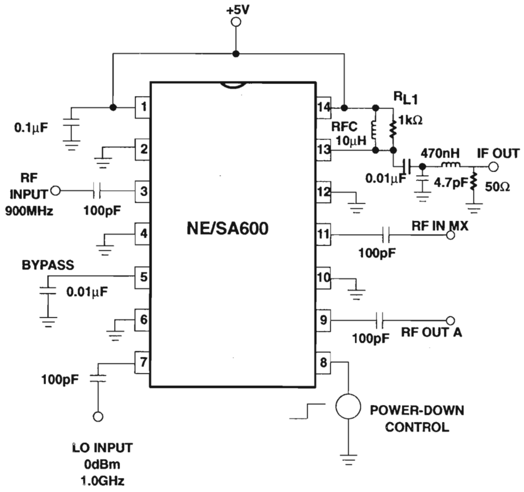


NOTES:
RATIO OF BYPASS TO SIGNAL COUPLING CAPS FOR LNA SHOULD BE 100:1 OR GREATER.
IF FILTER SHOULD BE AC COUPLED.

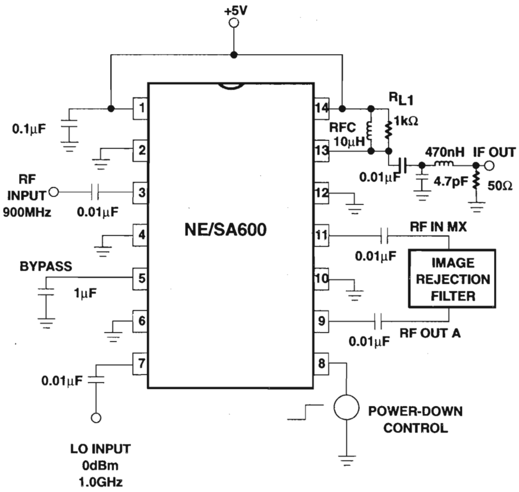
TEST FIGURE 1



TEST FIGURE 2

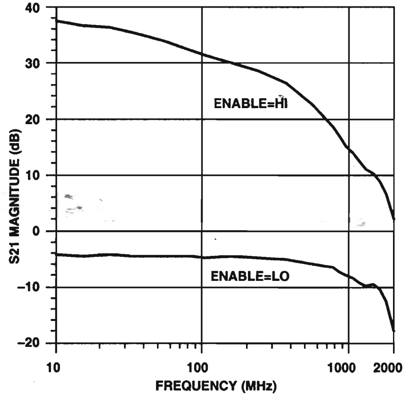


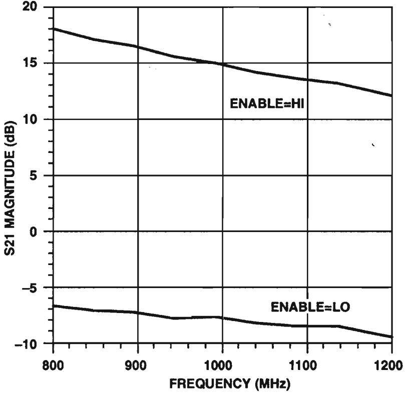
TEST FIGURE 3

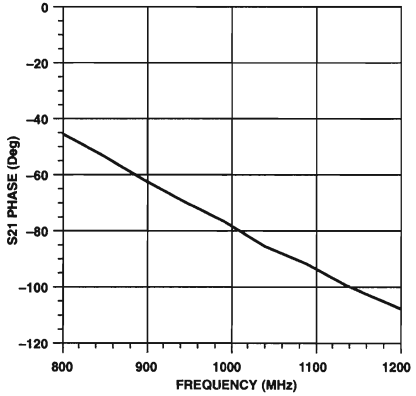


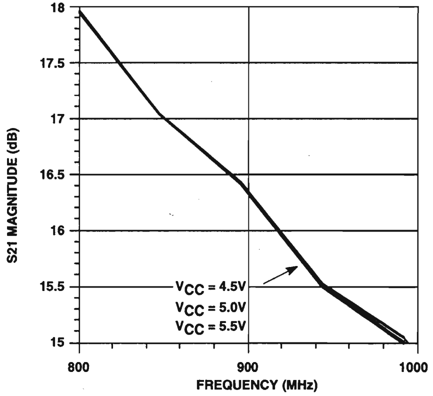
NOTE: All performance curves include the effects of the NE/SA600 evaluation board.

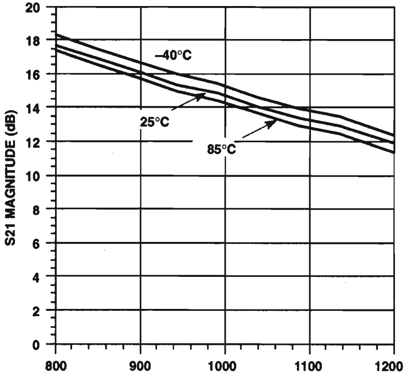
LNA S21 CHARACTERISTICS $4.5V \leq V_{CC} = V_{CCMX} \leq 5.5V$, Test Figure 1, unless otherwise specified.

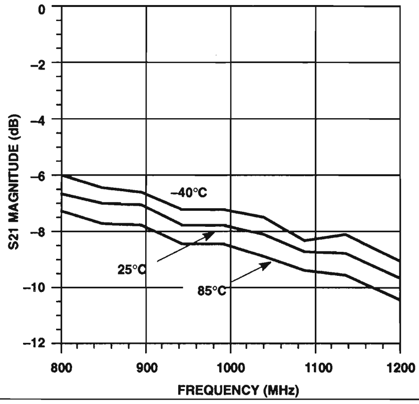

LNA S21 vs Frequency


LNA S21 vs Frequency

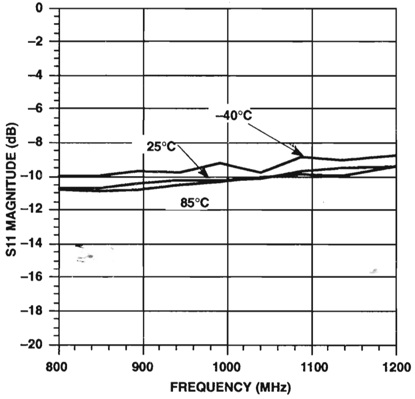

LNA S21 Phase vs Frequency

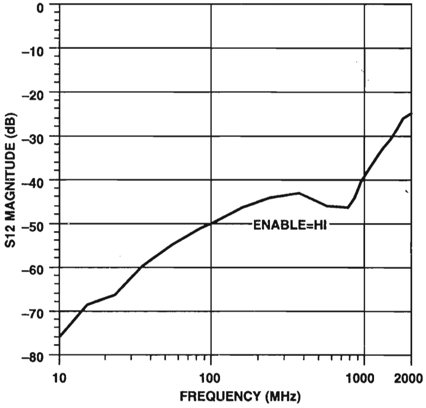

LNA S21 vs Frequency and V_{CC}

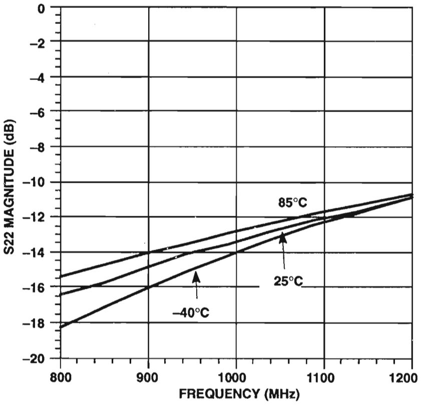

LNA S21 vs Frequency and Temperature


LNA Thru S21 vs Frequency and Temperature

LNA S11/S12/S22 CHARACTERISTICS $4.5V \le V_{CC} = V_{CCMX} \le 5.5V$, Test Figure 1, unless otherwise specified.


LNA S11 vs Frequency and Temperature


LNA S12 vs Frequency


LNA S22 vs Frequency and Temperature

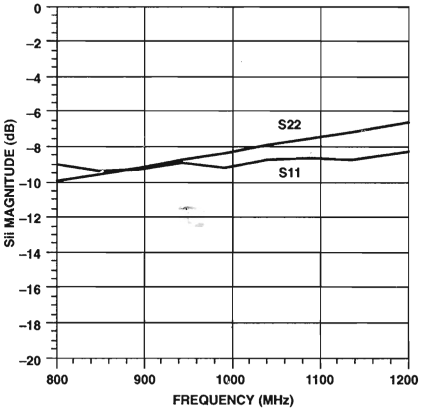

LNA Thru S11 and S22 vs Frequency

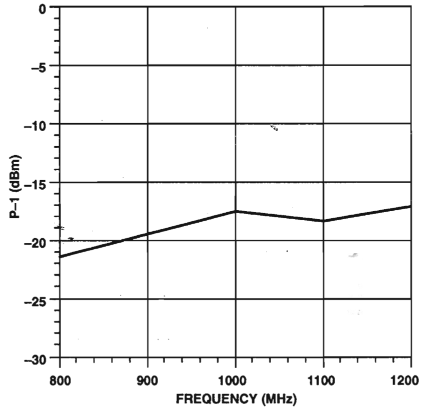
Table 1. S-Parameters

Freq	S11		S12		S21		S22	
MHz	dB	deg.	dB	deg.	dB	deg.	dB	deg.
800	–9.5	–160	–46	8	17.9	125	–18.0	151
900	–9.5	–172	–43	19	16.4	105	–15.8	122
1000	–9.4	–173	–40	17	15.1	88	–14.0	98
1100	–9.1	–200	–37	12	13.8	70	–12.4	77
1200	–8.9	–216	–35	1	12.9	55	–11.1	58

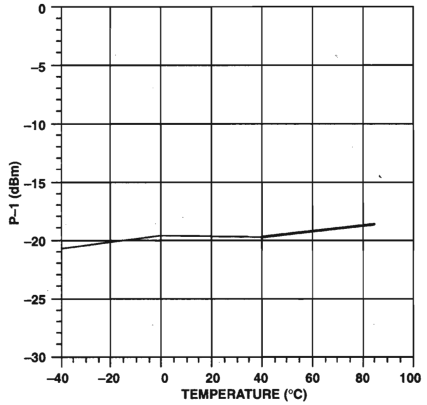
LNA OVERLOAD/NOISE/DISTORTION CHARACTERISTICS

4.5V ≤ V_{CC} = V_{CCMX} ≤ 5.5V, Test Fig. 1, unless otherwise specified.

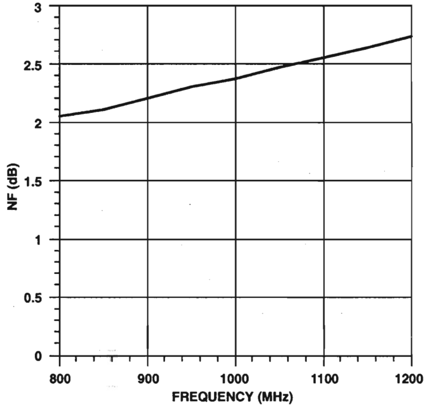
LNA Input 1dB Gain Compression Point vs Frequency



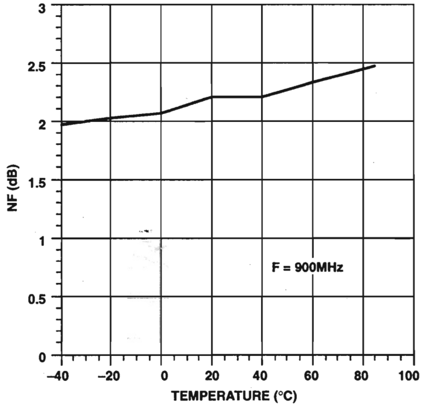
LNA Input 1dB Gain Compression Point vs Temperature



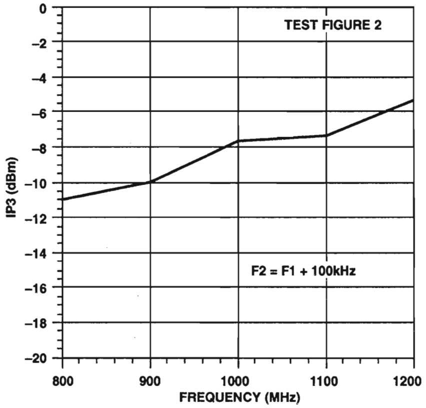
LNA 50Ω Noise Figure vs Frequency



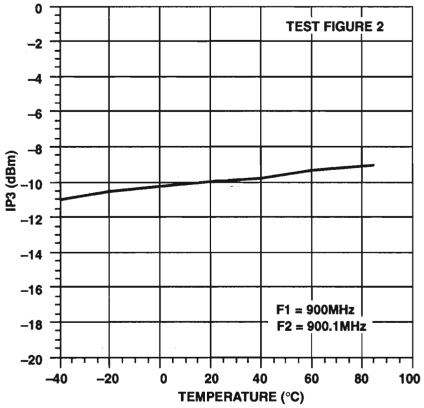
LNA 50Ω Noise Figure vs Temperature



LNA Input Third-Order Intercept vs Frequency

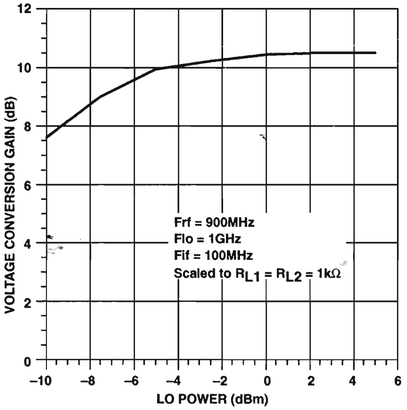


LNA Input Third-Order Intercept vs Temperature

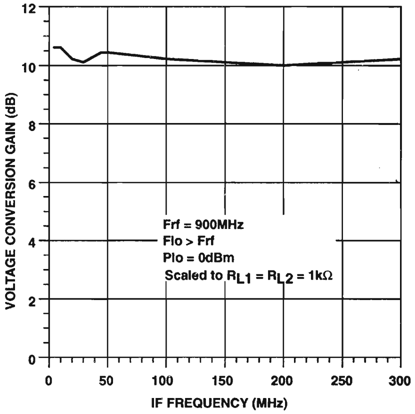


MIXER GAIN/NOISE CHARACTERISTICS $4.5V \le V_{CC} = V_{CCMX} \le 5.5V$, Test Figure 1, unless otherwise specified.

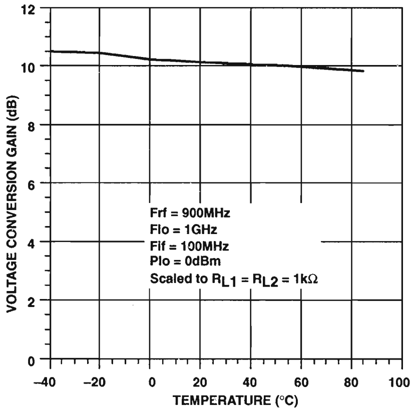
Mixer Voltage Conversion Gain vs LO Power



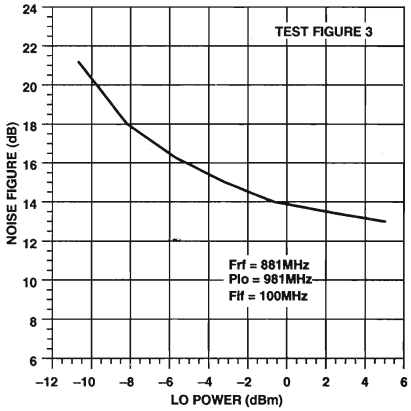
Mixer Voltage Conversion Gain vs IF Frequency



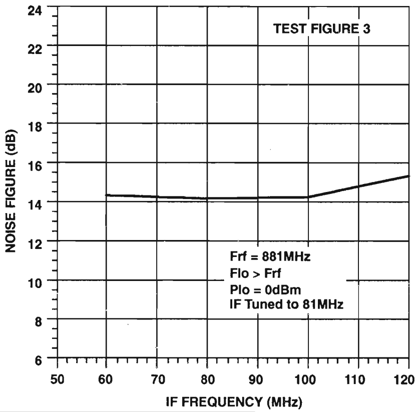
Mixer Voltage Conversion Gain vs Temperature



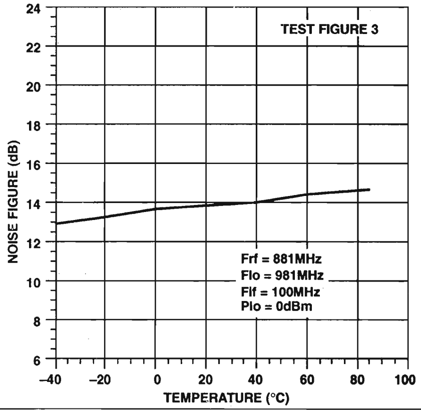
Mixer 50Ω Noise Figure vs LO Power



Mixer Noise Figure vs IF Frequency

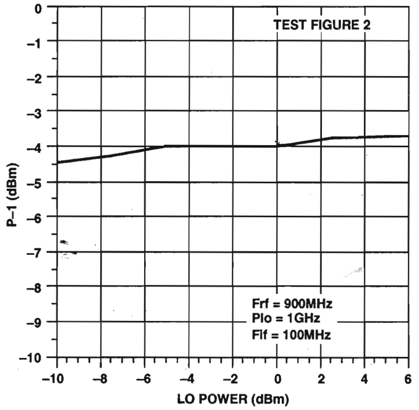


Mixer Noise Figure vs Temperature

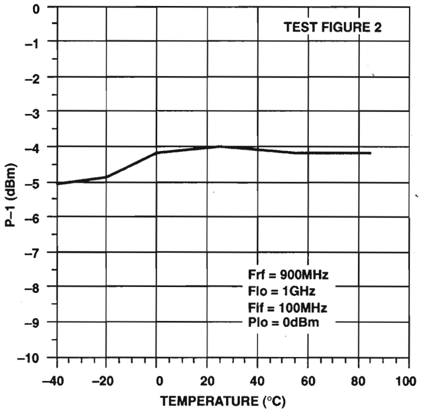


MIXER OVERLOAD/DISTORTION CHARACTERISTICS $4.5 \leq V_{CC} = V_{CCMX} \leq 5.5V$, Test Fig. 1, unless otherwise specified

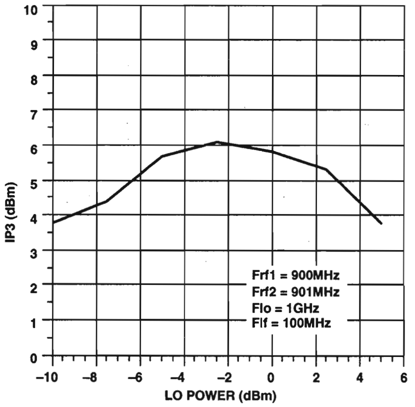
Mixer Input 1dB Gain Compression Point vs LO Power



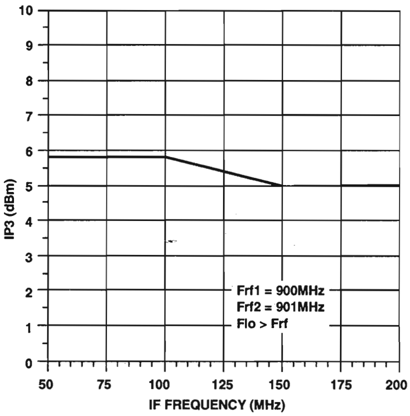
Mixer Input 1dB Gain Compression Point vs Temperature



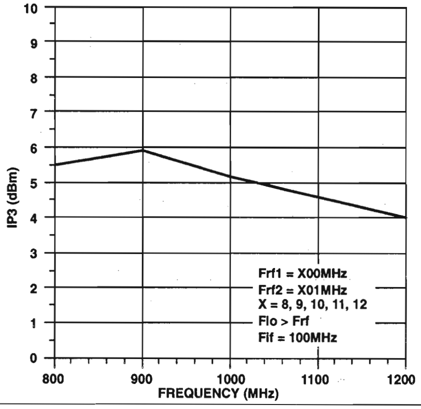
Mixer Input Third-Order Intercept Point vs LO Power



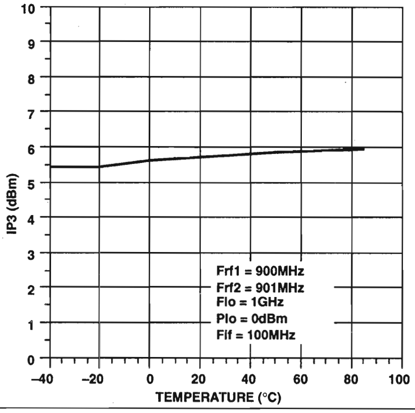
Mixer Input Third-Order Intercept Point vs IF Frequency



Mixer Input Third-Order Intercept Point vs RF Frequency



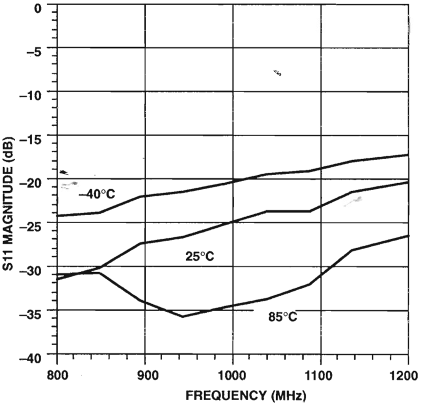
Mixer Input Third-Order Intercept Point vs Temperature



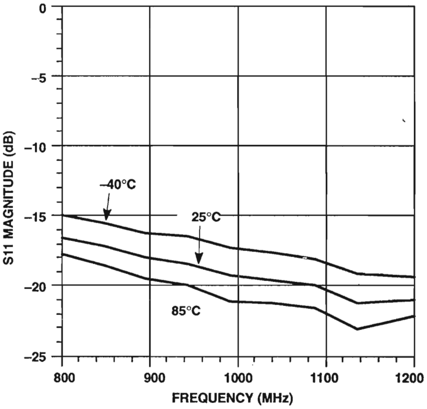
MIXER S11/ISOLATION/INTERFERENCE CHARACTERISTICS

4.5 ≤ $V_{CC} = V_{CCMX}$ ≤ 5.5V, Test Fig. 1, unless otherwise specified

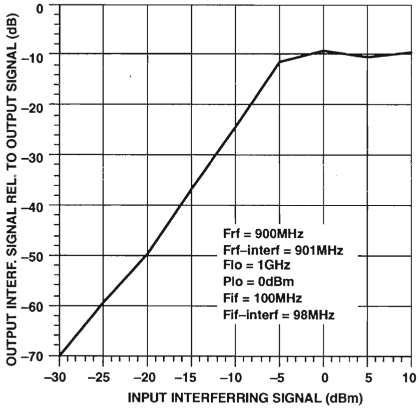
Mixer S11 at RF Port vs Frequency and Temperature



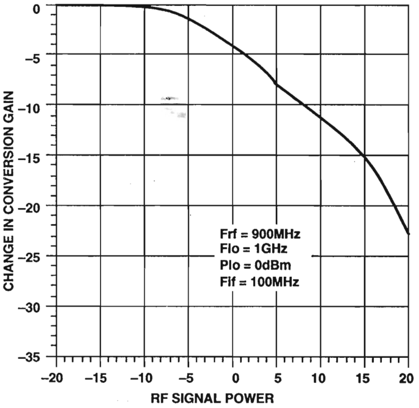
Mixer S11 at LO Port vs Frequency and Temperature



Mixer Output Interferring Signal vs Input Interferring Signal Strength

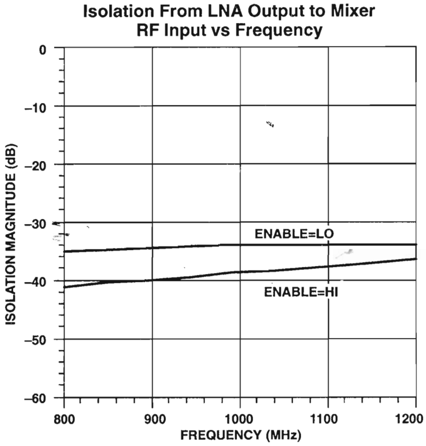


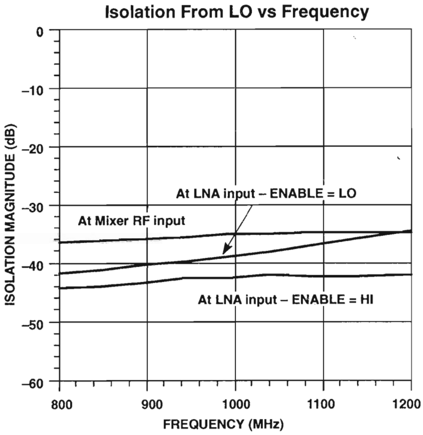
Conversion Gain Variation vs RF Signal Overdrive



OVERALL PERFORMANCE: ISOLATION CHARACTERISTICS

$4.5 \leq V_{CC} = V_{CCMX} \leq 5.5V$, Test Fig. 1, unless otherwise specified





SPECIFICATIONS

The goal of the Specifications section of the datasheet is to provide information on the NE/SA600 in such a way that the designer can estimate statistical variations, and can reproduce the measurements. To this end the high frequency measurements are specified with a particular PC board layout. Variations in board layout will cause parameter variations (sensitive parameters are discussed in the sections on the LNA and mixer below). For many RF parameters the ±3 sigma limits are specified. Statistically only 0.26% of the units will be outside these limits.

The LNA + mixer conversion gain is measured with an incident 900MHz signal and a 83MHZ SAW filter at the IF output. This measurement along with a gain measurement of the LNA ensure the correct operation of the chip and also allows a calculation of mixer conversion gain.

PIN DESCRIPTIONS AND OPERATIONAL LIMITS

RF_{INA}

Input of LNA, AC coupling required, DC = 0.78V, frequency range from DC to 2GHz, gain at low frequencies is 40dB — so be careful of overload, impedance below 50Ω, shunt 15-18nH inductor helps input match and noise figure.

RF_{OUTA}

Output of LNA, AC coupling required, DC = 1.27V, frequency range from DC to 2GHz, impedance above 50Ω.

BYPASS

Bypass capacitor should be 100 times larger than the largest signal coupling capacitor for the LNA, DC = 1.05V.

RF_{INMX}

Mixer RF port, AC coupling required, DC = 1.43V, frequency range from 100MHz to 2.5GHz, impedance close to 50Ω resistive.

LO_{IN}

Mixer LO port, AC coupling required, DC=3.35V, frequency range from 100MHz to 2.5GHz, impedance close to 50Ω resistive.

IF_{OUT}

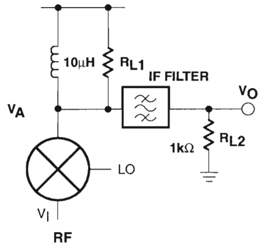
Mixer IF port, open-collector output with 1.6mA DC, frequency range DC to 1GHz, impedance approximately 1pF capacitive.

Enable

TTL/CMOS compatible input. Bias current approximately zero.

CONVERSION GAIN DEFINITIONS

Referring to the figure above, we define the ratio of V_A (at the IF frequency) to V_I (at the RF frequency) to be the Available Voltage Conversion Gain, or more simply Voltage Conversion Gain,



$$VG_C = 20\log\left(\frac{V_A}{V_I}\right)$$

where V_A and V_I are expressed in similar voltage units (such as peak-to-peak). The voltage output V_A is decreased by the IF Filter loss (and any other matching required). Typically, VG_C is 10.4dB for the NE/SA600 mixer with the net IF impedance equal to 500Ω.

It is more common to express the conversion gain in terms of power, so we have the Power Conversion Gain,

$$PG_C = 10\log\left(\frac{P_A}{P_I}\right) - 3dB$$

where $P_A = V_A^2 / R_{IF}$ and $P_I = V_I^2 / R_{RF}$. R_{IF} is the net resistance at the IF frequency at the IF port, and R_{RF} is the input impedance at the mixer RF port. With a 500Ω IF impedance and a 50Ω RF input impedance, the conversion gain works out to –2.6dB typically. The power delivered to the load is down 3dB with respect to the available power because of loss in R_{L1}.

THEORY OF OPERATION

The NE/SA600 is fabricated on the Philips Semiconductors advanced QUBiC technology that features 1µm channel length MOSFETs and 13GHz FT bipolar transistors.

LNA

The Low Noise Amplifier (LNA) is a two stage design incorporating feedback to stablize the amplifier. An external bypass capacitor of (typically) 0.01µF is used. The inputs and outputs are matched to 50Ω. The amplifier has two gain states: when the ENABLE pin is taken high, the amplifier draws 9mA of current and has 16dB of gain at 900MHz. When the ENABLE pin is low, the amplifier current goes to zero, and the amplifier is replaced by a thru. Typical loss for the thru is 7dB. This dual-gain state approach can be used in bang-bang control systems to achieve a low gain, high overload front-end as well as the more usual high gain, low overload front-end.

The amplifier has gain to frequencies past 2GHz, but a practical upper end is 1.6-1.7GHz. Both the input match and the noise figure (NF) can be improved with a shunt 15-18nH inductor at the input. Typically, the gain increases 0.4dB, the match improves to 13-16dB, and the noise figure drops to 1.95-2dB. Variations of any of the RF parameters with V_{CC} is negliglible, and variation with temperature is minimal.

Mixer

The mixer is a single-balanced topology designed to draw very low current, typically 4mA, and provide a very high input third-order intermodulation intercept point , typically IP3=+6dBm. The RF and LO ports impedances are nearly 50Ω resistive, and the IF output is an open collector. The open-collector output allows direct interfacing with high impedance IF filters, such as surface acoustic wave (SAW) filters without the need for external step-up transformers (which are needed for 50Ω output mixers).

The basic mixer is functional from DC to well over 2.5GHz, but RF and LO return losses degrade below 100MHz. The IF output can be used from DC to 500MHz or more, although typically the intermediate frequency is in the range 45-120MHz in many 900MHz receivers. To achieve the lowest noise, the LO drive level should be increased as high as possible, consistent with power dissipation limitations.

POWER SUPPLY ISSUES

V_{CC} bypassing is important, but not extremely critical because of the internal supply regulation of the NE/SA600. The Pin 1 V_{CC} supplies the LNA and powers overhead circuitry. Typical current draw is 9.8mA while enable is high (1mA powered down). The Pin 14 V_{CCMX} powers the mixer and typically has 3.2mA of current (assuming an inductor biasing the IFout back to V_{CCMX}). Care must be taken to avoid bringing any IC pin above V_{CC} by more than 0.3V, or below any ground by more than 0.3V. For example, this can occur if the enable pin is fed from a microcontroller that is powered up quicker than the NE/SA600. In this condition the internal electrostatic discharge (ESD) protection network may turn-on, possibly causing a part misfunction. Generally this condition is reversible, so long as the source creating the overstress is current limited to less than 100mA. To avoid the problem, make sure both V_{CC} pins are tied together near the IC, and install a 1kΩ resistor in series with the enable pin if it is likely to go above V_{CC}.

BOARD LAYOUT CONSIDERATIONS

The LNA is sensitive to mutual inductance from the input to ground. Therefore long narrow input traces will degrade the input match. Ideally, a top side ground-plane should be employed to maximize LNA gain and minimize stray coupling (such as LO to antenna). To avoid amplifier peaking, the output and input grounds should not be run together. Attach both grounds to a solid ground plane. A solid ground plane beneath the package will maximize gain. Top side to back side ground through holes are highly recommended.

The mixer is relatively insensitive to grounding. Care should be taken to minimize the capacitance on the RF port (Pin 11) for best noise figure. Also, the capacitance on the IFout pin must be kept small to avoid conversion gain rolloff when using high IF frequencies. The purpose of the inductor from IFout to V_{CC} is to set the midpoint of the IF swing to be V_{CC}. Without this inductor the part is sensitive to output overload under low V_{CC} (V_{CC} = 4.5V) and hot temperature conditions. The V_{CCMX} pin must be kept at the same potential as the V_{CC} pin.

APPLICATIONS INFORMATION

The NE/SA600 is a high performance, wide-band, low power, low noise amplifier (LNA) and mixer circuit integrated in a BiCMOS technology. It is ideally suited for RF receiver front-ends for both analog and digital communications systems.

There are several advantages to using the NE/SA600 as a high frequency front-end block instead of a discrete implementation. First is the simplicity of use. The NE/SA600 does not need any external biasing components. Due to the higher level of integration and small footprint (SO14) package it occupies less space on the printed circuit board and reduces the manufacturing cost of the system. Also the higher level of integration improves the reliability of the LNA and mixer over a discrete implementation with several components.

The LNA thru mode in NE/SA600 helps reduce power consumption in applications where the amplifiers can be disabled due to higher received signal strength (RSSI). Other advantages of this feature are described later in this section.

The mixer is an active mixer with excellent conversion gain at low LO input levels, so LO levels as low as -5dBm to -10dBm can be used depending on the applications requirement for mixer gain, mixer noise figure and mixer third order intercept point. This reduces the LO drive requirements from the VCO buffer, thus reducing its current consumption. Also, due to lower LO levels, the shielding requirements can be minimized or eliminated, resulting in substantial cost savings and weight and space reduction.

And last but not least, is the impedance matching at LNA inputs and outputs and mixer RF and LO input ports. Only those who have toiled through discrete transistor implementations for 50Ω input and output impedance matching can truly appreciate the elegance and simplicity of the NE/SA600 input and output impedance matching to 50Ω. Also, the mixer output impedance is high, so matching to a crystal or SAW IF filter becomes extremely easy without the need for additional IF impedance transformers (tapped-C networks with inductors or baluns).

The NE/SA600 applications and demo board features standard low cost 62mil FR-4 board. A top-side ground plane is used and 50Ω coplanar transmission lines are used. LO and RF_{INA} traces are perpendicular. Provisions for the image reject filter between RF_{OUTA} and RF_{INMX} are provided. A simple LC match for 80MHz IF is used so that 50Ω measurements can be made on the demo board.

The NE/SA600 applications evaluation board schematic is shown in Figure 1. The V_{CC} (Pin 1) and V_{CCMX} (Pin 14) are tied together and the power supply is bypassed with capacitors C5 and C6. These capacitors should be placed as close to the device as practically possible.

C1 is the DC blocking capacitor to the input of the LNA. L1 provides additional input matching to the LNA for an improved return loss (S11). This inductor can be a surface-mount component or can be easily drawn on the printed circuit board (small spiral or serpentine). This additional match improves the gain of the LNA by 0.4dB and lowers the noise figure to 2dB or less. If the typical gain of the LNA of 16dB is acceptable with 2.2dB of noise figure, then L1 can be eliminated. If the LNA input is fed from a duplexer or selectivity filter after the antenna, C1 can also be eliminated since the filter will also provide DC blocking. The LNA bypass capacitor C3 should be at least 100 times C1 or C9 for low frequency stability. Switch S1 toggles the LNA gain/through function. R1 is used only to limit the maximum current into the enable pin and only necessary if enable may power up before the V_{CC}.

C4 is a DC blocking capacitor for the LO input pin and may not be needed in actual applications if the VCO output is isolated and will not upset the internal DC biasing of the mixer. The image reject filter goes between the output of the LNA and the RF input to the mixer. Since the LO input, RF output and mixer input are all 50Ω matched impedances internally, there is no need for any external components. C8 and C9 are DC blocking capacitors to the connectors and will not be needed in an actual application.

R2 and L2 are the load to the mixer output which is typical of the IF crystal or SAW filters. C2 and L3 provide a match from the high impedance mixer output to a 50Ω test set-up (spectrum analyzer, etc.) and C7 is a DC blocking capacitor for the mixer output.

The printed circuit board layout for the schematic of Figure 1 is shown in Figure 3. It is a very simple printed circuit board layout with all the components on a single side. The layout also accomodates a two pole image reject filter between the LNA outupt and mixer input. All the input and output traces to the LNA and mixer should be 50Ω tracks with the exception of mixer output, which can be very narrow due to the higher impedances of the filter.

The NE/SA600 internal supply is very well regulated. This is seen from Figure 4 which shows the I_{CC} vs. V_{CC} for the NE/SA600. Table 1 shows the S11, S21, S22 and S21 for the LNA from 800-1200MHz. Typical measurements at 900MHz for the critical parameters such as gain, noise figure, IP_3, 1dB compression point, etc. as measured on an applications evaluation board are as follows :

LNA gain = 16.5dB
LNA through = –7dB
Mixer gain =–3dB (into a 50Ω load)
LNA noise figure = 2dB
Mixer noise figure = 14dB
LNA IP_3 = –10dBm (in gain mode)
LNA IP_3 = +26dBm (in through mode)
LNA 1dB compression point = –20dBm
Mixer 1dB compression point = –4dBm

The shunt inductor L1 for input match is optional. Figure 5 shows the effect of the inductor value from 8.2nH to 15nH on gain, noise figure and input match.

The total power gain for the LNA and mixer (excluding the image reject filter) in a system where the output of the mixer is loaded with 50Ω is about 14dB. In an actual system the output impedance of the mixer is usually much higher than 50Ω (more like 1kΩ or higher) and so it is more important to consider the voltage gain from the input at the LNA to the mixer output. The voltage gain in this case will be about 29.85V/V. The total noise figure for the LNA and mixer combination is be about 3.27dB. The input third order intercept point for the LNA and mixer is about -11dBm. In the LNA through mode, the intercept point for the combination is higher than +19dBm. This LNA through feature provides an additional boost to the total dynamic range of the system.

The NE/SA600 finds applications in many areas of RF communications. It is an ideal down converter block for high performance, low cost, low power RF communications transceivers. The front-end of a typical AMPS/TACS/NMT/TDMA/CDMA cellular phone is shown in Figure 2. This could also be the front-end of a VHF/UHF handheld transceiver, UHF cordless telephone or a spread spectrum system.

The antenna is connected to the duplexer input. The receiver output of the duplexer is connected to the RF input of the LNA. If the additional improvement in noise figure and gain are not needed to meet the system specifications then L1 and C1 can be eliminated. In TDMA systems, the NE/SA600 can be totally powered down by Q1 and the two resistors. In this mode the current consumption will be zero mA. Care should be taken in the software of the system to insure that the enable pin on NE/SA600 tied to the LNA gain control port is held low while the device is in total power down mode. L2 and C2 can be tuned to the IF frequency and to match to the IF filter impedance.

A complete analysis of the front-end shows that the total voltage gain from the antenna input to the mixer output is about 9.5V/V. This value includes a 3.2dB loss for the duplexer and a 1.8dB loss for the bandpass filter. The noise figure as referred to the antenna is 7dB and the input third order intercept point is about -7.5dBm. In LNA through mode the input third order intercept point increases to about +24dBm.

During normal operation of a handheld RF receiver the received signal strength (RSSI) is nominally greater than -100dBm. The signal only drops below this level due to severe multipath fading, shadow effect or when the receiver is at extreme fringes of cell coverage. The LNA through mode can be used here as a two step gain control such that when RSSI is below a certain threshold level (e.g. -90dBm), the LNA has a -7dB loss and the total current consumption of the NE/SA600 is only 4.3mA. The sensitivity of the system will not suffer because the received RF signal is much higher than the noise floor of the system. When the RSSI falls below a certain threshold (e.g. -95dBm) the LNA is enabled to give the full

16.5dB of gain with 2dB of noise figure. In this mode the current consumption is increased to 13mA. But for hand-held equipment, the average current consumption will be closer to 5-6mA. The other advantage of the LNA through mode besides power savings is the input overload characteristics. Due to the much higher input third order intercept point of the LNA (+26dBm), the receiver is immune to strong adjacent channel interference. Implementing this feature with an FM/IF device such as the NE625/7 with fast RSSI response and a window comparator toggling the LNA mode of NE/SA600, a fast two-step AGC with response time less than 10µs can be achieved. This is a very useful feature to equalize multipath fading effects in a mobile radio system.

In conclusion, the NE/SA600 offers higher level of integration, higher reliability, higher level of performance, ease of use, simpler system design at a cost lower than the discrete multi-transistor implementations. In addition, the NE/SA600 provides unique features to enhance receiver performance which are almost unattainable with discrete implementations.

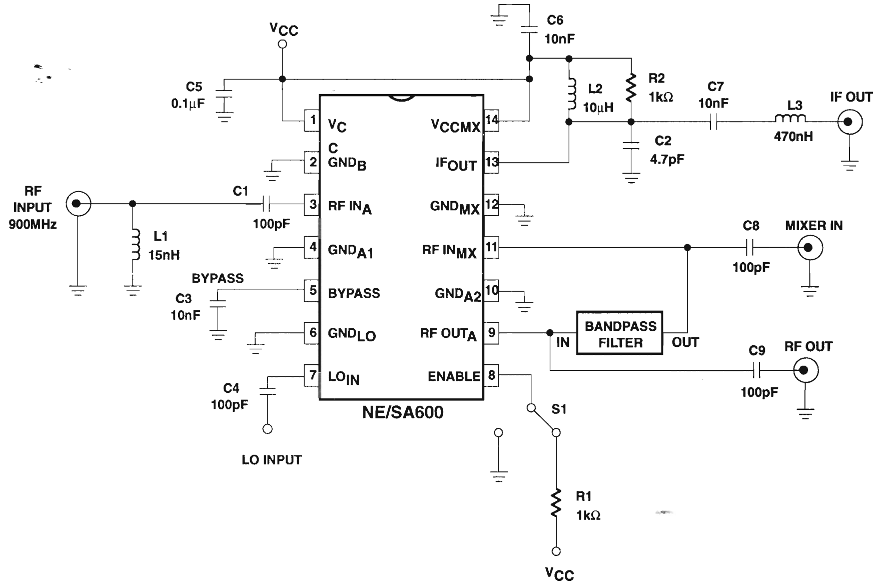


Figure 1.

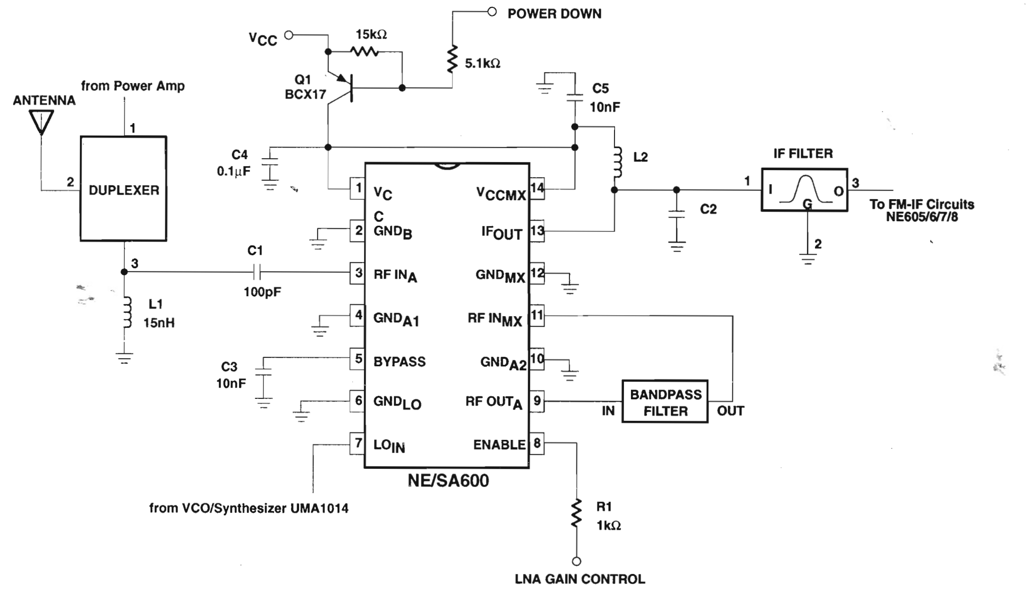

POWER DOWN
VCC
15kΩ
5.1kΩ
Q1
BCX17
C5
10nF
ANTENNA
from Power Amp
1
2
DUPLEXER
3
C4
0.1µF
L2
IF FILTER
1
I
O
G
3
2
To FM-IF Circuits
NE605/6/7/8
C2
1 VCC
2 GNDB
3 RF INA
4 GNDA1
5 BYPASS
6 GNDLO
7 LOIN
14 VCCMX
13 IFOUT
12 GNDMX
11 RF INMX
10 GNDA2
9 RF OUTA
8 ENABLE
NE/SA600
C1
100pF
L1
15nH
C3
10nF
BANDPASS FILTER
IN
OUT
from VCO/Synthesizer UMA1014
R1
1kΩ
LNA GAIN CONTROL

Figure 2.

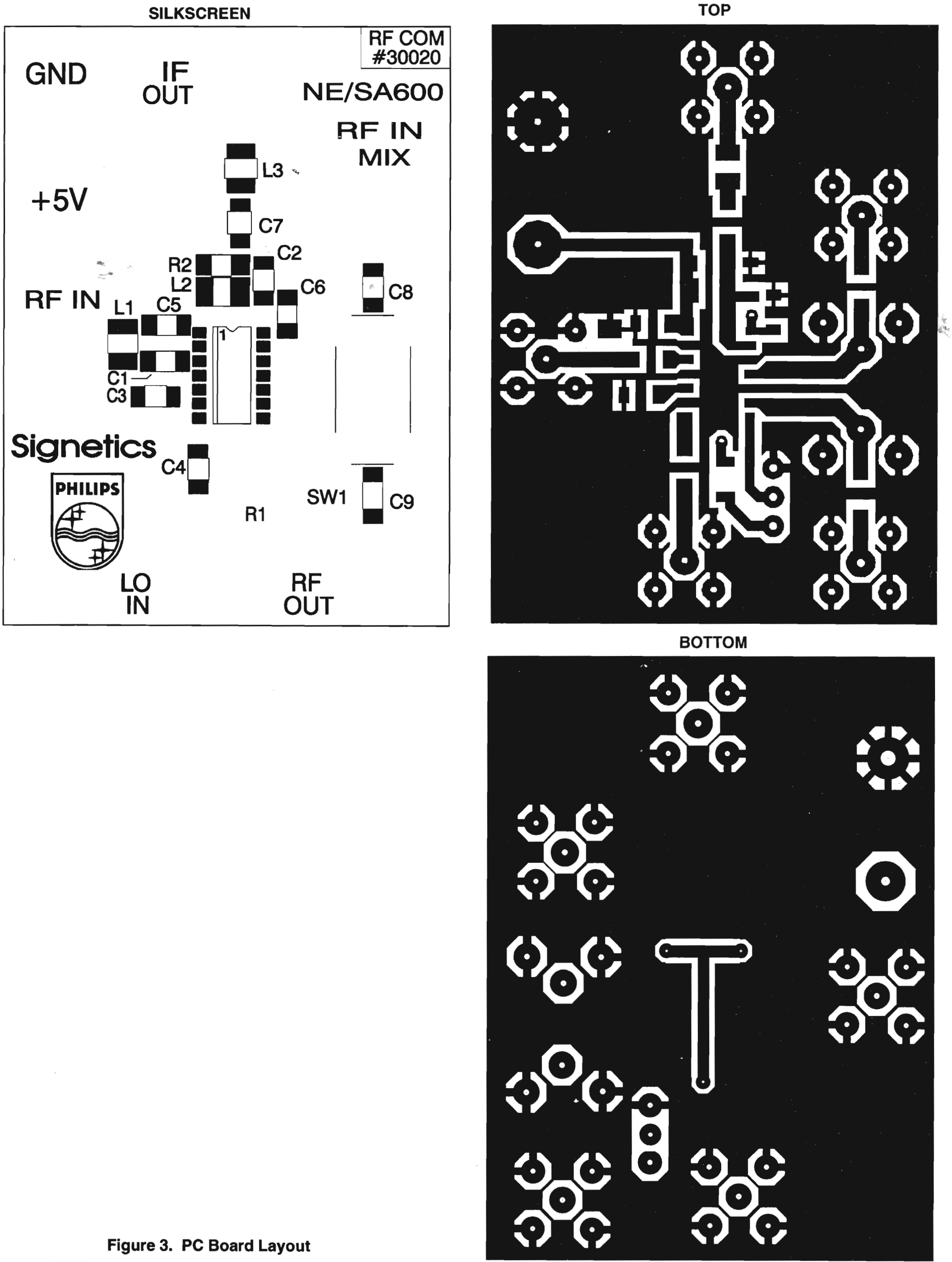


Figure 3. PC Board Layout

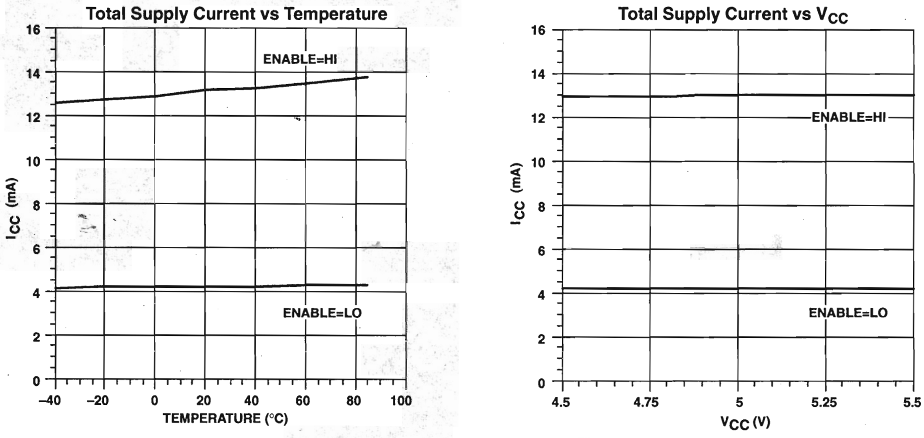


Figure 4.

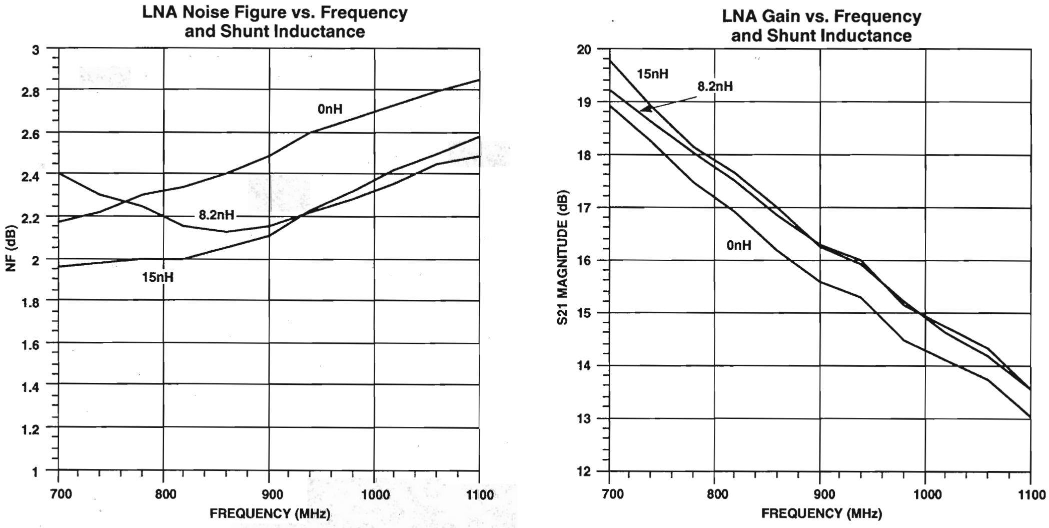


Figure 5.

Low voltage LNA and mixer - 1GHz

SA601

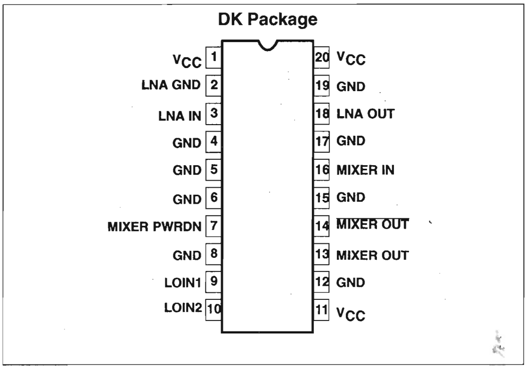
DESCRIPTION

The SA601 is a combined RF amplifier and mixer designed for high-performance low-power communication systems from 800-1200MHz. The low-noise preamplifier has a 1.6dB noise figure at 900MHz with 11.5dB gain and an IP3 intercept of -2dBm at the input. The gain is stabilized by on-chip compensation to vary less than ±0.2dB over -40 to +85°C temperature range. The wide-dynamic-range mixer has a 9.5dB noise figure and IP3 of –2dBm at the input at 900MHz. The nominal current drawn from a single 3V supply is 7.4mA. The Mixer can be powered down to further reduce the supply current to 4.4mA.

FEATURES

- Low current consumption: 7.4mA nominal, 4.4mA with the mixer powered-down
- Outstanding LNA noise figure: 1.6dB at 900MHz
- High system power gain: 18dB (LNA + Mixer) at 900MHz
- Excellent gain stability versus temperature and supply voltage
- External >-7dBm LO can be used to drive the mixer

PIN CONFIGURATION



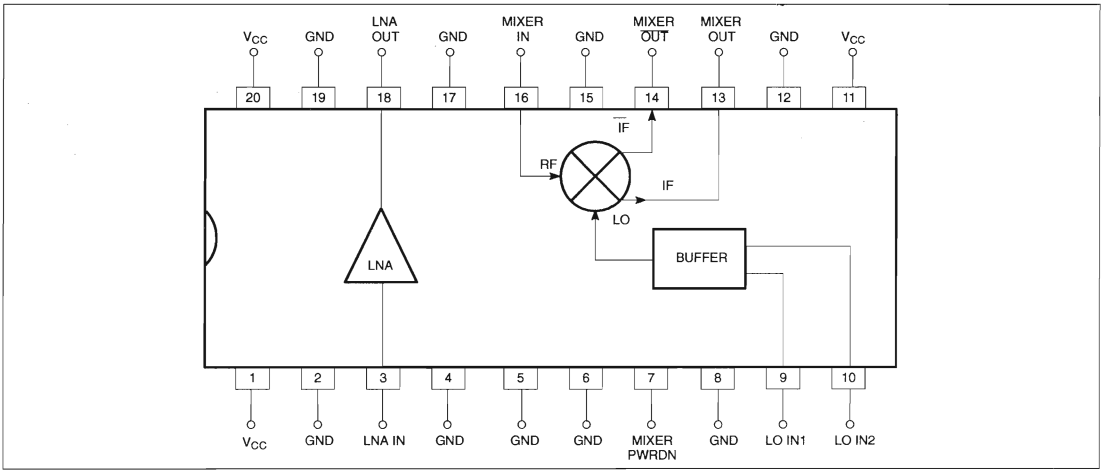
APPLICATIONS

- 900MHz cellular front-end (NADC, GSM, AMPS, TACS)
- 900MHz cordless front-end (CT1, CT2)
- 900MHz receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (Surface-mount, SSOP)	-40 to +85°C	SA601DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[3]

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[1]	-0.3 to +6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 20-Pin Plastic SSOP	980	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 8V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}: 20-Pin SSOP = 110°C/W
3. Pins 9 and 10 are sensitive to electrostatic discharge (ESD).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	2.7 to 5.5	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{CC}	Supply current			7.4		mA
		Mixer power-down input low		4.4		
V_{LNA-IN}	LNA input bias voltage			0.78		V
$V_{LNA-OUT}$	LNA output bias voltage			2.1		V
V_{MX-IN}	Mixer RF input bias voltage			0.94		V

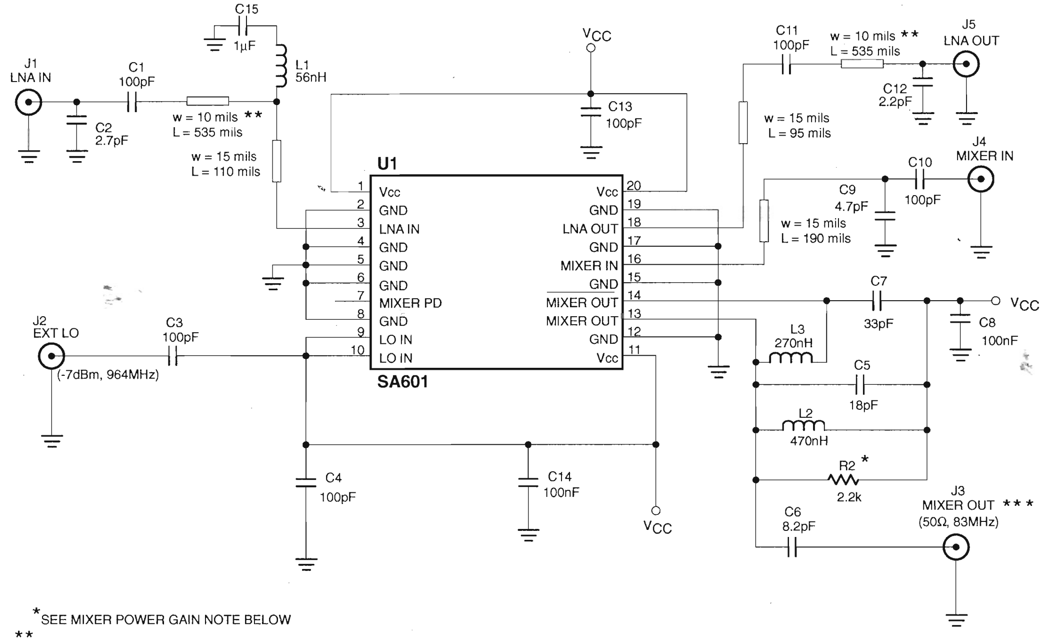
AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; LO_{IN} = -7dBm @ 964MHz; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			-3σ	TYP	+3σ	
S_{21}	Amplifier gain	881MHz	10	11.5	13	dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	881MHz		0.003		dB/°C
$\Delta S_{21}/\Delta f$	Gain frequency variation	800MHz - 1.2GHz		0.01		dB/MHz
S_{12}	Amplifier reverse isolation	881MHz		-20		dB
S_{11}	Amplifier input match[1]	881MHz		-10		dB
S_{22}	Amplifier output match[1]	881MHz		-10		dB
P_{-1dB}	Amplifier input 1dB gain compression	881MHz		-16		dBm
IP3	Amplifier input third order intercept	$f_2 - f_1$ = 25kHz, 881MHz	-3.5	-2	-0.5	dBm
NF	Amplifier noise figure	881MHz	1.3	1.6	1.9	dB
VG_C	Mixer voltage conversion gain: $R_P = R_L = 1k\Omega$	f_S = 881MHz, f_{LO} = 964MHz, f_{IF} = 83MHz	18.0	19.5	21.0	dB
PG_C	Mixer power conversion gain: $R_P = R_L = 1k\Omega$	f_S = 881MHz, f_{LO} = 964MHz, f_{IF} = 83MHz	5.0	6.5	8.0	dB
S_{11M}	Mixer input match[1]	881MHz		-10		dB
NF_M	Mixer SSB noise figure	881MHz	8.0	9.5	11.0	dB
P_{-1dB}	Mixer input 1dB gain compression	881MHz		-13		dBm
$IP3_M$	Mixer input third order intercept	$f_2 - f_1$ = 25kHz, 881MHz	-3.5	-2	-0.5	dBm
IP_{2INT}	Mixer input second order intercept	881MHz		12		dBm
P_{RFM-IF}	Mixer RF feedthrough	881MHz		-7		dB
P_{LO-IF}	LO feedthrough to IF	881MHz		-25		dB
P_{LO-RFM}	LO to mixer input feedthrough	881MHz		-38		dB
P_{LO-RF}	LO to LNA input feedthrough	881MHz		-40		dB
$P_{LNA-RFM}$	LNA output to mixer input	881MHz		-40		dB
P_{RFM-LO}	Mixer input to LO feedthrough	881MHz		-23		dB
LO_{IN}	LO drive level	964MHz		-7		dBm

NOTE:

1. Simple L/C elements are needed to achieve specified return loss.



*SEE MIXER POWER GAIN NOTE BELOW

** SPIRAL INDUCTORS ON NATURAL FR-4, 62 MILS THICK

*** SEE MIXER FILTER INTERFACE NOTE BELOW

Figure 1. Application Circuit

CIRCUIT TECHNOLOGY

LNA

Impedance Match: Intrinsic return loss at the input and output ports is 7dB and 9dB, respectively. With no external matching, the associated LNA gain is ≈10dB and the noise figure is ≈1.4dB. However, the return loss can be improved at 881MHz using suggested L/C elements (Figure 1) as the LNA is unconditionally stable.

Noise Match: The LNA achieves 1.6dB noise figure at 881MHz when S_{11} = -10dB. Further improvements in S_{11} will slightly decrease the NF and increase S_{21}.

Temperature Compensation: The LNA has a built-in temperature compensation scheme to reduce the gain drift to 0.003dB/°C from –40°C to +85°C.

Supply Voltage Compensation: Unique circuitry provides gain stabilization over wide supply voltage range. The gain changes no more than 0.5dB when V_{CC} increases from 3V to 5V.

LO Drive Level: Resistor R1 can be replaced by an inductor of 4.7nH and C13 should be adjusted to achieve a good return loss at the LO port. Under this condition, the mixer will operate with less than -10dBm LO drive.

IP3 Performance: C9 between Pin 16 and ground can be removed to introduce 3dB mismatch loss, while improving the IP3 to +3dBm. The associated noise figure is 11dB.

Mixer

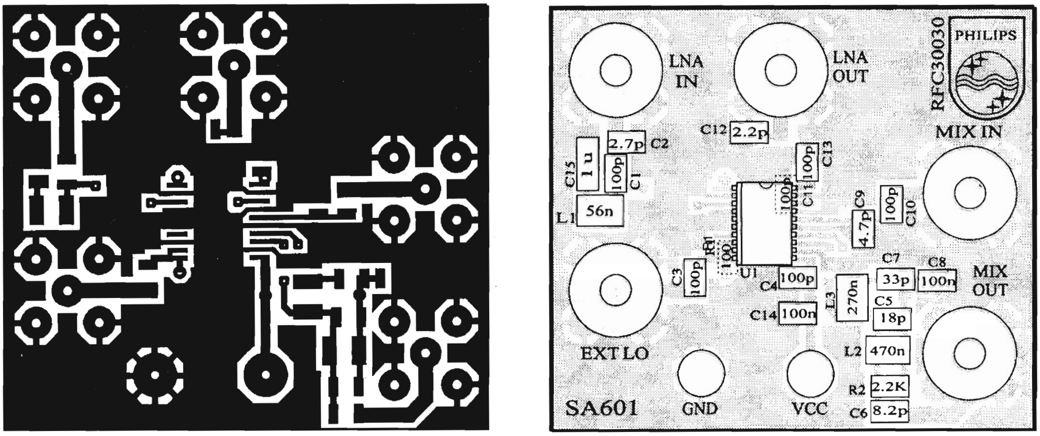
Input Match: The mixer is configured for maximum gain and best noise figure. The user needs to supply L/C elements to achieve this performance.

Power Gain: The gain can be increased by approximately 1.5dB by placing R2 across C7, instead of C5.

Power Down: The mixer can be disabled by connecting Pin 7 to ground. When the mixer is disabled, 3mA is saved.

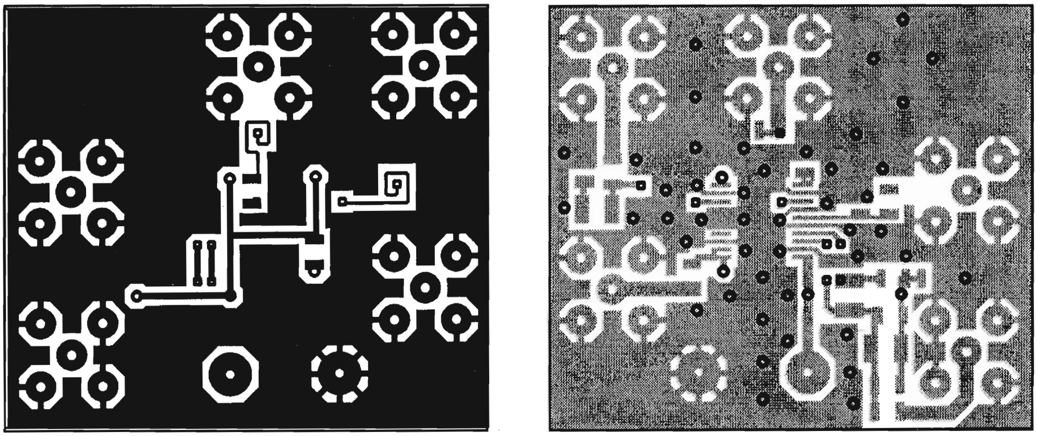
Power Combining: The mixer output circuit features passive power combining (patent pending) to optimize conversion gain and noise figure performance without using extra DC current or degrading the IP3. For IF frequencies significantly different than 83MHz, the component values must be altered accordingly.

Filter Interface: For system integration where a high impedance filter of 1kΩ is to be cascaded at the mixer IF output, capacitors C5 and C6 need to be changed to 27pF and 1000pF, respectively.



Top View

Silk Screen



Bottom View

Via Layer

Figure 2. SA601 Demoboard Layout (Not Actual Size)

TYPICAL PERFORMANCE CHARACTERISTICS

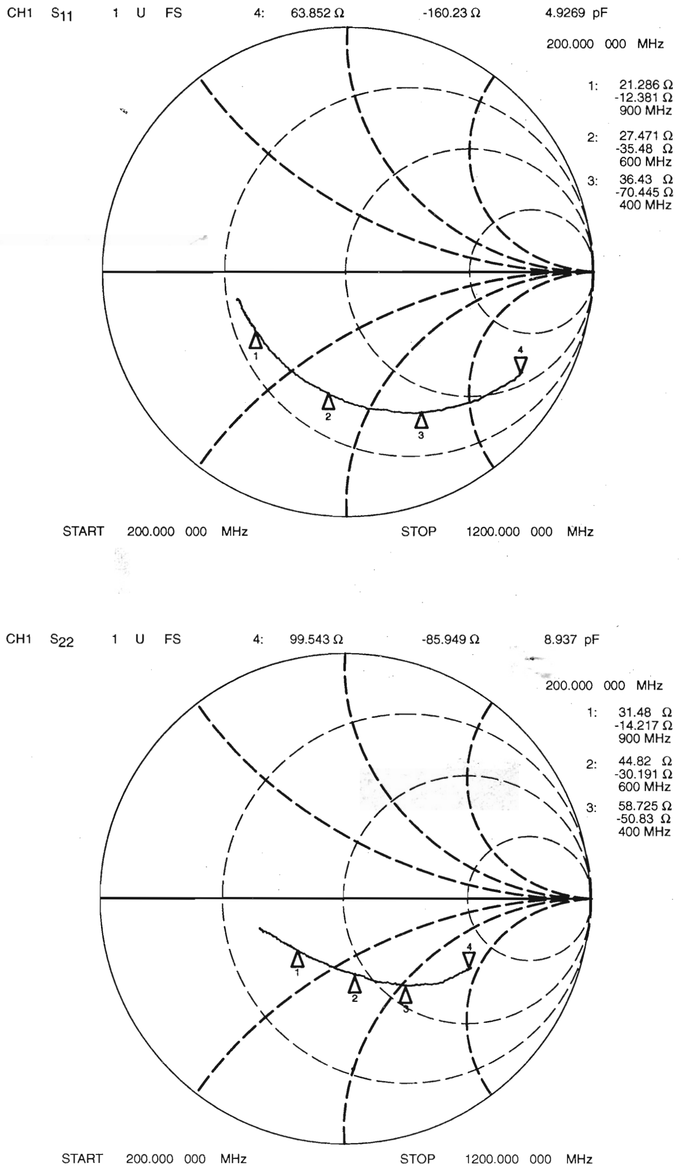


Figure 3. LNA Input and Output Match (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

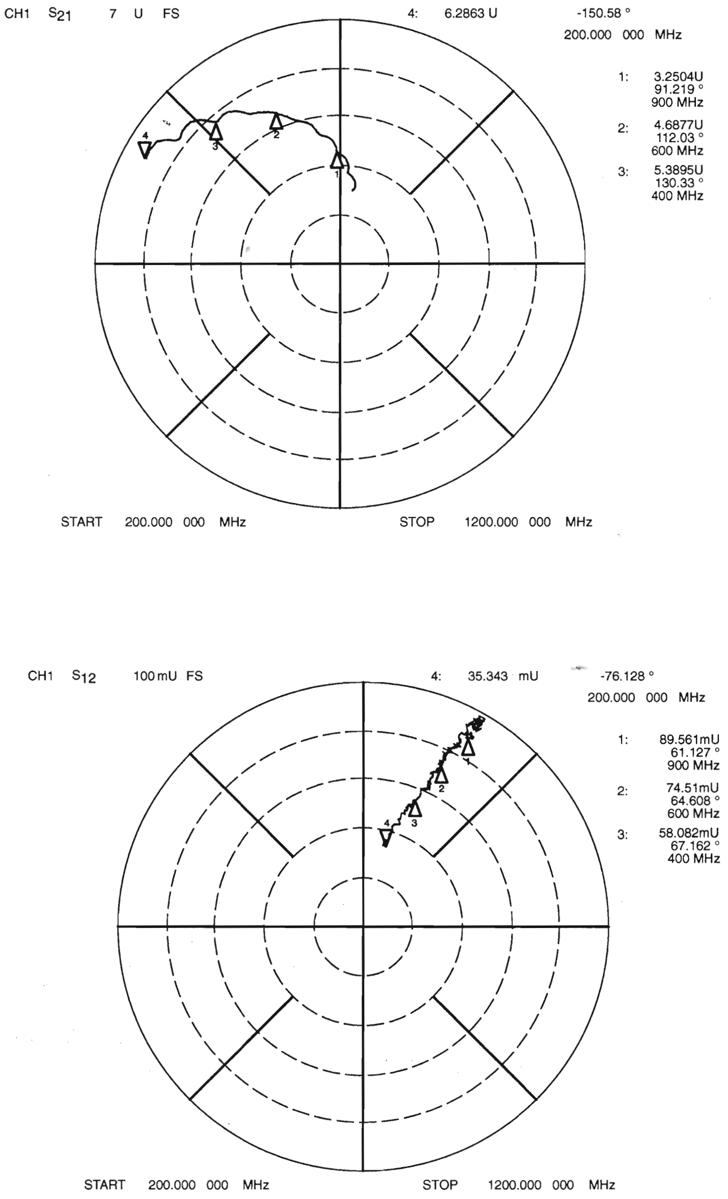


Figure 4. LNA Transmission and Isolation Characteristics (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

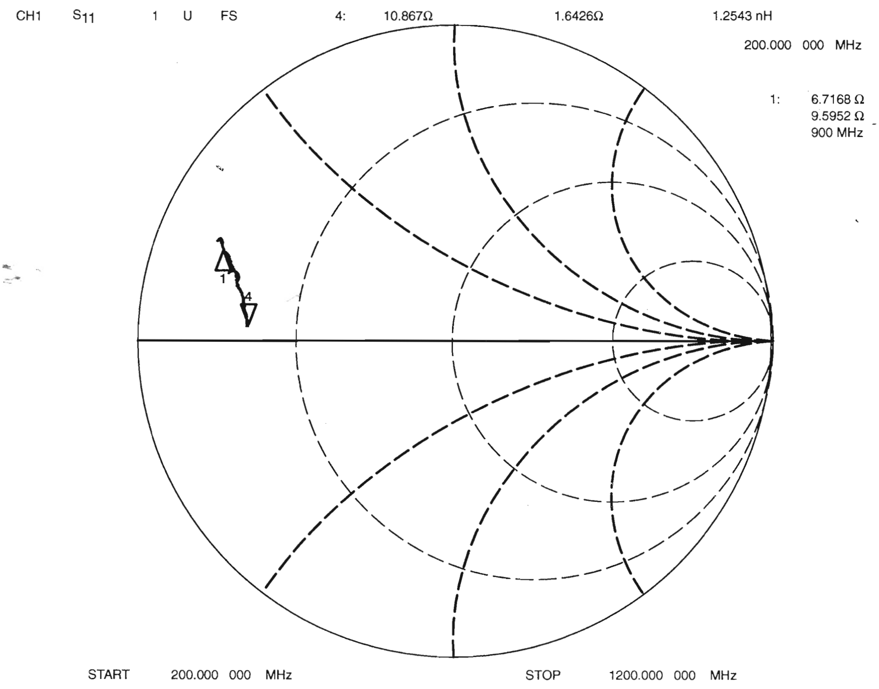


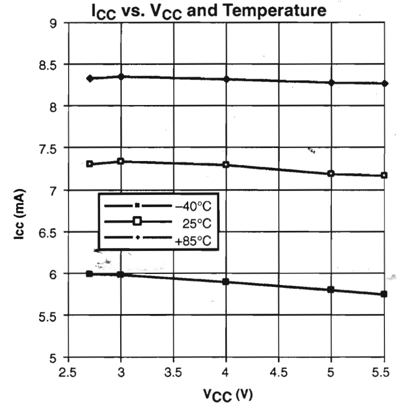
Figure 5. Mixer RF Input Match (at Device Pin)

Table 2. Typical LNA and Mixer S-Parameters

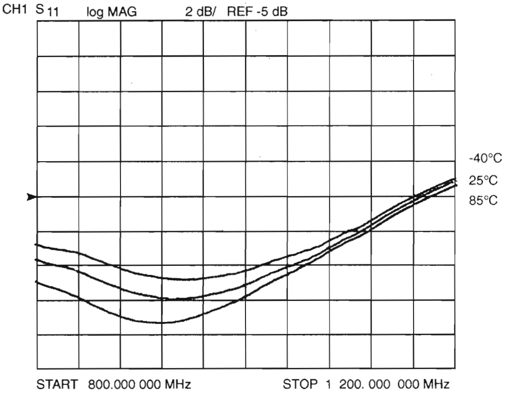
	LNA				Mixer
f	S_{11}	S_{22}	S_{21}	S_{12}	S_{11}
200MHz	63.852Ω – j 160.23Ω	99.543Ω – j 85.949Ω	6.2863U ∠ 150.58°	35.343mU ∠ 76.128°	10.867Ω + j 1.6426Ω
300MHz	44.879Ω – j 101.69Ω	73.387Ω – j 67.707Ω	5.8096U ∠ 140.47°	47.946mU ∠ 71.169°	10.4Ω + j 3.4609Ω
400MHz	36.43Ω – j 70.445Ω	58.725Ω – j 50.83Ω	5.3895U ∠ 130.33°	58.082mU ∠ 67.162°	10.067Ω + j 4.897Ω
500MHz	30.395Ω – j 48.393Ω	49.928Ω – j 38.813Ω	5.0428U ∠ 120.5°	66.44mU ∠ 66.388°	9.394Ω + j 6.0142Ω
600MHz	27.471Ω – j 35.48Ω	44.82Ω – j 30.191Ω	4.6877U ∠ 112.03°	74.51mU ∠ 64.608°	8.8945Ω + j 7.2227Ω
700MHz	24.428Ω – j 25Ω	39.268Ω – j 24.502Ω	4.2409U ∠ 104.44°	82.235mU ∠ 65.002°	8.1353Ω + j 8.1597Ω
800MHz	22.434Ω – j 17.255Ω	34.664Ω – j 18.59Ω	3.7491U ∠ 97.765°	86.582mU ∠ 62.743°	7.976Ω + j 9.1958Ω
900MHz	21.286Ω – j 12.381Ω	31.48Ω – j 14.217Ω	3.2504U ∠ 91.219°	89.561mU ∠ 61.127°	6.7168Ω + j 9.5952Ω
1000MHz	20.261Ω – j 8.7109Ω	27.887Ω – j 10.77Ω	2.8785U ∠ 84.957°	95.135mU ∠ 60.539°	6.2393Ω + j 10.271Ω
1100MHz	19.718Ω – j 6.252Ω	25.741Ω – j 8.2607Ω	2.5752U ∠ 82.893°	97.348mU ∠ 62.202°	6.0791Ω + j 10.571Ω
1200MHz	19.101Ω – j 4.9316Ω	23.584Ω – j 6.2715Ω	2.1386U ∠ 80.257°	96.558mU ∠ 61.563°	5.8185Ω + j 10.288Ω

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

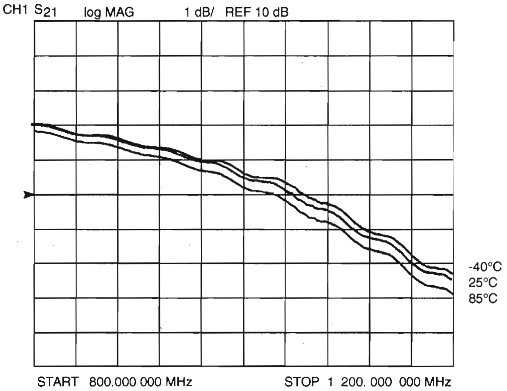
I_{CC} vs. V_{CC} and Temperature



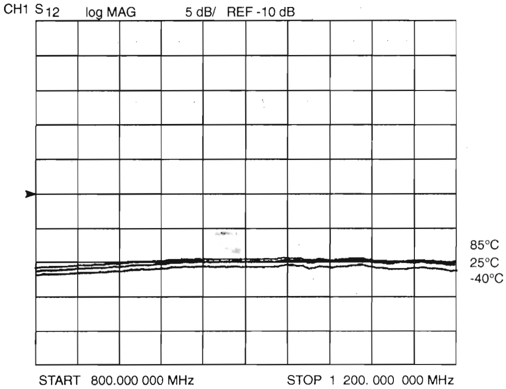
Mixer RF Input Match vs. Frequency (V_{CC} = 3V)



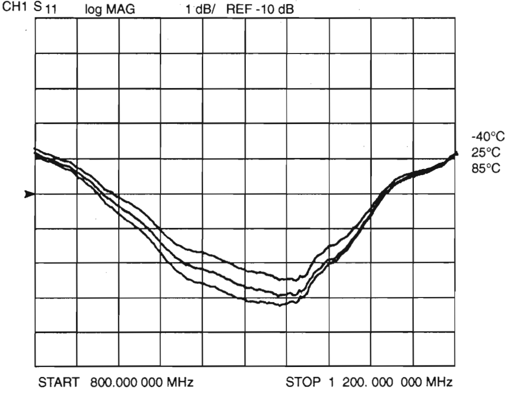
LNA Gain (S_{21}) vs. Frequency (V_{CC} = 3V)



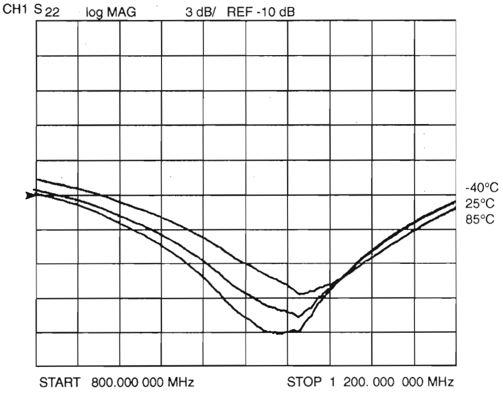
LNA Isolation (S_{12}) vs. Frequency (V_{CC} = 3V)



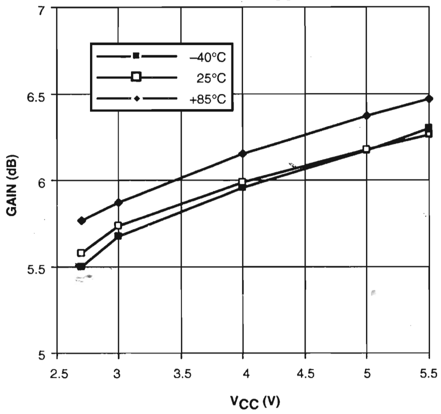
LNA Input Match (S_{11}) vs. Frequency (V_{CC} = 3V)



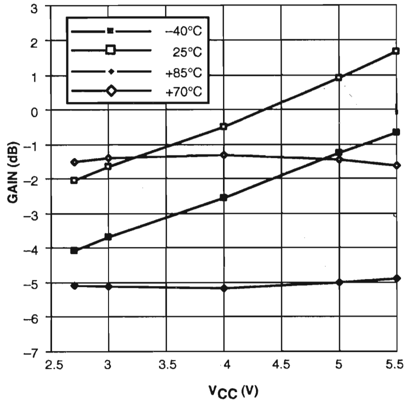
LNA Output Match (S_{22}) vs. Frequency (V_{CC} = 3V)



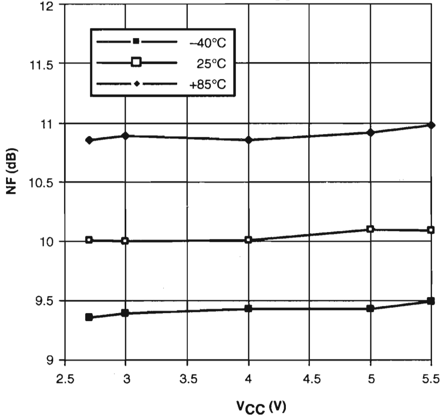
Mixer Gain @ 83MHz vs. V_{CC} and Temperature



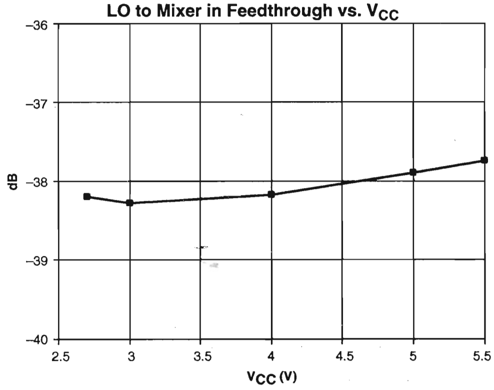
Mixer IP3 @ 83MHz vs. V_{CC} and Temperature



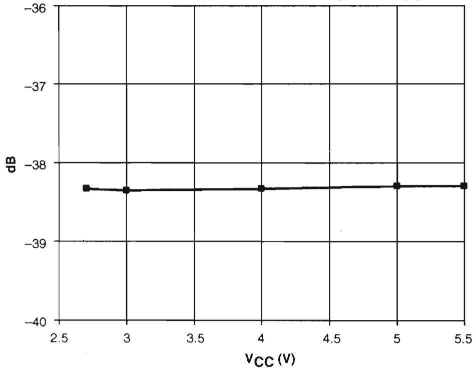
Mixer NF @ 83MHz vs. V_{CC} and Temperature



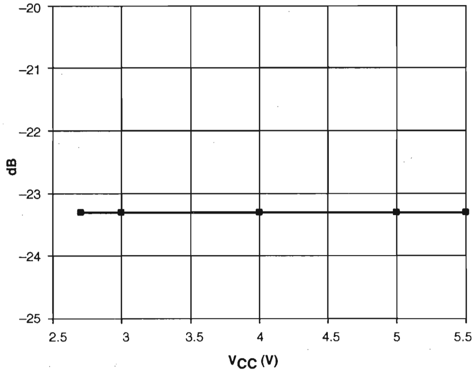
LO to Mixer in Feedthrough vs. V_{CC}



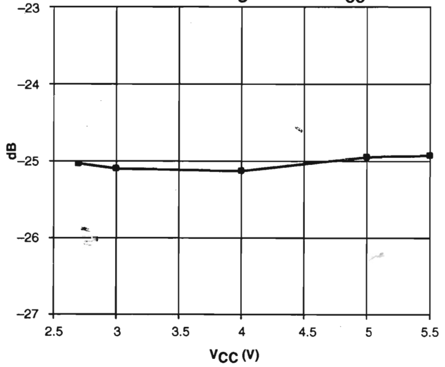
LO to LNA Input Feedthrough vs. V_{CC}



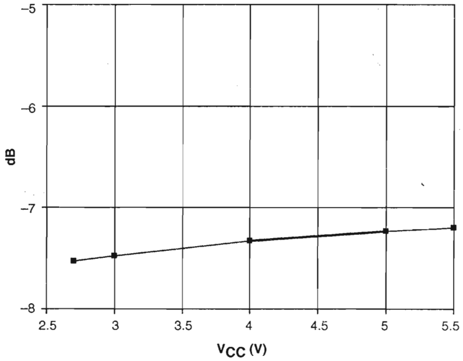
Mixer Input to LO Feedthrough vs. V_{CC}



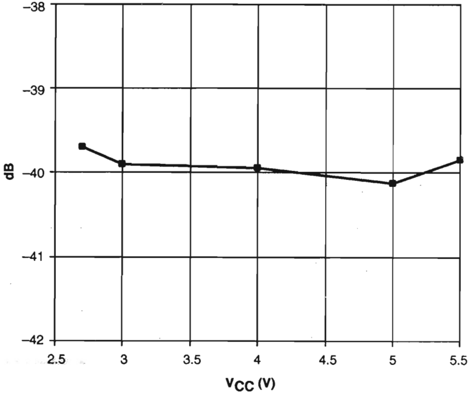
LO Feedthrough to IF vs. V_{CC}



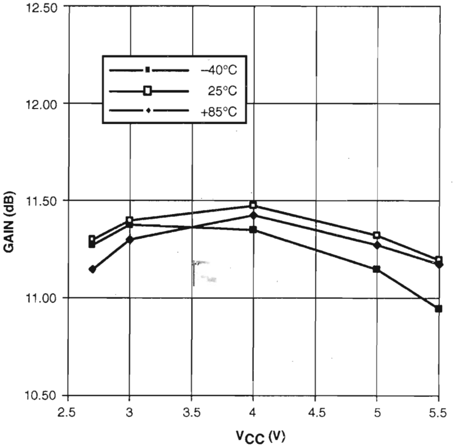
Mixer RF Feedthrough vs. V_{CC}



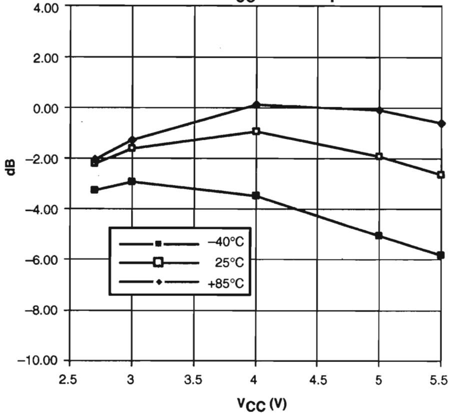
LNA Output to Mixer Input vs. V_{CC}



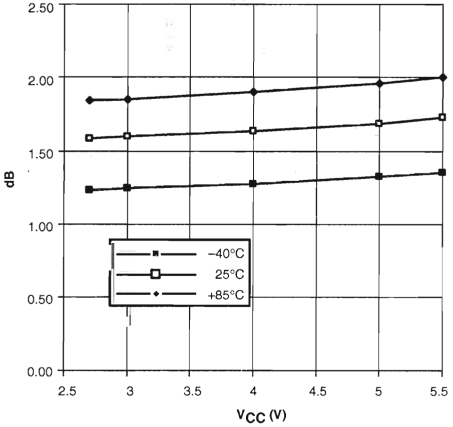
LNA Gain vs. V_{CC} and Temperature



LNA IP3 vs. V_{CC} and Temperature



LNA NF vs. V_{CC} and Temperature



Double-balanced mixer and oscillator NE/SA602A

DESCRIPTION

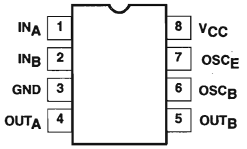
The NE/SA602A is a low-power VHF monolithic double-balanced mixer with input amplifier, on-board oscillator, and voltage regulator. It is intended for high performance, low power communication systems. The guaranteed parameters of the SA602A make this device particularly well suited for cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 18dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external LO. For higher frequencies the LO input may be externally driven. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low-power and noise characteristics make the NE/SA602A a superior choice for high-performance battery operated equipment. It is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface-mount miniature package).

FEATURES

- Low current consumption: 2.4mA typical
- Excellent noise figure: <4.7dB typical at 45MHz
- High operating frequency
- Excellent gain, intercept and sensitivity
- Low external parts count; suitable for crystal/ceramic filters
- SA602A meets cellular radio specifications

PIN CONFIGURATION

F, D and N Packages



APPLICATIONS

- Cellular radio mixer/oscillator
- Portable radio
- VHF transceivers
- RF data links
- HF/VHF frequency conversion
- Instrumentation frequency conversion
- Broadband LANs

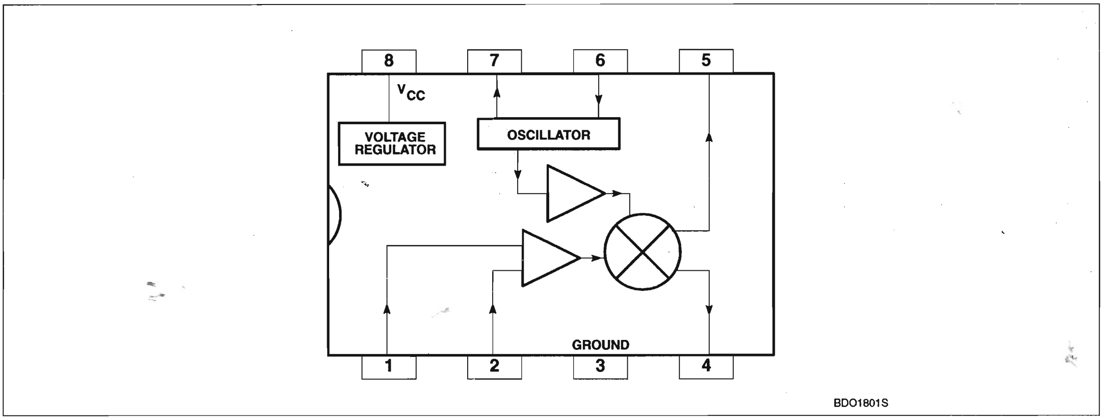
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Plastic (DIP)	0 to +70°C	NE602AN	0404B
8-Pin Plastic Small Outline (SO) package (Surface-mount)	0 to +70°C	NE602AD	0174C
8-Pin Ceramic Dual In-Line Package (Cerdip)	0 to +70°C	NE602AFE	0580A
8-Pin Plastic Dual In-Line Plastic (DIP)	-40 to +85°C	SA602AN	0404B
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA602AD	0174C
8-Pin Ceramic Dual In-Line Package (Cerdip)	-40 to +85°C	SA602AFE	0580A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE602A	0 to +70	°C
	SA602A	-40 to +85	°C
θ_{JA}	Thermal impedance D package	90	°C/W
	N package	75	°C/W

BLOCK DIAGRAM



AC/DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA602A			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	2.8	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figure at 45MHz			5.0	5.5	dB
	Third-order intercept point	RF_{IN} = -45dBm: f_1 = 45.0MHz f_2 = 45.06MHz		-13	-15	dBm
	Conversion gain at 45MHz		14	17		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3	3.5	pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

DESCRIPTION OF OPERATION

The NE/SA602A is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE/SA602A is designed for optimum low power performance. When used with the SA604 as a 45MHz cellular radio second IF and demodulator, the SA602A is capable of receiving -119dBm signals with a 12dB S/N ratio. Third-order intercept is typically -13dBm (that is approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues are not critical, the input to the NE602A should be appropriately scaled.

Besides excellent low power performance well into VHF, the NE/SA602A is designed to be flexible. The input, RF mixer output and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k II 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the "Q" of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required LO is beyond oscillation limits, or the system calls for an external LO, the external signal can be injected at Pin 6 through a DC blocking capacitor. External LO should be at least 200mV$_{P-P}$.

Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cellular radio. As shown, an overtone mode of operation is utilized. Capacitor C3 and inductor L1 suppress oscillation at the crystal fundamental frequency. In the fundamental mode, the suppression network is omitted.

Figure 6 shows a Colpitts varactor tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar transistors provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assure correct system operation.

When operated above 100MHz, the oscillator may not start if the Q of the tank is too low. A 22kΩ resistor from Pin 7 to ground will increase the DC bias current of the oscillator transistor. This improves the AC operating characteristic of the transistor and should help the oscillator to start. A 22kΩ resistor will not upset the other DC biasing internal to the device, but smaller resistance values should be avoided.

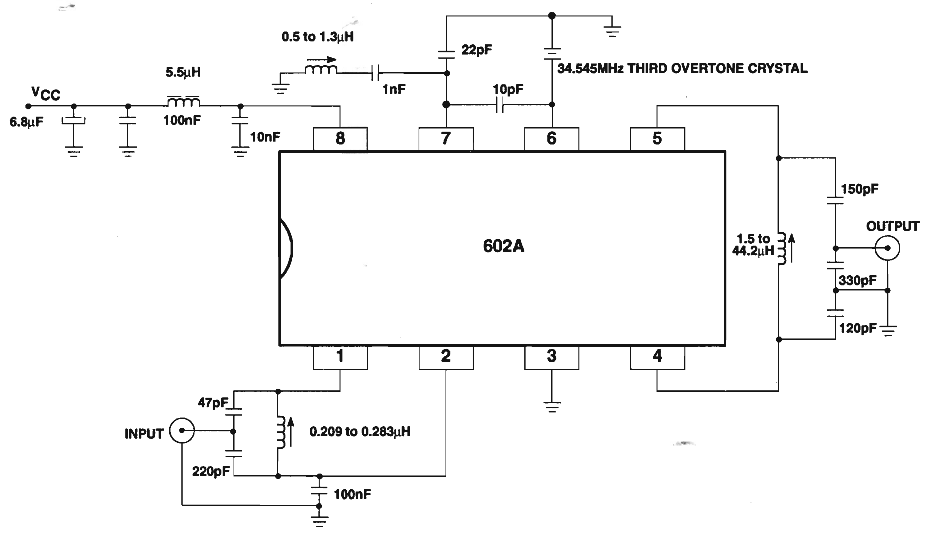


Figure 1. Test Configuration

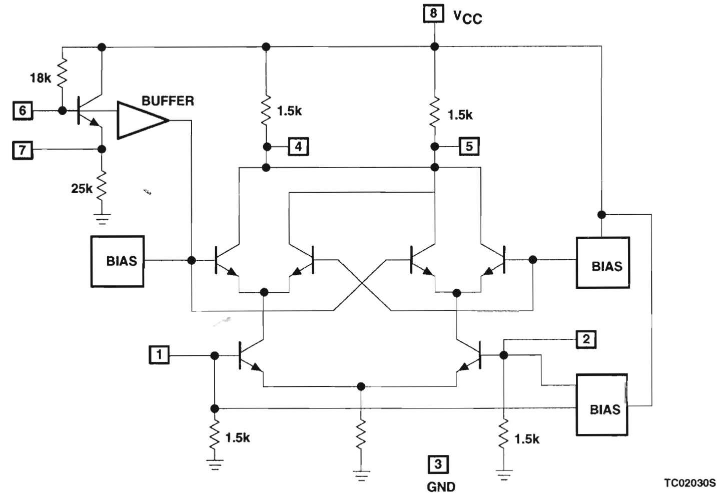
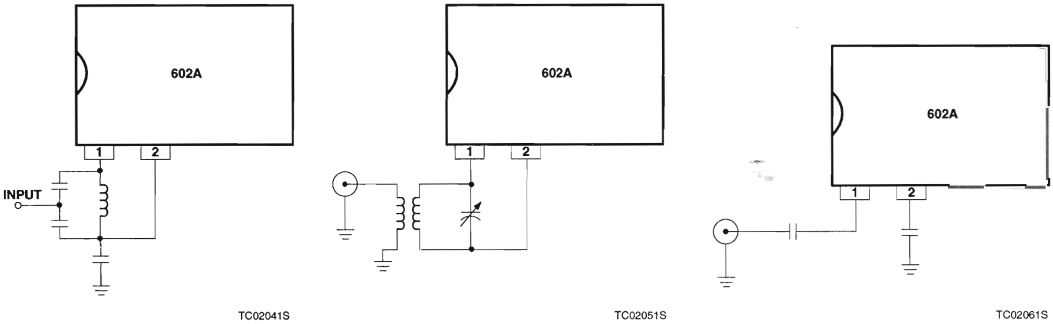


Figure 2. Equivalent Circuit

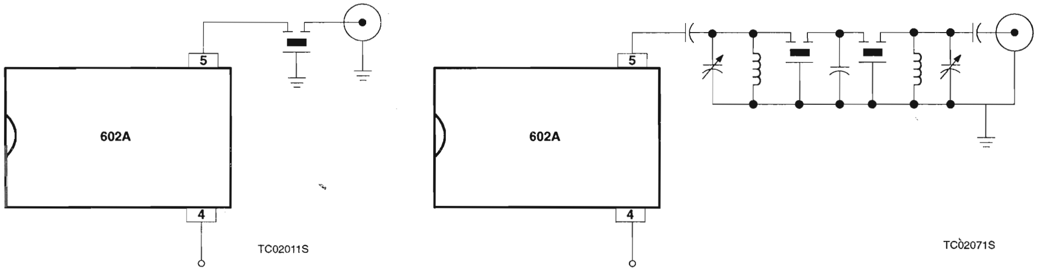


a. Single-Ended Tuned Input

b. Balanced Input (For Attenuation of Second-Order Products)

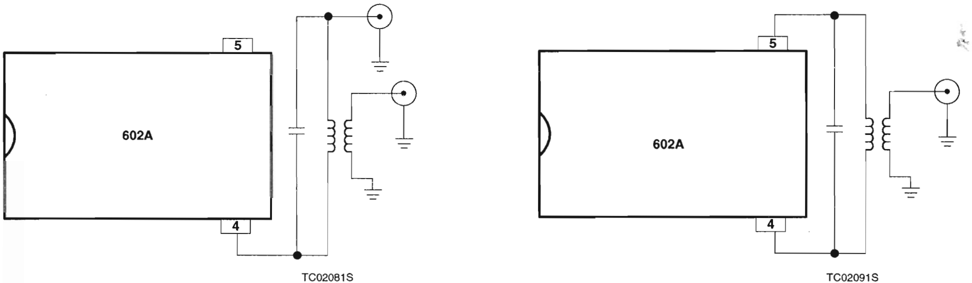
c. Single-Ended Untuned Input

Figure 3. Input Configuration



a. Single-Ended Ceramic Filter

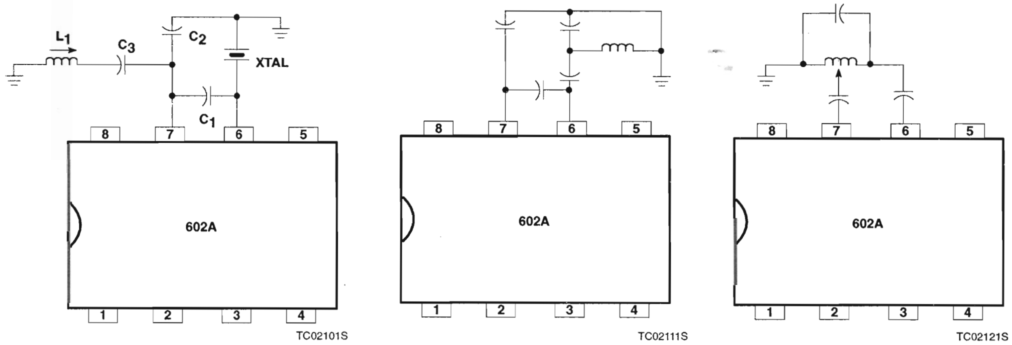
b. Single-Ended Crystal Filter



c. Single-Ended IFT

d.. Balanced Output

Figure 4. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)

b. Colpitts L/C Tank Oscillator

c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

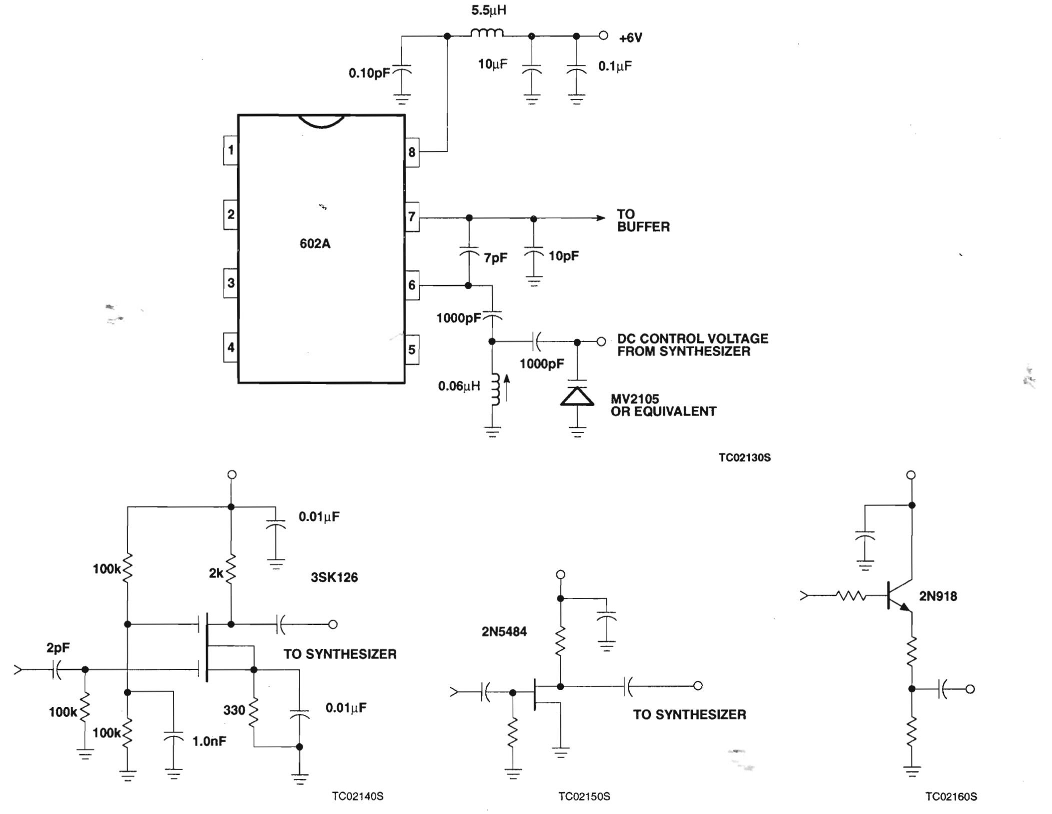


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

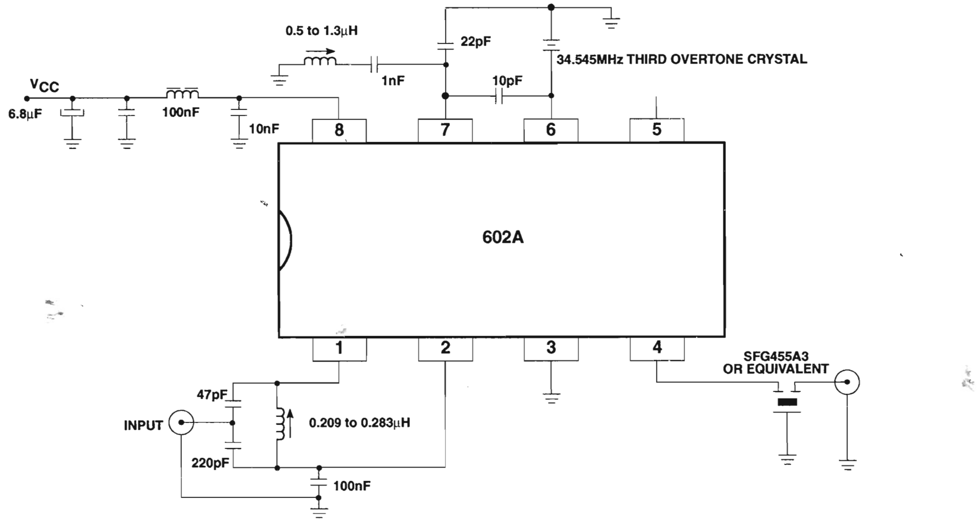


Figure 7. Typical Application for Cellular Radio

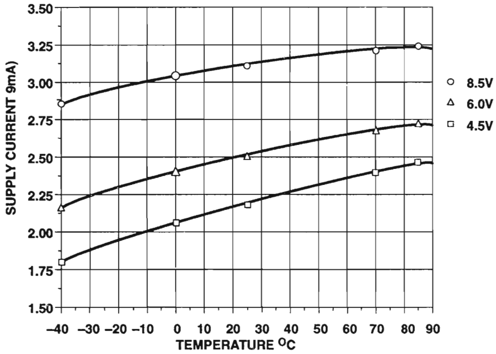


Figure 8. I_{CC} vs Supply Voltage

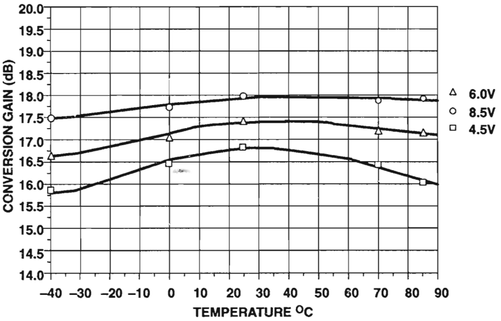


Figure 9. Conversion Gain vs Supply Voltage

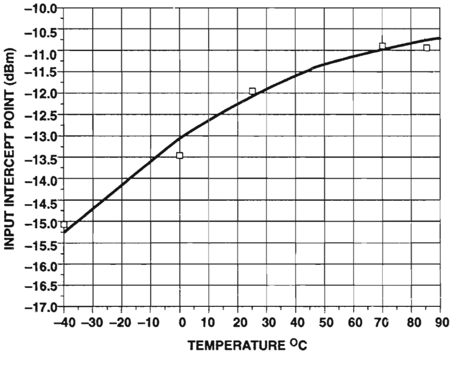


Figure 10. Third-Order Intercept Point

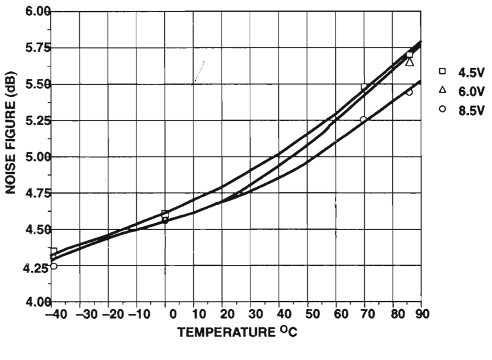


Figure 11. Noise Figure

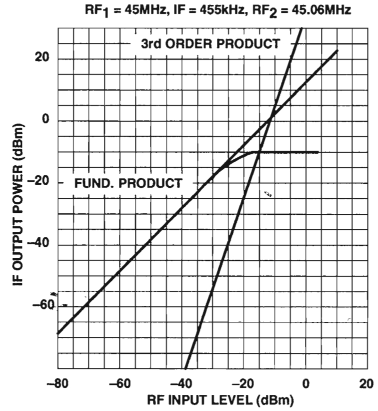


Figure 12. Third-Order Intercept and Compression

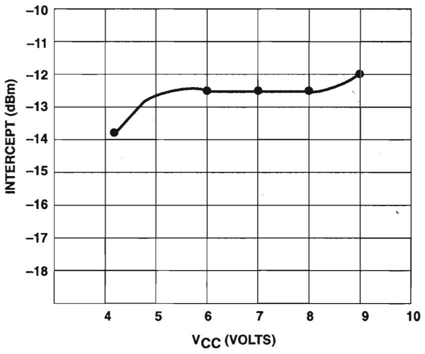


Figure 13. Input Third-Order Intermod Point vs V$_{CC}$

Double-balanced mixer and oscillator NE/SA612A

DESCRIPTION

The NE/SA612A is a low-power VHF monolithic double-balanced mixer with on-board oscillator and voltage regulator. It is intended for low cost, low power communication systems with signal frequencies to 500MHz and local oscillator frequencies as high as 200MHz. The mixer is a "Gilbert cell" multiplier configuration which provides gain of 14dB or more at 45MHz.

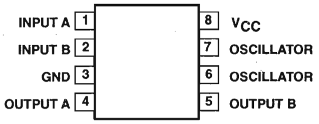
The oscillator can be configured for a crystal, a tuned tank operation, or as a buffer for an external L.O. Noise figure at 45MHz is typically below 6dB and makes the device well suited for high performance cordless phone/cellular radio. The low power consumption makes the NE/SA612A excellent for battery operated equipment. Networking and other communications products can benefit from very low radiated energy levels within systems. The NE/SA612A is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface mounted miniature package).

FEATURES

- Low current consumption
- Low cost
- Operation to 500MHz
- Low radiated energy
- Low external parts count; suitable for crystal/ceramic filter
- Excellent sensitivity, gain, and noise figure

PIN CONFIGURATION

D, N Packages



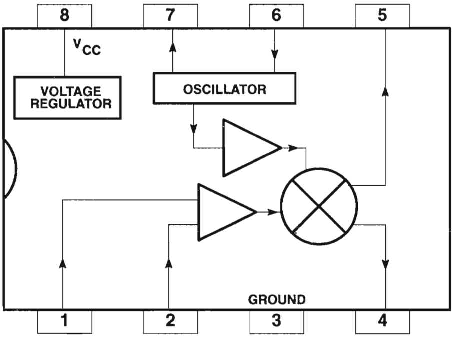
APPLICATIONS

- Cordless telephone
- Portable radio
- VHF transceivers
- RF data links
- Sonabuoys
- Communications receivers
- Broadband LANs
- HF and VHF frequency conversion
- Cellular radio mixer/oscillator

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Plastic (DIP)	0 to +70°C	NE612AN	0404B
8-Pin Plastic Small Outline (SO) package (Surface-Mount)	0 to +70°C	NE612AD	0174C
8-Pin Plastic Dual In-Line Plastic (DIP)	-40 to +85°C	SA612AN	0404B
8-Pin Plastic Small Outline (SO) package (Surface-Mount)	-40 to +85°C	SA612AD	0174C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Operating ambient temperature range NE SA	 0 to +70 -40 to +85	°C

AC/DC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{CC} = 6V, Figure 1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	3.0	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 45MHz			5.0		dB
	Third-order intercept point at 45MHz	RF_{IN}=-45dBm		-13		dBm
	Conversion gain at 45MHz		14	17		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3		pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

DESCRIPTION OF OPERATION

The NE/SA612A is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE/SA612A is designed for optimum low power performance. When used with the NE614A as a 45MHz cordless phone/cellular radio 2nd IF and demodulator, the NE/SA612A is capable of receiving -119dBm signals with a 12dB S/N ratio. Third-order intercept is typically -15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues not critical, the input to the NE/SA612A should be appropriately scaled.

TEST CONFIGURATION

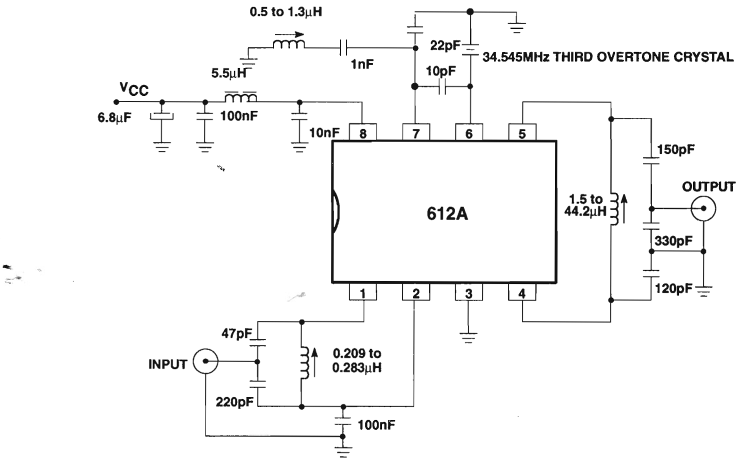


Figure 1. Test Configuration

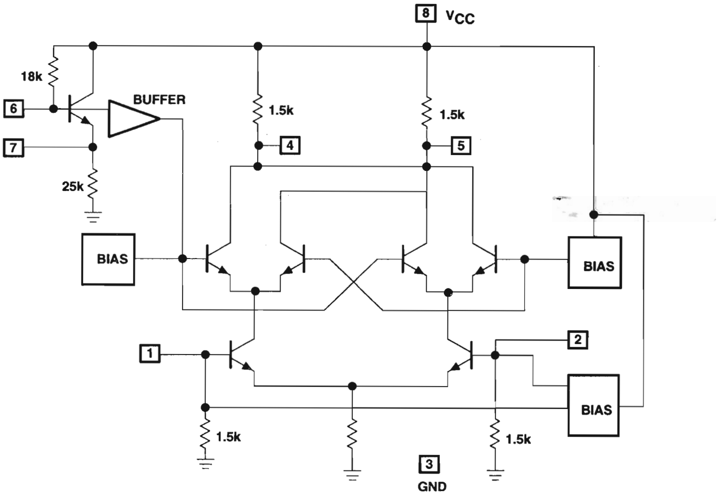


Figure 2. Equivalent Circuit

Besides excellent low power performance well into VHF, the NE/SA612A is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

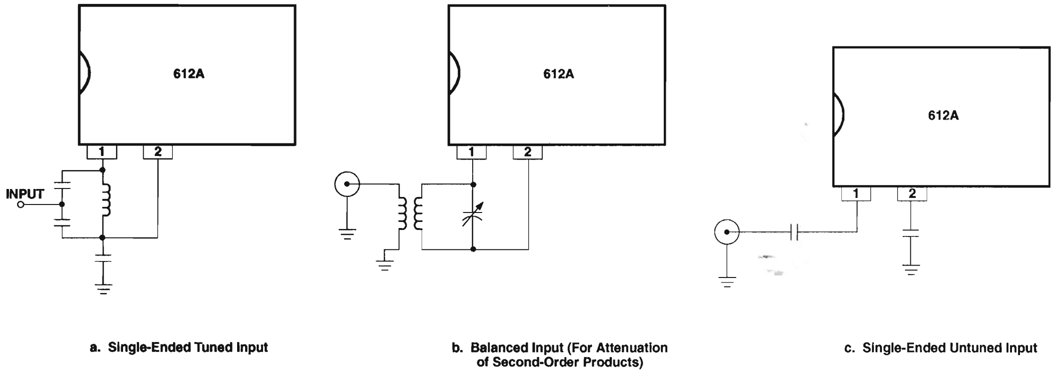
The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single-ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the Q of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be 200mV$_{P-P}$ minimum to 300mV$_{P-P}$ maximum.

Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cordless phones/cellular radio. In this circuit a third overtone parallel-mode crystal with approximately 5pF load capacitance should be specified. Capacitor C3 and inductor L1 act as a fundamental trap. In fundamental mode oscillation the trap is omitted.

Figure 6 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar circuits provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assume correct system operation.

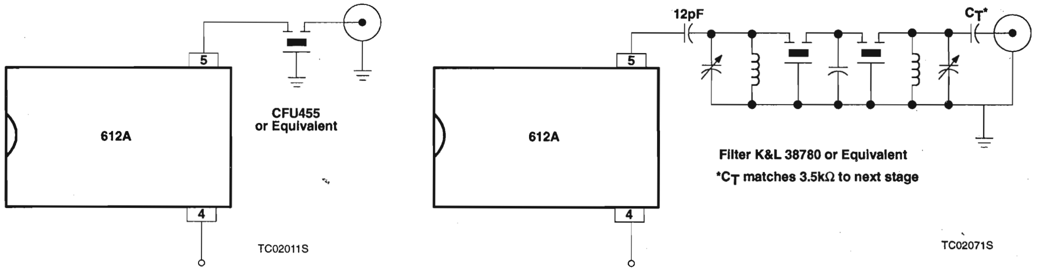


a. Single-Ended Tuned Input

b. Balanced Input (For Attenuation of Second-Order Products)

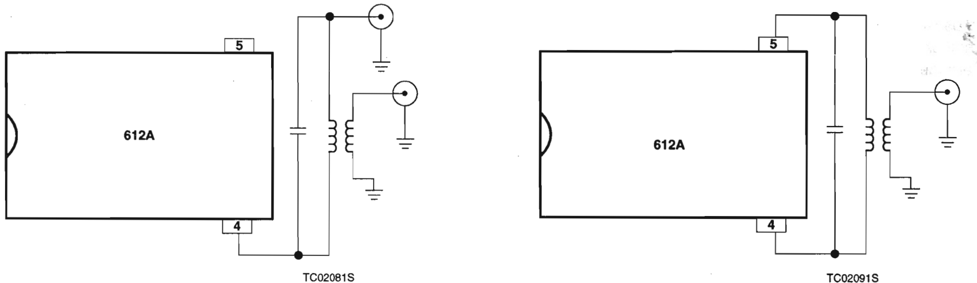
c. Single-Ended Untuned Input

Figure 3. Input Configuration


5
612A
4
CFU455
or Equivalent
TC02011S
12pF
CT*
5
612A
4
Filter K&L 38780 or Equivalent
*CT matches 3.5kΩ to next stage
TC02071S

a. Single-Ended Ceramic Filter

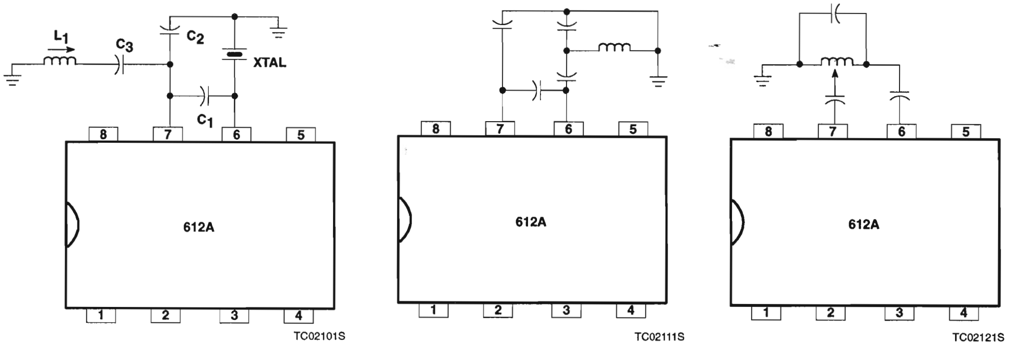
b. Single-Ended Crystal Filter



c. Single-Ended IFT

d.. Balanced Output

Figure 4. Output Configuration



a. Colpitts Crystal Oscillator
(Overtone Mode)

b. Colpitts L/C Tank Oscillator

c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

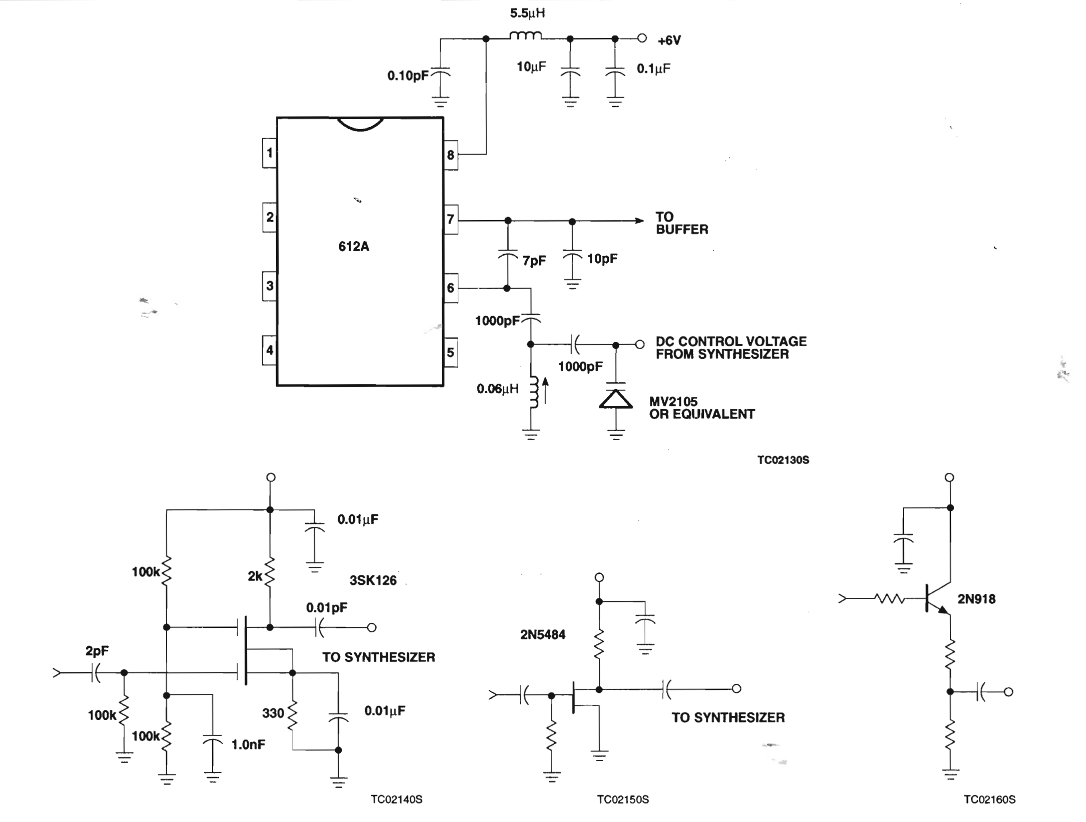


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

TEST CONFIGURATION

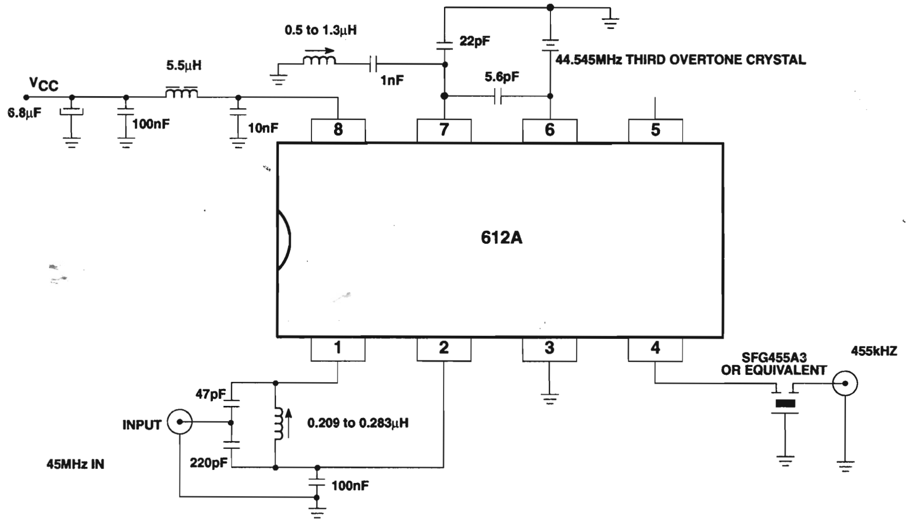


Figure 7. Typical Application for Cordless/Cellular Radio

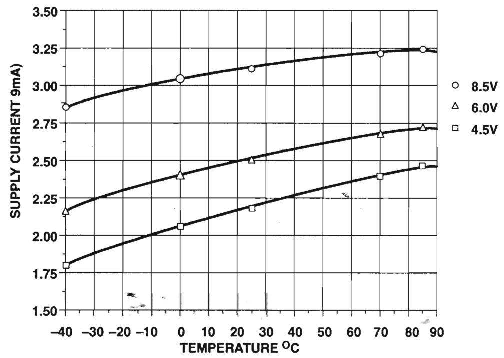


Figure 8. I_{CC} vs Supply Voltage

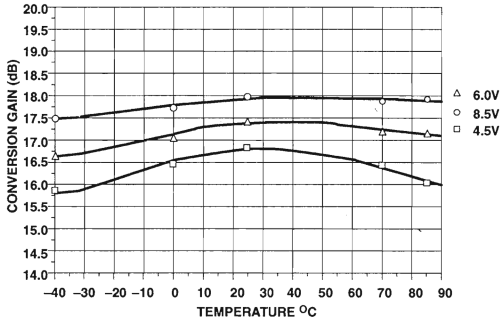


Figure 9. Conversion Gain vs Supply Voltage

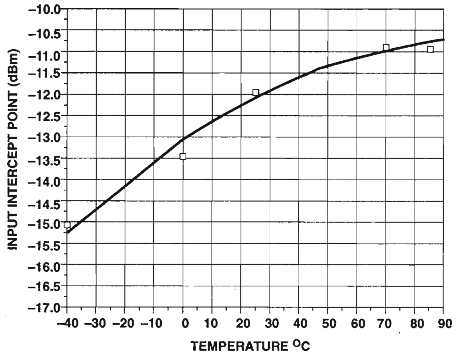


Figure 10. Third-Order Intercept Point

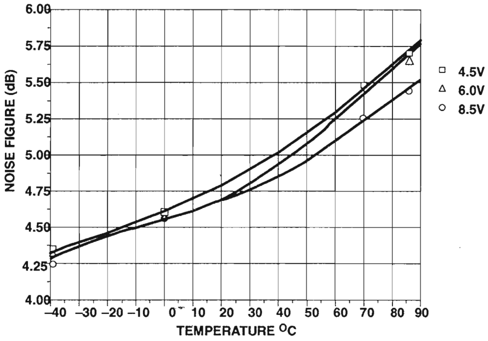


Figure 11. Noise Figure

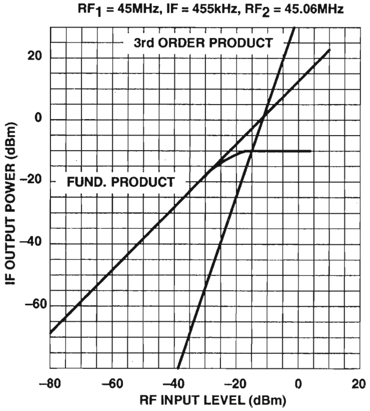


Figure 12. Third-Order Intercept and Compression

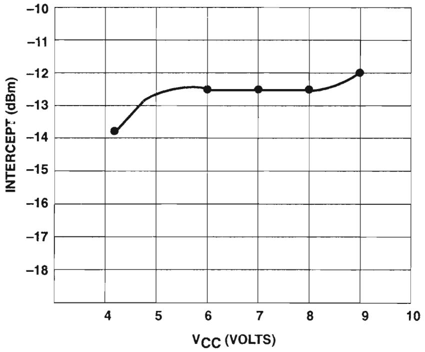


Figure 13. Input Third-Order Intermod Point vs V_{CC}

New low-power single sideband circuits

AN1981

Author: Robert J. Zavrell Jr.

INTRODUCTION

Several new integrated circuits now permit RF designers to resurrect old techniques of single-sideband generation and detection. The high cost of multi-pole crystal filters limits the use of the SSB mode to the most demanding applications, yet the advantages of SSB over full-carrier AM and FM are well documented (Ref 1 &2). The use of multi-pole filters can now be circumvented by reviving some older techniques without sacrificing performance. This has been made possible by the availability of some new RF and digital integrated circuits.

DESCRIPTION

Figure 1 shows the frequency spectrum of a 10MHz full-carrier double-sideband AM signal using a 1kHz modulating tone. This well-known type of signal is used by standard AM broadcast radio stations. Full-carrier AM's advantage is that envelope detection can be used in the receiver. Envelope detection is a simple and economical technique because it simplifies receiver circuitry. Figure 2 shows the time domain "envelope" of the same AM signal.

The 1kHz tone example of Figures 1 and 2 serves as a simple illustration of an AM signal. Typically, the sidebands contain complex waveforms for voice or data communications. In the full-carrier double sideband mode (AM), all the modulation information is contained in both sidebands, while the carrier "rides along" without contributing to the transfer of intelligence. Only one sideband without the carrier is needed to effectively transmit the modulation information. This mode is called "single-sideband suppressed carrier". Because of its reduced bandwidth, it has the advantages of improved spectrum utilization, better signal-to-noise ratios at low signal levels, and improved transmitter efficiency when compared with either FM or full-carrier AM. A finite frequency allocation using SSB can support three times the number of channels when compared with comparable FM or AM full-carrier systems.

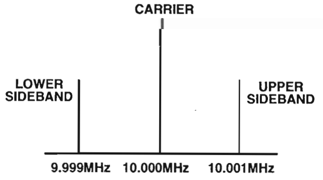


Figure 1. Frequency Domain Display of a 10MHz Carrier AM Modulated by a 1kHz Tone (Spectrum Analyzer Display)

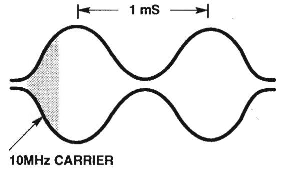


Figure 2. Time Domain Display of the Same Signal Shown in Figure 1. (Oscilloscope Display)

There are three basic methods of single-sideband generation. All three use a balanced modulator to produce a double-sideband suppressed carrier signal. The undesired sideband is then removed by phase and amplitude nulling (the phasing method), high Q multi-pole filters (the filter method), or a "third" method which is a derivation of the phasing technique called here the "Weaver" method for the apparent inventor. The reciprocal of the generator functions is employed to produce sideband detectors. Generators start with audio and produce the SSB signal; detectors receive the SSB signal and reproduce the audio. Since the sideband signal is typically produced at radio frequencies, it can be amplified and applied to an antenna or used as a subcarrier.

Reproduction of the audio signal in a full-carrier AM receiver is simplified because the carrier is present. The signal envelope, which contains the carrier and the sidebands, is applied to a non-linear device (typically a diode). The effect of envelope detection is to multiply the sideband signal by the carrier; this results in the recovery of the audio waveform. The mathematical basis for this process can be understood by studying trigonometric identities.

Since the carrier is not present in the received SSB signal, the receiver must provide it for proper audio detection. This signal from the local oscillator (LO) is applied to a mixer (multiplier) together with the SSB signal and detection occurs. This technique is called product detection and is necessary in all SSB methods. A major problem in SSB receivers is the ability to maintain accurate LO frequencies to prevent spectral shifting of the audio signal. Errors in this frequency will result in a "Donald Duck" sound which can render the signal unintelligible for large frequency errors.

Theory of Single-Sideband Detection

Figures 3 through 8 illustrate the three methods of SSB generation and detection. Since they are reciprocal operations, the circuitry for generation and detection is similar with all three methods. Duplication of critical circuitry is easy to accomplish in transceiver applications by using appropriate switching circuits.

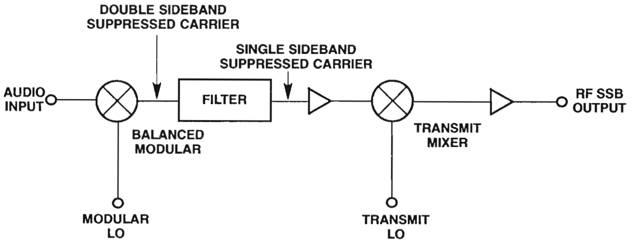


Figure 3. Filter Method SSB Generator

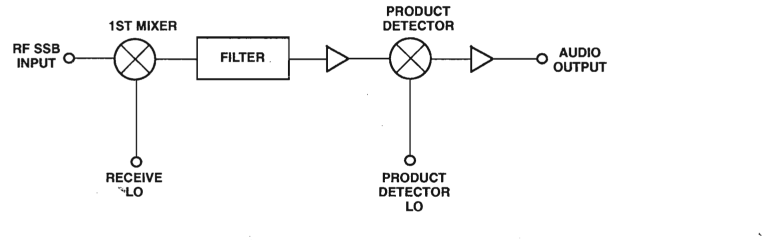


Figure 4. Filter Method SSB Detector

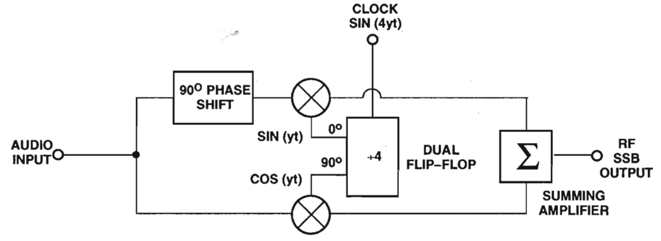


Figure 5. Phasing Method Generator

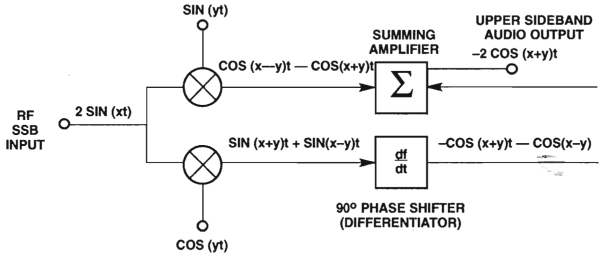


Figure 6. Phasing Method Detector with Simplified Mathematical Model

Figures 3 and 4 show the generation and detection techniques employed in the filter method. In the generator a double sideband signal is produced while the carrier is eliminated with the balanced modulator. Then the undesired sideband is removed with a high Q crystal bandpass filter. A transmit mixer is usually employed to convert the SSB signal to the desired output frequency. The detection scheme is the reciprocal. A receive mixer is used to convert the selected input frequency to the IF frequency, where the filter removes the undesired SSB response. Then the signal is demodulated in the product detector. A major drawback to the filter method is the fact that the filter is fixed-tuned to one frequency. This necessitates the receive and transmit mixers for multi-frequency operation.

Figures 5 and 6 show block diagrams of a generator and demodulator which use the phase method. Figure 6 also includes a mathematical model. The input signal (Cos(Xt)) is fed in-phase to two RF mixers where “X” is the frequency of the input signal. The other inputs to the mixers are fed from a local oscillator (LO) in quadrature (Cos(Yt) and Sin(Yt)), where “Y” is the frequency of the LO signal. By differentiating the output of one of the mixers and then summing with the other, a single sideband response is obtained.

Switching the mixer output that is differentiated will change the selected sideband, upper (USB) or lower (LSB). In most cases the mixer outputs will be the audio passband (300 to 3000Hz). Differentiating the passband involves a 90 degree phase shift over more than three octaves. This is the most difficult aspect of using the phasing method for voice band SSB.

For voice systems, difficulty of maintaining accurate broadband phase shift is eliminated by the technique used in Figures 7 and 8. The “Weaver” method is similar to the phasing method because both require two quadrature steps in the signal chain. The difference between the two methods is that the Weaver method uses a low frequency (1.8kHz) subcarrier in quadrature rather than the broad-band 90 degree audio phase shift. The desired sideband is thus “folded over” the 1.8kHz subcarrier and its energy appears between 0 and 1.5kHz. The undesired sideband appears 600Hz farther away between 2.1 and 4.8kHz. Consequently, sideband rejection is determined by a low-pass filter rather than by phase and amplitude balance. A very steep low-pass response in the Weaver method is easier to achieve than the very accurate phase and amplitude balance needed in the phasing

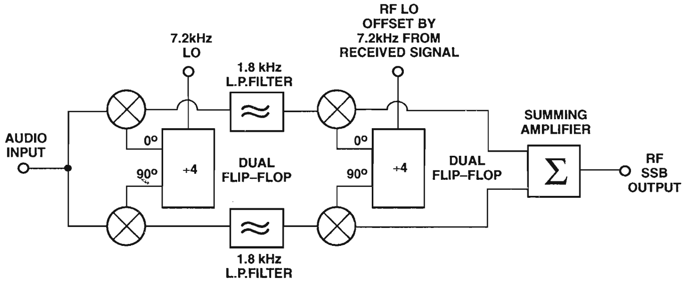


Figure 7. Weaver Method Generator

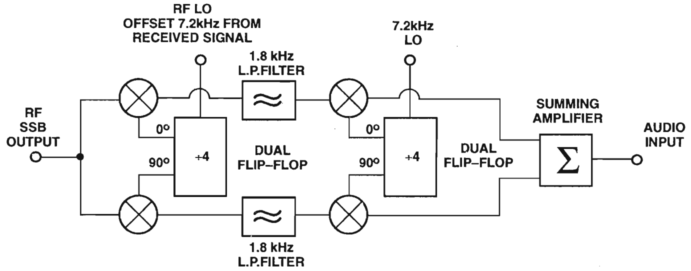


Figure 8. Weaver Method Detector

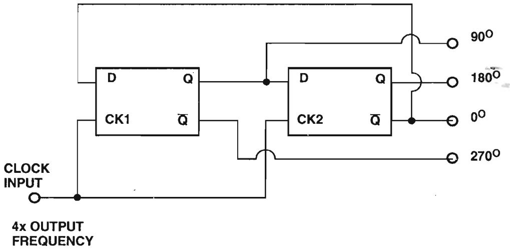


Figure 9. Dual Flip-Flop Quadrature Synthesis

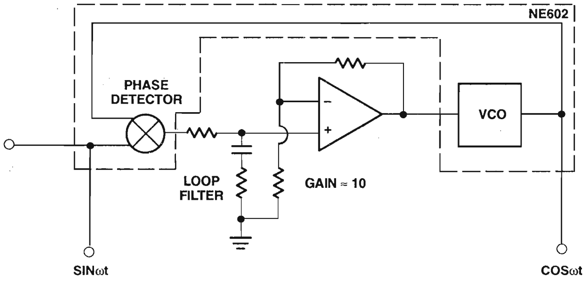


Figure 10. PLL Quadrature Synthesis

method. Therefore, better sideband rejection is possible with the Weaver method than with the phasing method.

Quadrature Dual Mixer Circuits

One of the two critical stages in the phasing method and both critical stages in the Weaver method require quadrature dual mixer circuits.

Figures 9 and 10 show two methods of obtaining quadrature LO signals for dual mixer applications. Other methods exist for producing quadrature LO signals, particularly use of passive LC circuits. LC circuits will not maintain a quadrature phase relationship when the operating frequency is changed. The two illustrated circuits are inherently broad-banded; therefore, they are far more flexible and do not require adjustment. These circuits are very useful for SSB circuits, but also can be applied to FSK, PSK, and QPSK digital communications systems.

The NE602 is a low power, sensitive, active, double-balanced mixer which shows excellent phase characteristics up to 200MHz. This makes it an ideal candidate for this and many other applications.

The circuit in Figure 9 uses a divide-by-four dual flip-flop that generates all four quadratures. Most of the popular dual flip-flops can be used in different situations. The HEF4013 CMOS device uses very little power and can maintain excellent phase integrity at clock rates up to several megahertz. Consequently, the HEF4013 can be used with the ubiquitous 455kHz intermediate frequency with excellent power economy. For higher clock rates (up to 120MHz for up to 30MHz operation), the fast TTL 74F74 is a good choice. It has been tested to 30MHz operating frequencies with good results (>30 dB SSB rejection). At lower frequencies (5MHz) sideband rejection increases to nearly 40dB with the circuits shown. The ultimate low frequency rejection is mainly a function of the audio phase shifter. Better performance is possible by employing higher tolerance resistors and capacitors.

The circuit in Figure 10 shows another technique for producing a broadband quadrature phase shift for the LO. The advantage of this circuit over the flip-flops is that the clock frequency is identical to the operating frequency; however, phase accuracy is more difficult to achieve. A PLL will maintain a quadrature phase relationship when the loop is closed and the VCO voltage is zero. The DC amplifier will help the accuracy of the quadrature condition by presenting gain to the VCO control circuit. The other problem that can arise is that PLL circuits tend to be noisy. Sideband noise is troublesome in both SSB and FM systems, but SSB is less sensitive to phase noise problems in the LO.

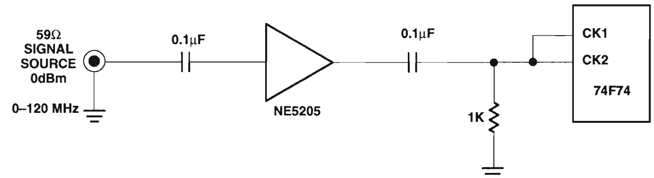


Figure 11. FAST TTL Driver from Analog Signal Source Using NE5205

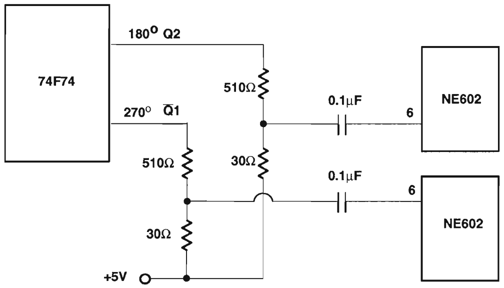


Figure 12. Interface Circuitry Between 74F74 and the NE602s

Figure 11 shows a circuit that is effective for driving the 74F74, or other TTL gates, with a signal generator or analog LO. The NE5205 provides about 20dB gain with 50Ω input and output impedances from DC to 450MHz. Minimum external components are required. The 1kΩ resistor is about optimum for "pulling" the input voltage down near the logic threshold. A 50Ω output level of 0dBm can be used to drive the NE5205 and 74F74 to 100MHz. Two NE5205s can be cascaded for even more sensitivity while maintaining extremely wide bandwidth. An advantage of using digital sources for the LO is that low-frequency power supply ripple will not cause hum in the receiver front end. This is a common problem in direct conversion designs.

Figure 12 shows the interface circuitry between the 74F74 and the NE602 LO ports. The total resistance reflects conservative current drain from the 74F74 outputs, while the tap on the voltage divider is optimized for proper NE602 operation. The low signal source impedance further helps maintain phase accuracy, and the isolation capacitor is miniature ceramic for DC isolation.

Audio Amplifiers and Switching

Using active mixers (NE602) in these types of circuits gives conversion gain, typically 18dB. More traditional applications use passive diode ring mixers which yield conversion loss, typically 7dB. Consequently, the detected audio level will be about 25dB higher when using the NE602. This fact can greatly reduce the first audio stage noise and gain requirements and virtually eliminate the "microphonic" effect common to direct conversion receivers. Traditional direct conversion receivers use passive audio LC filters at the mixer output and low noise, discrete JFETs or bipolars in the first stages. The very high audio sensitivity required by these amplifiers makes them respond to mechanical vibration – thus the "microphonics" result. The conversion gain allows use of a simple op amp stage (Figure 13) set up as an integrator to eliminate ultra-sonic and RF instability. The NE5534 is well known for its low noise, high dynamic range, and excellent audio characteristics (Reference 12) and makes an ideal audio amp for the 602 detector.

The sideband select function is easily accomplished with an HEF4053 CMOS analog switch. This triple double-pole switch drives the phase network discussed in the next section and also chooses one of two amplitude balance potentiometers, one for each sideband. Figure 14 illustrates this circuit. A buffer op amp is used with the two sideband select sections to reduce THD, maintain amplitude integrity, and not change the filter network input resistance values. The gain distribution within both legs of the receiver was found to be very consistent (within 1dB), thus the amplitude balance pots may be eliminated in less demanding applications. The NE602s have excellent gain as well as phase integrity.

Audio Phase Shift Circuits

The two critical stages for the phasing method are a dual quadrature mixer and a broadband audio phase shifter (differentiator). There are several broadband, phase shift techniques available. Figure 15 shows an analog all-pass differential phase shift circuit. When the inputs are shorted and driven with a microphone circuit, the outputs will be 90 degrees out-of-phase over the 300 to 3000Hz band. This "splitting" and phase shift is necessary for the phasing generator. For phasing demodulation the two audio detectors are fed to the two inputs. The outputs are then summed to affect the sideband rejection and audio output.

Standard 1% values are shown for the resistors and capacitors, although better gain tolerances can be obtained with 0.1% laser-trimmed integrated resistors. Polystyrene capacitors are preferred for better value tolerance and audio performance. Two quad op amps fit nicely into this application. One op amp serves as a switch buffer and the other three form a phasing section. The NE5514 quad op amps perform well for this application. Careful attention to active filter configurations can yield highly linear and very high dynamic range circuits. Yet these characteristics are much easier to achieve at audio than the common IF RF frequencies. This fact, coupled with the lack of IF tuned circuits, shielding, and higher power requirements make audio IF systems attractive indeed.

Figure 16 shows a "tapped" analog delay circuit which uses weighted values of resistors to affect the phase shift. Excellent phase and amplitude balance are possible with this technique, but the price for components is high. It should be stressed that the audio phase shift accuracy and amplitude balance are the limiting factors for SSB rejection when using the phase method; thus the higher cost may be justified in some applications.

Audio Processing

The summing amplifier is a conventional, inverting op amp circuit. It may be useful to configure a low-pass filter around this amplifier, and thus help the sharp audio filters which follow. Audio filters are necessary to shape the desired bandpass. Steep slope audio bandpass filters can be built from switched capacitor filters or from active filters requiring more op amps. Switched capacitor filters have the disadvantage of requiring a clock frequency in the RF range. Harmonics can cause interference problems if careful design techniques are not used. Also, better dynamic range is obtained with active filter techniques using "real" resistors although much work is being done with SCF's and performance is improving.

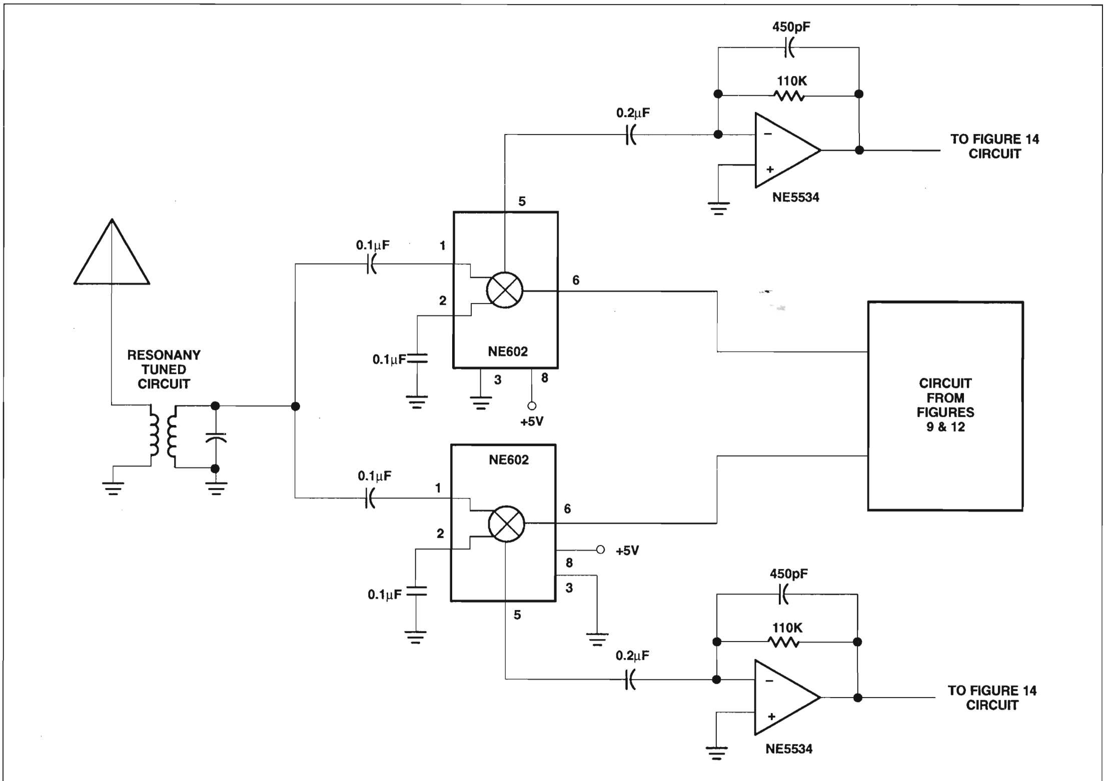


Figure 13. Phasing Method Detector for Direct Conversion Receiver

Direct conversion receivers rely heavily on audio filters for selectivity. Active analog or switched capacitor filters can produce the high Q and dynamic ranges necessary. Signal strength or "S-meters" can be constructed from the NE602's companion part, the NE604. The "RSSI" or "received signal strength indicator" function on the 604 provides a logarithmic response over a 90dB dynamic range and is easy to use at audio frequencies. Finally, the AGC (automatic gain control) function can also be performed in the audio section. Attack and delay times can be independently set with excellent distortion specifications with the NE572 compandor IC. The audio-derived AGC eliminates the need for gain controlling and RF stage, but relies on an excellent receiver front-end dynamic range. In ACSSB (Amplitude Compandored Single-Side Band) systems transmitter compression and receiver expansion are defined by individual system specifications.

Phasing-Filter Technique

High quality SSB radio specifications call for greater than 70dB sideband rejection. Using the circuits described in this paper for the phasing method, rejection levels of 35dB are obtainable with good reliability. Coupled with an inexpensive two-pole crystal or ceramic filter, the 70dB requirement is obtained. Also, the filtering ahead of the NE602 greatly improves the intermodulation performance of the receiver. Figure 17 shows a complete SSB receiver using the Phasing-Filter technique. The sensitivity of the NE602 allows low gain stages and low power consumption for the RF amplifier and first mixer. A new generation of low power CMOS frequency synthesizers is now available from several manufacturers including the TDD1742 and dual chip HEF4750/51 solutions.

Direct Conversion Receiver

The antenna can be connected directly to the input of the NE602 (via a bandpass filter) to form a direct conversion SSB receiver using the phasing method. 35dB sideband rejection is adequate for many applications, particularly where low power and portable battery operation are required. Figure 13 shows a typical circuit for direct conversion applications.

There are many other applications which can make use of SSB technology. Cordless telephones use FM almost exclusively. Eavesdropping could be greatly reduced for systems which employ SSB rather than FM. Furthermore, the better signal-to-noise ratio will extend the range, and battery life will be extended because no carrier is needed.

SSB is also used for subcarriers on microwave links and coaxial lines. Telephone communications networks that use SSB are called FDM or Frequency Domain Multiplex systems. The low power and high sensitivity of the NE602 can offer FDM designers new techniques for system configuration.

Weaver Method Receiver Techniques

The same quadrature dual mixer can be used for the first stage in both the phasing and Weaver method receiver. The subcarrier stage in the Weaver method receiver can use CMOS analog switches (HEF4066) for great power economy. Figure 18 shows a circuit for the subcarrier stage. A 1.8kHz subcarrier requires a 7.2kHz clock frequency. If switched capacitor filters are used for the low-pass and audio filters, a single clock generator can be used for all circuits with appropriate dividers. Furthermore, if the receiver is used as an IF circuit, the fixed LO signal could also be derived from the same clock. This has the added advantage that harmonics from the various circuits will not interfere with the received signal.

Results

The circuit shown in Figures 13, 14, and 15 has a 10dB S/N sensitivity of 0.5μV with a dynamic range of about 80dB. Single-tone audio harmonic distortion is below 0.05% with two-tone intermodulation products below 55dB at RF input levels only 5dB below the 1dB compression point. The sideband rejection is about 38dB at a 9MHz operating frequency. The good audio specifications are a side benefit to direct conversion receivers. When used with inexpensive ceramic or crystal filters, this circuit can provide these specifications with >70dB sideband rejection.

Conclusions

Single sideband offers many advantages over FM and full-carrier double-sideband modulation. These advantages include: more efficient spectrum use, better signal-to-noise ratios at low signal levels, and better transmitter efficiency. Many of the disadvantages can now be overcome by using old techniques and new state-of-the-art integrated circuits. Effective and inexpensive circuits can use direct conversion techniques with good results. 35dB sideband rejection with less than 1μV sensitivity is obtained with the NE602 circuits. 70dB sideband rejection and superior sensitivity are obtained by using phasing-filter techniques. Either the phasing or Weaver methods can be used in either the direct conversion or IF section applications. The filter and phase-filter methods can be used in only the IF application.

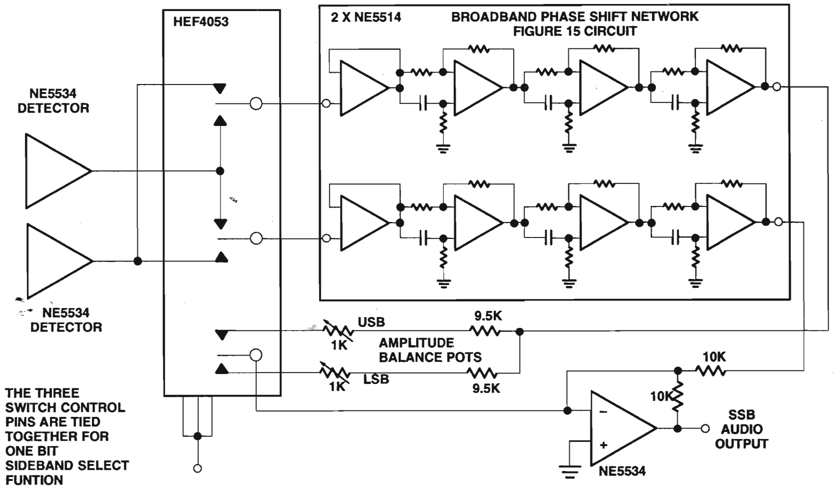


Figure 14. Sideband Select Switching Function

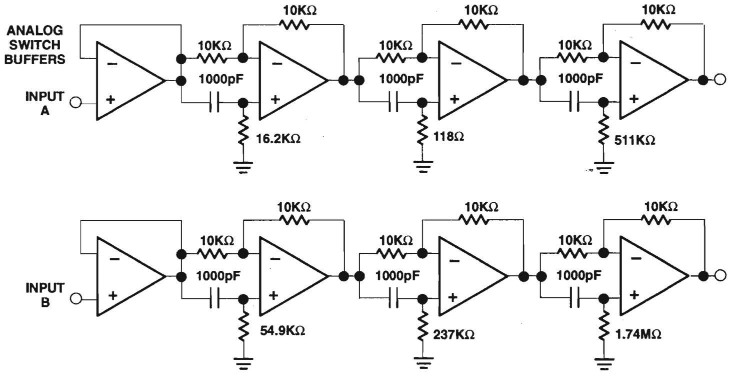


Figure 15

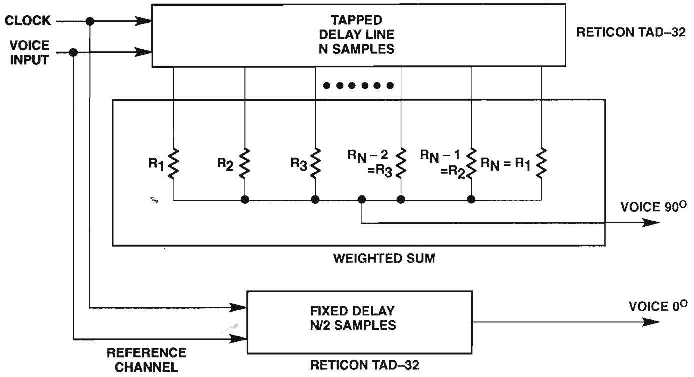
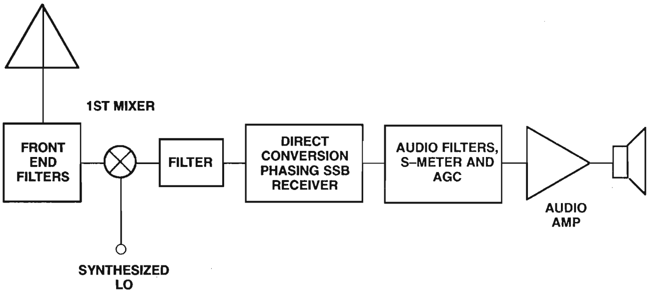


Figure 16. Broadband 90° Audio Phase Shift Technique Using Tapped Delay Line (Reference 4)


1ST MIXER
FRONT END FILTERS
FILTER
DIRECT CONVERSION PHASING SSB RECEIVER
AUDIO FILTERS, S–METER AND AGC
AUDIO AMP
SYNTHESIZED LO

Receivers built using this technique can exhibit excellent characteristics without resorting to expensive multi-pole filters or an IF amplifier chain.

Figure 17. Complete Phasing-Filter Receiver

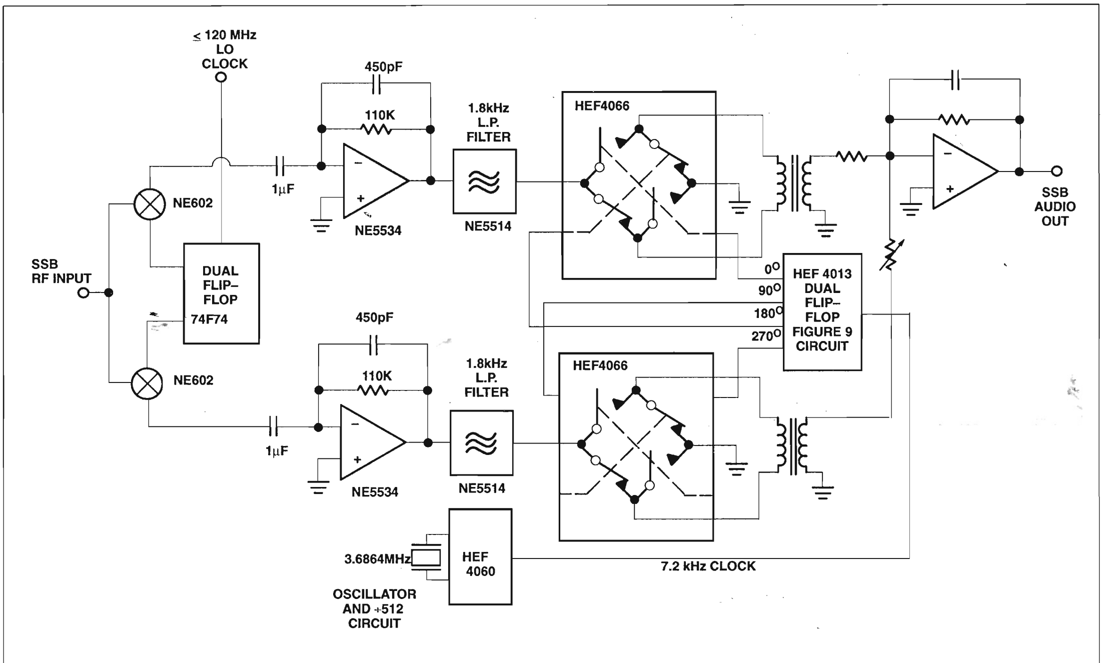


Figure 18. Weaver Method Receiver Concept Example for ≤ 30MHz Operation

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Applying the oscillator of the NE602 in low-power mixer applications

AN1982

Author: Donald Anderson

INTRODUCTION

For the designer of low power RF systems, the Philips Semiconductors NE602 mixer/oscillator provides mixer operation beyond 500MHz, a versatile oscillator capable of operation to 200MHz, and conversion gain, with only 2.5mA total current consumption. With a proper understanding of the oscillator design considerations, the NE602 can be put to work quickly in many applications.

DESCRIPTION

Figure 1 shows the equivalent circuit of the device. The chip is actually three subsystems: A Gilbert cell mixer (which provides differential input gain), a buffered emitter follower oscillator, and RF current and voltage regulation. Complete integration of the DC bias permits simple and compact application. The simplicity of the oscillator permits many configurations.

While the oscillator is simple, oscillator design isn't. This article will not address the rigors of oscillator design, but some practical guidelines will permit the designer to accomplish good performance with minimum difficulty.

Either crystal or LC tank circuitry can be employed effectively. Figure 2 shows the four most commonly used configurations in their most basic form.

In each case the Q of the tank will affect the upper frequency limits of oscillation: the higher the Q the higher the frequency. The NE602 is fabricated with a 6GHz process, but the emitter resistor from Pin 7 to ground is nominally 20k. With 0.25mA typical bias current, 200MHz oscillation can be achieved with high Q and appropriate feedback.

The feedback, of course, depends on the Q of the tank. It is generally accepted that a minimum amount of feedback should be used, so even if the choice is entirely empirical, a good trade-off between starting characteristics, distortion, and frequency stability can be quickly determined.

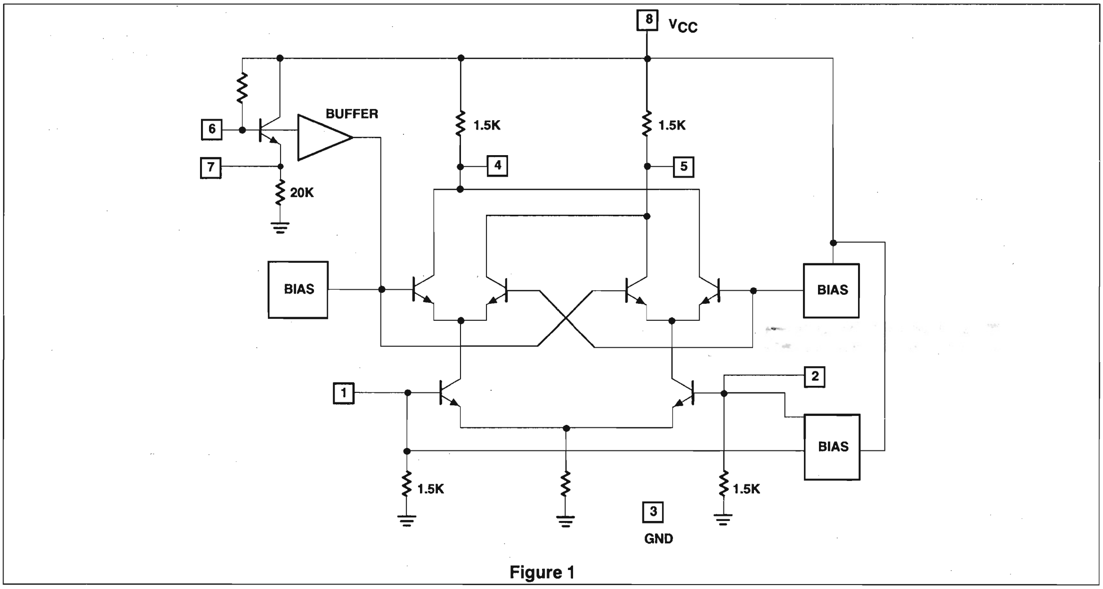
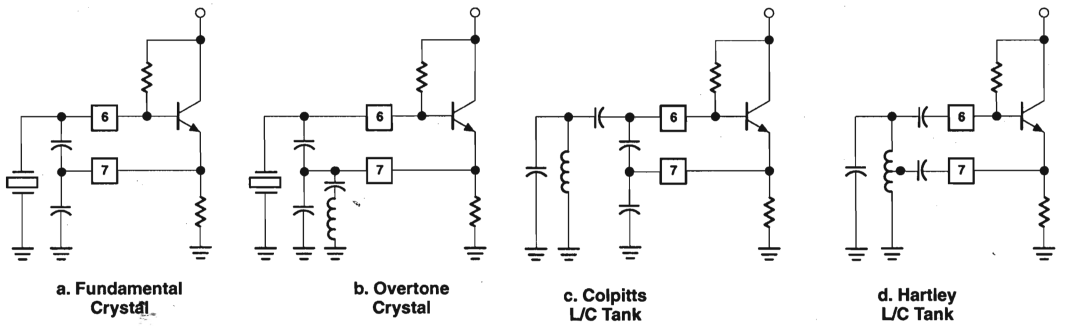


Figure 1



a. Fundamental Crystal

b. Overtone Crystal

c. Colpitts L/C Tank

d. Hartley L/C Tank

Figure 2

Crystal Circuit Considerations

Crystal oscillators are relatively easy to implement since crystals exhibit higher Q's than LC tanks. Figure 3 shows a complete implementation of the SA602 (extended temperature version) for cellular radio with a 45MHz first IF and 455kHz second IF.

The crystal is a third overtone parallel mode with 5pF of shunt capacitance and a trap to suppress the fundamental.

LC Tank Circuits

LC tanks present a little greater challenge for the designer. If the Q is too low, the oscillator won't start. A trick which will help if all else fails is to shunt Pin 7 to ground with a 22k resistor. In actual applications this has been effective to 200MHz with high Q ceramic capacitors and a tank inductor of 0.08mH and a Q of 90. Smaller resistor value will upset DC bias because of inadequate base bias at the input of the oscillator. An external bias resistor could be added from VCC to Pin 6, but this will introduce power supply noise to the frequency spectrum.

The Hartley configuration (Figure 2D) offers simplicity. With a variable capacitor tuning the tank, the Hartley will tune a very large range since all of the capacitance is variable. Please note that the inductor must be coupled to Pin 7 with a low impedance capacitor. The Colpitts oscillator will exhibit a smaller tuning range since the fixed feedback capacitors limit variable capacitance range; however, the Colpitts has good frequency stability with proper components.

Synthesized Frequency Control

The NE602 can be very effective with a synthesizer if proper precautions are taken to minimize loading of the tank and the introduction of digital switching transients into the spectrum. Figure 4 shows a circuit suitable for aircraft navigation frequencies (108–118MHz) with 10.7MHz IF.

The dual gate MOSFET provides a high degree of isolation from prescaler switching spikes. As shown in Figure 4, the total current consumption of the NE602 and 3SK126 is typically 3mA. The MOSFET input is from the emitter of the oscillator transistor to avoid loading the tank. The Gate 1 capacitance of the MOSFET in series with the 2pF coupling capacitor adds slightly to the feedback capacitance ratio. Use of the 22k resistor at Pin 7 helps assure oscillation without upsetting DC bias.

For applications where optimum buffering of the tank, or minimum current are not mandatory, or where circuit complexity must be minimized, the buffers shown in Figure 5 can be considered.

The effectiveness of the MRF931 (or other VHF bipolar transistors) will depend on frequency and required input level to the prescaler. A bipolar transistor will generally provide the least isolation. At low frequencies the transistor can be used as an emitter follower, but by VHF the base emitter junction will start to become a bidirectional capacitor and the buffer is lost.

The 2N5484 has an IDSS of 5mA max. and the 2SK126 has IDSS of 6mA max. making them suitable for low parts count, modest current buffers. The isolation is good.

Injected LO

If the application calls for a separate local oscillator, it is acceptable to capacitively-couple 200 to 300mV at Pin 6.

Summary

The NE602 can be an effective low power mixer at frequencies to 500MHz with oscillator operation to 200MHz. All DC bias is provided internal to the device so very compact designs are possible. The internal bias sets the oscillator DC current at a relatively low level so the designer must choose frequency selective components which will not load the transistor. If the guidelines mentioned are followed, excellent results will be achieved.

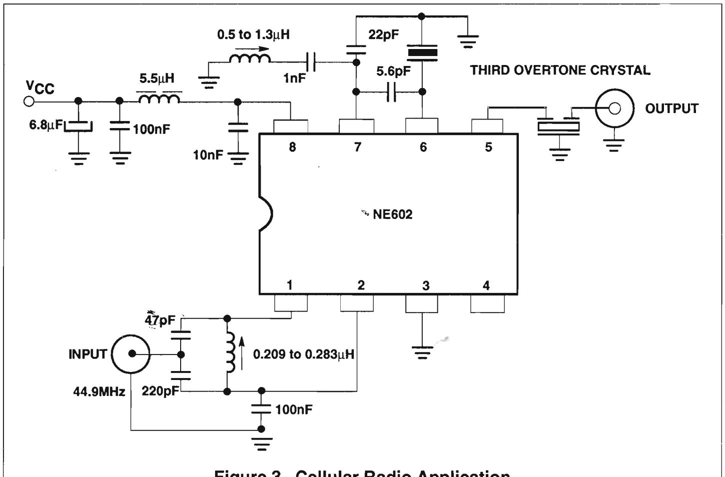
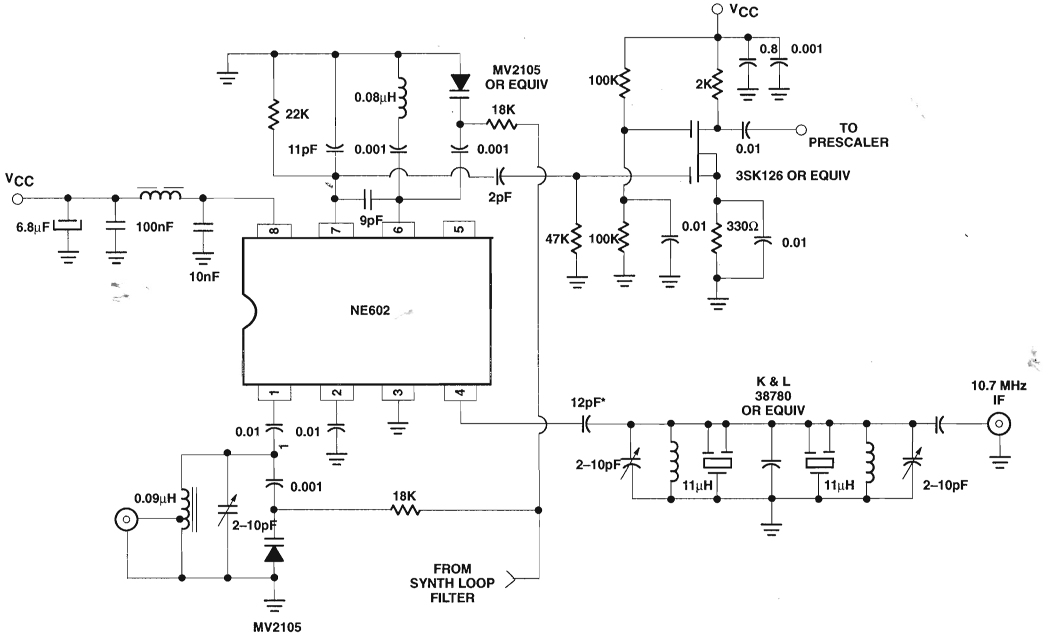


Figure 3. Cellular Radio Application

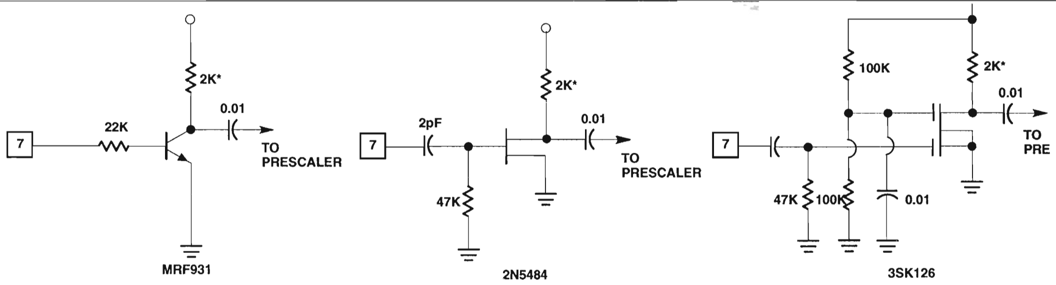


NOTES:

* Permits impedance match of NE602 output, i.e.: 1.5k filter impedance.

** Choose for impedance match to next stage.

Figure 4



NOTES:

* 2k or as necessary for current limits or prescaler impedance match.

Figure 5

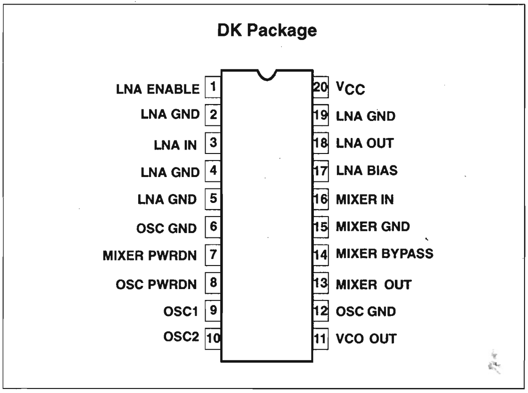
DESCRIPTION

The SA620 is a combined RF amplifier, VCO with tracking bandpass filter and mixer designed for high-performance low-power communication systems from 800-1200MHz. The low-noise preamplifier has a 1.6dB noise figure at 900MHz with 11.5dB gain and an IP3 intercept of -3dBm at the input. The gain is stabilized by on-chip compensation to vary less than ±0.2dB over -40 to +85°C temperature range. The wide-dynamic-range mixer has an 9dB noise figure and IP3 of –6dBm at the input at 900MHz. An external LO can be used in place of the internal VCO for improved mixer input IP3 and a 3mA reduction in current. The chip incorporates a through-mode option so the RF amplifier can be disabled and replaced by an attenuator ($S_{21} = -7.5$dB). This is useful for improving the overall dynamic range of the receiver when in an overload situation. The nominal current drawn from a single 3V supply is 10.4mA and 7.2mA in the thru-mode. Additionally, the VCO and Mixer can be powered down to further reduce the supply current to 1.2mA.

FEATURES

- Low current consumption: 10.4mA nominal, 7.2mA with thru-mode activated
- Outstanding noise figure: 1.6dB for the amplifier and 9dB for the mixer at 900MHz
- Excellent gain stability versus temperature and supply voltage
- Switchable overload capability
- Independent LNA, mixer and VCO power down capability
- Internal VCO automatic leveling loop
- Monotonic VCO frequency vs control voltage

PIN CONFIGURATION



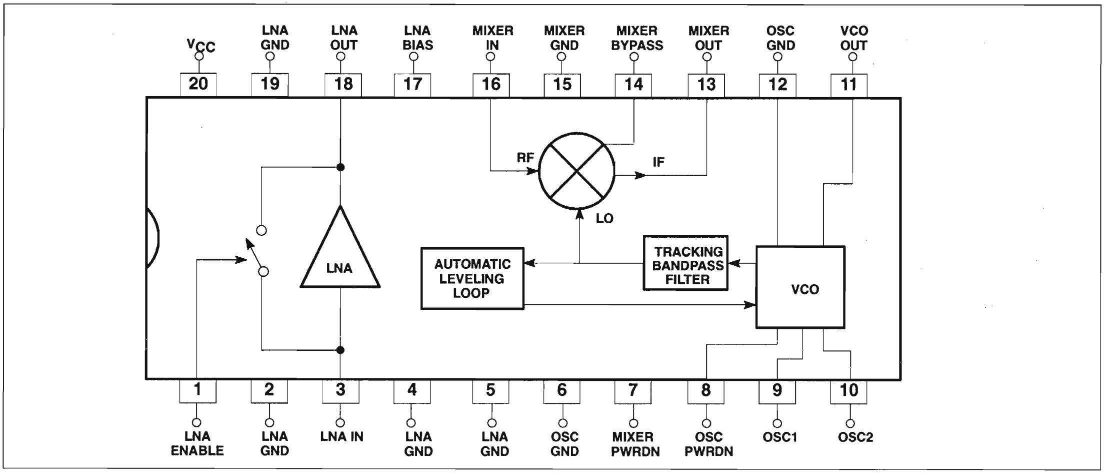
APPLICATIONS

- 900MHz cellular front-end
- 900MHz cordless front-end
- Spread spectrum receivers
- RF data links
- UHF frequency conversion
- Portable radio

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (Surface-mount, SSOP)	-40 to +85°C	SA620DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[1]	-0.3 to +6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 20-Pin Plastic SSOP	980	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 8V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance,
   θ_{JA}: 20-Pin SSOP = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	2.7 to 5.5	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{CC}	Supply current	LNA enable input high		10.4		mA
		LNA enable input low		7.2		mA
		VCO power-down input low		7.4		mA
		Mixer power-down input low		7.4		mA
		Full chip power-down		1.2		mA
V_T	Enable logic threshold voltage$^{\text{NO TAG}}$		1.2	1.5	1.8	V
V_{IH}	Logic 1 level	RF amp on	2.0		V_{CC}	V
V_{IL}	Logic 0 level	RF amp off	–0.3		0.8	V
I_{IL}	Enable input current	Enable = 0.4V	-1	0	1	µA
I_{IH}	Enable input current	Enable = 2.4V	-1	0	1	µA
V_{LNA-IN}	LNA input bias voltage	Enable = 2.4V		0.78		V
$V_{LNA-OUT}$	LNA output bias voltage	Enable = 2.4V		2.1		V
V_B	LNA bias voltage	Enable = 2.4V		2.1		V
V_{MX-IN}	Mixer RF input bias voltage			0.94		V

NOTE:
1. The ENABLE input must be connected to a valid logic level for proper operation of the SA620 LNA.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; Enable = +3V; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			-3σ	TYP	+3σ	
S_{21}	Amplifier gain	900MHz	10	11.5	13	dB
S_{21}	Amplifier gain in through mode	Enable = 0.4V, 900MHz	-9	-7.5	-6	dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity in pwr-dwn mode	900MHz		-0.014		dB/°C
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity enabled	900MHz		0.003		dB/°C
$\Delta S_{21}/\Delta f$	Gain frequency variation	800MHz - 1.2GHz		0.01		dB/MHz
S_{12}	Amplifier reverse isolation	900MHz		-20		dB
S_{11}	Amplifier input match[1]	900MHz		-10		dB
S_{22}	Amplifier output match[1]	900MHz		-12		dB
P_{-1dB}	Amplifier input 1dB gain compression	900MHz		-16		dBm
IP3	Amplifier input third order intercept	900MHz	-4.5	-3	-1.5	dBm
NF	Amplifier noise figure	900MHz	1.3	1.6	1.9	dB
t_{ON}	Amplifier turn-on time (Enable Lo → Hi)	See Figure 1		50		µs
t_{OFF}	Amplifier turn-off time (Enable Hi → Lo)	See Figure 1		5		µs
VG_C	Mixer voltage conversion gain: $R_P = R_L = 1k\Omega$,	f_S = 0.9GHz, f_{LO} = 0.8GHz, f_{IF} = 100MHz	14.5	16	17.5	dB
PG_C	Mixer power conversion gain: $R_P = R_L = 1k\Omega$,	f_S = 0.9GHz, f_{LO} = 0.8GHz, f_{IF} = 100MHz	1.5	3	4.5	dB
S_{11M}	Mixer input match[1]	900MHz		-10		dB
NF_M	Mixer SSB noise figure	900MHz	7.5	9	10.5	dB
P_{-1dB}	Mixer input 1dB gain compression	900MHz		-13		dBm
$IP3_M$	Mixer input third order intercept	f_2-f_1 = 1MHz, 900MHz	-7.5	-6	-4.5	dBm
IP_{2INT}	Mixer input second order intercept	900MHz		12		dBm
P_{RFM-IF}	Mixer RF feedthrough	900MHz		-20		dB
P_{LO-IF}	LO feedthrough to IF	900MHz		-25		dBm
P_{LO-RFM}	LO to mixer input feedthrough	900MHz		-30		dBm
P_{LO-RF}	LO to LNA input feedthrough	900MHz		-45		dBm
P_{VCO}	VCO buffer out	900MHz		-16		dBm
	VCO frequency range		300 (min)		1200 (max)	MHz
	VCO phase noise	Offset = 60kHz		-105		dBc/Hz

NOTE:
1. Simple L/C elements are needed to achieve specified return loss.

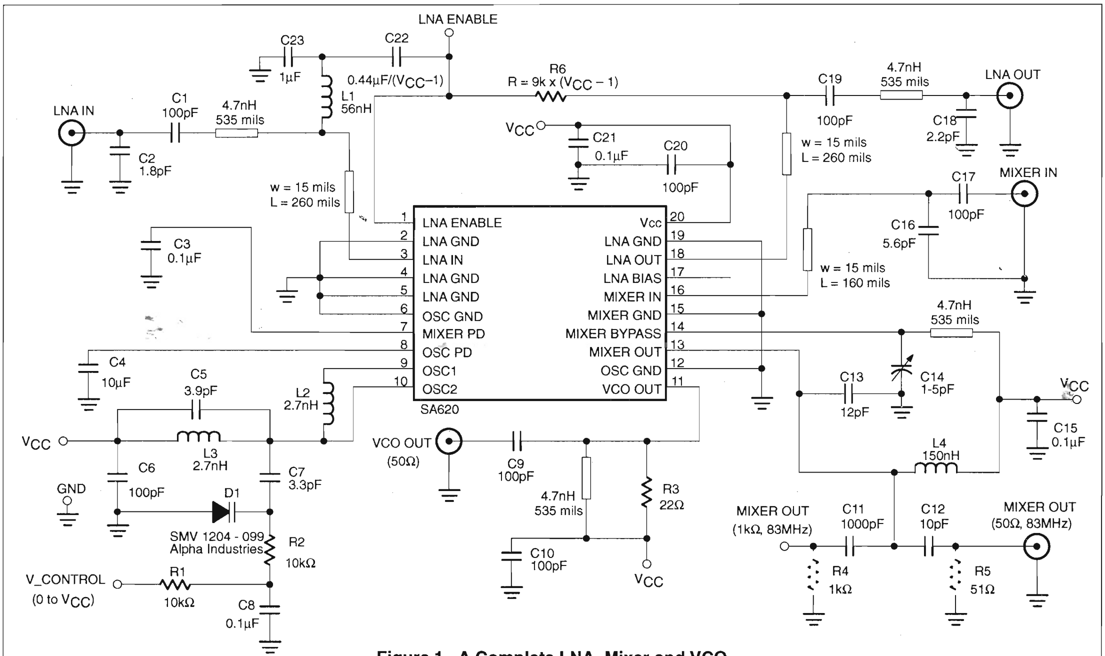


Figure 1. A Complete LNA, Mixer and VCO

CIRCUIT TECHNOLOGY

LNA

Impedance Match: Intrinsic return loss at the input and output ports is 7dB and 9dB, respectively. With no external matching, the associated LNA gain is ≈10dB and the noise figure is ≈1.4dB. However, the return loss can be improved at 900MHz using suggested L/C elements (Figure 1) as the LNA is unconditionally stable.

Noise Match: The LNA achieves 1.6dB noise figure at 900MHz when S_{11} = -10dB. Further improvements in S_{11} will slightly increase the NF and S_{21}.

Thru-Mode: A series switch can be activated to feed RF signals from LNA input to output with an attenuator (S_{21} = –7.5dB). As a result, the power handling is greatly improved and current consumption is decreased by 3.2mA as well. However, if this mode is not required, C23 and R6 can be deleted.

Temperature Compensation: The LNA has a built-in temperature compensation scheme to reduce the gain drift to 0.003dB/°C from –40°C to +85°C.

Supply Voltage Compensation: Unique circuitry provides gain stabilization over wide supply voltage range. The gain changes no more than 0.5dB when V_{CC} increases from 3V to 5V.

Mixer

Input Match: The mixer is configured for maximum gain and best noise figure. The user needs to supply L/C elements to achieve this performance.

Mixer Bypass: To optimize the IP3 of the mixer input, one must adjust the value of C14 for the given board layout. The value typically lies between 1 and 5pF. Once a value if selected, a fixed capacitor can be used. Further improvements in mixer IP3 can be achieved by inserting a resistive loss at the mixer input, at the expense of system gain and noise figure.

Tracking Bandpass Filter: At the LO input port of the mixer there is a second-order bandpass filter (approx. 50MHz bandwidth) which will track the VCO center frequency. The result is the elimination of low frequency noise injected into the mixer LO port without the need for an external LO filter.

Power Down: The mixer can be disabled by connecting Pin 7 to ground. If a Schottky diode is connected between Pin 1 (cathode) and Pin 7 (anode), the LNA disable signal will control both LNA and mixer simultaneously When the mixer is disabled, 3mA is saved.

Test Port: Resistor R5 can be substituted with an external test port of 50Ω input impedance. Since R5 and MIXER OUT have the same output power, the result is a direct power gain measurement.

VCO

Automatic Leveling Loop: An on-chip detector and loop amplifier will adjust VCO bias current to regulate the VCO amplitude regardless of the Q-factor (>10) of the resonator and varactor diode. However, the real current reduction will not occur until the VCO frequency falls below 500MHz. For a typical resonator the steady-state current is 3mA at 800MHz.

Buffered VCO Output: The VCO OUT (Pin 11) signal can drive an external prescaler directly (see also the Philips SA7025 low voltage, fractional-N synthesizer). The extracted signal levels need to be limited to –16dBm or less to maintain mixer IIP3.

Phase Noise: If close-in phase noise is not critical, or if an external synthesizer is used, C4 (Pin 8) can be decreased to a lower value.

Power-Down: The VCO can be disabled by connecting Pin 8 to ground. If a Schottky diode is connected between Pin 1 (cathode) and Pin 8 (anode), the LNA disable signal will control both LNA and VCO simultaneously. When the VCO is disabled, 3mA is saved.

TYPICAL PERFORMANCE CHARACTERISTICS

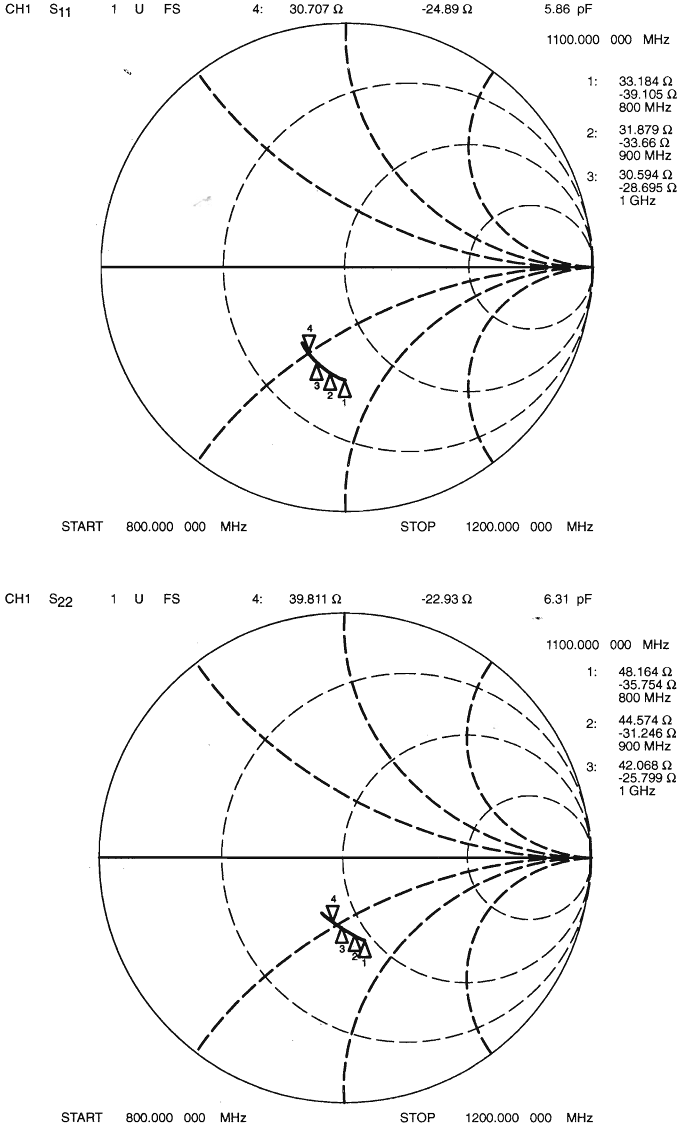


Figure 2. LNA Input and Output Match (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

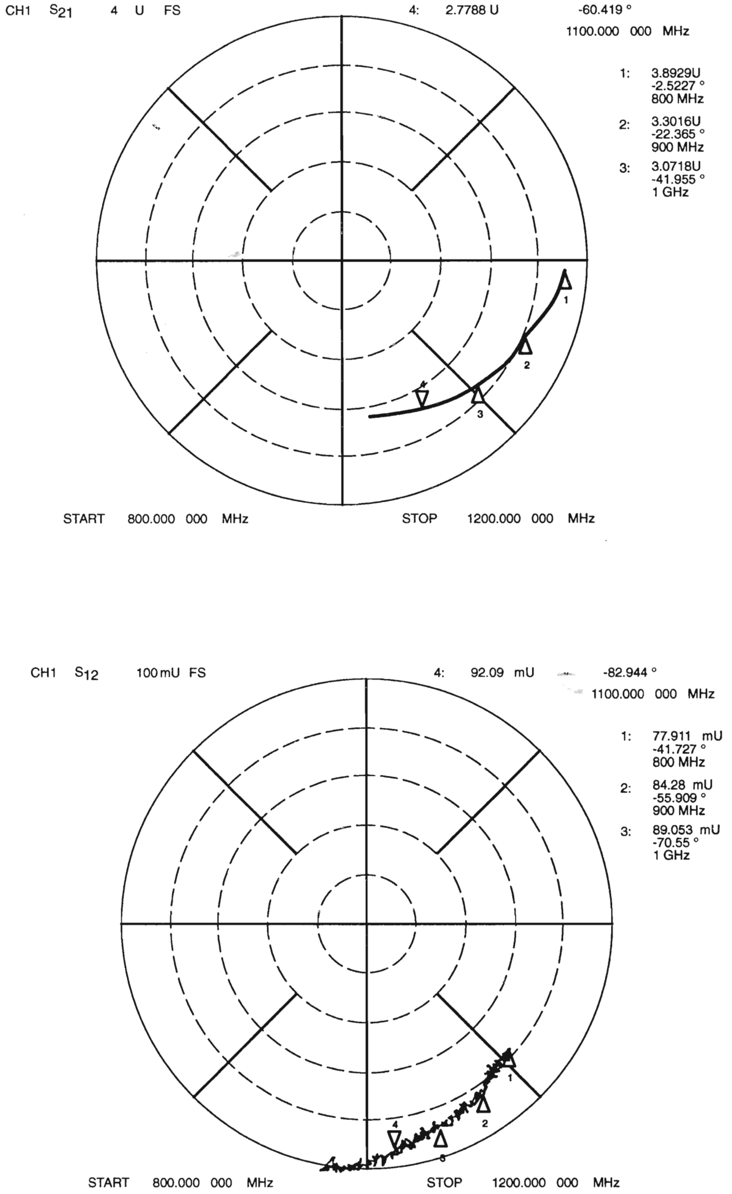


Figure 3. LNA Transmission and Isolation Characteristics (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

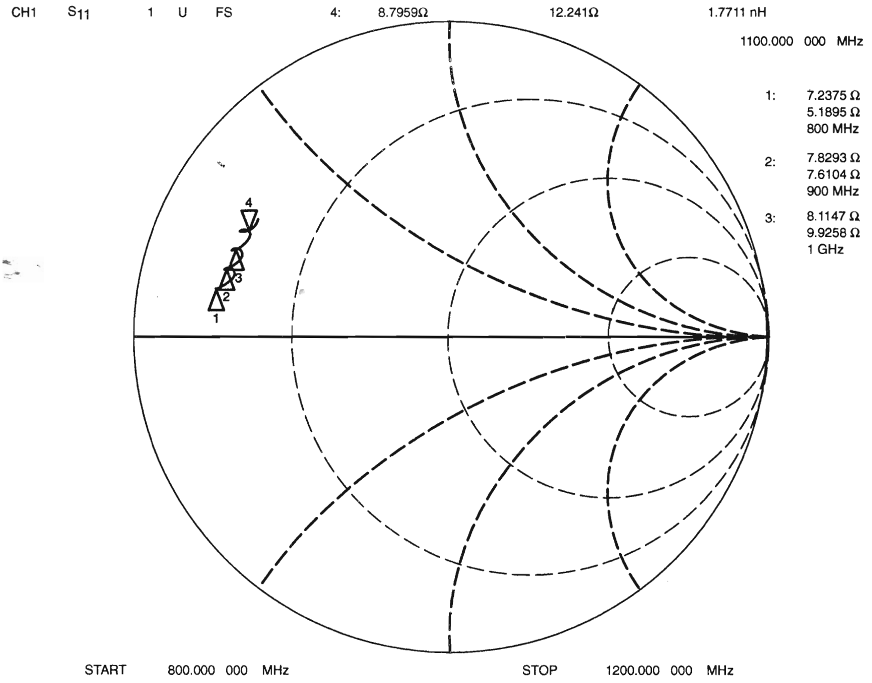
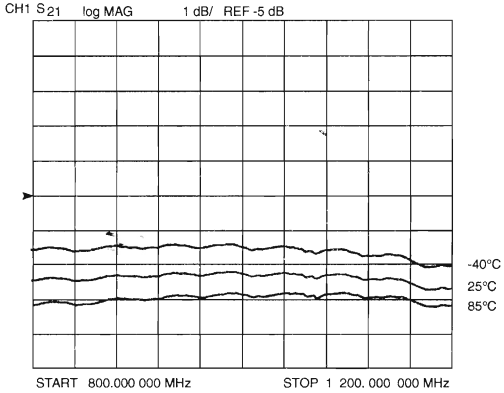


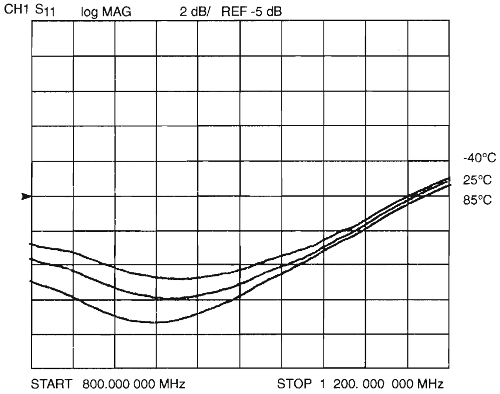
Figure 4. Mixer RF Input Match (at Device Pin)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

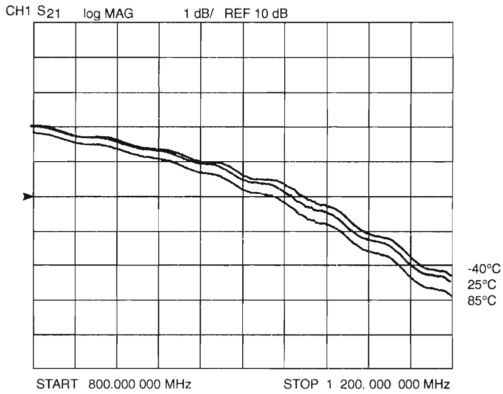
LNA Gain (S_{21}) In Through Mode vs. Frequency (V_{CC} = 3V)



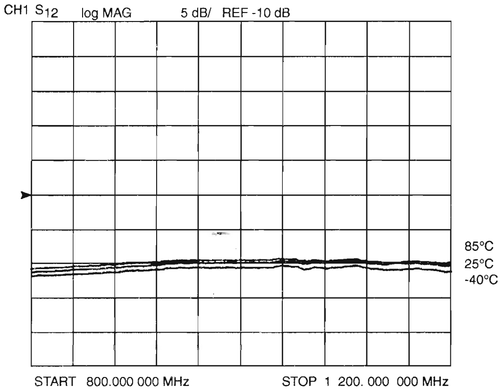
Mixer RF Input Match vs. Frequency (V_{CC} = 3V)



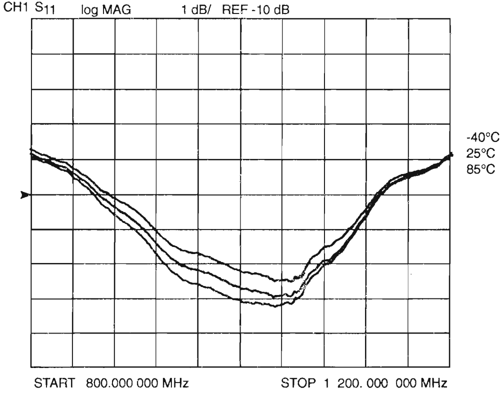
LNA Gain (S_{21}) vs. Frequency (V_{CC} = 3V)



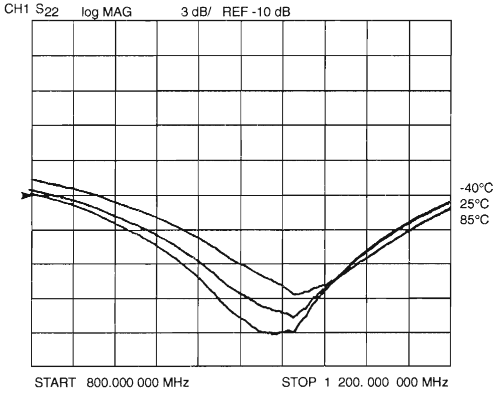
LNA Isolation (S_{12}) vs. Frequency (V_{CC} = 3V)



LNA Input Match (S_{11}) vs. Frequency (V_{CC} = 3V)

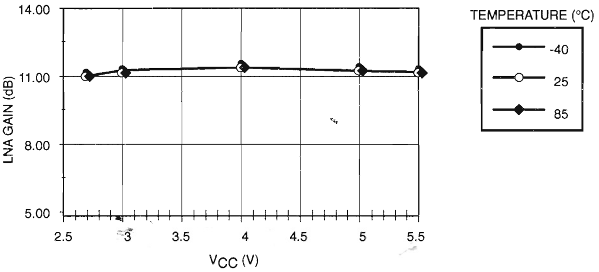


LNA Output Match (S_{22}) vs. Frequency (V_{CC} = 3V)

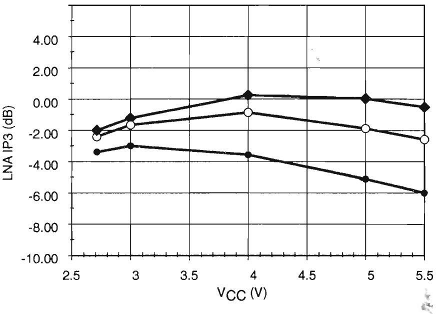


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

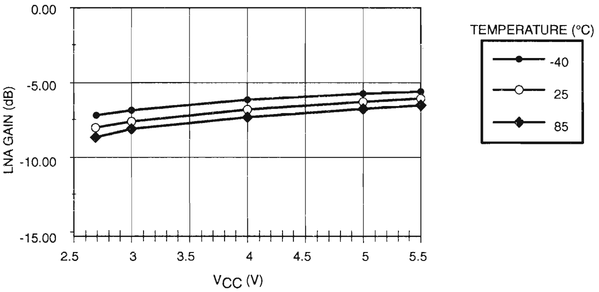
LNA Gain (Enabled) vs. Supply Voltage



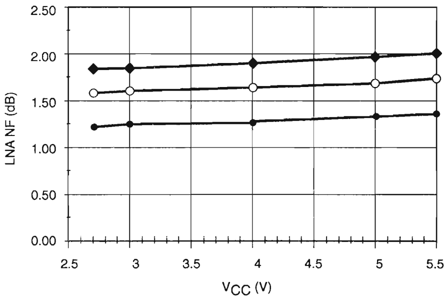
LNA IP3 (Enabled) vs. Supply Voltage



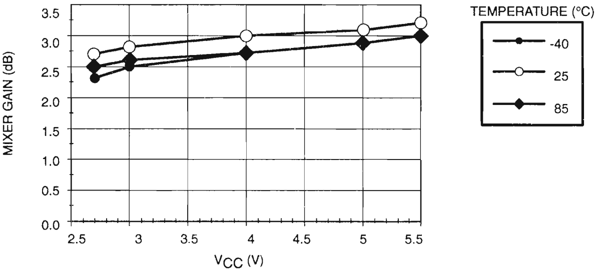
LNA Gain (Disabled) vs. Supply Voltage



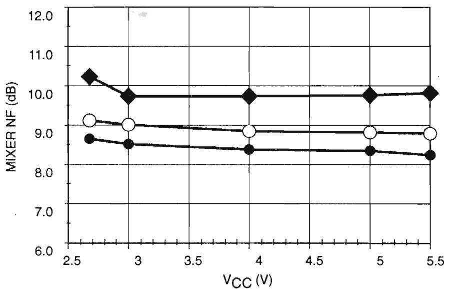
LNA Noise Figure (Enabled) vs. Supply Voltage



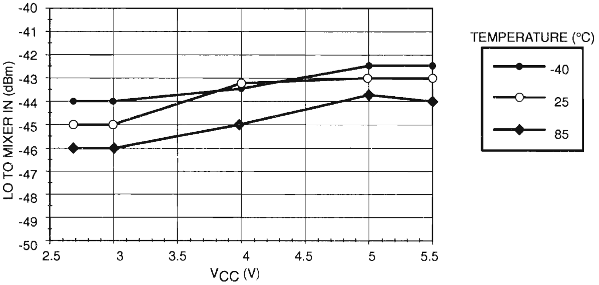
Mixer Power Gain vs. Supply Voltage



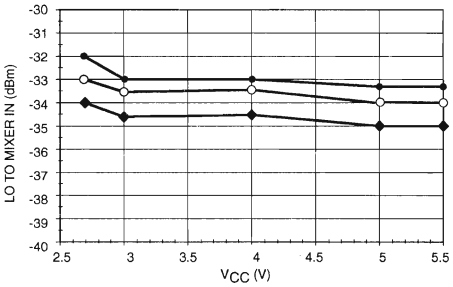
Mixer Noise Figure vs. Supply Voltage



LO to RF In Leakage vs. Supply Voltage

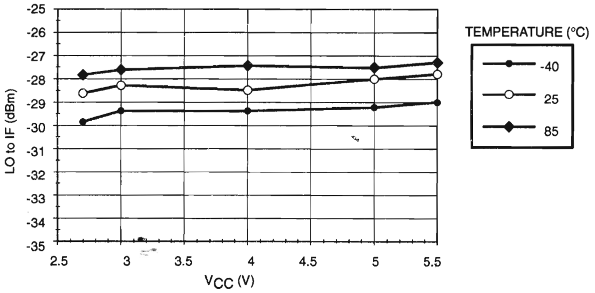


LO to Mixer In Leakage vs. Supply Voltage

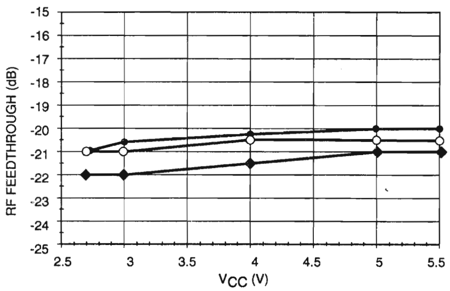


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

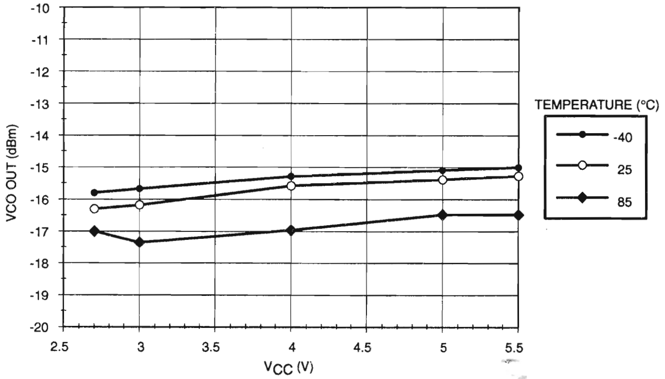
LO to IF Leakage vs. Supply Voltage



Mixer RF Feedthrough Leakage vs. Supply Voltage

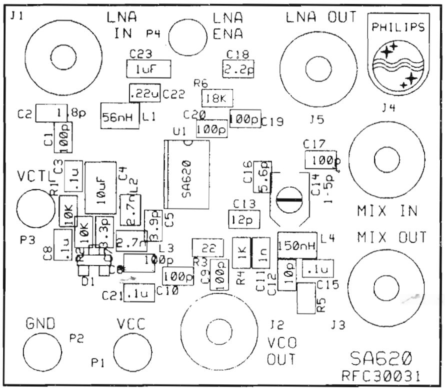


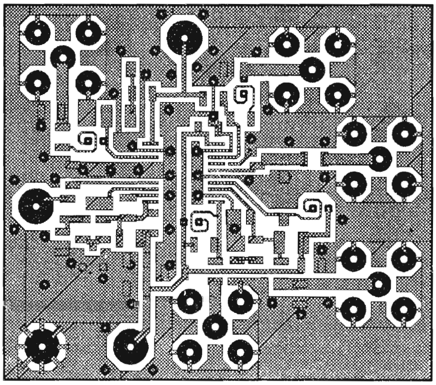
VCO Output Power vs. Supply Voltage

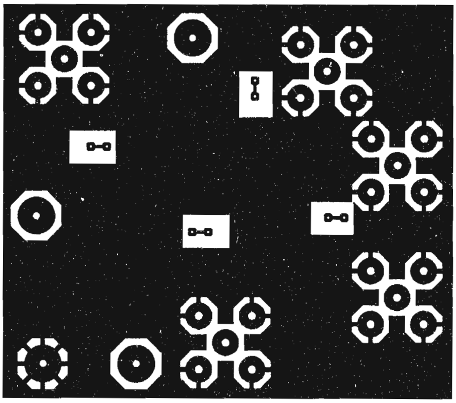


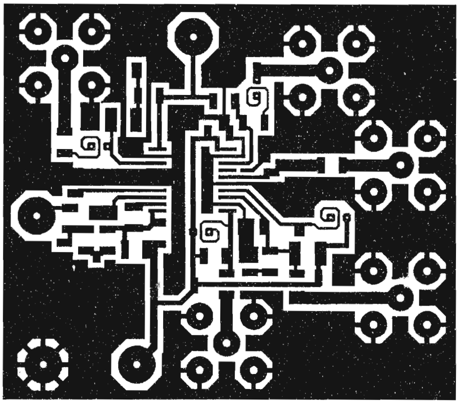
Low voltage LNA, mixer and VCO — 1GHz

SA620









Low voltage GSM front-end transceiver | SA1620

DESCRIPTION

The SA1620 is a combined receive (Rx) and transmit (Tx) front-end for GSM cellular telephones. The receive path contains two low noise amplifiers (LNA1 and LNA2) with four switchable attenuation steps. A Gilbert Cell mixer in the receive path down-converts the RF signal to a first IF of 70MHz to 500MHz. A second Gilbert Cell in the transmit path transposes a GMSK or phase modulated IF to RF by image reject mixing. A buffered LO signal is fed to Rx and Tx mixers. Rx or Tx path or the entire circuit may be powered-down.

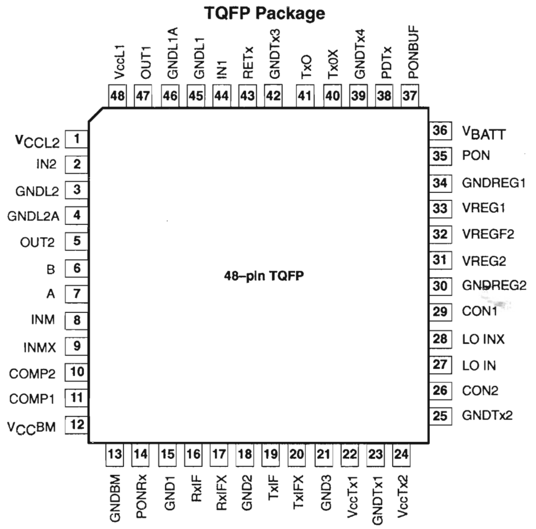
FEATURES

- Excellent noise figure: <2dB for the LNAs at 950MHz
- LNAs matched to 50Ω
- LNAs with gain control, 59dB dynamic range in four discrete steps
- Gain stability ±0.5dB within -40 to 85°C
- Absolute gain tolerance in the Rx path: ±2dB (active mode)
- Feedthrough attenuation LNA1 to Rx mixer ≥ 35dB
- Tx power adjustable from -3 to +12dBm by external resistor
- Direct supply: 2.7V to 5.5V
- Battery supply voltage V_{BATT} = 3.3V to 7.5V or direct supply
- Two DC regulators programmable for 2.9V, 3.3V, 3.6V or 5V
- Low current consumption: 25mA for Rx or 65mA for Tx
- Fully compatible with SA1638 GSM IF Digital I/Q circuit

APPLICATIONS

- 900MHz front end for GSM hand-held units
- Portable radio, TDMA systems

PIN CONFIGURATION



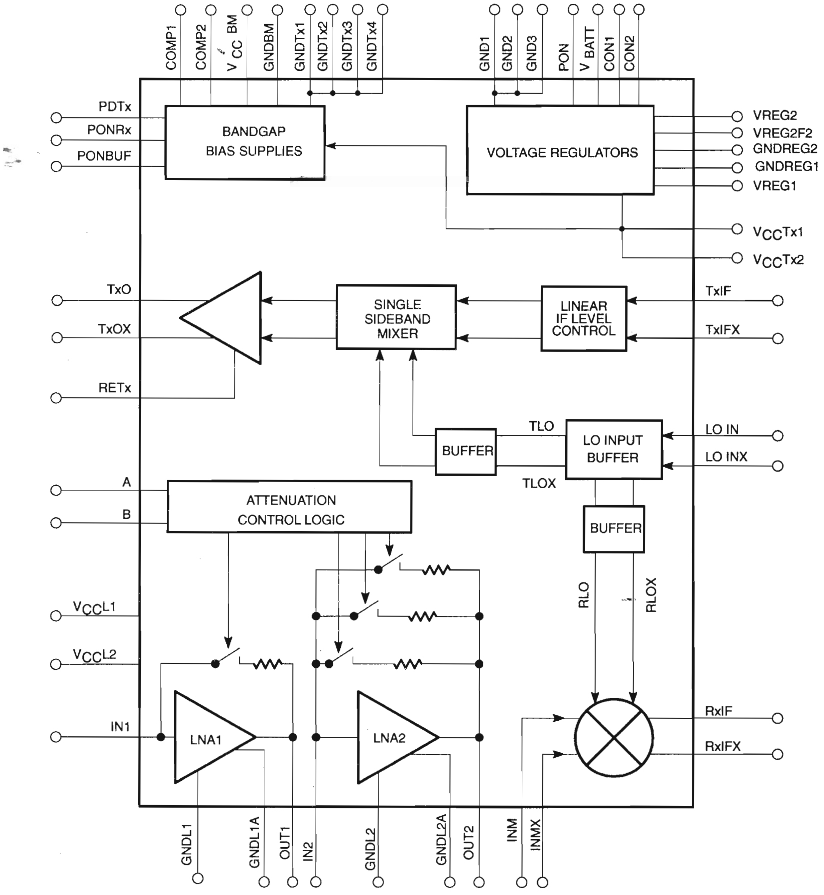
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48-Pin Thin Quad Flat Pack (TQFP)	-40 to +85°C	SA1620BE	1706B

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXX}	Supply voltages	2.7 to 5.5	V
V_{BATT}	Battery voltage	3.3 to 7.5	V
T_A	Operating ambient temperature range	-40 to +85	°C

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin Name	Description
DC Regulators		
15	GND1	Ground of regulator supply
18	GND2	Ground of regulator supply
21	GND3	Ground of regulator supply
26	CON2	Control 2, voltage select for regulator 1 and 2
29	CON1	Control 1, voltage select for regulator 1 and 2
30	GNDREG2	Ground of regulator 2
31	VREG2	Output of regulator 2
32	VREG2F2	Feedback of regulator 2
33	VREG1	Output of regulator 1
34	GNDREG1	Ground of regulator 1
35	PON	Power-on input of regulators
36	V_{BATT}	Input of regulator 1 and 2
Rx Path		
1	$V_{CC}L2$	Positive supply for LNA2
2	IN2	Input LNA2
3	GNDL2	Ground L2 for LNA2
4	GNDL2A	Ground L2A for LNA2
5	OUT2	Output LNA2
6	B	Attenuation select B for LNA1 and LNA2
7	A	Attenuation select A for LNA1 and LNA2
8	INM	RF input for Rx mixer, open emitter
9	INMX	Inverse RF input for Rx mixer, open emitter
10	COMP2	Capacitor for bias stabilization
11	COMP1	Capacitor for bias stabilization
12	$V_{CC}BM$	V_{CC} for Rx Bias and Rx mixer
13	GNDBM	Ground for Rx Bias and Rx mixer
14	PONRx	Power on input for Rx bias supply
16	RxIF	IF output, open collector
17	RxIFX	Inverse IF output, open collector
44	IN1	Input to LNA1
45	GNDL1	Ground L1 for LNA1
46	GNDL1A	Ground L1A for LNA1
47	OUT1	Output LNA1
48	$V_{CC}L1$	Positive supply for LNA1
Tx Path		
19	TxIF	IF input for Tx
20	TxIFX	Inverse IF input for Tx
22	$V_{CC}Tx1$	Positive supply for Tx input
23	GNDTx1	Ground for Tx input
24	$V_{CC}Tx2$	Positive supply for LO and Tx input
25	GNDTx2	Ground for LO and Tx input
38	PDTx	Power down Tx input
39	GNDTx4	Ground for Tx output
40	TxOX	Inverse Tx output, open collector
41	TxO	Tx output, open collector
42	GNDTx3	Ground 1 for Tx output side
43	RETx	Reference resistor for Tx output current
Elements for Tx and Rx Path		
27	LO IN	Input for Local Oscillator signal
28	LO INX	Inverse input for LO or AC ground
37	PONBUF	Power on first stage LO input buffer and bias

NOTES:

1. There are no ESD protection diodes at Pins 16, 17, 40 and 41. Thus, open-collector outputs may have increased DC voltage or higher AC peak voltage.
2. Pins 15, 18 and 21 are connected to each other and to a separate ground in REG1 and REG2.
3. Pins 23, 25, 42 and 39 are connected to each other and to the Tx path, LO buffer and associated bias supplies.
4. Pins 22 and 24 are connected to each other providing a sense input. They are also connected to the Tx path, LO buffer and associated bias supplies.
5. Pins 30 and 34 are not internally connected. They must be connected to external grounds.
6. Pins 48, 1, and 12 are not internally connected and have no ESD protection diodes between them. Power may be saved by connecting $V_{CC}L1$ or $V_{CC}L2$ to ground if LNA1 or LNA2 are not needed.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXX}	Supply voltages	-0.3 to +6.0	V
V_{BATT}	Battery voltage	-0.3 to +8.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CCXX}+0.3)	V
ΔV	$V_{CC}Tx1,2$ pins to $V_{CC}BM$	-0.3 to +1	V
ΔVG	Any GND pin to any other GND pin	0	V
P_D	Power dissipation, $T_A = 25°C$ (still air)	800	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C
V_{TXO}, V_{TXOX}	Positive RF peak voltage at Tx outputs	6	V
V_{RXIF}, V_{RXIFX}	Positive IF peak voltage at Rx mixer outputs	6	V

NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}. 48-pin TQFP: $\theta_{JA} = 67°C/W$.

DC REGULATORS

Two low drop regulators (REG1 and REG2) are included on the chip and may be used to deliver the supply voltage of the main circuitry (e.g., 2.9V) out of the battery (at V_{BATT} = 3.3 to 7.5V) as shown in Figure 6 and in Table 1.

REG1 is intended to supply, at least, the internal functions of the SA1620. Both regulators may also be used for external circuitry. For this application, different voltages may be programmed as shown in Table 1.

The transmitter supply pins (V_{CC}Tx1,2) also operate as a sensor connection in the feedback loop of REG1 and must be externally connected to pin VREG1. For REG2, the sensor pin VREGF2 must be connected to VREG2.

All ground pins are internally bonded to the header except for pins GNDL1, GNDREG1 and GNDREG2.

When both regulators are not used, connect pins V_{BATT}, PON, CON1, CON2, VREG1, VREG2 and VREG2F2 to ground.

Table 1. DC Regulator Output Voltage Control Pins

CON1	CON2	VREG1	VREG2	UNITS
L	L	2.9 ± 5%	2.9 ± 5%	V
L	H	3.3 ± 5%	3.3 ± 5%	V
H	L	3.6 ± 5%	3.6 ± 5%	V
H	H	5.0 ± 5%	5.0 ± 5%	V

NOTES:

1. The 2.9V setting allows ±5% and 55mV headroom above the 2.7V limit.
2. Logic levels at CON1 and CON2:
   H – Open circuit. Pin must not be connected externally. Logic high level supplied on chip.
   L – Connected to ground.
3. Currents at CON1 and CON2:
   H – 0μA
   L (PON = H) – 50μA
   L (PON = L) – <1μA

Table 2. DC Regulators

SYMBOL	PARAMETER	RATING	UNITS
V_{BATT}	Common positive input voltage at both regulators	3.3 to 7.5	V
VREG1, VREG2	Output voltages of regulators 1 and 2	See Table 1	V
I_{INT1}	Internal current of REG1 in power-on mode	$4 + I_{VREG1}/10$	mA
I_{INT2}	Internal current of REG2 in power-on mode	$2.5 + I_{VREG2}/10$	mA
I_{INT01}, I_{INT02}	Internal current in power-down mode	<15	μA
$I_{VREG1MAX}$[5]	Max output current at VREG1	100	mA
$I_{VREG2MAX}$[5]	Max output current at VREG2	30	mA
C13[4]	Capacitor at pin VREG1	0.1 to 1000	μF
C14[4]	Capacitor at pin VREG2	0.1 to 500	μF
BW[6]	V_{BATT} = 3.3V, I_{REG1} = 0.1mA	0.03	kHz
	V_{BATT} = 3.3V, I_{REG1} = 100mA	60	
	V_{BATT} = 7.5V, I_{REG1} = 100mA	80	
F_{REG}[8]	f ≤100kHz	≤–50	dB
	10MHz	≤–25	
	100MHz	tbd	
	400MHz	≤–30	

NOTES:

1. Power-on pin of Regulator 1 and 2: PON
2. Input currents at PON: <1μA. There are no pull-up or pull-down resistors.
3. Feedthrough attenuation from the logic input PON to the outputs VREG1 and VREG2: ≥40dB.
4. Recommended load capacitors: In every case C13 = C14 = 100nF to ground with series resistance ≤0.1Ω. Additional capacitor optional ≤1000μF with series resistance ≤5Ω.
5. At $T_j \geq 150°C$ a thermal switch reduces the output current.
6. Typical open loop bandwidths of regulator 1 at V_{REG1} = 2.9V and C13 = 100nF.
7. Switch on times: tbd
8. Feedthrough attenuation (at the indicated frequency f) from the input V_{BATT} to the outputs V_{REG1} and V_{REG2} at V_{BATT} = 3.3V, (CON1=CON2=L): $F_{REG}(f) = V_{REG}(f) / V_{BATT}(f)$.

DC ELECTRICAL CHARACTERISTICS

V_{CCxxx} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Transmitter						
$I_{VCCTX1,2}$	Current at pins V_{CC}Tx1,2	Tx active	35	44	58	mA
R1	External resistor[1]			240		Ω
V_{R1}	Internal supply at pin RETx	V_{CC}Tx1,2 = 2.7V		0.43		V
		V_{CC}Tx1,2 = 5.5V		0.45		
I_{R1}	Current at pin RETx	R1 = 240Ω, V_{CC}Tx1,2 = 2.7V		1.7		mA
		R1 = 240Ω, V_{CC}Tx1,2 = 5.5V		1.8		
I_{TXO}+ I_{TXOX}	Current sum at pins TxO + TxOX	R1 = 240Ω, V_{CC}Tx1,2 = 2.7V		20		mA
		R1 = 240Ω, V_{CC}Tx1,2 = 5.5V		22		
Low noise amplifiers						
I_{VCC}L1	Current at pin V_{CC}L1	G1hi mode		3.5		mA
I_{VCC}L2	Current at pin V_{CC}L2	G2hi mode		3.5		mA
Rx mixer						
I_{RxIF}	Output current at pin RxIF			4.5		mA
I_{RxIFX}	Output current at pin RxIFX			4.5		mA
I_{VCC}BM	Current at pin V_{CCBM}	PONBUF = H		0.8		mA
Logic levels[2]						
V_{IH}	Logic 1 level		2.0		V_{CCBM}	V
V_{IL}	Logic 0 level		0		0.8	V
I_I	Input logic current				1	µA
C_{Ia}	Input logic capacitance			1.7		pF

NOTES:

1. The output current I_{TXO} + I_{TXOX} is adjustable by the external resistor R1. I_{TXO} + I_{TXOX} = 10 * I_{R1}, IR1 = V_{R1}/R1,
2. Thresholds are independent of supply voltages. Thus the SA1620 is compatible with SA1638 and with the power down inputs of usual external voltage regulators.

AC ELECTRICAL CHARACTERISTICS

V_{CCXX} = +3V, T_A = 25°C; RF = 925-960MHz; IF=400MHz, f_{LO}=RF + IF; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Low Noise Amplifier LNA1[1]						
S_{21}	Gain	G1hi mode		10		dB
		G1hi mode, RF = 1800MHz		-1.5		
		G1lo mode		-11.6		
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	G1hi mode		0.003		dB/°C
		G1lo mode		0.0140		
$\Delta S_{21}/\Delta V_{CCL1}$	Gain/voltage sensitivity			0.1		dB/V
$\Delta S_{21}/\Delta f$	Gain frequency variation			0.01		dB/MHz
S_{12}	Reverse isolation	G1hi mode		-19		dB
S_{11}	Input match[2]	50Ω		-11		dB
S_{22}	Output match[2]	50Ω		-14		dB
P_{-1dB}	Input 1dB gain compression	G1hi mode		-14		dBm
IIP3	Input third order intercept			-5		dBm
NF	Noise figure			1.7	2	dB
t_{ON}	Turn-on time			7		µs
t_{OFF}	Turn-off time			0.5		µs
Low Noise Amplifier LNA2[1]						
S_{21}	Gain	G2hi mode		10.3		dB
		G2hi mode, RF = 1800MHz		0.5		dB
		G2lo1 mode		-7.7		dB
		G2lo2 mode		-20.7		
		G2lo3 mode		-27.8		
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	G2hi mode		0.003		dB/°C
		G2lo1,2,3 modes		0.014		
$\Delta S_{21}/\Delta V_{CCL2}$	Gain/voltage sensitivity			0.1		dB/V
$\Delta S_{21}/\Delta f$	Gain frequency variation			0.01		dB/MHz
S_{12}	Reverse isolation	G2hi mode		-24		dB
S_{11}	Input match[2]	50Ω		-13		dB
S_{22}	Output match[2]	50Ω		-15		dB
P_{-1dB}	Input 1dB gain compression	G2hi mode		-16		dBm
IIP3	Input third order intercept			-7		dBm
NF	Noise figure			2.0		dB
t_{ON}	Turn-on time			7		µs
t_{OFF}	Turn-off time			0.5		µs
Rx Mixer						
VG_C	Voltage conversion gain			19.3		dB
PG_C	Power conversion gain	R3=R4 = 800Ω		+8.2		dB
		RF = 1800MHz		-4		
$PG_C/\Delta T$	Gain temperature sensitivity					dB/°C
$PG_C/\Delta f$	Gain frequency variation					dB/MHz
S_{11}	Mixer input match at ports INM and INMX[3]			-13		dB
NF_M	SSB combined noise figure			10		dB
P_{-1dB}	Input 1dB compression	R3 = R4 = 800Ω		-7.3		dBm
IIP3	Input third order intercept			0		dBm
IIP2	Input second order intercept			19		dBm
G_{RFM-IF}	RF feedthrough	400MHz		-26		dB
$G_{LOfloor}$	LO floor feedthrough	400MHz		-30	-25	dB
G_{LO-IF}	LO feedthrough to IF	1.3GHz		-16		dB

AC ELECTRICAL CHARACTERISTICS (cont.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Rx Mixer (cont.)						
G_{LO-RFM}	LO to mixer input feedthrough	1.3GHz		-53		dBm
G_{LO-RF1}	LO to RF LNA1 input feedthrough	1.3GHz		-85		dBm
G_{LNA1-2}	LNA1 output to LNA2 input feedthrough	400MHz 1290-1760MHz		-41 -26		dB
G_{LNA2-M}	LNA2 output to mixer input feedthrough	1290-1760MHz		-23		dB
G_{LNA1-M}	LNA1 output to mixer input feedthrough	400MHz 1290-1760MHz		-50 -35		dB
LO input						
Z_{IN}	Input impedance (each single-ended input)	1.3GHz		35-j97		Ω
P_{IN}	Input power			-18		dBm
A_{SAT}	Transistor saturation limit, max input amplitude			500		mV
Tx IF input						
$\|Z_{IN}\|$	Input impedance	400MHz		2		kΩ
P_{IN}	Input power			-25		dBm
Tx RF output						
P_{OUT}	R1 = 250Ω, R5 = R6 = 200Ω, V_{CC}Tx1,2 = 2.7V			8.2		dBm
	R1 = 250Ω, R5 = R6 = 200Ω, V_{CC}Tx1,2 = 5.5V			9.2		dBm

NOTES:

1. If the LNA1 is not needed, connect pin V_{CC}L1 and IN1 to GND. If the LNA2 is not needed, connect pin V_{CC}L2 and IN2 to GND.
2. Simple L/C elements are needed to achieve specified return loss.
3. The mixer RF inputs (emitters of a Gilbert Cell) may be driven by a symmetrical matching network.
4. Input symmetry suppression is such that the product 6*RF–4*LO is to be suppressed by at least 66dB relative to the wanted IF output when the input to the mixer is at –32dBm.

Table 3. Power-Down and Tx/Rx Control Logic

No.	PONBUF	PDTX	PONRX	MODE	RESULT
1	H	H	L	Standby	LO buffer active, Tx and Rx path inactive
2	H	L	L	Transmit	LO buffer active, Tx path active, Rx path inactive (LNAs + mixer)
3	H	H	H	Receive	Tx path inactive, LO buffer and Rx path active (LNAs + mixer)
4	H	L	H	Calibrate	Tx path and Rx LNAs inactive, LO buffer and Rx mixer active
5	L	x	x	Power-Down	Tx- and Rx-path, LO buffers and Bias inactive

NOTES:

1. Logic levels of PONBUF, PDTx and PONRx: TTL, see DC Electrical Characteristics.
2. Logic levels / polarities are compatible with Philips Semiconductors Power Amp Controller PCA5075 and synthesizers UMA1019 or SA8025.
3. First stage of LO buffer and parts of bias supply are powered on by PONBUF.
4. Tx- or Rx-paths may be activated for special timeslots. Lines 1 and 4 show options to support DC offset calibrations at baseband mixers, following in the receiver chain (SA1638).
5. Feedthrough attenuation PONBUF, PDTx, and PONRx to outputs: [tbd]

Table 4. Gain Control Logic for LNA1 and LNA2

INPUT		ATTENUATION STEP	GAIN		POWER CONSUMPTION	
a	b		LNA1	LNA2	LNA1	LNA2
H	H	0	G1hi	G2hi	on	on
H	L	1	G1hi	G2lo1	on	off
L	H	2	G1hi	G2lo2	on	off
L	L	3	G1lo	G2lo3	off	off

NOTES:

1. Logic levels of a and b: TTL
2. For values of G1hi and G1lo, G2hi, G2lo1, G2lo2 and G2lo3 see LNA1 and LNA2 AC Electrical Characteristics.
3. Feedthrough attenuation A and B to outputs: tbd.

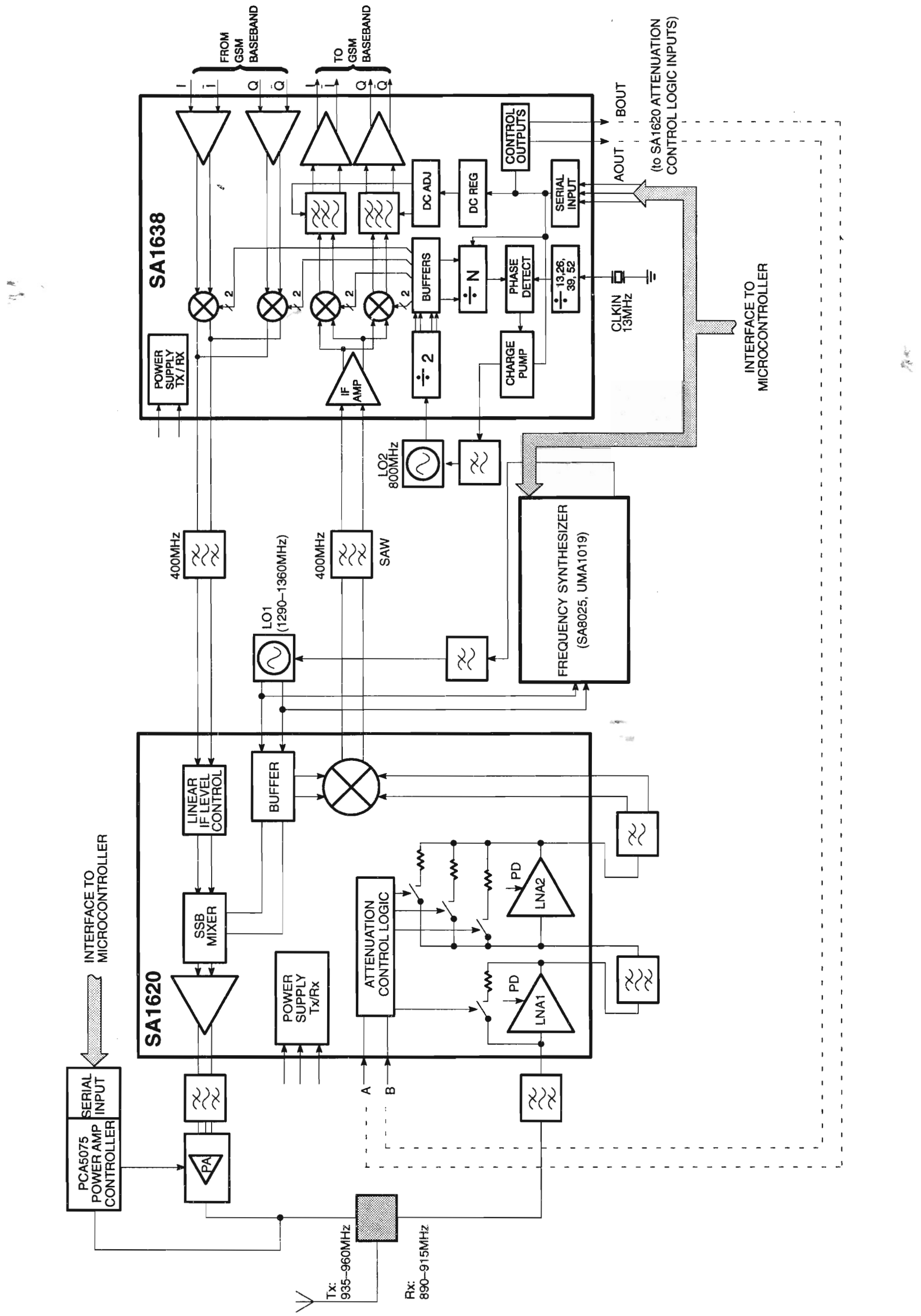

FROM GSM BASEBAND
TO GSM BASEBAND
I
Ī
Q
Q̄
SA1638
POWER SUPPLY TX / RX
2
2
2
2
BUFFERS
÷ 2
IF AMP
÷ N
PHASE DETECT
CHARGE PUMP
÷ 13, 26, 39, 52
DC ADJ
DC REG
SERIAL INPUT
CONTROL OUTPUTS
AOUT
BOUT
(to SA1620 ATTENUATION CONTROL LOGIC INPUTS)
CLKIN 13MHz
INTERFACE TO MICROCONTROLLER
LO2 800MHz
FREQUENCY SYNTHESIZER (SA8025, UMA1019)
400MHz
400MHz
SAW
LO1 (1290–1360MHz)
SA1620
LINEAR IF LEVEL CONTROL
BUFFER
SSB MIXER
POWER SUPPLY Tx/Rx
ATTENUATION CONTROL LOGIC
PD
LNA2
PD
LNA1
A
B
INTERFACE TO MICROCONTROLLER
SERIAL INPUT
PCA5075 POWER AMP CONTROLLER
PA
Tx: 935–960MHz
Rx: 890–915MHz

Figure 5.

Overview of Dual GSM/PCN Architecture

The SA1620 RF front-end and SA1638 IF transceivers form a dual conversion architecture which uses a common IF and standard I/Q baseband interface for both transmit and receive paths. This approach avoids the screening difficulties of direct modulation in the transmit direction and the mass production and practical performance issues related to direct conversion in the receive direction. The time division multiplex nature of the GSM system permits integration of the transmit and receive functions together on the one RF and one IF chips. This simplifies the distribution of local oscillator signals, maximizes circuitry commonality, and reduces power consumption.

The SA1620 and SA1638 allow considerable flexibility to optimize the transceiver design for particular price/size/performance requirements, through choice of appropriate RF and IF filters. The IF may be chosen freely in the range 70–500MHz. The same IF can be used in the transmit and receive directions. Alternately, different IFs can be used if the SA1638 synthesizer frequency is switched between transmit and receive timeslots. The comparison frequency of the SA1638 PLL is high in order to provide fast switching time.

With suitable choice of the IF, an identical SA1638 IF receiver design can be used for both 900MHz GSM and 1800MHz PCN (DCS1800) equipment.

General Benefits/Advantages

- 2.7V operation. Compatible with 3V digital technology and portable applications. (Higher voltage operation also possible, if desired.)
- Excellent dynamic range. The availability of two LNAs allows flexibility in receiver dynamic design for portable and mobile GSM spec. applications with appropriate filters. If for a particular application a GaAs or discrete front-end is desired, one of the LNAs can be left unpowered. The placing of the AGC gains switches at the front means that for most of the time some attenuation will be inserted, further increasing typical dynamic performance beyond that specified by GSM.
- High power transmit output driver, delivering +7.5dBm output. This is sufficient to drive a filter and power amplifier input, without a driver amplifier. To avoid unnecessary current consumption the output power can be reduced, if not required, by appropriate choice of an external resistor.
- DC offsets generated in the receive channel are independent of the AGC setting, and correctable by software to prevent erosion of signal handling dynamic range by DC offsets. Independence of DC from AGC setting is achieved by putting the gain switches in the RF front-end.
- Minimal high-quality filter requirements. As a result of the integration in the SA1638 of high quality channel selectivity filters, only sufficient filtering is needed in the receive path to provide blocking protection for the second mixers. This reduces receiver cost and size.
- Operation at a high IF allows RF image reject filters to be relaxed. For example, at a 400MHz IF, the natural gain roll-off in the LNAs and mixer suppresses the image signal in the 1800MHz band by typically 28dB below the desired 900MHz band signal.

Receive Path

Multiple LNAs allow the flexibility to exploit the best choice of currently available filters (on performance, size, or cost grounds). This approach is preferable to a single high-gain stage as the stray cross-coupling effects between pins remain manageable. In a single stage amplifier this would limit the amount of rejection of out-of-band signals that could be achieved, and would also limit the amount of AGC attenuation that could be practically implemented.

The LNAs are powered up only when PONBUF, PDTx and PONRx are high, to allow a high degree of battery economy. If greater sensitivity is required for an application, an external preamplifier circuit can be used instead of LNA1, and LNA1 left unconnected.

A special mode is provided with just the IF output related circuitry active in order to allow calibration of the DC offset at the SA1638 baseband receive outputs. This offset contains a contribution due to coupling effects between the second local oscillator and the IF circuitry, and therefore the receiver is set up in the receive state (but with incoming signals excluded) to allow accurate offset calibration.

Gain Control

Gain control is implemented in the SA1620 RF front-end. This avoids the disruption of the DC offset at the baseband IQ outputs that is typically caused by changes in the AGC. The SA1620 and SA1638 are designed so that the GSM dynamic range requirements can be met with the AGC remaining on the maximum gain setting.

These gain steps scale the dynamic range of the received signal (e.g., 90dB for GSM) into the dynamic range of the baseband processing device.

The absolute gain tolerances may be measured together with the attenuation tolerances of external filters during production of the receiver equipment. After software calibration switching from one dynamic range to another will cause only minor errors.

Tx Path

TXIF and TXIFX are differential IF inputs for phase modulated signals (e.g., GMSK). There is an IF level control loop which provides a constant amplitude to an image reject up mixer. Thus, this mixer operates linearly in the IF path, independent of IF level tolerances.

The single sideband up mixer is sufficient in quadrature to achieve the typical performance indicated in Table 6 over an IF range of 250 to 500MHz. The mixer is operating in switching mode by well matched 0° and 90° LO signals, optimized for 1.1 to 1.5GHz.

The Tx output stage operates in switching mode. Thus, parasitic AM at the IF is not transferred. The outputs TXO and TXOX may be used symmetrically or single-ended. Some spurious emissions will be very low when a symmetrical output signal is used.

$P_{OUT} = 6.25 * (R_5 + R_6) * (I_{R1})^2$

with $R_5 = R_6$ according to Figure 6 and $I_{R1} = V_{R1}/R1$ according to DC Electrical Characteristics. P_{OUT} is adjustable with R1 and is accurate to within ±1dB over the full voltage range 2.7 to 5.5V, and ±0.5dB from a given supply voltage. The absolute limit of the negative peak voltage swing at pins TxO and TxOX is $V_{SAT} = V_{CC}Tx1,2 - 1V$. The absolute limit of the positive peak voltage is +6V.

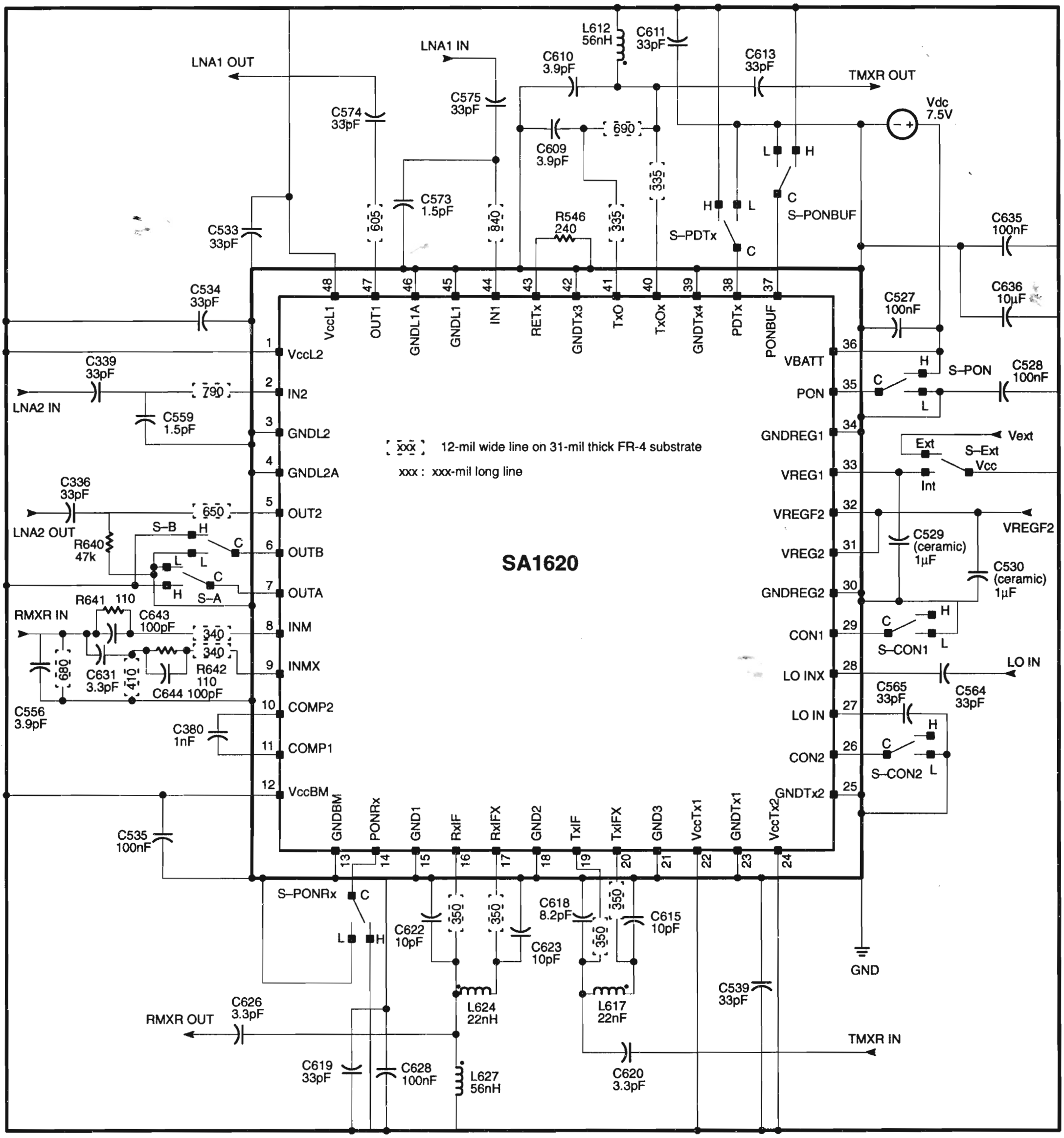


Figure 6. Application Circuit

LO Input

The LO input is used in Tx- and in Rx-mode.

Only one synthesizer PLL is necessary to supply the LO input with different frequencies in Tx and Rx timeslots.

The LO input buffer should only be set in power-down mode together with the PLL. As further buffering is included on chip there will be no influence on the PLL in active mode when the SA1620 Rx- or Tx-path is power On or Off. Current consumption can thus be saved by powering on the Rx- and Tx-circuitry just before it is required, without disruption of the LO circuitry. LO input pins LO IN and LO INX may be used single-ended or symmetrically.

Table 5. GSM/DSC1800 Frequency Specification

(GSM 05.05, Version 4.2.0, April 1992) Mobile Stations Frequency Bands

	GSM	EGSM	DCS1800	Unit
Tx	890 to 915	880.2 to 915	1710 to 1785	MHz
Rx	935 to 960	925.2 to 960	1805 to 1880	MHz

Table 6. Measured Tx Output Frequency and Tx Mixer Products

IF=400MHz, symmetrical load at pins TxO, TxOX.

No.	SPECTRAL LINE f=n*IF+m*LO MHz					RELATIVE POWER OF SPECTRAL LINE			REMARKS
	LO = 1280MHz	LO = 1300MHz	LO = 1315MHz	Order					
				n	m	min dBc	typ dBc	max dBc	
1	80	100	115	–3	1		–70		
2	160	200	230	–6	2		–76		
3	320	300	285	4	–1		–60		
4	400	400	400	1	0		–46		IF
5	480	500	515	–2	1		–31		
6	560	600	630	–5	2		–62		
7	720	700	685	5	–1		–56		
8	800	800	800	2	0		–37		2)
9	880	900	915	–1	1		0		1)
10	960	1000	1030	–4	2		–46		3)
11	1020	1100	1185	6	–1		–63		
12	1200	1200	1200	3	0		–60		
13	1280	1300	1315	0	1		–32		LO
14	1360	1400	1430	–3	2		–46		
15	1440	1500	1545	–6	3		–64		
16	1600	1600	1600	4	0		–75		
17	1680	1700	1715	1	1		–50		4) 5)
18	1760	1800	1830	–2	2		–34		3)
19	1840	1900	1945	–5	3		–68		3)
20	2000	2000	2000	5	0		–77		
21	2080	2100	2115	2	1		–74		
22	2160	2200	2230	–1	2		–67		
23	2240	2300	2345	–4	3		–59		
24	2400	2400	2400	6	0		–75		
25	2480	2500	2515	3	1		–76		
26	2560	2600	2630	0	2		–70		2LO

NOTE:
1. Desired Tx output frequency LO–IF corresponding to EGSM Tx band in Table 5.
2. (LO+IF)–(LO–IF) = 2 * IF
3. See Rx bands in Table 5
4. LO+IF = mixer image frequency
5. See Tx bands in Table 5

Table 7. Measured Tx Output Noise Floor

Measured 10MHz away from spectral lines of Table 6.

Frequency MHz		dBc/Hz			REMARKS
		MIN	TYP	MAX	
< 860			–135		
860 to 880			–134		
880.2 to 890			–133		EGSM TX extension
890 to 915			–133		GSM TX
915 to 925			–133		
925.2 to 935			–134		EGSM RX extension
935 to 960			–135		GSM RX
960 to 1000			–135		
1000 to 1710			–135		
1710 to 1785			–146		DCS1800 TX
1785 to 1805			–145		
1805 to 1880			–144		DCS1800 RX
1880 to 12750			–147		
>12750			tbd		

Tx Noise Density at Adjacent Channel

Measured 200kHz away from Tx–RF: ≤–130dBc/Hz

FM front-end IC TDA1574

GENERAL DESCRIPTION

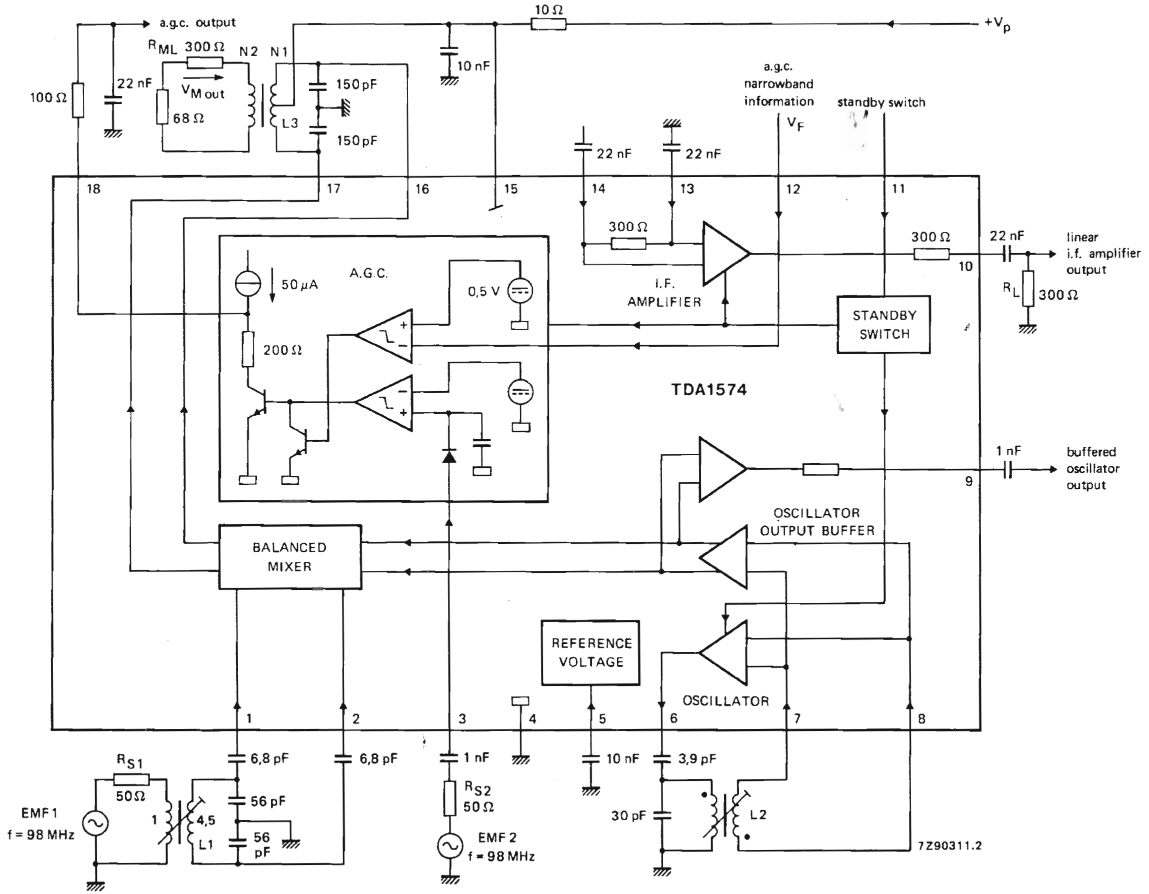
The TDA1574 is a monolithic integrated FM tuner circuit designed for use in the r.f./i.f. section of car radios and home-receivers. The circuit comprises a mixer, oscillator and a linear i.f. amplifier for signal processing, plus the following additional features.

Features

- Keyed automatic gain control (a.g.c.)
- Regulated reference voltage
- Buffered oscillator output
- Electronic standby switch
- Internal buffered mixer driving

QUICK REFERENCE DATA

Supply voltage range (pin 15)	V_P		7 to 16	V
Mixer input bias voltage (pins 1 and 2)	$V_{1,2\text{-}4}$	typ.	1	V
noise figure	NF	typ.	9	dB
Oscillator output voltage (pin 6)	$V_{6\text{-}4}$	typ.	2	V
output admittance at pin 6 for f = 108,7 MHz	Y22	typ.	1,5 + j2	mS
Oscillator output buffer				
D.C. output voltage (pin 9)	$V_{9\text{-}4}$	typ.	6	V
Total harmonic distortion	THD	typ.	−15	dBC
Linear i.f. amplifier output voltage (pin 10)	$V_{10\text{-}4}$	typ.	4,5	V
noise figure at $R_S = 300\ \Omega$	NF	typ.	6,5	dB
Keyed a.g.c. output voltage range (pin 18)	$V_{18\text{-}4}$		+ 0,5 to V_P—0,3	V



Coil data

L1: TOKO MC-108, 514HNE-150014S14; L = 0,078 μH
L2: TOKO MC-111, E516HNS-200057; L = 0,08 μH
L3: TOKO coil set 7P, N1 = 5,5 + 5,5 turns, N2 = 4 turns

Fig. 1 Block diagram and test circuit.

FUNCTIONAL DESCRIPTION

Mixer

The mixer circuit is a double balanced multiplier with a preamplifier (common base input) to obtain a large signal handling range and a low oscillator radiation.

Oscillator

The oscillator circuit is an amplifier with a differential input. Voltage regulation is achieved by utilizing the symmetrical tanh-transfer-function to obtain low order 2nd harmonics.

Linear IF amplifier

The IF amplifier is a one stage, differential input, wideband amplifier with an output buffer.

Keyed AGC

The AGC processor combines narrow- and wideband information via an RF level detector, a comparator and an ANDing stage. The level dependent, current sinking output has an active load, which sets the AGC threshold.

The AGC function can either be controlled by a combination of wideband and narrowband information (keyed AGC), or by a wideband information only, or by narrowband information only. If only narrowband AGC is wanted pin 3 should be connected to pin 5. If only wideband AGC is wanted pin 12 should be connected to pin 13.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_P = V_{15\text{-}4}$	max.	18	V
Mixer output voltage (pins 16 and 17)	$V_{16,\ 17\text{-}4}$	max.	35	V
Standby switch input voltage (pin 11)	$V_{11\text{-}4}$	max.	23	V
Reference voltage (pin 5)	$V_{5\text{-}4}$	max.	7	V
Field strength input voltage (pin 12)	$V_{12\text{-}4}$	max.	7	V
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}	−55 to +	150	°C
Operating ambient temperature range	T_{amb}	−40 to	+ 85	°C

THERMAL RESISTANCE

From junction to ambient (in free air)	$R_{th\ j\text{-}amb}$	=	80	K/W

Note

All pins are short-circuit protected to ground.

CHARACTERISTICS

$V_P = V_{15\text{-}4} = 8{,}5$ V; $T_{amb} = 25\ ^{o}C$; measured in test circuit Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 15)					
Supply voltage	$V_P = V_{15\text{-}4}$	7	–	16	V
Supply current (except mixer)	$I_P = I_{15}$	16	23	30	mA
Reference voltage (pin 5)	$V_{5\text{-}4}$	3,9	4,1	4,4	V
Mixer					
D.C. characteristics					
Input bias voltage (pins 1 and 2)	$V_{1,2\text{-}4}$	–	1	–	V
Output voltage (pins 16 and 17)	$V_{16,17\text{-}4}$	4	–	35	V
Output current (pin 16 + pin 17)	$I_{16} + I_{17}$	–	4,0	–	mA
A.C. characteristics (f_i = 98 MHz)					
Noise figure	NF	–	9	–	dB
Noise figure including transforming network	NF	–	11	–	dB
3rd order intercept point	$EMF1_{IP3}$	–	115	–	dBμV
Conversion power gain $10 \log \frac{4\ (V_{M(out)}\ 10{,}7\ \text{MHz})^2}{(EMF1\ 98\ \text{MHz})^2} \times \frac{R_{S1}}{R_{ML}}$	G_P	–	14	–	dB
Input resistance (pins 1 and 2)	$R_{1,2\text{-}4}$	–	14	–	Ω
Output capacitance (pins 16 and 17)	$C_{16,17}$	–	13	–	pF
Oscillator					
D.C. characteristics					
Input voltage (pins 7 and 8)	$V_{7,8\text{-}4}$	–	1,3	–	V
Output voltage (pin 6)	$V_{6\text{-}4}$	–	2	–	V
A.C. characteristics (f_{osc} = 108,7 MHz)					
Residual FM (Bandwidth 300 Hz to 15 kHz); de-emphasis = 50 μs	Δf	–	2,2	–	Hz

parameter	symbol	min.	typ.	max.	unit
Linear i.f. amplifier					
D.C. characteristics					
Input bias voltage (pin 13)	$V_{13\text{-}4}$	–	1,2	–	V
Output voltage (pin 10)	$V_{10\text{-}4}$	–	4,5	–	V
A.C. characteristics (f_i = 10,7 MHz)					
Input impedance					
	$R_{14\text{-}13}$	240	300	360	Ω
	$C_{14\text{-}13}$	–	13	–	pF
Output impedance					
	$R_{10\text{-}4}$	240	300	360	Ω
	$C_{10\text{-}4}$	–	3	–	pF
Voltage gain					
$20 \log \frac{V_{10\text{-}4}}{V_{14\text{-}13}}$	G_{VIF}	27	30	–	dB
$T_{amb} = -40$ to $+85$ °C	ΔG_{VIF}	–	0	–	dB
1 dB compression point (r.m.s. value)					
at V_P = 8,5 V	$V_{10\text{-}4rms}$	–	750	–	mV
at V_P = 7,5 V	$V_{10\text{-}4rms}$	–	550	–	mV
Noise figure					
at R_S = 300 Ω	NF	–	6,5	–	dB
Keyed a.g.c.					
D.C. characteristics					
Output voltage range (pin 18)	$V_{18\text{-}4}$	0,5	–	V_P–0,3	V
A.G.C. output current					
at $I_3 = \phi$ or					
$V_{12\text{-}4}$ = 450 mV; $V_{18\text{-}4} = V_P/2$	$-I_{18}$	25	50	100	μA
at $V_{3\text{-}4}$ = 2 V and					
$V_{12\text{-}4}$ = 1 V; $V_{18\text{-}4} = V_{15\text{-}4}$	I_{18}	2	–	5	mA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Narrowband threshold					
at $V_{3\text{-}4}$ = 2 V; $V_{12\text{-}4}$ = 550 mV	$V_{18\text{-}4}$	–	–	1	V
at $V_{3\text{-}4}$ = 2 V; $V_{12\text{-}4}$ = 450 mV	$V_{18\text{-}4}$	V_P–0,3	–	–	V
A.C. characteristics (f_i = 98 MHz)					
Input impedance					
	$R_{3\text{-}4}$	–	4	–	kΩ
	$C_{3\text{-}4}$	–	3	–	pF
Wideband threshold (r.m.s. value) (see figures 2, 3, 4 and 5)					
at $V_{12\text{-}4}$ = 0,7 V; $V_{18\text{-}4}$ = $V_P/2$; I_{18} = 0	$EMF2_{rms}$	–	17	–	mV
Oscillator output buffer (pin 9)					
D.C. output voltage	$V_{9\text{-}4}$	–	6,0	–	V
Oscillator output voltage (r.m.s. value)					
at $R_L = \infty$; C_L = 2 pF	$V_{9\text{-}4(rms)}$	–	110	–	mV
at R_L = 75 Ω	$V_{9\text{-}4(rms)}$	30	50	–	mV
D.C. output impedance	$R_{9\text{-}15}$	–	2,5	–	kΩ
Signal purity					
Total harmonic distortion	THD	–	–15	–	dBC
Spurious frequencies					
at EMF1 = 0,2 V; R_{S1} = 50 Ω	f_S	–	–35	–	dBC
Electronic standby switch (pin 11)					
Oscillator; linear i.f. amplifier; a.g.c.					
at T_{amb} = –40 to + 85 °C					
Input switching voltage					
for threshold ON; $V_{18\text{-}4} = \geqslant V_P-3$ V	$V_{11\text{-}4}$	0	–	2,3	V
for threshold OFF; $V_{18\text{-}4} = \leqslant 0,5$ V	$V_{11\text{-}4}$	3,3	–	23	V
Input current					
at ON condition; $V_{11\text{-}4}$ = 0 V	$-I_{11}$	–	–	150	µA
at OFF condition; $V_{11\text{-}4}$ = 23 V	I_{11}	–	–	10	µA
Input voltage					
at $I_{11} = \phi$	$V_{11\text{-}4}$	–	–	4,4	V

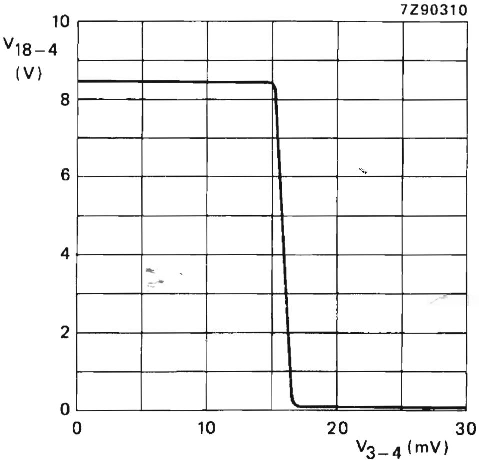


Fig. 2 Keyed a.g.c. output voltage $V_{18\text{-}4}$ as a function of r.m.s. input voltage $V_{3\text{-}4}$. Measured in test circuit Fig. 1 at $V_{12\text{-}4} = 0{,}7$ V; $I_{18} = \phi$.

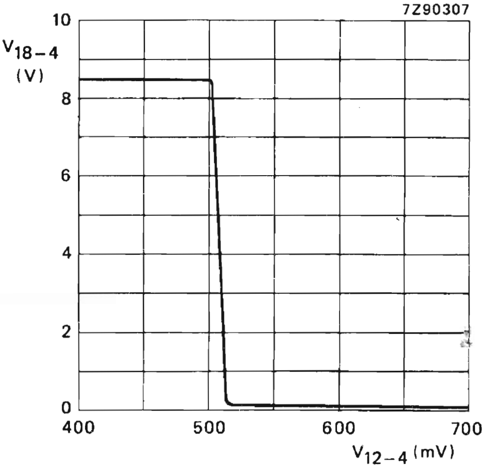


Fig. 3 Keyed a.g.c. output voltage $V_{18\text{-}4}$ as a function of input voltage $V_{12\text{-}4}$. Measured in test circuit Fig. 1 at $V_{3\text{-}4} = 2$ V; $I_{18} = \phi$.

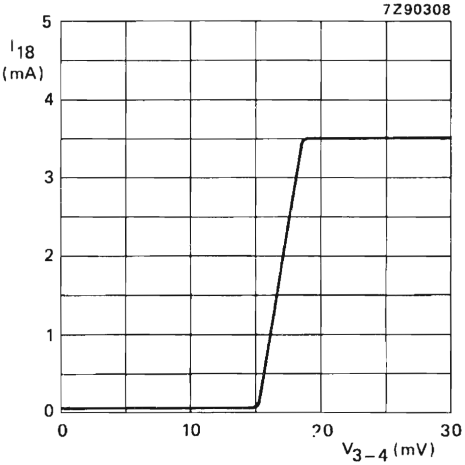


Fig. 4 Keyed a.g.c. output current I_{18} as a function of r.m.s. input voltage $V_{3\text{-}4}$. Measured in test circuit Fig. 1 at $V_{12\text{-}4} = 0{,}7$ V; $V_{18\text{-}4} = 8{,}5$ V.

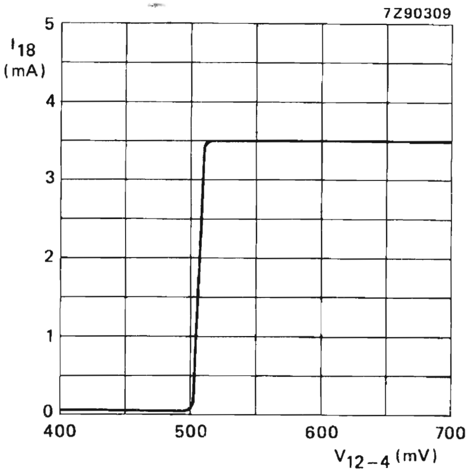
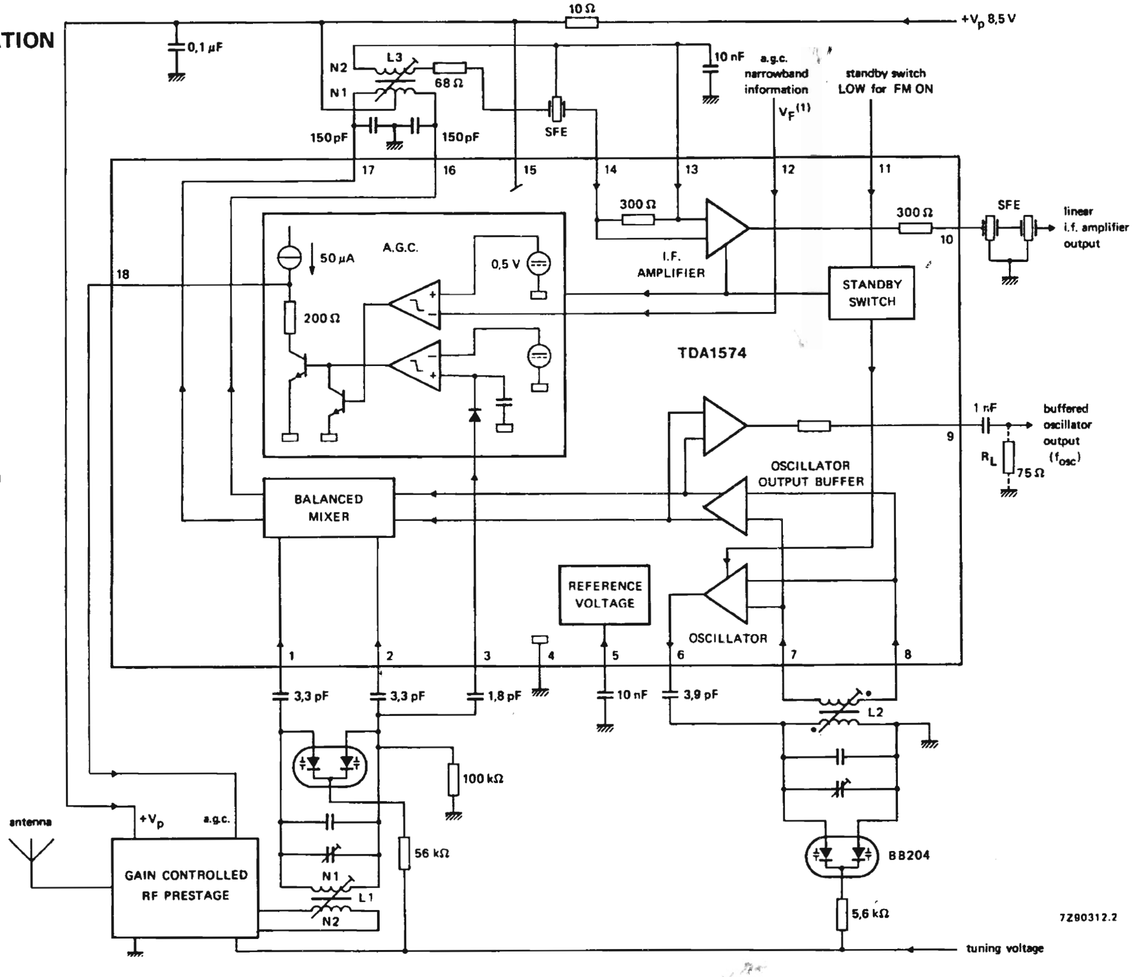


Fig. 5 Keyed a.g.c. output current I_{18} as a function of input voltage $V_{12\text{-}4}$. Measured in test circuit Fig. 1 at $V_{3\text{-}4} = 2$ V; $V_{18\text{-}4} = 8{,}5$ V.

APPLICATION INFORMATION



Coil data

L1: TOKO MC-108,
514HNE-15023S15,
N1 = 5,5 turns, N2 = 1 turn

L2:
L3: see Fig. 1

(1) Field strength indication of main i.f. amplifier.

Integrated FM tuner for radio receivers TDA1574T

GENERAL DESCRIPTION

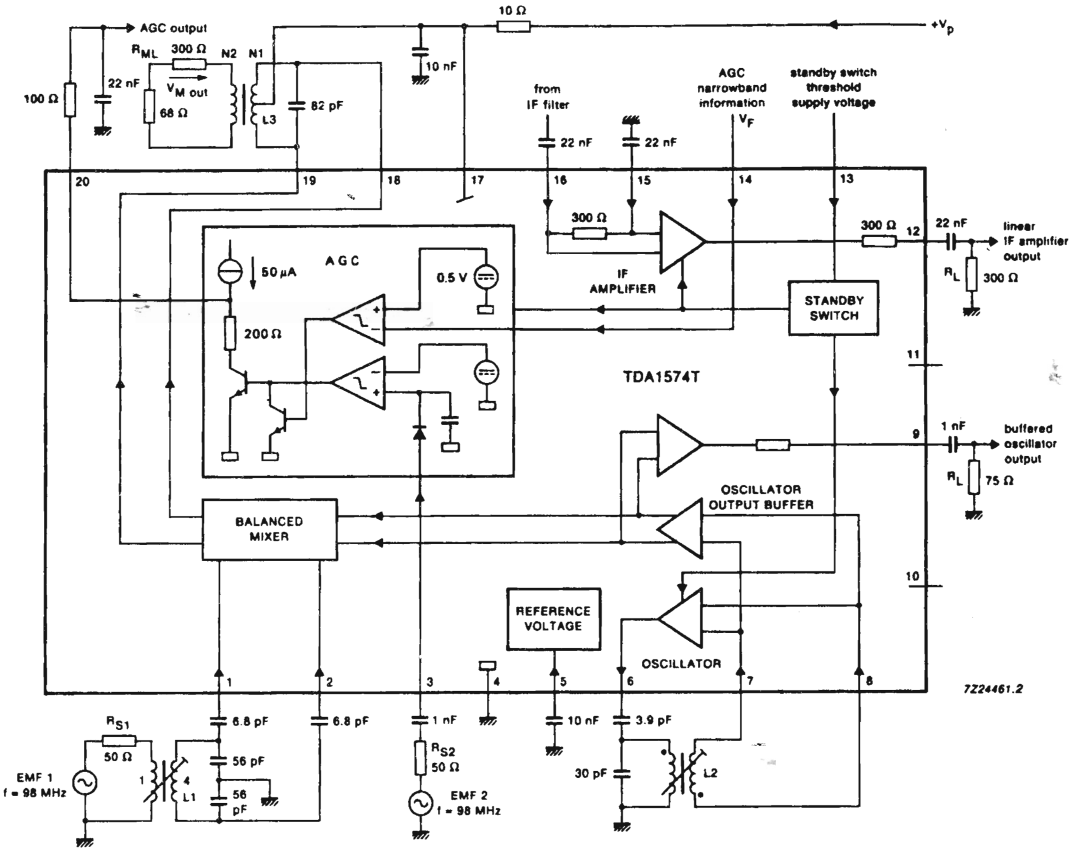
The TDA1574T is an integrated FM tuner circuit designed for use in the RF/IF section of car radios and home-receivers. The circuit contains a mixer and an oscillator and a linear IF amplifier for signal processing. The circuit also incorporates the following features.

Features

- Keyed Automatic Gain Control (AGC)
- Regulated reference voltage
- Buffered oscillator output
- Electronic standby switch
- Internal buffered mixer driving

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range (pin 17)		V_P	7	–	14	V
Mixer input bias voltage (pins 1 and 2)		$V_{1,2\text{-}4}$	–	1	–	V
Noise factor		NF	–	9	–	dB
Oscillator output voltage (pin 6)		$V_{6\text{-}4}$	–	2	–	V
Output admittance at pin 6	f = 108.7 MHz	Y22	–	1.5 + j2		ms
Oscillator output buffer DC output voltage (pin 9)		$V_{9\text{-}4}$	–	6	–	V
Total harmonic distortion		THD	–	–15	–	dB
Linear IF amplifier output voltage (pin 12)		$V_{12\text{-}4}$	–	4.5	–	V
Noise factor	R_S = 300 Ω	NF	–	6.5	–	dB
Keyed AGC output voltage range (pin 20)		$V_{20\text{-}4}$	0.5	–	V_P–0.3	V



Coil data

L1: TOKO MC-108, 514HNE-150023S14; L = 0.078 μH

L2: TOKO MC-111, E516HNS-200057; L = 0.08 μH

L3: TOKO Coil set 7P, N1 = 5.5 + 5.5 turns, N2 = 4 turns

Fig.1 Block diagram and test circuit.

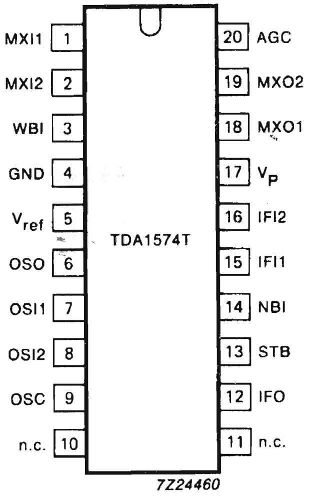


Fig.2 Pinning diagram.

PINNING

1. Mixer input 1
2. Mixer input 2
3. Wideband information input
4. Ground
5. Voltage reference
6. Oscillator output
7. Oscillator input 1
8. Oscillator input 2
9. Buffered oscillator output
10. Not connected
11. Not connected
12. IF output
13. Standby switch
14. Narrowband information input
15. IF input 1
16. IF input 2
17. Supply voltage
18. Mixer output 1
19. Mixer output 2
20. AGC output

FUNCTIONAL DESCRIPTION

Mixer

The mixer circuit uses a double balanced multiplier with a preamplifier (common base input) in order to obtain a large signal handling range and low oscillator radiation.

Oscillator

The oscillator circuit uses an amplifier with a differential input. Voltage regulation is achieved by utilizing the symmetrical tan h-transfer-function to obtain low order 2nd harmonics.

Linear IF amplifier

The IF amplifier is a one stage, differential input, wideband amplifier with an output buffer.

Keyed AGC

The AGC processor combines narrow and wideband information via an RF level detector, a comparator and an ANDing stage. The level dependent current sinking output has an active load which sets the AGC threshold.

The AGC function can either be controlled by a combination of wideband and narrowband information (keyed AGC) or by a wideband/narrowband information only. If narrowband AGC is required pin 3 should be connected to pin 5. If wideband AGC is required pin 14 should be connected to pin 15.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 17)		$V_{17\text{-}4}$	–	14	V
Mixer output voltage (pins 18 and 19)		$V_{18,19\text{-}4}$	–	35	V
Standby switch input voltage (pin 13)		$V_{13\text{-}4}$	–	23	V
Reference voltage (pin 5)		$V_{5\text{-}4}$	–	7	V
Total power dissipation		P_{tot}	–	500	mW
Storage temperature range		T_{stg}	–55	+ 150	°C
Operating ambient temperature range		T_{amb}	–40	+ 85	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\,j\text{-}a}$ = 95 K/W

CHARACTERISTICS

$V_P = V_{17\text{-}4} = 8.5$ V; $T_{amb} = 25\ ^oC$; measured in test circuit Fig.1;
All measurements are with respect to ground (pin 4); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply (pin 17)						
Supply voltage	$V_P = V_{17}$	V_{17}	7	–	14	V
Supply current (except mixer)	$I_P = I_{17}$	I_{17}	16	23	30	mA
Reference voltage (pin 5)		V_5	4.0	4.2	4.4	V
Mixer						
DC characteristics						
Input bias voltage (pins 1 and 2)		$V_{1,2}$	–	1	–	V
Output voltage (pins 18 and 19)		$V_{18,19}$	4	–	35	V
Output current (pins 18 and 19)		I_{18+19}	–	4.5	–	mA
AC characteristics	$f_i = 98$ MHz					
Noise figure		NF	–	9	–	dB
Noise figure including transforming network		NF	–	11	–	dB
3rd order intercept point		$EMF1_{IP3}$	–	115	–	dB/μV
Conversion power gain	note 1	G_{CP}	–	14	–	dB
Input resistance (pins 1 and 2)		$R_{1,2}$	–	14	–	Ω
Output capacitance (pins 18 and 19)		$C_{18,19}$	–	13	–	pF
Oscillator						
DC characteristics						
Input voltage (pins 7 and 8)		$V_{7,8}$	–	1.3	–	V
Output voltage (pin 6)		V_6	–	2	–	V
AC characteristics						
Residual FM (bandwidth = 300 Hz to 15 kHz)	de-emphasis = 50 μs	Δf	–	2.2	–	Hz
Linear IF amplifier						
DC characteristics						
Input bias voltage (pin 15)		V_{15}	–	1.2	–	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output voltage (pin 12)		V_{12}	–	4.5	–	V
AC characteristics	f_i = 10.7 MHz					
Input impedance		$R_{16\text{-}15}$ $C_{16\text{-}15}$	240 –	300 13	360 –	Ω pF
Output impedance		R_{12} C_{12}	240 –	300 3	360 –	Ω pF
Voltage gain	note 2	G_v	27	30	–	dB
Voltage gain with variation of temperature	T_{amb} = –40 to + 85 °C	ΔG_T	–	0	–	dB
1 dB compression point (RMS value)						
at V_P = 8.5 V		$V_{12(rms)}$	–	750	–	mV
at V_P = 7.5 V		$V_{12(rms)}$	–	550	–	mV
Signal-to-noise ratio	R_S = 300 Ω	S/N	–	6.5	–	dB
Keyed AGC						
DC characteristics						
Output voltage range (pin 20)		ΔV_{20}	0.5	–	V_P–0.3	V
AGC output current						
at I_3 = 0 or V_{14} = 450 mV; V_{20} = $V_P/2$		$-I_{20}$	25	50	100	µA
at V_3 = 2 V and V_{14} = 1 V; V_{20} = V_{15}		I_{20}	2	–	5	mA
Narrowband threshold						
at V_3 = 2 V; V_{14} = 550 mV		V_{20}	–	–	1	V
at V_3 = 2 V; V_{14} = 450 mV		V_{20}	V_P–0.3	–	–	V
AC characteristics	f_i = 98 MHz					
Input impedance		R_3 C_3	– –	4 3	– –	kΩ pF

parameter	conditions	symbol	min.	typ.	max.	unit
Wideband threshold (RMS value) (see Figs 3, 4, 5 and 6) at $V_{14} = 0.7$ V; $V_{20} = V_P/2$; $I_{20} = 0$		$EMF_{2(rms)}$	–	17	–	mV
Oscillator output buffer (pin 9)						
DC output voltage		V_9	–	6	–	V
Oscillator output voltage (RMS value)						
at R_L = oo; C_L = 2 pF		$V_{9(rms)}$	–	110	–	mV
at $R_L = 75\ \Omega$		$V_{9(rms)}$	30	50	–	mV
DC output resistance		$R_{9\text{-}17}$	–	2.5	–	kΩ
Signal purity						
Total harmonic distortion		THD	–	–15	–	dB
Spurious frequencies at EMF1 = 1 V; $R_{S1} = 50\ \Omega$		f_S	–	–35	–	dB
Electronic standby switch (pin 11)						
Oscillator; linear IF amplifier; AGC	T_{amb} = –40 to + 85 °C					
Input switching voltage						
for threshold ON	$V_{20} = > V_P{-}3$ V	V_{13}	0	–	2.3	V
for threshold OFF	$V_{20} = < 0.5$ V	V_{13}	3.3	–	23	V
Input current						
at ON condition	$V_{13} = 0$ V	$-I_{13}$	–	–	150	μA
at OFF condition	$V_{13} = 23$ V	$-I_{13}$	–	–	10	μA
Input voltage	$I_{13} = 0$	V_{13}	–	–	4.4	V

Notes to the characteristics

1. Power gain conversion is equated by the following equation:

$$10 \log \frac{4\,(V_{M(out)}\ 10.7\ \text{MHz})^2}{(\text{EMF1}\ 98\ \text{MHz})^2} \times \frac{R_{S1}}{R_{ML}}$$

2. Voltage gain is equated by the following equation:

$$20 \log \frac{V_{12}}{V_{16\text{-}15}}$$

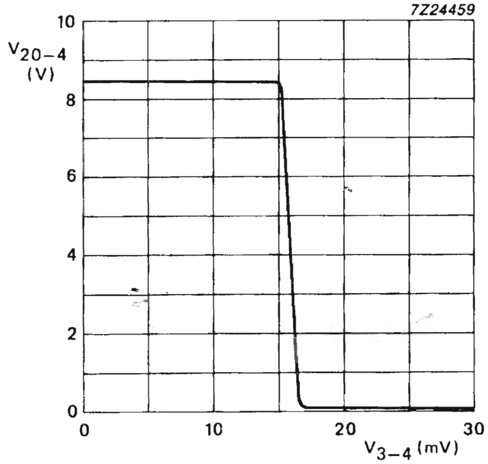


Fig.3 Keyed AGC output voltage V_{20} as a function of RMS input voltage V_3. Measured in test circuit Fig.1 at V_{14} = 0.7 V; I_{20} = 0.

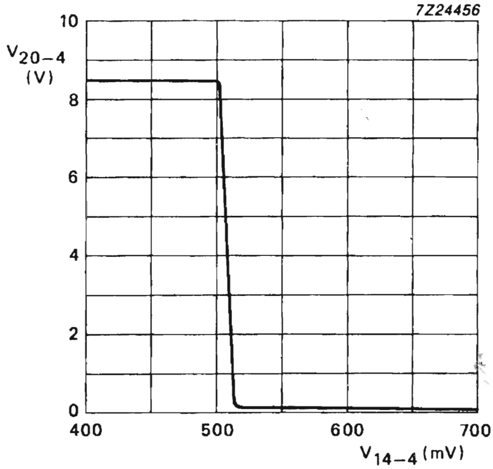


Fig.4 Keyed AGC output voltage V_{20} as a function of input voltage V_{14}. Measured in test circuit Fig.1 at V_3 = 2 V; I_{20} = 0.

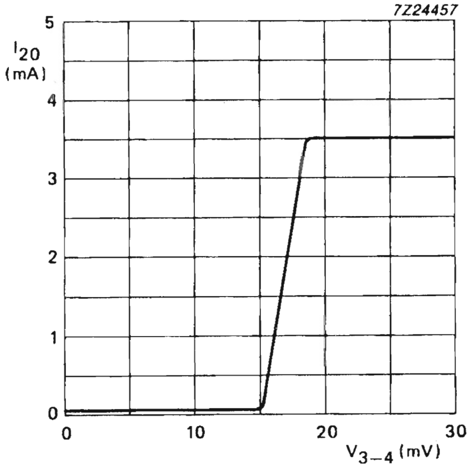


Fig.5 Keyed AGC output current I_{20} as a function of RMS input voltage V_3. Measured in test circuit Fig.1 at V_{14} = 0.7 V; V_{20} = 8.5 V.

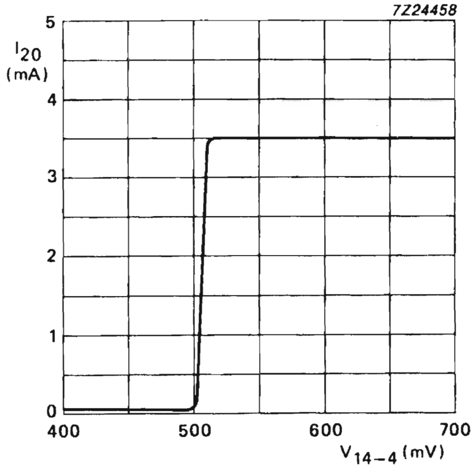
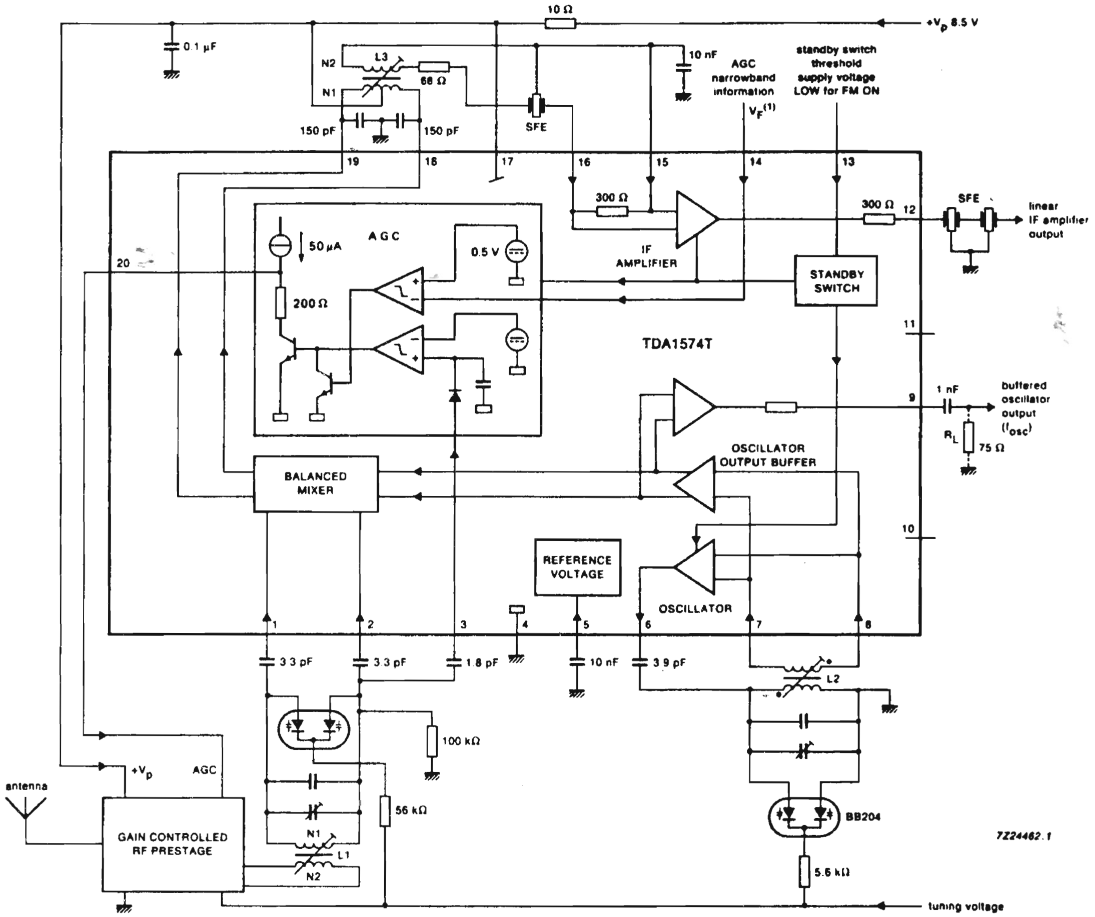


Fig.6 Keyed AGC output voltage I_{20} as a function of input voltage V_{14}. Measured in test circuit Fig.1 at V_3 = 2 V; V_{20} = 8.5 V.



Coil data

L1: TOKO MC-108, N1 = 5.5 turns, N2 = 1 turn

L2:
L3: } see Fig.1

(1) Field strength indication of main IF amplifier.

Fig.7 TDA1574T application diagram.

TV VHF mixer/oscillator UHF preamplifier TDA5030A

GENERAL DESCRIPTION

The TDA5030A provides VHF local oscillator, VHF mixer and UHF IF preamplifier functions for VHF/UHF television receivers. It includes a buffered output from the VHF local oscillator, a VHF/UHF switching circuit and an IF amplifier stage for an external SAW filter.

Features

- Balanced VHF mixer
- Voltage-controlled VHF local oscillator
- IF amplifier for SAW filter
- UHF IF preamplifier
- Local oscillator buffer output for external prescaler
- Voltage stabilizer
- UHF/VHF switching circuit
- Electrostatic discharge protection diodes at pins 10, 11, 12 and 13

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	pin 15	V_P	10	–	13,2	V
Supply current		I_P	–	42	–	mA
VHF mixer frequency range		f	50	–	470	MHz
Conversion gain			–	24,5	–	dB
Conversion noise	300 MHz		–	10	–	dB
Input signal for 1% cross modulation			–	99	–	dBμV
Storage temperature range		T_{stg}	–55	–	+ 125	°C
Operating ambient temperature range		T_{amb}	–25	–	+ 85	°C

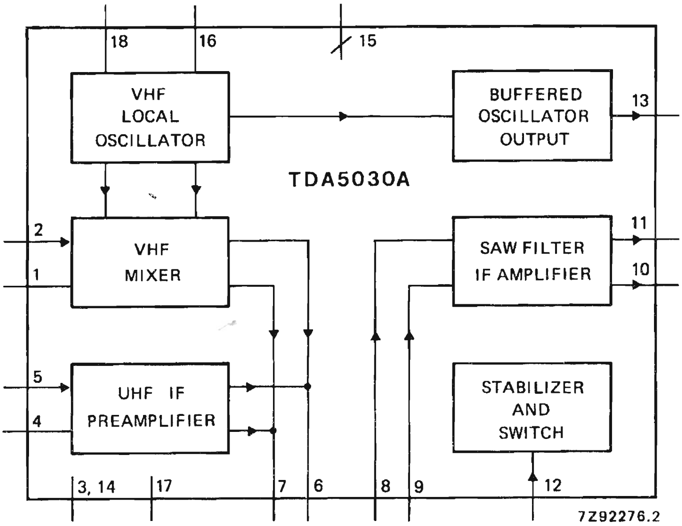


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 15	$V_P = V_{15\text{-}3}$	–	14	V
Input voltage	pins 1, 2, 4 and 5	V_i	0	5	V
VHF switching voltage	pin 12	V_{12}	0	V_{15}+ 0,3	V
Output current	pins 10, 11 or 13	$-I_{10,11,13}$	–	10	mA
Short-circuit time on outputs	pins 10 and 11	t_{ss}	–	10	s
Storage temperature range		T_{stg}	–55	+ 125	°C
Operating ambient temperature range		T_{amb}	–25	+ 85	°C
Junction temperature range		T_j	–	+ 125	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\,j\text{-}a}$ 55 K/W

CHARACTERISTICS

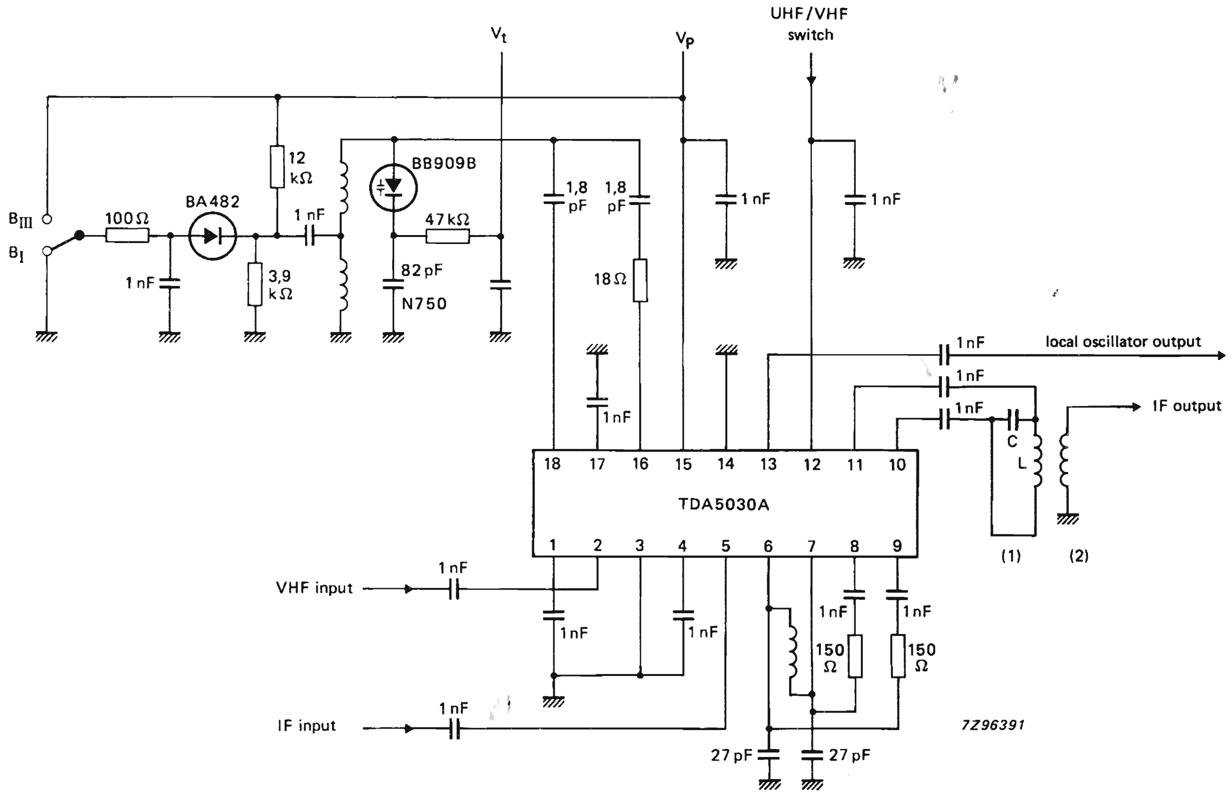
Measured in circuit of Fig. 2, $V_P = V_{15\text{-}3} = 12$ V, $T_{amb} = 25$ °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	pin 15	$V_{15\text{-}3}$	10	–	13,2	V
Supply current		I_{15}	–	42	55	mA
Switch voltage level for VHF	pin 12	V_{12}	0	–	2,5	V
Switch voltage level for UHF	pin 12	V_{12}	9,5	–	V_{15}+0,3	V
Switch current	UHF selected	I_{12}	–	–	0,7	mA
VHF mixer (including IF amplifier)						
Frequency range		f	50	–	470	MHz
Noise factor	pin 2					
	f = 50 MHz	F	–	7,5	9	dB
	f = 225 MHz	F	–	9	10	dB
	f = 300 MHz	F	–	10	12	dB
	f = 470 MHz	F	–	11	13	dB
Optimum source conductance	pin 2					
	f = 50 MHz	G	–	0,5	–	mS
	f = 225 MHz	G	–	1,1	–	mS
	f = 300 MHz	G	–	1,2	–	mS
Input conductance	pin 2					
	f = 50 MHz	G_i	–	0,23	–	mS
	f = 225 MHz	G_i	–	0,5	–	mS
	f = 300 MHz	G_i	–	0,67	–	mS
Input capacitance	pin 2					
	f = 50 MHz	C_i	–	2,5	–	pF
Input voltage for 1% cross-modulation (in channel)		$V_{2\text{-}3}$	97	99	–	dBμV
Input voltage for 10 kHz pulling (in channel)	f < 300 MHz	$V_{2\text{-}14}$	100	–	–	dBμV
Voltage gain		A_V	22,5	24,5	26,5	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
UHF preamplifier (including IF amplifier)						
Input conductance	pin 5	G_i	–	0,3	–	mS
Input capacitance	pin 5	C_i	–	3,0	–	pF
Noise factor	pin 5	F	–	5	6	dB
Optimum source conductance	pin 5	G	–	3,3	–	mS
Input voltage for 1% cross-modulation (in channel)		$V_{5\text{-}14}$	88	90	–	dBμV
Voltage gain		A_v	31,5	33,5	35,5	dB
VHF mixer						
Conversion transadmittance	pins 2 to 6,7	$Y_{c2\text{-}6,7}$	–	5,7	–	mS
Output impedance	pins 6 and 7	Z_o	–	1,6	–	kΩ
VHF oscillator						
Frequency range		f	70	–	520	MHz
Frequency shift	ΔV_P = 10%; f = 70–330 MHz	Δf	–	–	200	kHz
Frequency drift	ΔT = 15 K; f = 70–330 MHz	Δf	–	–	250	kHz
Frequency drift	between 5 s and 15 min after switch-on	Δf	–	–	200	kHz
SAW filter IF amplifier						
Input impedance	$Z_{10,11}$ = 2 kΩ; f = 36 MHz	$Z_{8,9}$	–	300+ j100	–	Ω
Transimpedance		$Z_{8,9\text{-}10,11}$	–	2,2	–	kΩ
Output reflection coefficient:	f = 36 MHz					
modulus			0,45	0,37	0,41	
phase			−63	−112	−134	deg

parameter	conditions	symbol	min.	typ.	max.	unit
VHF local oscillator output buffer						
Output voltage	pin 13 R_L = 75 Ω f < 100 MHz	V_{13}	14	20	–	mV
	f > 100 MHz	V_{13}	10	20	–	mV
Output impedance	f = 100 MHz	Z_{13}	–	90	–	Ω
RF signal on-local oscillator output	R_L = 75 Ω V_i = 1 V; f ⩽ 225 MHz	RF/(RF+LO)	–	–	10	dB
	V_i = 0,3 V; f = 225–300 MHz	RF/(RF+LO)	–	–	10	dB
IF signal on local oscillator output	UHF selected; R_L = 75 Ω; V_i = 350 mV	IF/(IF+LO)	–	–	3	mV
Local oscillator harmonics w.r.t. local oscillator output signal	R_L = 75 Ω		–	–	–14	dB



(1) C = 18 pF, L = 2,2 μH, f_{CL} = 36,5 MHz.

(2) Turns ratio = 7 : 1, load = 50 Ω.

Fig. 2 Test circuit.

Image rejecting front-end for GSM applications UAA2072M

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for up to 60 dB on-chip image rejection
- Programmable IF I/Q combiner
- On-chip programmable quadrature network
- Very fast 3-wire control bus
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast ON/OFF power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 900 MHz front-end for GSM hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers.

GENERAL DESCRIPTION

UAA2072M contains both a receiver front-end and a high frequency transmit mixer intended to be used in the GSM (Global System for Mobile communications) cellular telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2072M is its ability to provide at least 30 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed and the duplexer design is eased, compared with a conventional front-end design.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO − IF frequency can form the IF signal. An internal switch allows the use of infradyne or supradyne reception. The precision needed for this signal processing is achieved by compensating for process spreads and trimming for the choosen IF frequency and the LO band centre frequency via a 3-wire serial bus interface.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection. The overall phase rotation is programmable for maximum image rejection at a given IF. The IF output drivers have differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers. The centre frequency of the phase shifter is adjustable for maximum image rejection in a given band. The all-pass filters outputs are buffered before being fed to the receive mixers.

The transmit section consists of a down-conversion mixer and a transmit IF driver stage. In the transmit mode an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced, and 200 Ω is used as standard RF impedance.

A 3-pin unidirectional serial interface is used to program the circuits, using 16-bit words. This data bus allows compensation of process spreads, and is used to adjust for maximum image rejection performance at a given IF.
It also offers a selection to reject the upper or lower image frequency and control over the different power-down modes. Special care has been taken for fast power-up switching.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	4.5	4.8	5.3	V
I_{CCRX}	receive supply current	26	31.5	38	mA
I_{CCTX}	transmit supply current	10	12	14	mA
I_{CCPD}	supply current in power-down	–	–	50	µA
T_{amb}	operating ambient temperature	−30	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2072M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

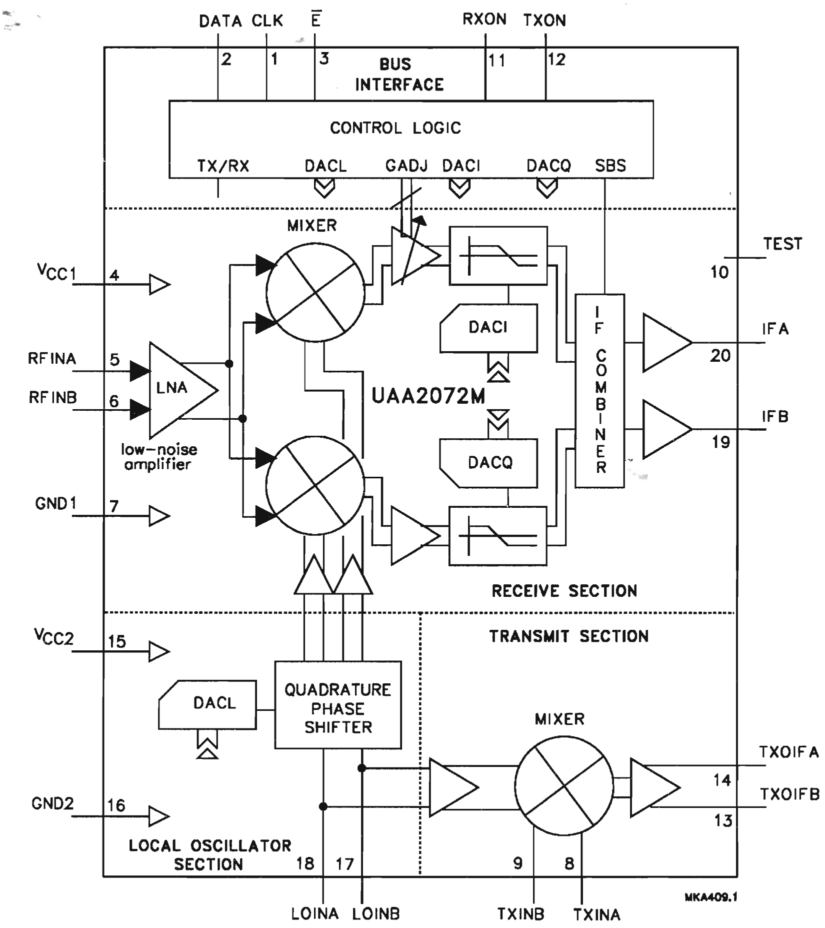


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	serial bus clock
DATA	2	serial bus data
$\overline{E}$	3	serial bus enable (active LOW)
V_{CC1}	4	supply voltage for LNA, IF parts and TX mixer
RFINA	5	RF balance input A
RFINB	6	RF balance input B
GND1	7	ground for synthesizer buffer and logic
TXINA	8	transmit mixer input A (balanced)
TXINB	9	transmit mixer input B (balanced)
TEST	10	reserved for test purposes, should be connected to ground
RXON	11	hardware power-on for receive parts
TXON	12	hardware power-on for transmit mixer
TXOIFB	13	transmit mixer IF output B (balanced)
TXOIFA	14	transmit mixer IF output A (balanced)
V_{CC2}	15	supply voltage for local oscillator parts
GND2	16	ground for LO parts
LOINB	17	LO input B (balanced)
LOINA	18	LO input A (balanced)
IFB	19	IF output (balanced)
IFA	20	IF output (balanced)

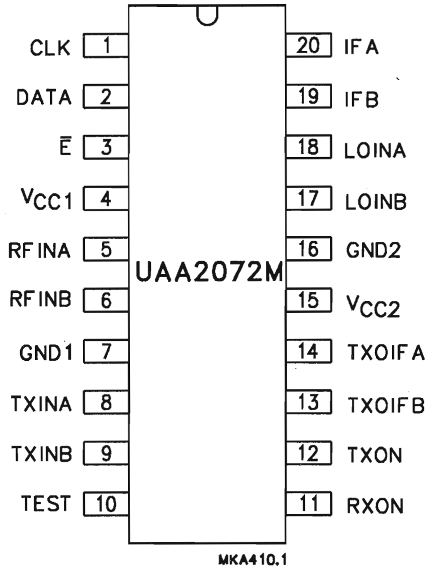


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type, the whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

The serial bus interface is used for tuning to maximum image rejection at a given IF. The contents of registers ip5 to ip0 and qp5 to qp0 (named IF phase adjustment words) are digital-to-analog converted in the DACI and DACQ blocks. The obtained internal voltages control the phase shift in I and Q; thus allowing them to be trimmed precisely to 45° and 135° at any given IF between 30 and 90 MHz. The gain in the I channel is slightly adjustable using the four bits ga3 to ga0 to allow compensation of small gain mismatches between I and Q.

One bit (sbs) allows selection between infradyne or supradyne reception.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics. The RF impedance level is 200 Ω, choosen to minimize current consumption at best noise performance.

The IF output is differential and of the open-collector type. Typical application will load the output with a differential 1 kΩ load; i.e. a 1 kΩ resistor load at each IF output, plus a 2 kΩ resistor to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The path to V_{CC} for the DC current is achieved via tuning inductors. The output voltage is limited to $V_{CC} + 3V_{be}$ or 3 diode forward voltage drops.

In the event of only one output being used, a 1 kΩ resistive load in parallel with a tuning inductor to V_{CC}, provides a matched 1 kΩ output to the external IF filter.

Fast switching, ON/OFF, of the receive section is controlled by the hardware input RXON or via the bus interface by changing the srx-bit in the internal register.

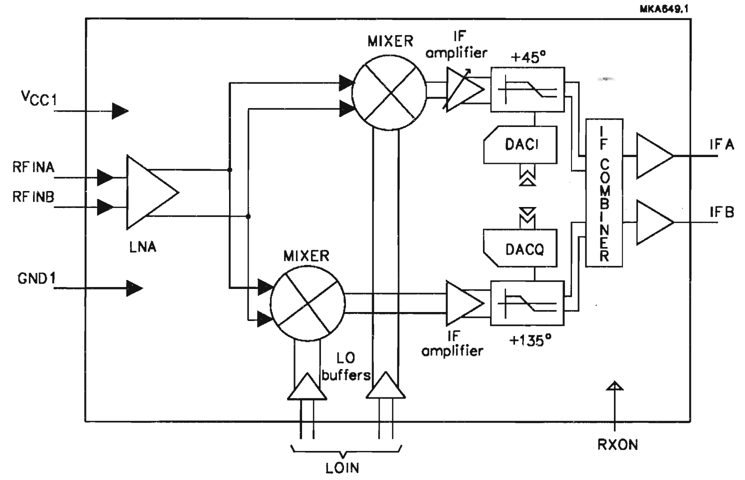


Fig.3 Block diagram, receive section.

Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The centre frequency of the receive band is adjustable by programming via the serial bus. The word 'lo5 to lo0' named LO Quad Centre Frequency Adjustment word is converted to an analog voltage in a digital-to-analog converter (DACL, see Fig.4). This voltage trims the all-pass network to the selected LO frequency range. To obtain the 30 dB specified image rejection the precision required on this trimming remains low.

The LO input impedance is 100 Ω differential. Switching from RX to TX or power-down mode has little influence on the LO input impedance.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF and down-convert it to a modulated transmit IF frequency which is phase locked with the baseband modulation.

The transmit mixer provides a differential input at 200 Ω and a differential output driver buffer for a 1 kΩ load. The IF outputs are low impedance (common collector type).

Fast switching, ON/OFF, of the transmit section is controlled by the hardware input TXON or via the serial bus interface by changing the stx-bit in the internal register.

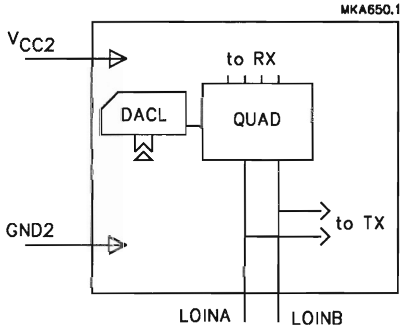


Fig.4 Block diagram, LO section.

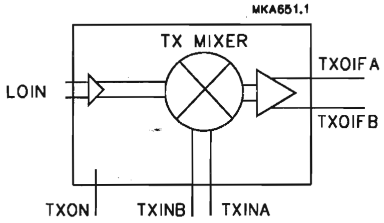


Fig.5 Block diagram, transmit mixer.

Serial bus interface

The 3-wire serial bus interface allows control over the selective power-up of the transmit, receive and LO buffer circuits, the tuning of the LO quadrature and IF quadrature circuits and the selection of sideband rejection. The interface consists of a 16-bit programming register, three working latches and three DACs which provide the tuning voltages for the image rejection of the receive quadrature circuits.

BUS FORMAT

A 3-wire unidirectional bus is used to program the circuit, the 3 wires being: DATA, CLOCK (CLK) AND ENABLE ($\overline{E}$). The timing diagram is illustrated in Fig.4. The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their corresponding data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed working latch when $\overline{E}$ returns HIGH.
Only the last 16 bits clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. If $\overline{E}$ returns HIGH while CLK is still LOW, the extra clock edge produced will cause data shift. The bus interface will not output any address recognition.

Data is entered with the most significant bit first. The leading 12 bits make up the data field, while the trailing 4 bits comprise the address. The first bit entered is p1, the last bit p16. The bits in the programming registers and addresses are arranged as shown in Table 1.

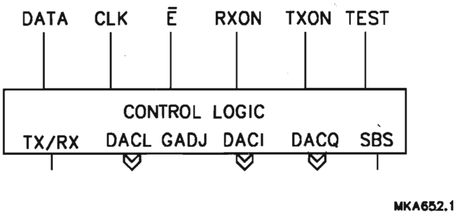


Fig.6 Block diagram, serial bus interface.

Table 1 Register bit allocation

REGISTER BIT ALLOCATION															
FIRST															**LAST**
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16
DATA FIELD												ADDRESS			
dt11	dt10	dt9	dt8	dt7	dt6	dt5	dt4	dt3	dt2	dt1	dt0	ad3	ad2	ad1	ad0
This register is reserved for test purposes and should not be programmed												0	0	0	0
X	X	X	X	sbs	X	X	X	X	hpn	srx	stx	0	0	0	1
ga3	ga2	ga1	ga0	X	X	lo5	lo4	lo3	lo2	lo1	lo0	0	0	1	0
ip5	ip4	ip3	ip2	ip1	ip0	qp5	qp4	qp3	qp2	qp1	qp0	0	0	1	1

Table 2 Bit allocation description

BIT	REMARKS	LOGIC		PRESET
stx	software transmit power-on	1 = power-up	0 = power-down	0
srx	software receive power-on	1 = power-up	0 = power-down	0
hpn	hardware priority not (selects if power status of blocks is controlled via hardware or software)	1 = soft priority	0 = hard priority	0
sbs	sideband select	1 = upper sideband selected	0 = lower sideband selected	0
ga3 to ga0	IF I channel gain adjustment			0111
lo5 to lo0	LO quadrature centre frequency adjustment			011111
ip5 to ip0	IF I channel phase adjustment			011111
qp5 to qp0	IF Q channel phase adjustment			011111
X	not used			

Table 3 details the different power-up modes of the circuit. Attention should be paid to the hpn-bit. This bit enables the RXON and TXON pins to take any logic position when software programming for power-up is used.

Table 3 Control of power status (note 1)

REGISTER BIT STATUS			EXTERNAL PIN LEVEL		CIRCUITS POWER STATUS	
hpn	**stx**	**srx**	**TXON**	**RXON**	**TRANSMIT**	**RECEIVE**
0	X	X	LOW	LOW	off	off
0	X	X	LOW	HIGH	off	on
0	X	X	HIGH	LOW	on	off
0	X	X	HIGH	HIGH	on (2)	on(2)
1	0	0	x	x	off	off
1	0	1	x	x	off	on
1	1	0	x	x	on	off
1	1	1	x	x	on(2)	on(2)

Notes

1. X = don't care; x = HIGH or LOW logic voltage level applied at designated pin.
2. Circuit is operative in this mode but specification is NOT guaranteed.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	v
ΔGND	difference in ground supply voltage applied between GND1 and GND2	–	0.6	V
$P_{I(max)}$	maximum power input	–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
$P_{dis(max)}$	maximum power dissipation in quiet air	–	250	mW
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2 (method 3015.5).

DC CHARACTERISTICS

V_{CC} = 4.8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: V_{CC1}, V_{CC2}, LOINA and LOINB						
V_{CC}	supply voltage	over full temperature range	4.5	4.8	5.3	V
I_{CCRX}	supply current	receive mode active; DC tested	26	31.5	38	mA
I_{CCTX}	supply current	transmit mode active; DC tested	10	12	14	mA
I_{CCPD}	supply current in power-down mode	DC tested	–	–	50	µA
Pins: CLK, DATA, $\overline{E}$, RXON, TXON and TEST						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		3	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} – 0.4 V	–1	–	+1	µA
I_{IL}	LOW level static input current	pin at 0.4 V	–1	–	+1	µA
Pins: RFINA and RFINB						
V_I	DC input voltage level	receive mode enabled	1.7	2.1	2.4	V
Pins: IFA and IFB						
I_O	DC output current	receive mode enabled	2.0	2.5	3.5	mA
Pins: TXINA and TXINB						
V_I	DC input voltage level	transmit section enabled	1.8	2.2	2.5	V
Pins: TXOIFA and TXOIFB						
V_O	DC output voltage level	transmit section enabled	2.5	2.9	3.4	V

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 4.8 V; T_{amb} = –30 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
Z_{RFI}	RF input impedance	balanced	–	200	–	Ω
f_{RFI}	RF input frequency		925	–	960	MHz
RL_{RF}	return loss on matched RF input impedance	note 1	15	20	–	dB
G_{CP}	conversion power gain	RF impedance to 1 IF output matched to 500 Ω	20	23	26	dB
		RF impedance to differential IF outputs matched to 1 kΩ differential	23	26	29	dB
G_{rip}	gain ripple as a function of RF frequency	note 2	–	0.1	0.5	dB
ΔG/T	gain variation with temperature	note 2	–20	–15	–10	mdB/K
$CP1_{RX}$	1 dB input compression point	note 1	–26	–24.5	–	dBm
$IP2_{RX}$	2nd order intercept point referenced to the RF input	single-ended output; note 2	+15	+22	–	dBm
$IP2D_{RX}$	2nd order intercept point referenced to the RF input differential	differential output; note 2	–	+32	–	dBm
$IP3_{RX}$	3rd order intercept point referenced to the RF input	note 2	–18	–15	–	dBm
F_{RX}	overall noise figure	RF input to differential IF output; notes 2 and 3	–	4	5	dB
$Z_{L(IF)}$	typical application IF output load impedance	unbalanced	–	500	–	Ω
$C_{L(IF)}$	IF output load capacitance	unbalanced	–	–	2	pF
f_{IF}	IF frequency range	RF < LO	30	71	90	MHz
		RF > LO	30	45	50	MHz
f_{IR}	image frequency rejection	note 4	30	–	–	dB
f_{IRp}	image rejection at preset	superheterodyne; f_{IF} = 71 MHz; note 1	30	35	–	dB
Local oscillator section (receive section enabled)						
f_{LO}	LO input frequency		875	–	1050	MHz
Z_{LO}	LO input impedance	balanced	–	100	–	Ω
RL_{LO}	return loss on matched input (including standby mode)	note 2	10	15	–	dB
$P_{i(LO)}$	LO input power level		–7	–4	+3	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 1	40	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit section (transmit section enabled)						
Z_O	TX IF output impedance		–	–	200	Ω
Z_L	TX IF load impedance		–	1 000	–	Ω
C_L	maximum TX IF load capacitance		–	–	2	pF
$Z_{i(RF)}$	TX RF input impedance	balanced	–	200	–	Ω
f_{TXmix}	TX mixer input frequency		880	–	915	MHz
RL_{TX}	return loss on matched TX input	note 2	15	20	–	dB
G_{CP}	conversion power gain	from 200 Ω to 1 kΩ output	8	10	12	dB
$f_{o(TX)}$	TX mixer output frequency		40	–	200	MHz
$CP1_{TX}$	1 dB input compression point		–20	–15	–	dBm
$IP2_{TX}$	2nd order intercept point		–	+20	–	dBm
$IP3_{TX}$	3rd order intercept point		–10	–7	–	dBm
F_{TX}	noise figure	double sideband; note 2	–	–	12	dB
RI_{TX}	reverse isolation	TXIN to LOIN; note 2	40	–	–	dB
I_{TX}	isolation	LOIN to TXIN; note 2	40	–	–	dB
Timing						
t_{stu}	start-up time of each block		1	5	20	μs

Notes

1. Measured and guaranteed only on UAA2072M demonstration board at T_{amb} = +25 °C.
2. Measured and guaranteed only on UAA2072M demonstration board.
3. This value includes printed-circuit board and balun losses.
4. This value might be dependent upon control values sent by a microcontroller via the serial bus. This performance is maintained over the RF band for a fixed phase rotation control word.

TIMING CHARACTERISTICS

Typical values measured at V_{CC} = 4.8 V; T_{amb} = 25 °C; maximum value conditions under maximum clock speed; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial bus interface					
f_{clk}	clock frequency	–	–	13	MHz
Serial programming clock (pin CLK)					
t_r	rise time	–	10	40	ns
t_f	fall time	–	10	40	ns
T_{cy}	clock period	75	–	–	ns
Enable programming (pin $\overline{E}$)					
t_{START}	delay to rising edge of clock	30	–	–	ns
t_{END}	delay from last edge of clock	10	–	–	ns
t_W	minimum inactive pulse width	75	–	–	ns
t_{NEW}	delay from $\overline{E}$ inactive to new data	150	–	–	ns
Register serial input data (pin DATA)					
t_{su}	input data to CLK set-up time	20	–	–	ns
t_h	input data to CLK hold time	20	–	–	ns

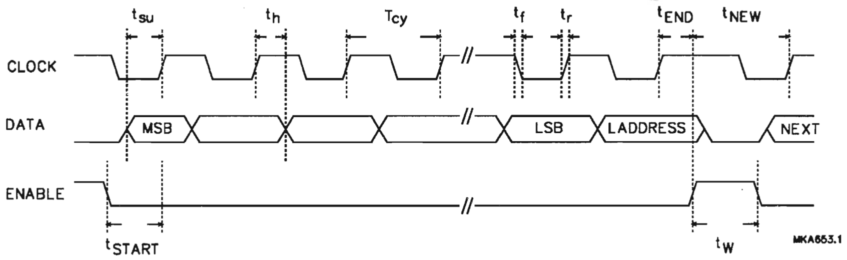


Fig.7 Serial bus timing diagram.

APPLICATION INFORMATION

Figure 8 illustrates the electrical diagram of the UAA2072M Philips demonstration board. All matching is to 50 Ω for measurement purposes. Different values will be used in a real application.

Component manufacturers

All surface mounted resistors and capacitors are manufactured by Philips Components. The small value capacitors are multi-layer ceramic with NPO dielectric.

The inductors are manufactured by Coilcraft UK.

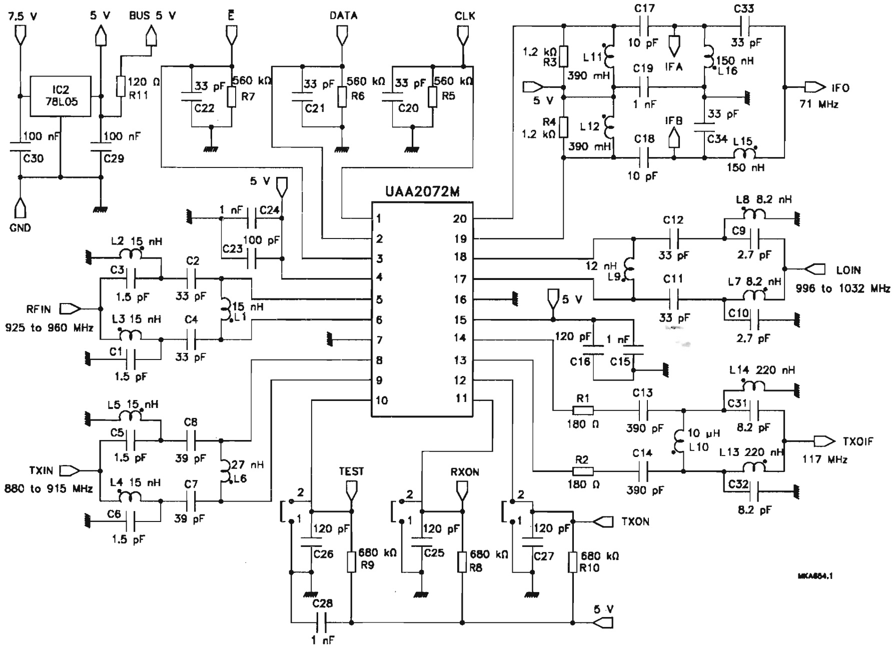


Fig.8 Application diagram.

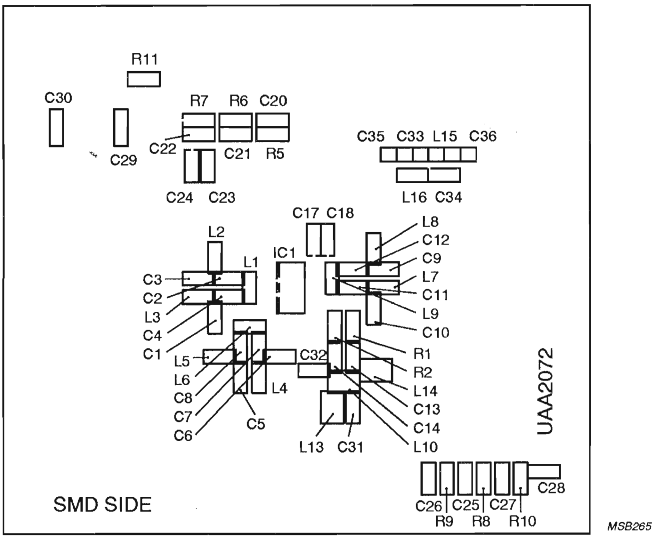


Fig.9 Printed-circuit board, SMD side.

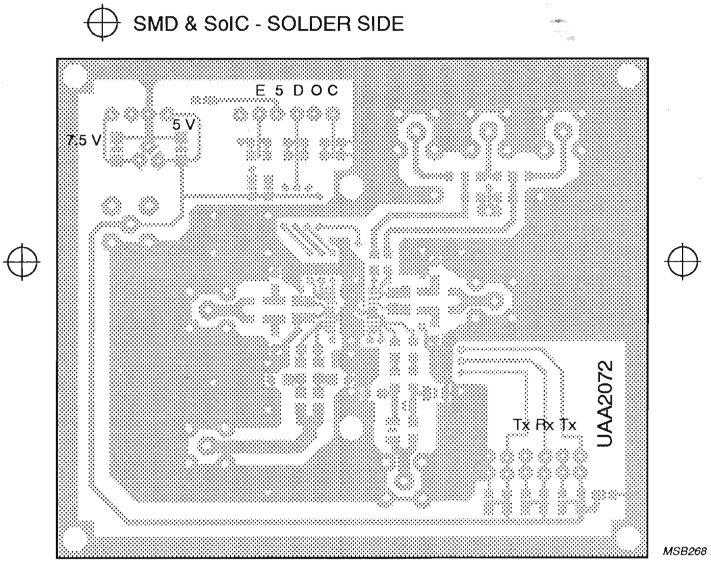


Fig.10 Printed-circuit board, SMD solder side.

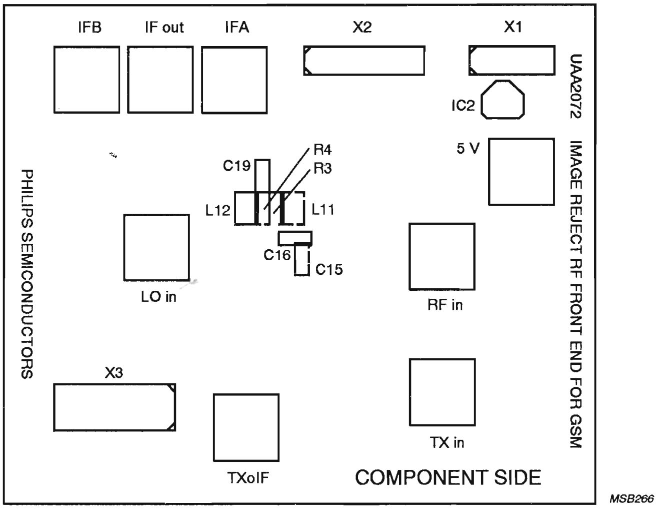


Fig.11 Printed-circuit board, component side for image reject RF front-end for GSM.

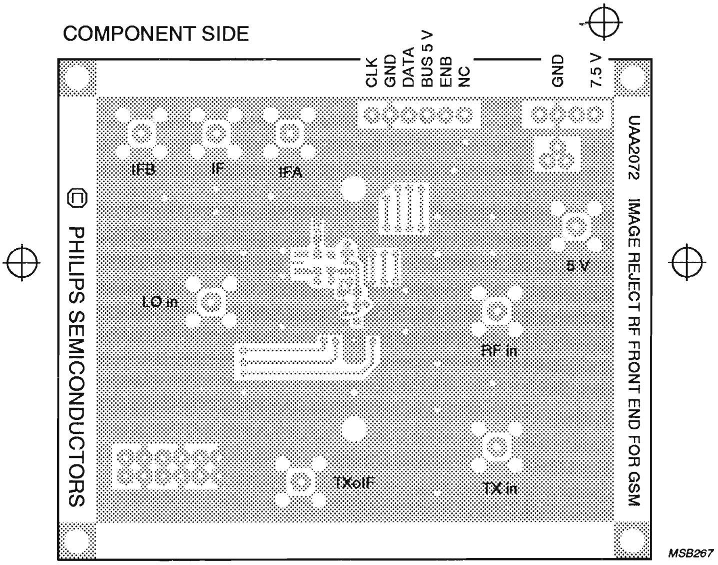


Fig.12 Printed-circuit board, component solder side for image reject RF front-end for GSM.

DEMONSTRATION BOARD - PARTS LIST

COMPONENT	VALUE	SIZE	LOCATION
Resistors			
R1	180 Ω	0805	TXOIF
R2	180 Ω	0805	TXOIF
R3	1.2 kΩ	0805	IF
R4	1.2 kΩ	0805	IF
R5	560 kΩ	0805	CLK
R6	560 kΩ	0805	DATA
R7	560 kΩ	0805	$\overline{E}$
R8	680 kΩ	0805	RXON
R9	680 kΩ	0805	TEST
R10	680 kΩ	0805	TXON
R11	120 Ω	0805	5 V BUS
Capacitors			
C1	1.5 pF	0805	RFIN
C2	33 pF	0805	RFIN
C3	1.5 pF	0805	RFIN
C4	33 pF	0805	RFIN
C5	1.5 pF	0805	TXIN
C6	1.5 pF	0805	TXIN
C7	39 pF	0805	TXIN
C8	39 pF	0805	TXIN
C9	2.7 pF	0805	LOIN
C10	2.7 pF	0805	LOIN
C11	33 pF	0805	LOIN
C12	33 pF	0805	LOIN
C13	390 pF	0805	TXOIF
C14	390 pF	0805	TXOIF
C15	1 nF	0805	V_{CC2}
C16	120 pF	0805	V_{CC2}
C17	10 pF	0805	IFO
C18	10 pF	0805	IFO
C19	1 nF	0805	IF / 5 V
C20	33 pF	0805	CLK
C21	33 pF	0805	DATA
C22	33 pF	0805	$\overline{E}$
C23	100 pF	0805	V_{CC1}
C24	1 nF	0805	V_{CC1}
C25	120 pF	0805	RXON
C26	120 pF	0805	TEST
Capacitors			
C27	120 pF	0805	TXON
C28	1 nF	0805	5 V
C29	100 nF	1206	5 V regulator
C30	100 nF	1206	5 V regulator
C31	8.2 pF	0805	TXOIF
C32	8.2 pF	0805	TXOIF
C33	33 pF	0805	IFO
C34	33 pF	0805	IFO
C35	link	0805	IF/NOT USED
C36	link	0805	IF/NOT USED
Inductors			
L1	15 nH	0805	RFIN
L2	15 nH	0805	RFIN
L3	15 nH	0805	RFIN
L4	15 nH	0805	TXIN
L5	15 nH	0805	TXIN
L6	27 nH	0805	TXIN
L7	8.2 nH	0805	LOIN
L8	8.2 nH	0805	LOIN
L9	12 nH	0805	LOIN
L10	10 µH	1008	TXOIF/OPTIONAL
L11	390 nH	1008	IFO
L12	390 nH	1008	IFO
L13	220 nH	1008	TXOIF
L14	220 nH	1008	TXOIF
L15	150 nH	0805	IFO
L16	150 nH	0805	IFO

Other components

COMPONENT	DESCRIPTIONS
IC1	UAA2072M
IC2	5 V regulator; type 78L05
SMA/RIM	sockets for RF and IF inputs/outputs
SMB	5 V socket (optional, in place of IC2)
X1, X2 and X3	various 2.54 mm (0.1 inch) connectors

Image rejecting front-end for GSM applications UAA2073M

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for at least 30 dB on-chip image rejection
- IF I/Q combination network for 50 to 90 MHz
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast ON/OFF power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 900 MHz front-end for GSM hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers.

GENERAL DESCRIPTION

UAA2073M contains both a receiver front-end and a high frequency transmit mixer intended to be used in the GSM (Global System for Mobile communications) cellular telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2073M is its ability to provide over 30 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed and the duplexer design is eased, compared with a conventional front-end design.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO – IF frequency can form the IF signal. An internal switch allows the use of infradyne or supradyne reception. Image rejection is at an optimum when the IF is 71 MHz and local oscillator is above the wanted signal.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection.The IF driver has differential outputs of open-collector type.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers. The all-pass filters outputs are buffered before been fed to the receive mixers.

The transmit section consists of a down-conversion mixer and a transmit IF driver stage. In the transmit mode an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced to reduce EMC issues.

Fast power-up switching is possible. A synthon mode enables LO buffers independent of the other circuits. When SYNTHON pin is high, all internal buffers on the LO path of the circuit are turned on, thus minimizing LO pulling when remainder of receive chain is powered-up.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	3.6	3.75	5.3	V
I_{CCRX}	receive supply current	–	26	–	mA
I_{CCTX}	transmit supply current	–	16	–	mA
I_{CCPD}	supply current in power-down	–	–	50	μA
T_{amb}	operating ambient temperature	–30	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2073M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

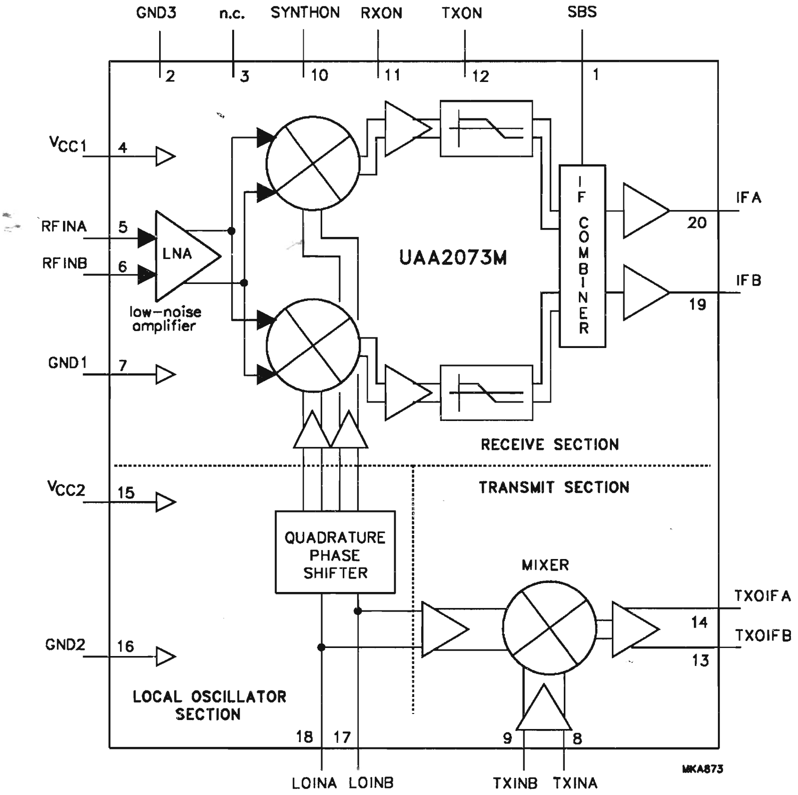


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SBS	1	sideband selection (LOW = LO > RF)
GND3	2	ground 3
n.c.	3	not connected
V_{CC1}	4	supply voltage for LNA, IF parts and TX mixer
RFINA	5	RF balance input A
RFINB	6	RF balance input B
GND1	7	ground 1 for receiver and transmitter mixer
TXINA	8	transmit mixer input A (balanced)
TXINB	9	transmit mixer input B (balanced)
SYNTHON	10	hardware power-on of internal LO buffer
RXON	11	hardware power-on for receive parts
TXON	12	hardware power-on for transmit mixer
TXOIFB	13	transmit mixer IF output B (balanced)
TXOIFA	14	transmit mixer IF output A (balanced)
V_{CC2}	15	supply voltage for LO parts
GND2	16	ground 2 for LO parts
LOINB	17	LO input B (balanced)
LOINA	18	LO input A (balanced)
IFB	19	IF output (balanced)
IFA	20	IF output (balanced)

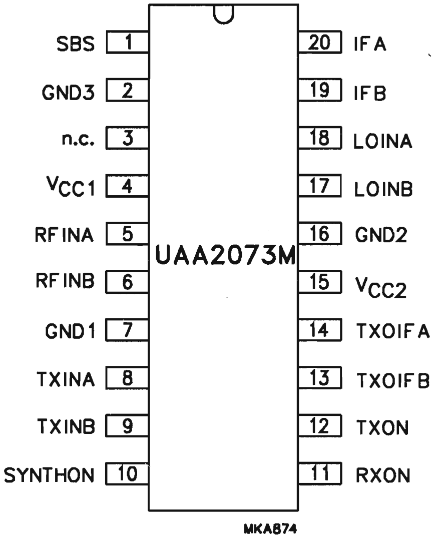


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type, the whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Pin (SBS) allows selection between infradyne or supradyne reception.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics. The RF impedance level is 150 Ω, choosen to minimize current consumption at best noise performance.

The IF output is differential and of the open-collector type, tuned for 71.3 MHz. Typical application will load the output with a differential 500 Ω load; i.e. a 500 Ω resistor load at each IF output, plus a 1 kΩ resistor to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The path to V_{CC} for the DC current is achieved via tuning inductors. The output voltage is limited to V_{CC} + $3V_{be}$ or 3 diode forward voltage drops.

In the event of only one output being used, a 1 kΩ resistive load in parallel with a tuning inductor to V_{CC}, provides a matched 1 kΩ output to the external IF filter.

Fast switching, ON/OFF, of the receive section is controlled by the hardware input RXON.

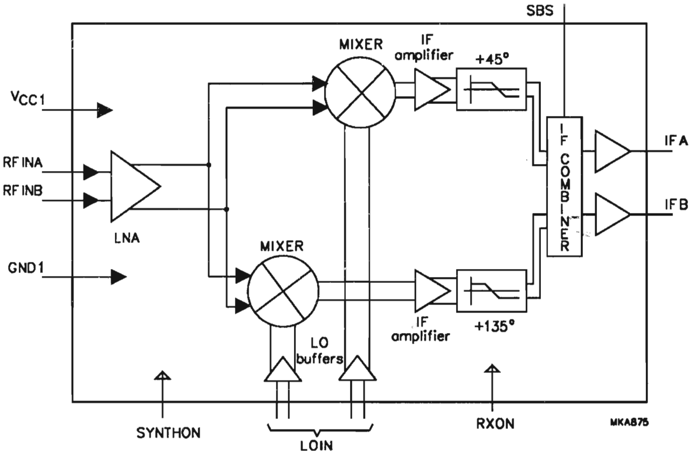


Fig.3 Block diagram, receive section.

Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The LO input impedance is 50 Ω differential.

A synthon mode is used to power-up the buffering on the LO inputs, minimizing the pulling effect on the external VCO when entering transmit or receive modes.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF and down-convert it to a modulated transmit IF frequency which is phase locked with the baseband modulation.

The transmit mixer provides a differential input at 200 Ω and a differential output driver buffer for a 1 kΩ load. The IF outputs are low impedance (common collector type).

Fast switching, ON/OFF, of the transmit section is controlled by the hardware input TXON.

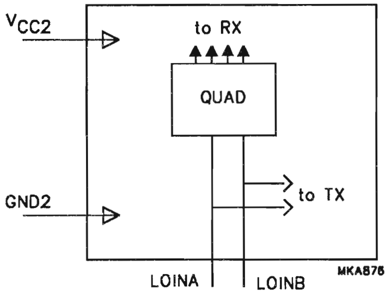


Fig.4 Block diagram, LO section.

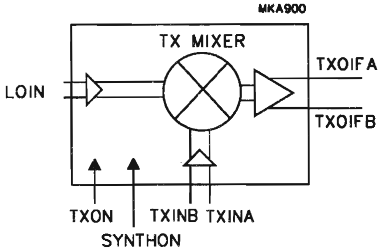


Fig.5 Block diagram, transmit mixer.

Table 1 Control of power status

EXTERNAL PIN LEVEL			CIRCUIT MODE OF OPERATION
TXON	RXON	SYNTHON	
LOW	LOW	LOW	power-down mode
LOW	HIGH	LOW	receive section on
HIGH	LOW	LOW	transmit section on
LOW	LOW	HIGH	synthon on mode, transmit and receive LO buffers enabled
LOW	HIGH	HIGH	receive section on and synthon mode active
HIGH	LOW	HIGH	transmit section on and synthon mode active
HIGH	HIGH	LOW	receive and transmit sections on
HIGH	HIGH	HIGH	receive and transmit sections on

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	V
ΔGND	difference in ground supply voltage applied between GND1 and GND2	–	0.6	V
$P_{I(max)}$	maximum power input	–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
$P_{dis(max)}$	maximum power dissipation in quiet air	–	250	mW
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2 (method 3015.5).

DC CHARACTERISTICS

V_{CC} = 3.75 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: V_{CC1}, V_{CC2}, LOINA and LOINB						
V_{CC}	supply voltage	over full temperature range	3.6	3.75	5.3	V
I_{CCRX}	supply current	receive mode active; DC tested	–	26	–	mA
I_{CCTX}	supply current	transmit mode active; DC tested	–	16	–	mA
I_{CCPD}	supply current in power-down mode	DC tested	–	–	50	μA
Pins: SYNTHON, RXON and TXON						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		3	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} – 0.4 V	–1	–	+1	μA
I_{IL}	LOW level static input current	pin at 0.4 V	–1	–	+1	μA
Pins: RFINA and RFINB						
V_I	DC input voltage level	receive mode enabled	1.7	2.1	2.4	V
Pins: IFA and IFB						
I_O	DC output current	receive mode enabled	2.0	2.5	3.5	mA
Pins: TXINA and TXINB						
V_I	DC input voltage level	transmit section enabled	1.8	2.2	2.5	V
Pins: TXOIFA and TXOIFB						
V_O	DC output voltage level	transmit section enabled	2.5	2.9	3.4	V

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 3.75 V; T_{amb} = −30 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
Z_{RFI}	RF input impedance	balanced	–	150	–	Ω
f_{RFI}	RF input frequency		925	–	960	MHz
RL_{RF}	return loss on matched RF input impedance	note 1	15	20	–	dB
G_{CP}	conversion power gain	differential RF input to any IF output matched to 50 Ω	17	20	23	dB
		differential RF input to differential IF output matched to 1 kΩ differential	20	23	26	dB
G_{rip}	gain ripple as a function of RF frequency	note 2	–	0.1	0.5	dB
ΔG/T	gain variation with temperature	note 2	−20	−15	−10	mdB/K
$CP1_{RX}$	1 dB input compression point	note 1	−24.5	−23.0	–	dBm
$IP2_{RX}$	2nd order intercept point referenced to the RF input	single-ended output; note 2	+22	–	–	dBm
$IP2D_{RX}$	2nd order intercept point referenced to the RF input differential	differential output; note 2	–	+32	–	dBm
$IP3_{RX}$	3rd order intercept point referenced to the RF input	note 2	−18	−15	–	dBm
F_{RX}	overall noise figure	RF input to differential IF output; notes 2 and 3	–	3.5	4.5	dB
$Z_{L(IF)}$	typical application IF output load impedance	unbalanced	–	250	–	Ω
$C_{L(IF)}$	IF output load capacitance	unbalanced	–	–	2	pF
f_{IF}	IF frequency range	RF < LO	50	71	90	MHz
		RF > LO	50	71	90	MHz
f_{IR}	image frequency rejection		30	–	–	dB
f_{IRp}	image rejection at preset	superheterodyne; f_{IF} = 71 MHz; note 1	30	35	–	dB
Local oscillator section (transmit and receive section enabled, SYNTHON = 1)						
f_{LO}	LO input frequency		850	–	1100	MHz
Z_{LO}	LO input impedance	balanced	–	50	–	Ω
RL_{LO}	return loss on matched input (including standby mode)	note 2	10	15	–	dB
$P_{i(LO)}$	LO input power level		−7	−4	+3	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 1	40	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit section (transmit section enabled)						
Z_O	TX IF output impedance		–	–	200	Ω
Z_L	TX IF load impedance		–	100	–	Ω
C_L	maximum TX IF load capacitance		–	–	2	pF
$Z_{i(RF)}$	TX RF input impedance	balanced	–	200	–	Ω
f_{TXmix}	TX mixer input frequency		890	–	915	MHz
RL_{TX}	return loss on matched TX input	note 2	15	20	–	dB
G_{CP}	conversion power gain	from 200 Ω to 1 kΩ output	8	10	12	dB
$f_{o(TX)}$	TX mixer output frequency		40	–	200	MHz
$CP1_{TX}$	1 dB input compression point		−22	−17	–	dBm
$IP2_{TX}$	2nd order intercept point		–	+20	–	dBm
$IP3_{TX}$	3rd order intercept point		−12	−9	–	dBm
F_{TX}	noise figure	double sideband; note 2	–	–	12	dB
RI_{TX}	reverse isolation	TXIN to LOIN; note 2	40	–	–	dB
I_{TX}	isolation	LOIN to TXIN; note 2	40	–	–	dB
Timing						
t_{stu}	start-up time of each block		1	5	20	μs

Notes

1. Measured and guaranteed only on UAA2073M demonstration board at T_{amb} = +25 °C.
2. Measured and guaranteed only on UAA2073M demonstration board.
3. This value includes printed-circuit board and balun losses.

2 GHz image rejecting front-end UAA2077BM

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for over 30 dB on-chip image rejection
- IF I/Q combiner at 188 MHz
- On-chip quadrature network
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast ON/OFF power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 1800 MHz front-end for DCS1800 hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers e.g. PCS, RF-LANS.

GENERAL DESCRIPTION

UAA2077BM contains both a receiver front-end and a high frequency transmit mixer intended to be used in mobile telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2077BM is its ability to provide over 25 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO – IF frequency can form the IF signal. An internal switch allows the use of infradyne or supradyne reception.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection. The IF driver has differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers.The centre frequency of the phase shifter is adjustable for maximum image rejection in a given band. The all-pass filters outputs are buffered before being fed to the receive mixers.

The transmit section consists of a low-noise amplifier, and a down-conversion mixer. In the transmit mode an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced.

Pins allow a selection of whether to reject the upper or lower image frequency and control of the different power-down modes. Special care has been taken for fast power-up switching.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	3.6	4.0	5.3	V
I_{CCRX}	receive supply current	22	27	33	mA
I_{CCTX}	transmit supply current	10	14	18	mA
I_{CCPD}	supply current in power-down	–	–	50	µA
T_{amb}	operating ambient temperature	–30	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2077BM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

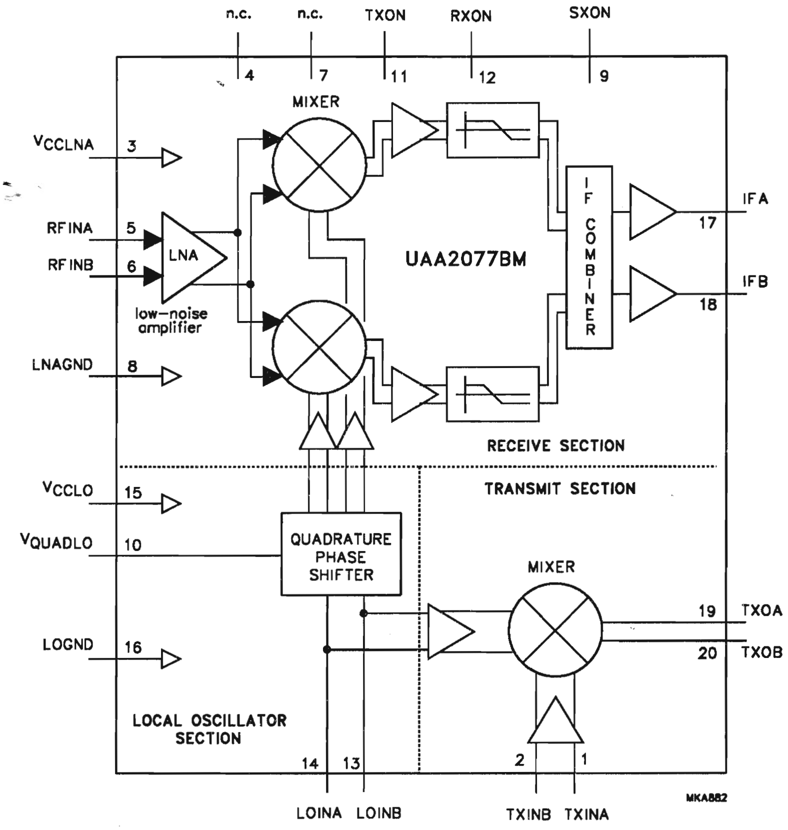


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TXINA	1	transmit mixer input A (balanced)
TXINB	2	transmit mixer input B (balanced)
V_{CCLNA}	3	supply voltage for LNA, IF parts and TX mixer
n.c.	4	not connected
RFINA	5	RF balance input A
RFINB	6	RF balance input B
n.c.	7	not connected
LNAGND	8	ground for LNA parts
SXON	9	synthon mode enable
V_{QUADLO}	10	input voltage for LO quadrature trimming
TXON	11	hardware power-on of the transmit parts
RXON	12	hardware power-on of the receive parts
LOINB	13	LO input B (balanced)
LOINA	14	LO input A (balanced)
V_{CCLO}	15	supply voltage for LO parts
LOGND	16	ground for LO parts
IFA	17	IF output A (balanced)
IFB	18	IF output B (balanced)
TXOIFA	19	transmit mixer IF output A (balanced)
TXOIFB	20	transmit mixer IF output B (balanced)

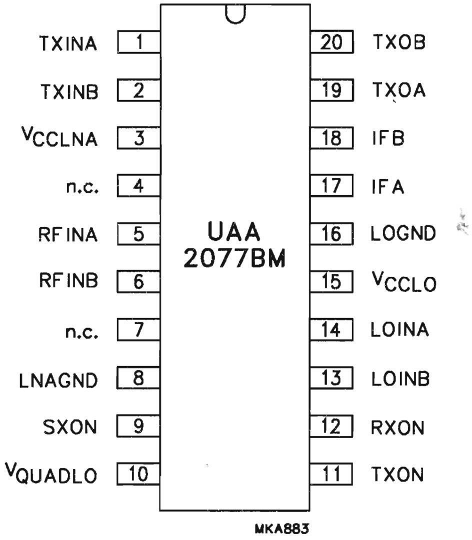


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type, the whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics. The RF impedance level is 30 Ω, choosen to minimize current consumption at best noise performance.

The IF output is differential and of the open-collector type. Typical application will load the output with a differential 1 kΩ load; i.e. a 1 kΩ resistor load at each IF output, plus a 2 kΩ to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The path to V_{CC} for the DC current is achieved via tuning inductors. The output voltage is limited to V_{CC} + $3V_{be}$ or 3 diode forward voltage drops.

Fast switching, ON/OFF, of the receive section is controlled by the hardware input RXON.

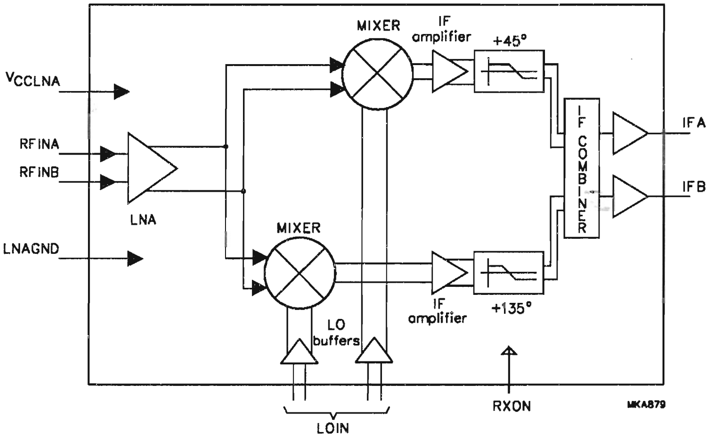


Fig.3 Block diagram, receive section.

Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The centre frequency of the receive band is adjustable by the voltage on pin V_{QUADLO}. This voltage trims the all-pass network to the selected LO frequency range. Over 30 dB of image rejection can be obtained by trimming at this point.

The LO input impedance is 35 Ω differential. A synthon mode is used to power-up all LO input buffers, thus minimizing the pulling effect on the external VCO when entering receive or transmit mode. This mode is active when SXON = 1.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF which is down-converted to a modulated transmit IF frequency which is phase locked with the baseband modulation.

The transmit mixer provides a differential input at 30 Ω and a differential HIGH impedance output. The IF outputs are HIGH impedance (open-collector type); i.e. a 500 Ω resistor load at each IF output, plus a 1 kΩ to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The mixer can also be used for frequency up-conversion.

Fast switching, ON/OFF, of the transmit section is controlled by the hardware input TXON.

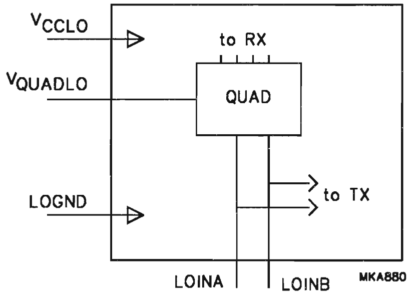


Fig.4 Block diagram, LO section.

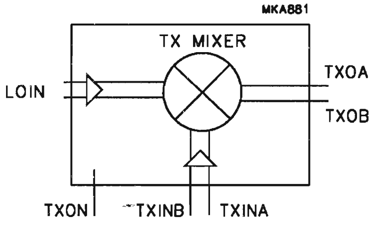


Fig.5 Block diagram, transmit mixer.

Table 1 Control of power status

EXTERNAL PIN LEVEL			CIRCUIT MODE OF OPERATION
TXON	RXON	SXON	
LOW	LOW	LOW	power-down mode
LOW	HIGH	LOW	receive section on, infradyne reception
HIGH	LOW	LOW	transmit section on
LOW	LOW	HIGH	synthon mode
LOW	HIGH	HIGH	receive section on and synthon mode active, infradyne reception
HIGH	LOW	HIGH	transmit section on and synthon mode active
HIGH	HIGH	LOW	receive section on supradyne reception
HIGH	HIGH	HIGH	receive section on and synthon mode active, supradyne reception

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	v
ΔGND	difference in ground supply voltage applied between LOGND and LNAGND	–	0.6	V
$P_{I(max)}$	maximum power input	–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
$P_{dis(max)}$	maximum power dissipation in quiet air	–	250	mW
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2 (method 3015.5).

DC CHARACTERISTICS

V_{CC} = 4.0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: V_{CCLNA}, V_{CCLO}						
V_{CC}	supply voltage	over full temperature range	3.6	4.0	5.3	V
I_{CCRX}	supply current	receive mode active; DC tested	22	27	33	mA
I_{CCTX}	supply current	transmit mode active; DC tested	10	14	18	mA
I_{CCPD}	supply current in power-down mode	DC tested	–	–	50	μA
I_{CCSX}	supply current	synthon mode only	4	7	10	mA
I_{CCSRX}	supply current	receive and synthon mode active	–	29	–	mA
I_{CCSTX}	supply current	transmit and synthon mode active	–	18	–	mA
Pins: RXON, TXON and SXON						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		3	–	V_{CC}	V
V_{IL}	LOW level input voltage		−0.3	–	0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} – 0.4 V	−1	–	+1	μA
I_{IL}	LOW level static input current	pin at 0.4 V	−1	–	+1	μA
Pins: RFINA and RFINB						
V_I	DC input voltage level	receive mode enabled	1.8	2.0	2.2	V
Pins: IFA and IFB						
I_O	DC output current	receive mode enabled	2.0	2.5	3.5	mA
Pins: TXINA and TXINB						
V_I	DC input voltage level	transmit section enabled	1.8	2.0	2.2	V
Pins: TXOIFA and TXOIFB						
I_O	DC output current	transmit section enabled	–	0.9	–	mA
Pins: LOINA and LOINB						
V_{LOIN}	DC input voltage level	RX, TX or SXON HIGH	–	3.3	–	V

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 4.0 V; T_{amb} = –30 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
Z_{RFI}	RF input impedance	balanced at 1850 MHz	–	35	–	Ω
f_{RFI}	RF input frequency		1800	–	2000	MHz
RL_{RF}	return loss on matched RF input	balanced; note 1	11	15	–	dB
G_{CP}	conversion power gain	differential RF input to differential IF outputs loaded to 1 kΩ differential	17	20	23	dB
G_{rip}	gain ripple as a function of RF frequency	between 1805 and 1880 MHz; note 2	–	0.1	–	dB
ΔG/T	gain variation with temperature	note 2	–20	–15	–10	mdB/K
$CP1_{RX}$	1 dB input compression point	note 1	–25	–22.5	–	dBm
$IP2D_{RX}$	2nd order intercept point referenced to the RF input differential	differential output; note 2	–	tbf	–	dBm
$IP3_{RX}$	3rd order intercept point referenced to the RF input	note 2	–20	–17	–	dBm
F_{RX}	overall noise figure	RF input to differential IF output; notes 2 and 3	–	4.3	5.0	dB
$Z_{L(IF)}$	typical application IF output load impedance	balanced	–	1	–	kΩ
RL_{IF}	return loss on matched IF input	balanced; note 1	11	15	–	dB
f_{IF}	IF frequency range	RF < LO	170	188	210	MHz
f_{IR}	image frequency rejection	V_{QUADLO} tuned	–	32	–	dB
IR	image rejection	infradyne; f_{IF} = 188 MHz; note 4	25	27	–	dB
Local oscillator section (receive section enabled)						
f_{LO}	LO input frequency		1600	–	2200	MHz
Z_{LO}	LO input impedance	balanced	–	35	–	Ω
RL_{LO}	return loss on matched input (including standby mode)	note 2	9	12	–	dB
$P_{i(LO)}$	LO input power level		–6	–3	+3	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 1	40	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit section (transmit section enabled)						
Z_L	TX IF typical load impedance		–	500	–	Ω
RL_{TXIF}	return loss on matched transmitter IF input		11	15	–	dB
$Z_{i(RF)}$	TX RF input impedance	balanced at 1750 MHz	–	40	–	Ω
f_{TXmix}	TX mixer input frequency		1600	–	2000	MHz
RL_{TX}	return loss on matched TX input	note 2	10	15	–	dB
G_{CP}	conversion power gain	differential transmitter input to differential transmitter IF output loaded with 500 Ω differential	6	9	12	dB
$f_{o(TX)}$	TX mixer output frequency		50	–	400	MHz
$CP1_{TX}$	1 dB input compression point		–23	–20	–	dBm
$IP2_{TX}$	2nd order intercept point		–	+22	–	dBm
$IP3_{TX}$	3rd order intercept point		–17	–14	–	dBm
F_{TX}	noise figure	double sideband; note 2	–	6	9	dB
RI_{TX}	reverse isolation	TXIN to LOIN; note 2	40	–	–	dB
I_{TX}	isolation	LOIN to TXIN; note 2	40	–	–	dB
Timing						
t_{stu}	start-up time of each block		1	5	20	μs

Notes

1. Measured and guaranteed only on UAA2077BM demonstration board at T_{amb} = +25 °C.
2. Measured and guaranteed only on UAA2077BM demonstration board.
3. This value includes printed-circuit board and balun losses.
4. V_{QUADLO} open-circuit.

Advanced pager receiver UAA2080T

FEATURES

- Wide frequency range: VHF, UHF and 900 MHz bands
- High sensitivity
- High dynamic range
- Electronically adjustable filters on chip
- Suitable for data rates up to 2400 bits/s
- Wide frequency offset and deviation range
- Fully POCSAG compatible FSK receiver
- Power on/off mode selectable by the chip enable input
- Low supply voltage; low power consumption
- High integration level
- Interfaces directly to the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.

APPLICATIONS

- Wide area paging
- On-site paging
- Telemetry
- RF security systems
- Low bit-rate wireless data links.

GENERAL DESCRIPTION

The UAA2080 is a high-performance low-power radio receiver circuit primarily intended for VHF, UHF and 900 MHz pager receivers for wide area digital paging systems, employing direct FM non-return-to-zero (NRZ) frequency shift keying (FSK).

The receiver design is based on the direct conversion principle where the input signal is mixed directly down to the baseband by a local oscillator on the signal frequency. Two complete signal paths with signals of 90° phase difference are required to demodulate the signal. All channel selectivity is provided by the built-in IF filters. The circuit makes extensive use of on-chip capacitors to minimize the number of external components.

The UAA2080 was designed to operate together with the PCA5000A, PCF5001 or PCD5003 POCSAG decoders, which contain a digital input filter for optimum call success rate.

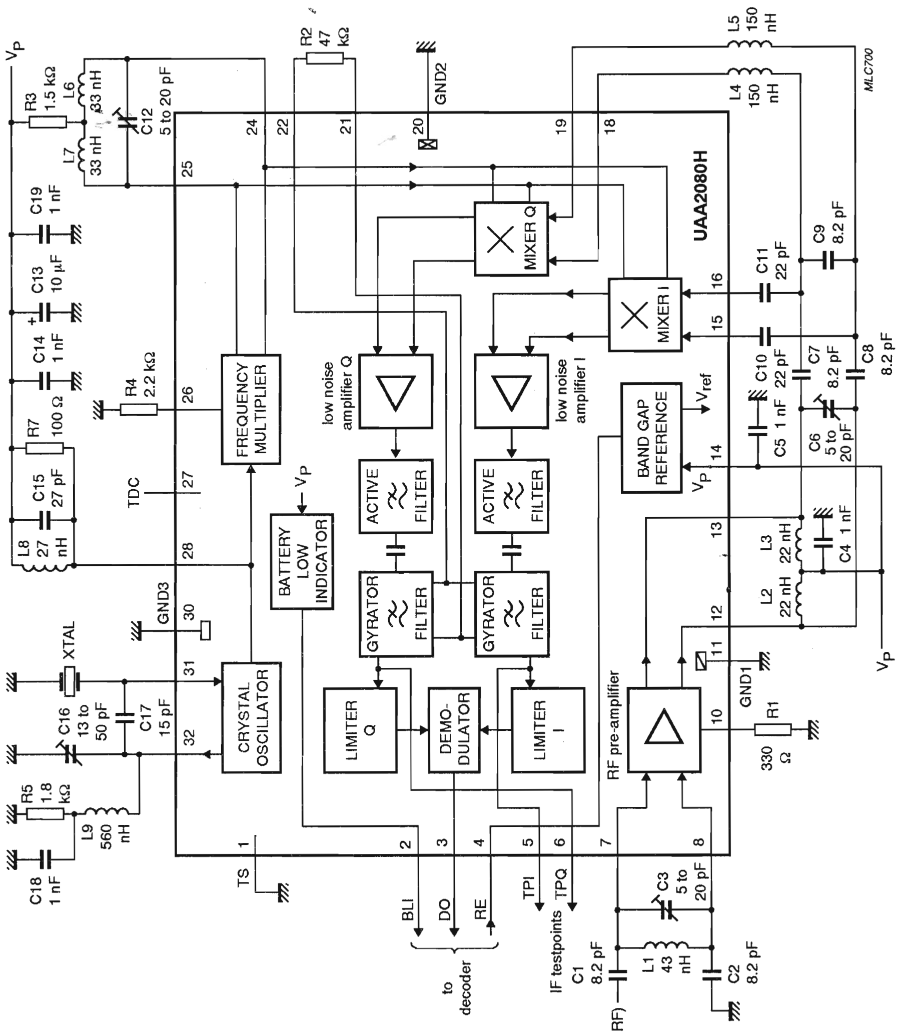
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2080H	TQFP32	plastic thin quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-2
UAA2080T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
UAA2080U	28 pads	naked die; see Fig.9	

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		1.9	2.05	3.5	V
I_P	supply current		2.3	2.7	3.2	mA
$I_{P(off)}$	stand-by current		–	–	3	μA
$P_{i(ref)}$	RF input sensitivity	BER ≤ $^3/_{100}$; ±4 kHz deviation; data rate 1200 bits/s; T_{amb} = 25 °C				
		$f_{i(RF)}$ = 173 MHz	–	−126.5	−123.5	dBm
		$f_{i(RF)}$ = 470 MHz	–	−124.5	−121.5	dBm
		$f_{i(RF)}$ = 930 MHz	–	−120.0	−114.0	dBm
$P_{i(mix)}$	mixer input sensitivity	BER ≤ $^3/_{100}$; $f_{i(RF)}$ = 470 MHz; ±4 kHz deviation; data rate 1200 bits/s; T_{amb} = 25 °C	–	−115.0	−110.0	dBm
V_{th}	detection threshold for battery LOW indicator		1.95	2.05	2.15	V
T_{amb}	operating ambient temperature		−10	–	+70	°C

BLOCK AND TEST DIAGRAMS (173 MHz)



Pins 9, 17, 23 and 29 are not connected.

Fig.1 Block, test and application diagram drawn for TQFP32; $f_{i(RF)}$ = 172.941 MHz.

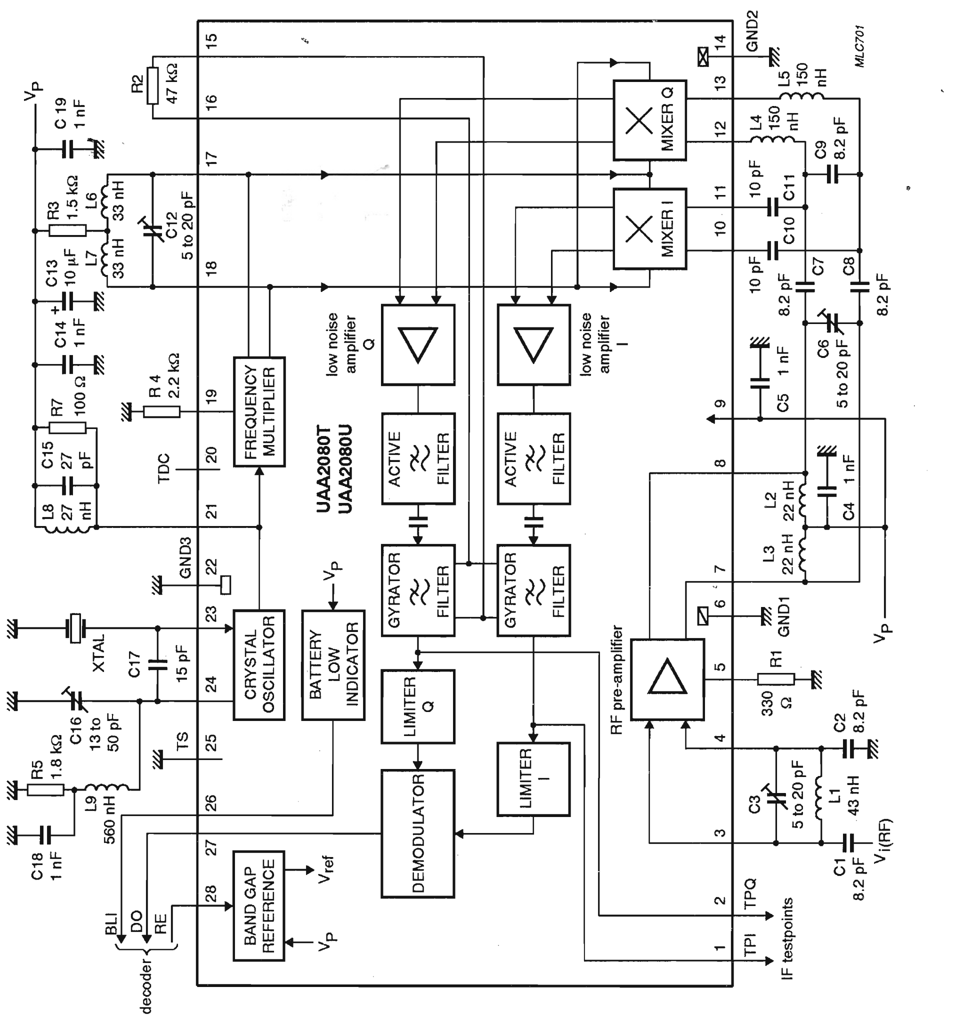


Fig.2 Block, test and application diagram drawn for SO28 and naked die; $f_{i(RF)} = 172.941$ MHz.

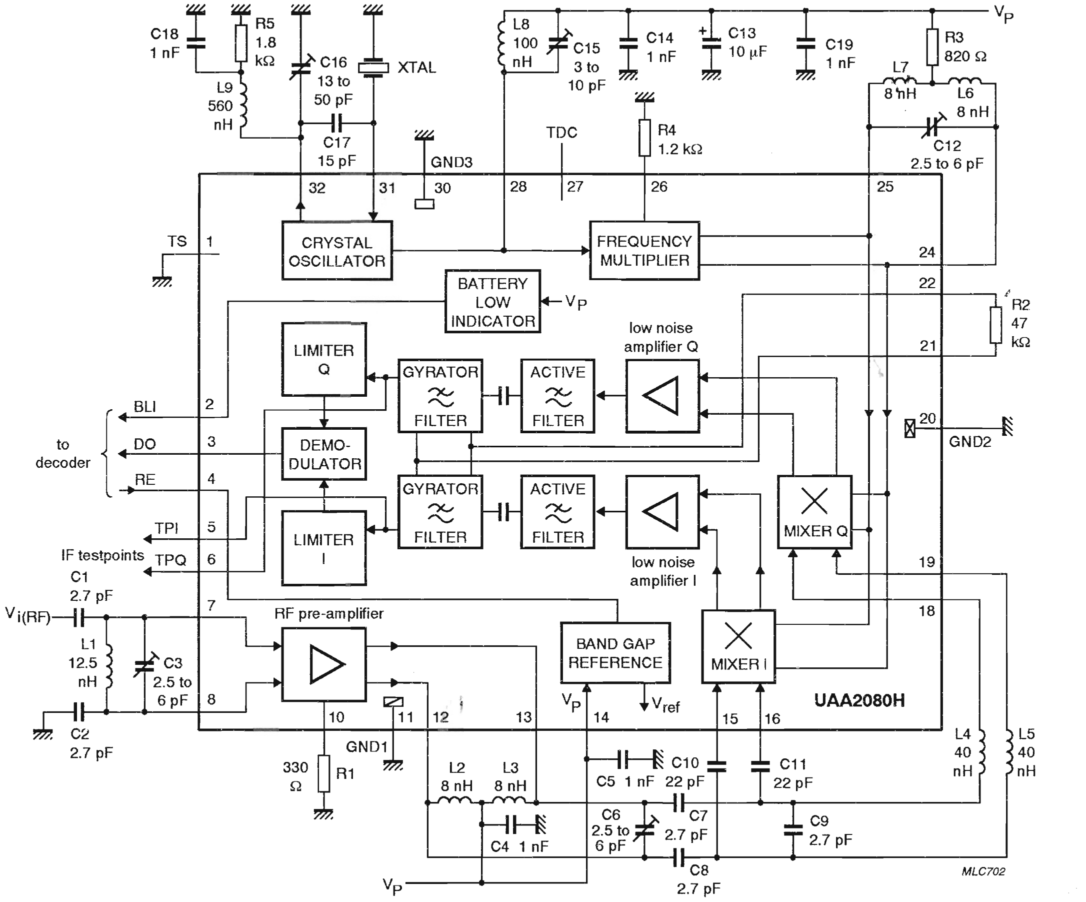
Table 1 Tolerances of components shown in Figs 1 and 2 (notes 1 and 2)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1	±5	Q_{min} = 100 at 173 MHz
L2, L3, L6, L7	±20	Q_{min} = 50 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L4, L5	±10	Q_{min} = 30 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L8	±20	Q_{min} = 30 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L9	±10	Q_{min} = 30 at 57 MHz; TC = (+25 to +125) × 10^{-6}/K
Resistors		
R1 to R7	±2	TC = +50 × 10^{-6}/K
Capacitors		
C1, C2, C7, C8, C9, C15	±5	TC = (0 ±30) × 10^{-6}/K; tan $\delta \leq 30 \times 10^{-4}$ at 1 MHz
C3, C6, C12	–	TC = (−750 ±300) × 10^{-6}/K; tan $\delta \leq 50 \times 10^{-4}$ at 1 MHz
C4, C5, C14, C18, C19	±10	TC = (0 ±30) × 10^{-6}/K; tan $\delta \leq 10 \times 10^{-4}$ at 1 MHz
C10, C11	±5	TC = (0 ±30) × 10^{-6}/K; tan $\delta \leq 21 \times 10^{-4}$ at 1 MHz
C13	±20	
C16	–	TC = (−1700 ±500) × 10^{-6}/K; tan $\delta \leq 50 \times 10^{-4}$ at 1 MHz
C17	±5	TC = (0 ±30) × 10^{-6}/K; tan $\delta \leq 26 \times 10^{-4}$ at 1 MHz

Notes

1. Recommended crystal: f_{XTAL} = 57.647 MHz (crystal with 8 pF load), 3rd overtone, pullability >2.75 × 10^{-6}/pF (change in frequency between series resonance and resonance with 8 pF series capacitor at 25 °C), dynamic resistance R1 < 40 Ω, Δf = ±5 × 10^{-6} for T_{amb} = −10 to +55 °C with 25 °C reference, calibration plus aging tolerance: −5 × 10^{-6} to +15 × 10^{-6}.
2. This crystal recommendation is based on economic aspects and practical experience. Normally the spreads for R1, pullability and calibration do not show their worst case limits simultaneously in one crystal. In such a rare event, the tuning range will be reduced to an insufficient level.

BLOCK AND TEST DIAGRAMS (470 MHz)



Pins 9, 17, 23 and 29 are not connected.

Fig.3 Block, test and application diagram drawn for TQFP32; $f_{i(RF)}$ = 469.95 MHz.

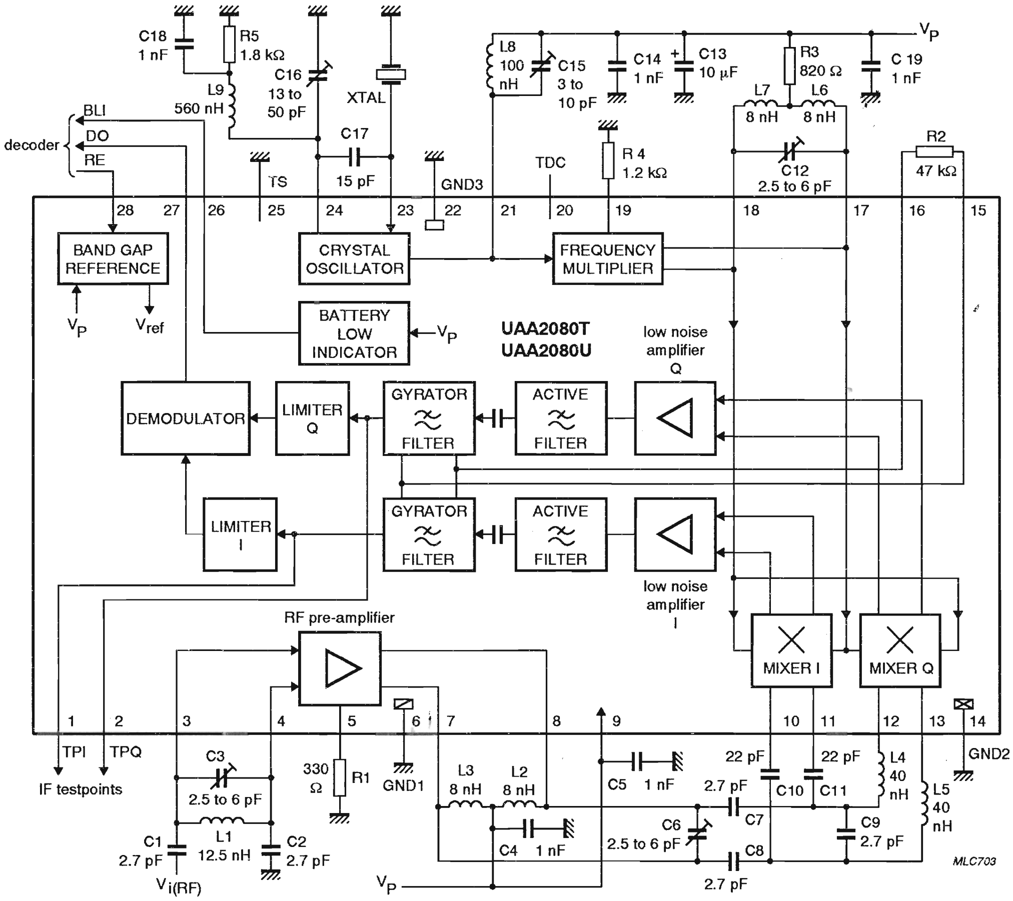


Fig.4 Block, test and application diagram drawn for SO28 and naked die; $f_{i(RF)}$ = 469.95 MHz.

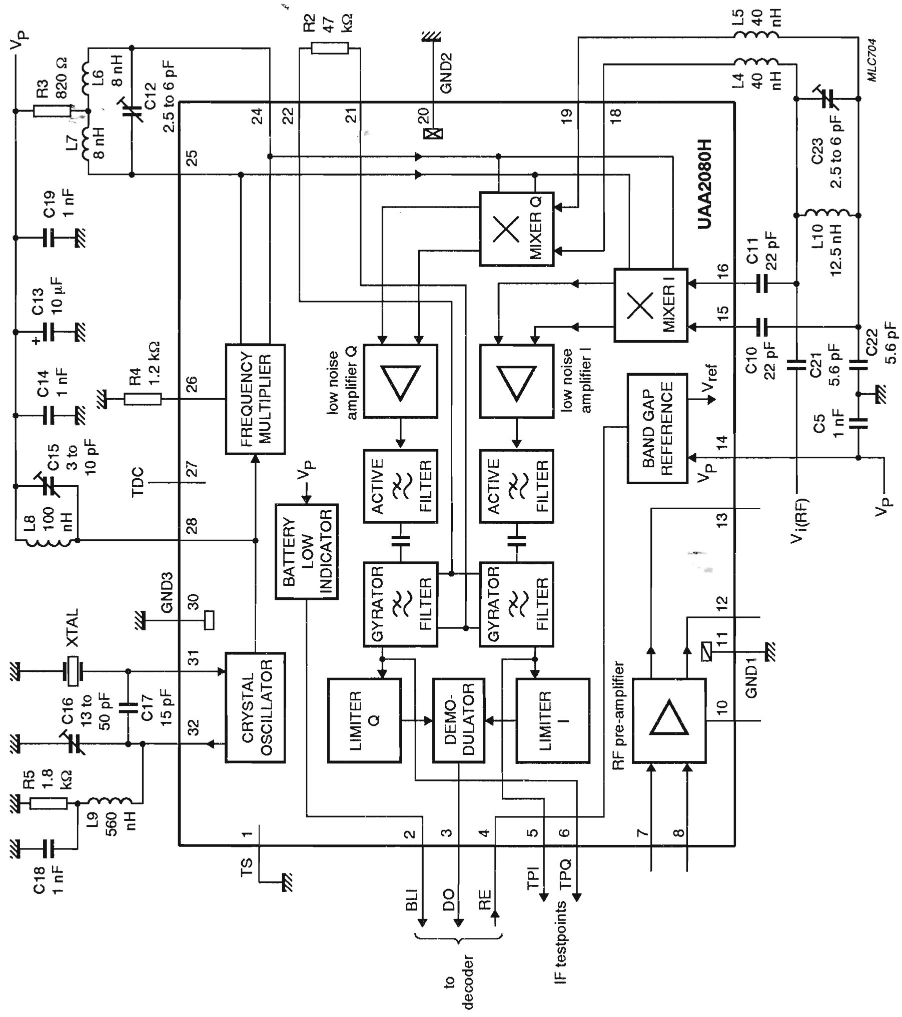


Fig.5 Mixer input sensitivity test circuit; $f_{i(RF)}$ = 469.95 MHz.

Table 2 Tolerances of components shown in Figs 3, 4 and 5 (notes 1 and 2)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1, L10	±5	Q_{min} = 145 at 470 MHz
L2, L3, L6, L7	±20	Q_{min} = 50 at 470 MHz; TC = (+25 to +125) × 10^{-6}/K
L4, L5	±10	Q_{min} = 40 at 470 MHz; TC = (+25 to +125) × 10^{-6}/K
L8	±10	Q_{min} = 30 at 156 MHz; TC = (+25 to +125) × 10^{-6}/K
L9	±10	Q_{min} = 40 at 78 MHz; TC = (+25 to +125) × 10^{-6}/K
Resistors		
R1 to R5	±2	TC = +50 × 10^{-6}/K
Capacitors		
C1, C2, C7, C8, C9	±5	TC = (0 ±30) × 10^{-6}/K; tan $\delta \leq 30 \times 10^{-4}$ at 1 MHz
C3, C6, C12, C23	–	TC = (–750 ±300) × 10^{-6}/K; tan $\delta \leq 50 \times 10^{-4}$ at 1 MHz
C4, C5, C14, C18 to C22	±10	TC = (0 ±30) × 10^{-6}/K; tan $\delta \leq 10 \times 10^{-4}$ at 1 MHz
C10, C11	±5	TC = (0 ±30) × 10^{-6}/K; tan $\delta \leq 21 \times 10^{-4}$ at 1 MHz
C13	±20	
C16	–	TC = (–1 700 ±500) × 10^{-6}/K; tan $\delta \leq 50 \times 10^{-4}$ at 1 MHz
C17	±5	TC = (0 ±30) × 10^{-6}/K; tan $\delta \leq 26 \times 10^{-4}$ at 1 MHz

Notes

1. Recommended crystal: f_{XTAL} = 78.325 MHz (crystal with 8 pF load), 3rd overtone, pullability >2.75 × 10^{-6}/pF (change in frequency between series resonance and resonance with 8 pF capacitor at 25 °C), dynamic resistance R1 < 30 Ω, Δf = ±5 × 10^{-6} for T_{amb} = −10 to +55 °C with 25 °C reference, calibration plus aging tolerance: −5 × 10^{-6} to +15 × 10^{-6}.
2. This crystal recommendation is based on economic aspects and practical experience. Normally the spreads for R1, pullability and calibration do not show their worst case limits simultaneously in one crystal. In such a rare event, the tuning range will be reduced to an insufficient level.

BLOCK AND TEST DIAGRAM (930 MHz)

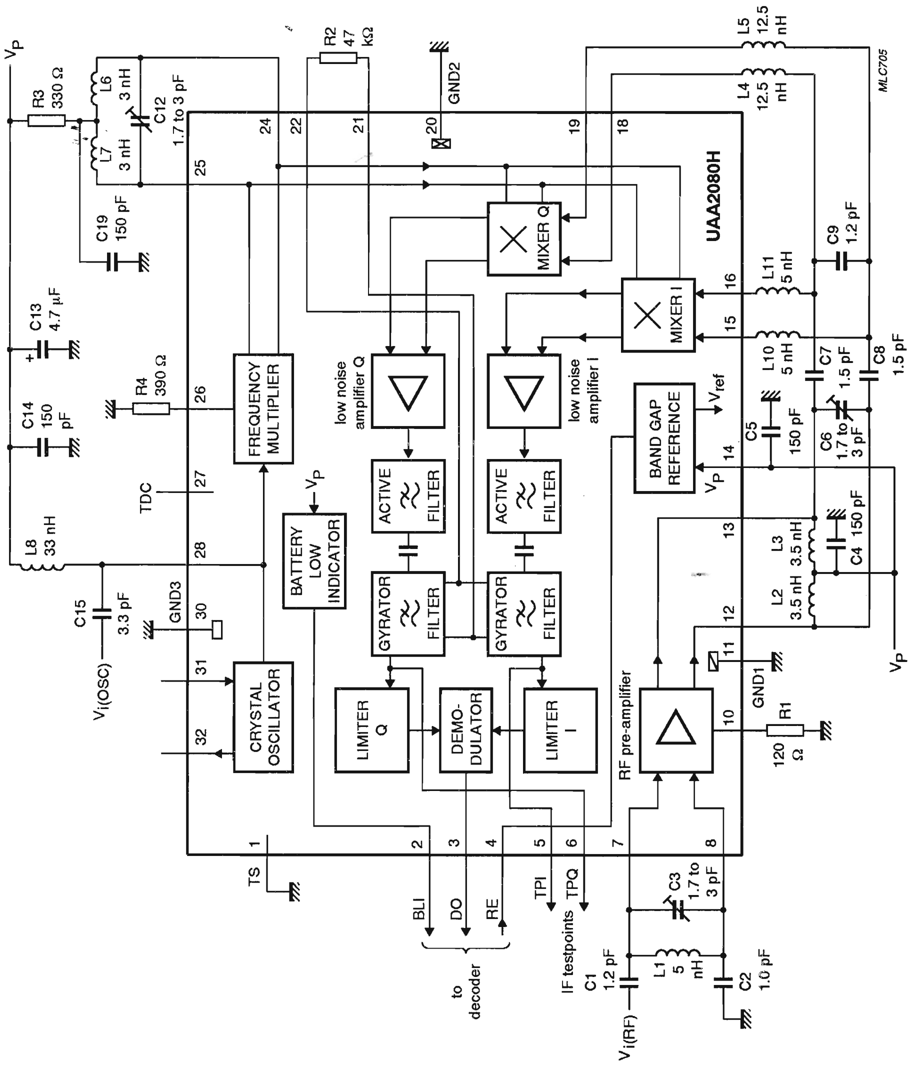


Fig.6 Test circuit; $f_{i(RF)}$ = 930.50 MHz.

Pins 9, 17, 23 and 29 are not connected.

Table 3 Tolerances of components shown in Fig.6 (note 1)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1	±10	Q_{typ} = 150 at 930 MHz
L2, L3, L6, L7	–	microstrip inductor
L4, L5	±5	Q_{typ} = 100 at 930 MHz
L8	±10	Q_{typ} = 65 at 310 MHz
L10, L11	±10	Q_{typ} = 150 at 930 MHz
Resistors		
R1 to R4	±2	TC = $(0 \pm 200) \times 10^{-6}$/K;
Capacitors		
C1, C2, C7, C8, C9, C15	±5	TC = $(0 \pm 30) \times 10^{-6}$/K; tan $\delta \leq 30 \times 10^{-4}$ at 1 MHz
C3, C6, C12	–	TC = $(0 \pm 200) \times 10^{-6}$/K; tan $\delta \leq 30 \times 10^{-4}$ at 1 MHz
C4, C5, C14, C19	±10	TC = $(0 \pm 30) \times 10^{-6}$/K; tan $\delta \leq 10 \times 10^{-4}$ at 1 MHz
C13	±20	

Note

1. The external oscillator signal $V_{i(OSC)}$ has a frequency of f_{OSC} = 310.1667 MHz.

PINNING (TQFP32)

SYMBOL	PIN	DESCRIPTION
TS	1	test switch; connection to ground for normal operation
BLI	2	battery LOW indicator output
DO	3	data output
RE	4	receiver enable input
TPI	5	IF test point; I channel
TPQ	6	IF test point; Q channel
VI1RF	7	pre-amplifier RF input 1
VI2RF	8	pre-amplifier RF input 2
n.c.	9	not connected
RRFA	10	external emitter resistor for pre-amplifier
GND1	11	ground 1 (0 V)
VO2RF	12	pre-amplifier RF output 2
VO1RF	13	pre-amplifier RF output 1
V_P	14	supply voltage
VI2MI	15	I channel mixer input 2
VI1MI	16	I channel mixer input 1
n.c.	17	not connected
VI1MQ	18	Q channel mixer input 1
VI2MQ	19	Q channel mixer input 2
GND2	20	ground 2 (0 V)
COM	21	gyrator filter resistor; common line
RGYR	22	gyrator filter resistor
n.c.	23	not connected
VO1MUL	24	frequency multiplier output 1
VO2MUL	25	frequency multiplier output 2
RMUL	26	external emitter resistor for frequency multiplier
TDC	27	DC test point; no external connection for normal operation
OSC	28	oscillator collector
n.c.	29	not connected
GND3	30	ground 3 (0 V)
OSB	31	oscillator base; crystal input
OSE	32	oscillator emitter

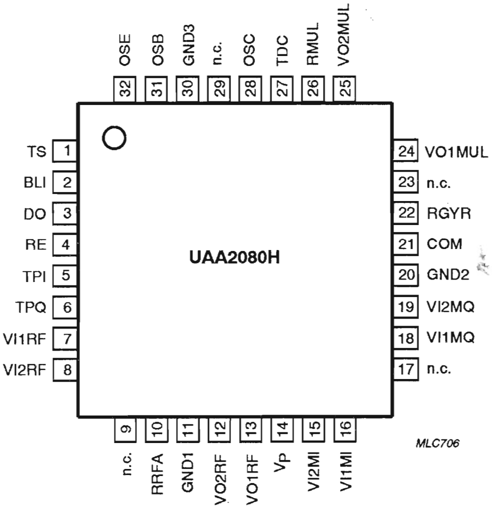


Fig.7 Pin configuration; TQFP32.

PINNING (SO28)

SYMBOL	PIN	DESCRIPTION
TPI	1	IF test point; I channel
TPQ	2	IF test point; Q channel
VI1RF	3	pre-amplifier RF input 1
VI2RF	4	pre-amplifier RF input 2
RRFA	5	external emitter resistor for pre-amplifier
GND1	6	ground 1 (0 V)
VO2RF	7	pre-amplifier RF output 2
VO1RF	8	pre-amplifier RF output 1
V_P	9	supply voltage
VI2MI	10	I channel mixer input 2
VI1MI	11	I channel mixer input 1
VI1MQ	12	Q channel mixer input 1
VI2MQ	13	Q channel mixer input 2
GND2	14	ground 2 (0 V)
COM	15	gyrator filter resistor; common line
RGYR	16	gyrator filter resistor
VO1MUL	17	frequency multiplier output 1
VO2MUL	18	frequency multiplier output 2
RMUL	19	external emitter resistor for frequency multiplier
TDC	20	DC test point; no external connection for normal operation
OSC	21	oscillator collector
GND3	22	ground 3 (0 V)
OSB	23	oscillator base; crystal input
OSE	24	oscillator emitter
TS	25	test switch; connection to ground for normal operation
BLI	26	battery LOW indicator output
DO	27	data output
RE	28	receiver enable input

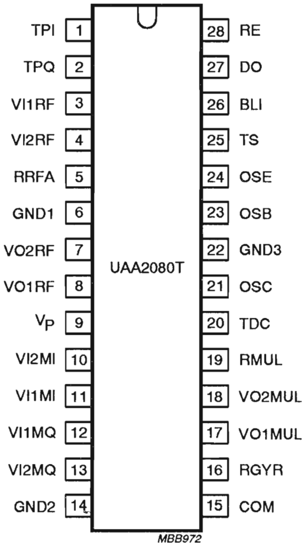
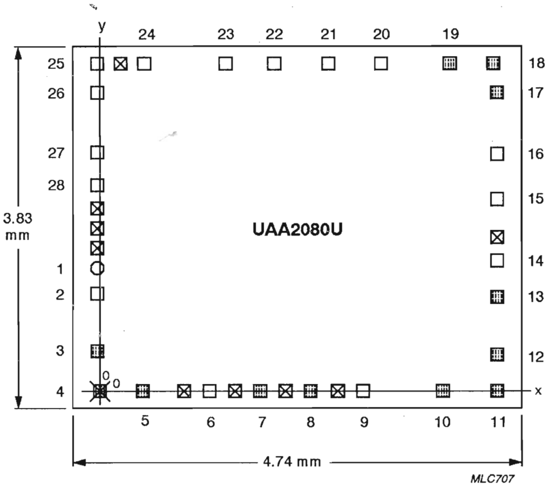


Fig.8 Pin configuration; SO28.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

See Table 4 for bonding pad description and locations for x/y co-ordinates.



Where:

○ Pad number 1 (diameter 124 µm)

□ Pad 124 µm x 124 µm

☒ Pad not used

▦ Pad 100 µm x 100 µm

☒ Pad 100 µm x 100 µm with reference point

Chip area: 18.15 mm^2.
Chip thickness: 380 ±20 µm.
Drawing not to scale.

Fig.9 Bonding pad locations.

Table 4 Bonding pad centre locations (dimensions in μm)

SYMBOL	PAD	DESCRIPTION	x	y
TPI	1	IF test point; I channel	–32	1296
TPQ	2	IF test point; Q channel	–32	1000
VI1RF	3	pre-amplifier RF input 1	–32	360
VI2RF	4	pre-amplifier RF input 2; note 1	0	0
RRFA	5	external emitter resistor for pre-amplifier	472	0
GND1	6	ground 1 (0 V)	1160	0
VO2RF	7	pre-amplifier RF output 2	1688	0
VO1RF	8	pre-amplifier RF output 1	2232	0
V_P	9	supply voltage	2760	0
VI2MI	10	I channel mixer input 2	3608	0
VI1MI	11	I channel mixer input 1	4216	0
VI1MQ	12	Q channel mixer input 1	4216	360
VI2MQ	13	Q channel mixer input 2	4216	960
GND2	14	ground 2 (0 V)	4216	1360
COM	15	gyrator filter resistor; common line	4216	2024
RGYR	16	gyrator filter resistor	4216	2496
VO1MUL	17	frequency multiplier output 1	4216	3136
VO2MUL	18	frequency multiplier output 2	4176	3456
RMUL	19	external emitter resistor for frequency multiplier	3668	3458
SENSE	20	battery LOW detector sense input	2952	3456
OSC	21	oscillator collector	2312	3456
GND3	22	ground 3 (0 V)	1832	3456
OSB	23	oscillator base; crystal input	1328	3456
OSE	24	oscillator emitter	432	3456
TS	25	test switch; connection to ground for normal operation	–32	3456
BLI	26	battery LOW indicator output	–32	3136
DO	27	data output	–32	2512
RE	28	receiver enable input	–32	2152
		lower left corner of chip (typical values)	–278	–186

Note

1. All x/y co-ordinates are referenced to the centre of pad 4 (VI2RF); see Fig.9.

INTERNAL CIRCUITS

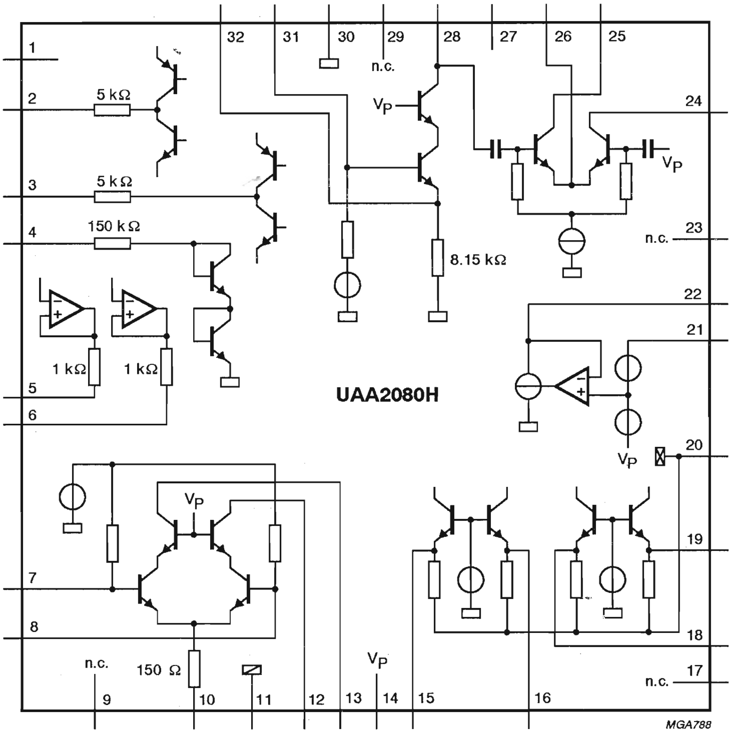


Fig.10 Internal circuits drawn for TQFP32.

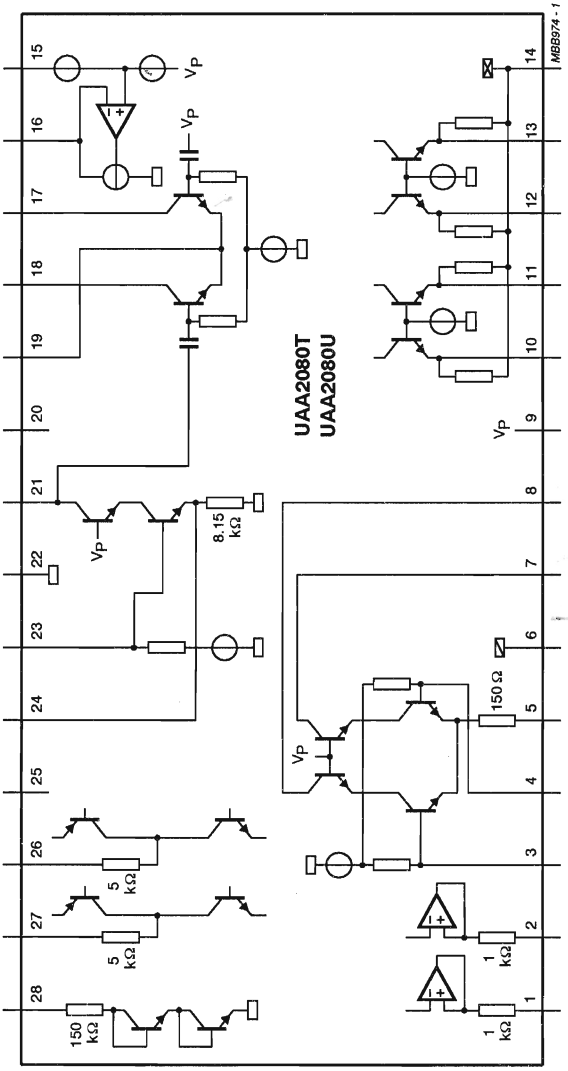


Fig.11 Internal circuits drawn for SO28 and naked die.

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Figs 1 to 6.

Radio frequency amplifier

The RF amplifier is an emitter-coupled pair driving a balanced cascode stage, which drives an external balanced tuned circuit. Its bias current is set by an external 300 Ω resistor R1 to typically 770 μA. With this bias current the optimum source resistance is 1.3 kΩ at VHF and 1.0 kΩ at UHF. At 930 MHz a higher bias current is required to achieve optimum gain. A value of 120 Ω is used for R1, which corresponds with a bias current of approximately 1.3 mA and an optimum source resistance of approximately 600 Ω.The capacitors C1 and C2 transform a 50 Ω source resistance to this optimum value. The output drives a tuned circuit with capacitive divider (C7, C8 and C9) to provide maximum power transfer to the phase-splitting network and the mixers.

Mixers

The double balanced mixers consist of common base input stages and upper switching stages driven from the frequency multiplier. The 300 Ω input impedance of each mixer acts together with external components (C10, C11; L4, L5 respectively) as phase shifter/power splitter to provide a differential phase shift of 90 degrees between the I channel and the Q channel. At 930 MHz all external phase shifter components are inductive (L10, L11; L4, L5).

Oscillator

The oscillator is based on a transistor in common collector configuration. It is followed by a cascode stage driving a tuned circuit which provides the signal for the frequency multiplier. The oscillator bias current (typically 250 μA) is determined by the 1.8 kΩ external resistor R5. The oscillator frequency is controlled by an external 3rd overtone crystal in parallel resonance mode. External capacitors between base and emitter (C17) and from emitter to ground (C16) make the oscillator transistor appear as having a negative resistance for small signals; this causes the oscillator to start. Inductance L9 connected in parallel with capacitor C16 to the emitter of the oscillator transistor prevents oscillation at the fundamental frequency of the crystal.

The resonant circuit at output pin OSC selects the second harmonic of the oscillator frequency. In other applications a different multiplication factor may be chosen.

At 930 MHz an external oscillator circuit is required to provide sufficient local oscillator signal for the frequency multiplier.

Frequency multiplier

The frequency multiplier is an emitter-coupled pair driving an external balanced tuned circuit. Its bias current is set by external resistor R4 to typically 190 μA (173 MHz), 350 μA (470 MHz) and 1 mA (930 MHz). The oscillator signal is internally AC coupled to one input of the emitter-coupled pair while the other input is internally grounded via a capacitor. The frequency multiplier output signal between pins VO1MUL and VO2MUL drives the upper switching stages of the mixers. The bias voltage on pins VO1MUL and VO2MUL is set by external resistor R3 to allow sufficient voltage swing at the mixer outputs. The value of R3 depends on the operating frequency: 1.5 kΩ (173 MHz), 820 Ω (470 MHz) and 330 Ω (930 MHz).

Low noise amplifiers, active filters and gyrator filters

The low noise amplifiers ensure that the noise of the following stages does not affect the overall noise figure. The following active filters before the gyrator filters reduce the levels of large signals from adjacent channels. Internal AC couplings block DC offsets from the gyrator filter inputs.

The gyrator filters implement the transfer function of a 7th order elliptic filter. Their cut-off frequencies are determined by the 47 kΩ external resistor R2 between pins RGYR and COM. The gyrator filter output signals are available on IF test pins TPI and TPQ.

Limiters

The gyrator filter output signals are amplified in the limiter amplifiers to obtain IF signals with removed amplitude information.

Demodulator

The limiter amplifier output signals are fed to the demodulator. The demodulator output DO is going LOW or HIGH depending upon which of the input signals has a phase lead.

Battery LOW indicator

The battery LOW indicator senses the supply voltage and sets its output HIGH when the supply voltage is less than V_{th} (typically 2.05 V). Low battery warning is available at BLI.

Band gap reference

The whole chip can be powered-up and powered-down by enabling and disabling the band gap reference via the receiver enable pin RE.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).
Ground pins GND1, GND2 and GND3 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	−0.3	+8.0	V
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−10	+70	°C
V_{es}	electrostatic handling (note 1)			
	pins VI1RF and VI2RF	−1500	+2000	V
	pin RRFA	−500	+2000	V
	pins VO1RF and VO2RF	−2000	+250	V
	pins V_P and OSB	−500	+500	V
	pins OSC and OSE	−2000	+500	V
	other pins	−2000	+2000	V

Note

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor.

DC CHARACTERISTICS

V_P = 2.05 V; T_{amb} = −10 to +70 °C (typical values at T_{amb} = 25 °C); measurements taken in test circuit Fig.1, 2, 3 or 4 with crystal at pin OSB disconnected; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		1.9	2.05	3.5	V
I_P	supply current	V_{RE} = HIGH; $f_{i(RF)}$ = 173 and 470 MHz	2.3	2.7	3.2	mA
		V_{RE} = HIGH; $f_{i(RF)}$ = 930 MHz	2.9	3.4	3.9	mA
$I_{P(off)}$	stand-by current	V_{RE} = LOW	–	–	3	μA
Receiver enable input (pin RE)						
V_{IH}	HIGH level input voltage		1.4	–	V_P	V
V_{IL}	LOW level input voltage		0	–	0.3	V
I_{IH}	HIGH level input current	$V_{IH} = V_P$ = 3.5 V	–	–	20	μA
V_{IL}	LOW level input current	V_{IL} = 0 V	0	–	−1.0	μA
Battery LOW indicator output (pin BLI)						
V_{OH}	HIGH level output voltage	$V_P < V_{th}$; I_{BLI} = −10 μA	V_P − 0.5	–	–	V
V_{OL}	LOW level output voltage	$V_P > V_{th}$; I_{BLI} = +10 μA	–	–	0.5	V
V_{th}	voltage threshold for battery LOW indicator		1.95	2.05	2.15	V
Demodulator output (pin DO)						
V_{OH}	HIGH level output voltage	I_{DO} = −10 μA	V_P − 0.5	–	–	V
V_{OL}	LOW level output voltage	I_{DO} = +10 μA	–	–	0.5	V

AC CHARACTERISTICS (173 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Fig.1 or 2; $f_{i(RF)}$ = 172.941 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ±25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ 3⁄100; note 1	–	−126.5	−123.5	dBm
		T_{amb} = −10 to +70 °C; note 2	–	–	−120.5	dBm
		V_P = 1.9 V	–	–	−117.5	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	69	72	–	dB
		T_{amb} = −10 to +70 °C	67	–	–	dB
α_{ci}	IF filter channel imbalance		–	–	2	dB
α_c	co-channel rejection		–	4	7	dB
α_{sp}	spurious immunity		50	60	–	dB
α_{im}	intermodulation immunity		55	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 3	78	85	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 4	–	–	5	ms

Notes

1. The bit error rate BER is measured using the test facility shown in Fig.13. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
2. Capacitor C16 requires re-adjustment to compensate temperature drift.
3. Δf is the frequency offset between the required signal and the interfering signal.
4. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

AC CHARACTERISTICS (470 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Fig.3 or 4; $f_{i(RF)}$ = 469.950 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ± 25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 1	–	–124.5	–121.5	dBm
		T_{amb} = –10 to +70 °C; note 2	–	–	–118.5	dBm
		V_P = 1.9 V	–	–	–115.5	dBm
Mixer input						
$P_{i(mix)}$	input sensitivity	BER ≤ $^3/_{100}$; note 3	–	–115.0	–110.0	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	67	70	–	dB
		T_{amb} = –10 to +70 °C	65	–	–	dB
α_{ci}	IF filter channel imbalance		–	–	2	dB
α_c	co-channel rejection		–	4	7	dB
α_{sp}	spurious immunity		50	60	–	dB
α_{im}	intermodulation immunity		55	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 4	75	82	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 5	–	–	5	ms

Notes

1. The bit error rate BER is measured using the test facility shown in Fig.13. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
2. Capacitor C16 requires re-adjustment to compensate temperature drift.
3. Test circuit Fig.5. $P_{i(mix)}$ is the maximum available power at the input of the test board. The bit error rate BER is measured using the test facility shown in Fig.13.
4. Δf is the frequency offset between the required signal and the interfering signal.
5. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

AC CHARACTERISTICS (930 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Fig.6 (note 1); $f_{i(RF)}$ = 930.500 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ± 25 μs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 2	–	–120.0	–114.0	dBm
		V_P = 1.9 V	–	–	–108.0	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	60	69	–	dB
α_c	co-channel rejection		–	5	10	dB
α_{sp}	spurious immunity		40	60	–	dB
α_{im}	intermodulation immunity		53	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 3	65	74	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 4	–	–	5	ms

Notes

1. The external oscillator signal $V_{i(OSC)}$ has a frequency of f_{OSC} = 310.1667 MHz and a level of –15 dBm.
2. The bit error rate BER is measured using the test facility shown in Fig.13. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
3. Δf is the frequency offset between the required signal and the interfering signal.
4. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

TEST INFORMATION

Tuning procedure for AC tests

1. Turn on the signal generator: $f_{gen} = f_{i(RF)} + 4$ kHz, no modulation, $V_{i(RF)} = 1$ mV (RMS).
2. Measure the IF with a counter connected to test pin TPI. Tune C16 to set the crystal oscillator to achieve $f_{IF} = 4$ kHz Change the generator frequency to $f_{gen} = f_{i(RF)} - 4$ kHz and check that f_{IF} is also 4 kHz. For a received input frequency $f_{i(RF)} = 172.941$ MHz the crystal frequency is $f_{XTAL} = 57.647$ MHz, while for $f_{i(RF)} = 469.950$ MHz the crystal frequency is $f_{XTAL} = 78.325$ MHz. For a received input frequency $f_{i(RF)} = 930.500$ MHz an external oscillator signal must be used with $f_{i(OSC)} = 310.1667$ MHz and a level of −15 dBm (for definition of crystal frequency, see Table 1).
3. Set the signal generator to nominal frequency ($f_{i(RF)}$) and turn on the modulation deviation ±4.0 kHz, 600 Hz square wave modulation, $V_{i(RF)} = 1$ mV (RMS). Note that the RF signal should be reduced in the following tests, as the receiver is tuned, to ensure $V_{o(IF)} = 10$ to 50 mV (p-p) on test pins TPI or TPQ.
4. Tune C15 (oscillator output circuit) and C12 (frequency multiplier output) to obtain a peak audio voltage on pin TPI.
5. Tune C3 and C6 (RF input and mixer input) to obtain a peak audio voltage on pin TPI. When testing the mixer input sensitivity tune C23 instead of C3 and C6 (test circuit Fig.5).
6. Check that the output signal on pin TPQ is within 3 dB in amplitude and at 90° (±20°) relative phase of the signal on pin TPI.
7. Check that data signal appears on output pin DO and proceed with the AC test.

AC test conditions

Table 5 Definitions for AC test conditions (see Table 6)

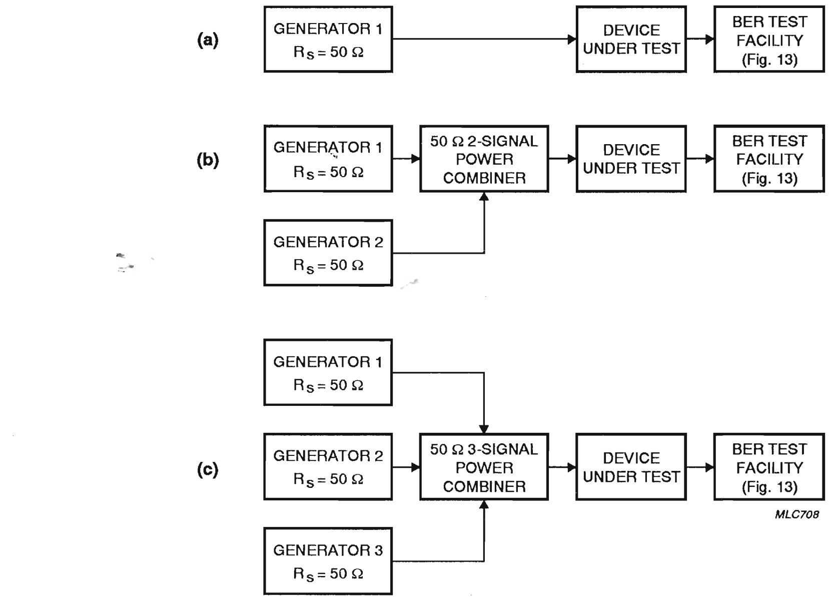
SIGNAL	DESCRIPTION
Modulated test signal 1	
Frequency	172.941, 469.950 or 930.500 MHz
Deviation	±4.0 kHz
Modulation	1200 baud pseudo random bit sequence
Rise time	250 ±25 μs (between 10% and 90% of final value)
Modulated test signal 2	
Deviation	±2.4 kHz
Modulation	400 Hz sine wave
Other definitions	
f_1	frequency of signal generator 1
f_2	frequency of signal generator 2
f_3	frequency of signal generator 3
Δf_{cs}	channel spacing (20 kHz)
P_1	maximum available power from signal generator 1 at the test board input
P_2	maximum available power from signal generator 2 at the test board input
P_3	maximum available power from signal generator 3 at the test board input
$P_{i(ref)}$	maximum available power at the test board input to give a Bit Error Rate (BER) ≤ $^3/_{100}$ for the modulated test signal 1, in the absence of interfering signals and under the conditions as specified in Chapters “AC characteristics (173 MHz)”, “AC characteristics (470 MHz)” and “AC characteristics (930 MHz)”

Table 6 AC test conditions (notes 1 and 2)

SYMBOL	PARAMETER	CONDITIONS	TEST SIGNALS
α_a	adjacent channel selectivity; Fig.12(b)	$f_2 = f_1 \pm \Delta f_{CS}$ generator 1: modulated test signal 1 generator 2: modulated test signal 2	 $P_1 = P_{i(ref)} + 3$ dB $P_2 = P_1 + \alpha_{a(min)}$
α_c	co-channel rejection; Fig.12(b)	$f_2 = f_1 \pm$ up to 3 kHz generator 1: modulated test signal 1 generator 2: modulated test signal 2	 $P_1 = P_{i(ref)} + 3$ dB $P_2 = P_1 - \alpha_{c(max)}$
α_{sp}	spurious immunity; Fig.12(b)	$f_2 = 100$ kHz to 2 GHz generator 1: modulated test signal 1 generator 2: modulated test signal 2	 $P_1 = P_{i(ref)} + 3$ dB $P_2 = P_1 + \alpha_{sp(min)}$
α_{im}	intermodulation immunity; Fig.12(c)	$f_2 = f_1 \pm \Delta f_{cs}$; $f_3 = f_1 \pm 2\Delta f_{cs}$ generator 1: modulated test signal 1 generator 2: unmodulated generator 3: modulated test signal 2	 $P_1 = P_{i(ref)} + 3$ dB $P_2 = P_1 + \alpha_{im(min)}$ $P_3 = P_2$
α_{bl}	blocking immunity; Fig.12(b)	$f_2 = f_1 \pm 1$ MHz generator 1: modulated test signal 1 generator 2: modulated test signal 2	 $P_1 = P_{i(ref)} + 3$ dB $P_2 = P_1 + \alpha_{bl(min)}$
f_{offset}	frequency offset range; Fig.12(a)	deviation = ±4.0 kHz, $f_1 = f_{i(RF)} \pm 2$ kHz ($f_{offset(min)}$) generator 1: modulated test signal 1	 $P_1 = P_{i(ref)} + 3$ dB
Δf_{dev}	deviation range; Fig.12(a)	deviation = ±2.5 to ±7 kHz; ($\Delta f_{dev(min)}$ to $\Delta f_{dev(max)}$) generator 1: modulated test signal 1	 $P_1 = P_{i(ref)} + 3$ dB
t_{on}	receiver turn-on time; Fig.12(a)	note 3 generator 1: modulated test signal 1	 $P_1 = P_{i(ref)} + 10$ dB

Notes

1. The tests are executed without load on pins TPI and TPQ.
2. All minimum and maximum values correspond to a bit error rate (BER) ≤ $^3/_{100}$ in the wanted signal (P_1).
3. The BER measurement is started 5 ms ($t_{on(max)}$) after V_{RE} goes HIGH; BER is then measured for 100 bits (BER ≤ $^3/_{100}$).



(a) One generator.
(b) Two generators.
(c) Three generators.

Fig.12 Test configurations.

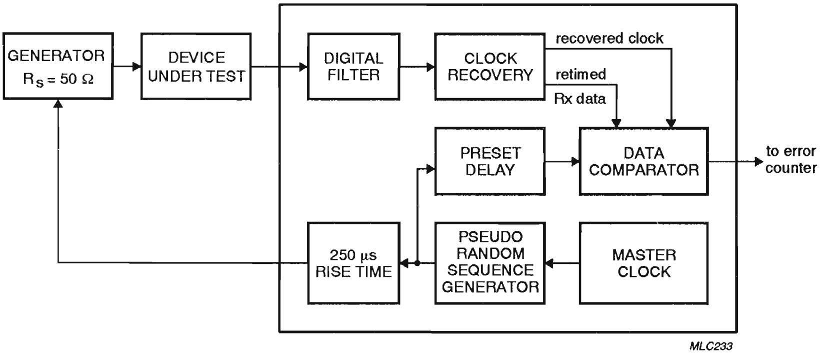


Fig.13 BER test facility.

PRINTED-CIRCUIT BOARDS

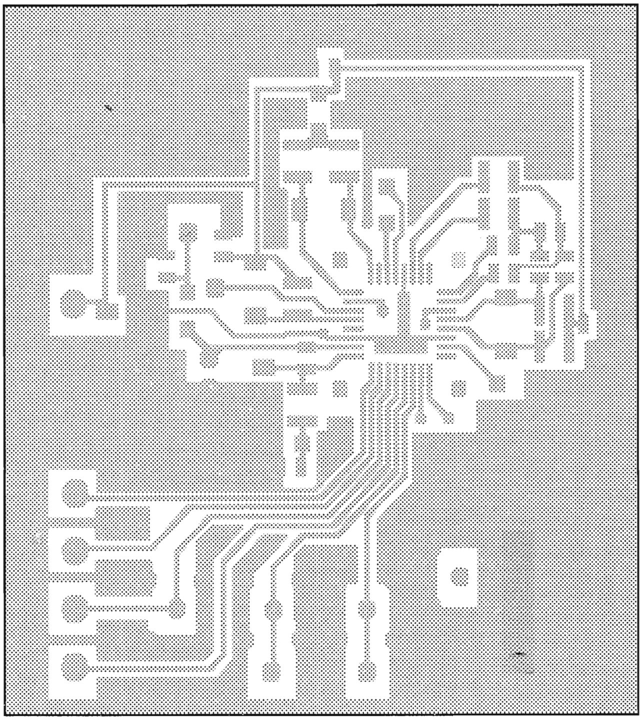


Fig.14 PCB top view for TQFP32; test circuit Figs 1 and 3.

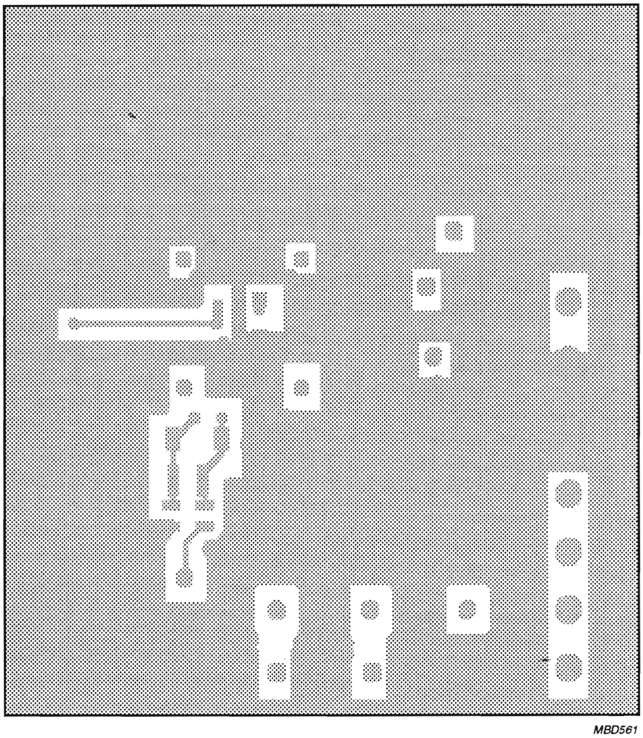
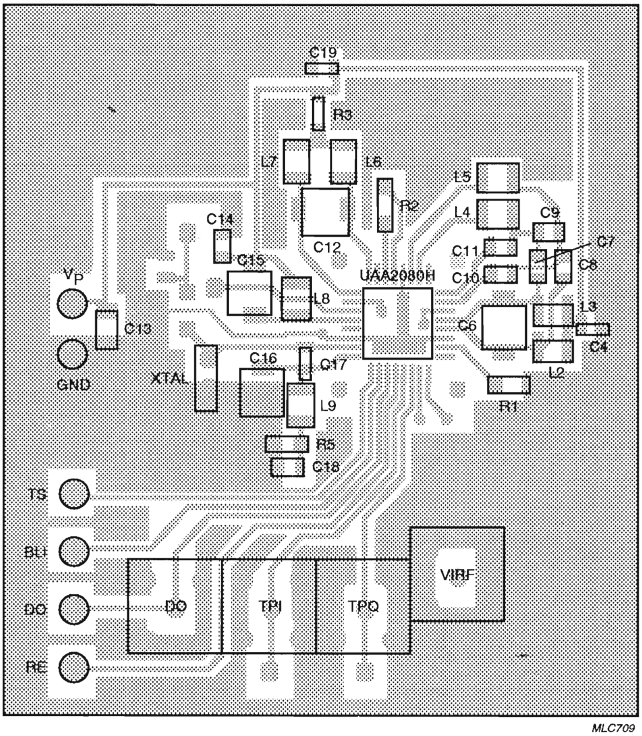


Fig.15 PCB bottom view for TQFP32; test circuit Figs 1 and 3.



V_{EE} = GND; V_C = V_P.

Fig.16 PCB top view with components for TQFP32; test circuit Fig.3.

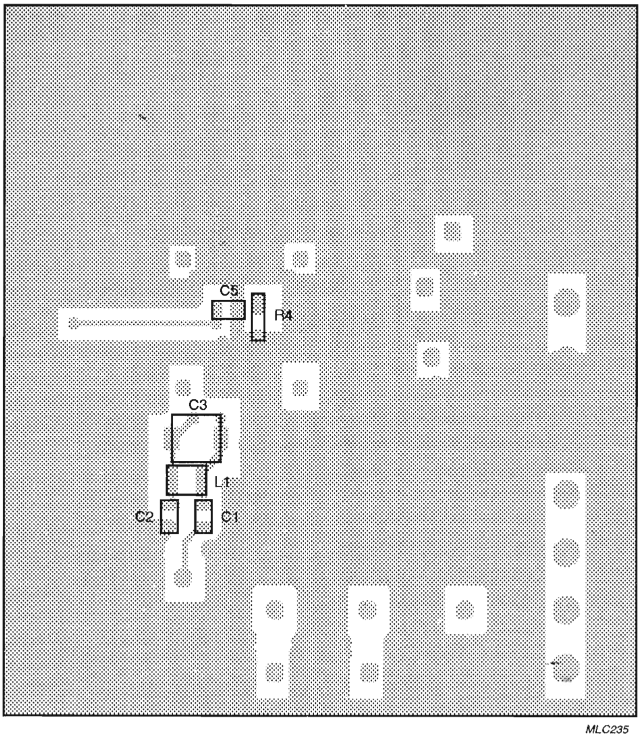


Fig.17 PCB bottom view with components for TQFP32; test circuit Fig.3.

Advanced pager receiver

UAA2080T

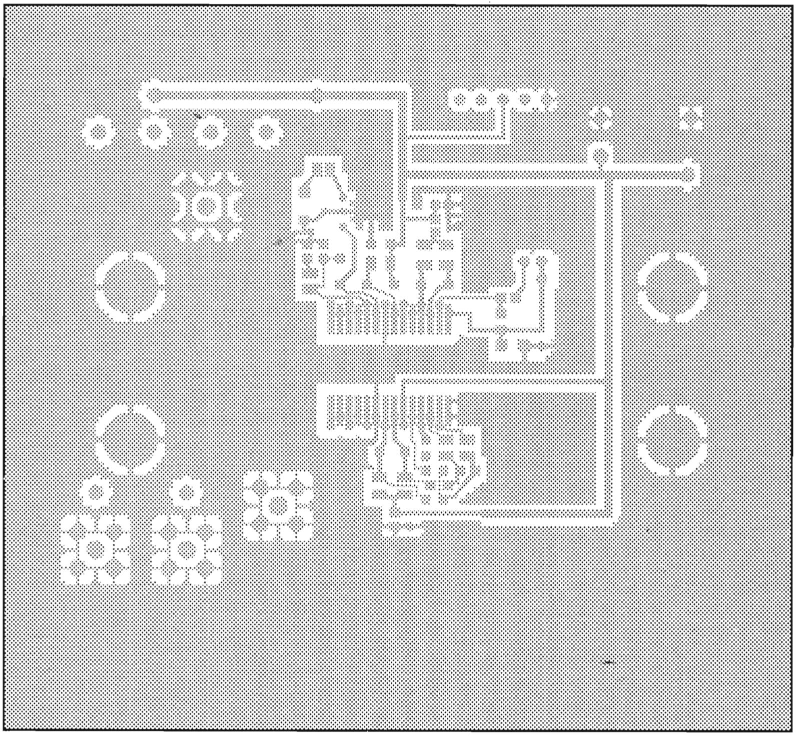


Fig.18 PCB top view for SO28; test circuit Figs 2 and 4.

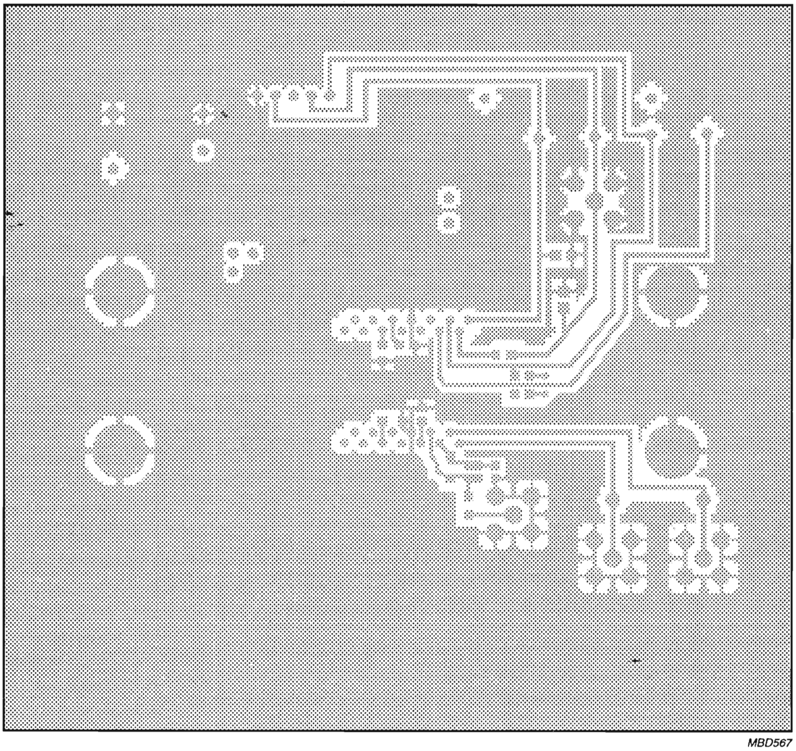
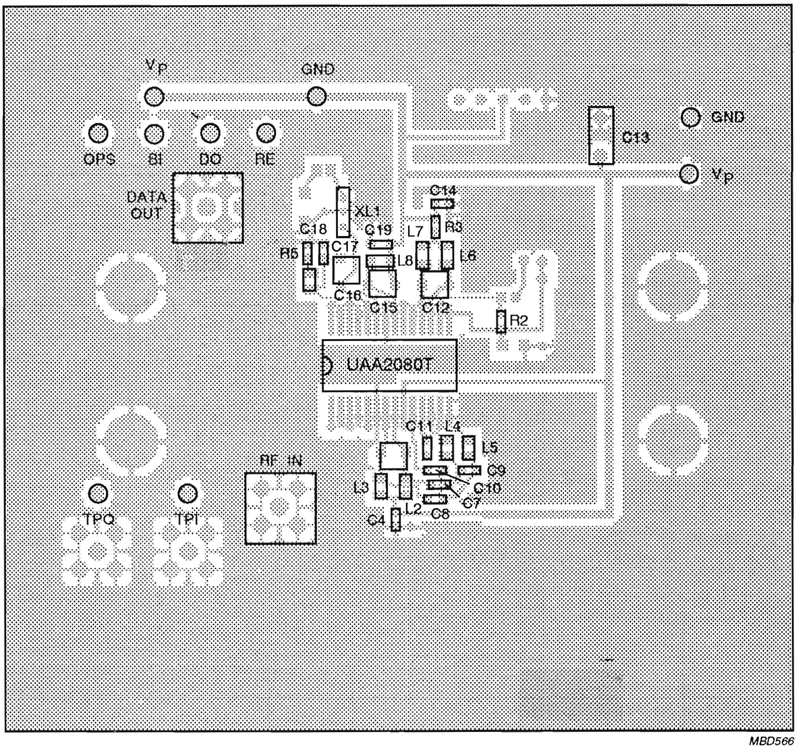


Fig.19 PCB bottom view for SO28; test circuit Figs 2 and 4.



V_{EE} = GND; V_{CC} = V_P; BI = BLI; OPS = TS.

Fig.20 PCB top view with components for SO28; test circuit Fig.4.

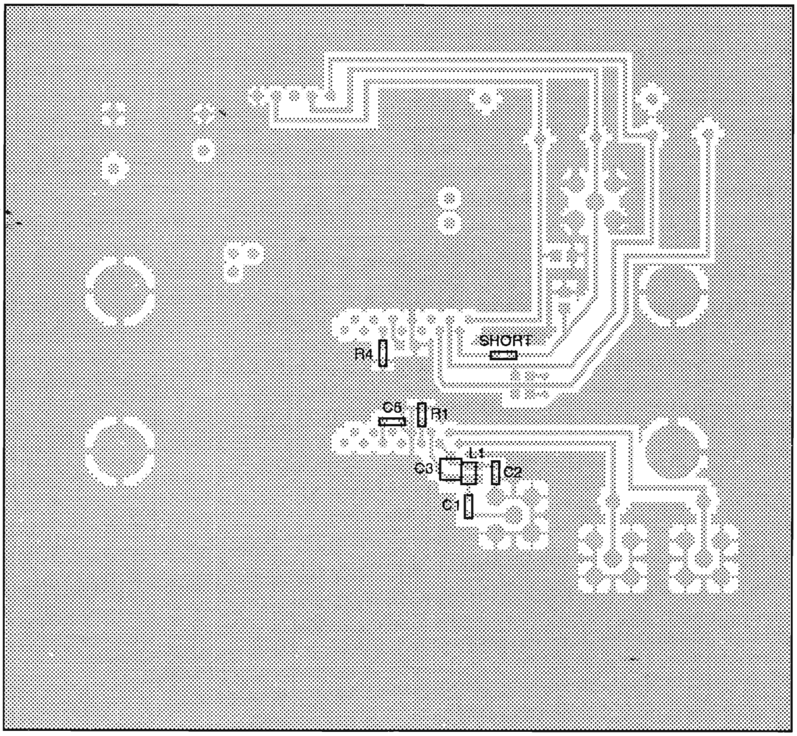


Fig.21 PCB bottom view with components for SO28; test circuit Fig.4.

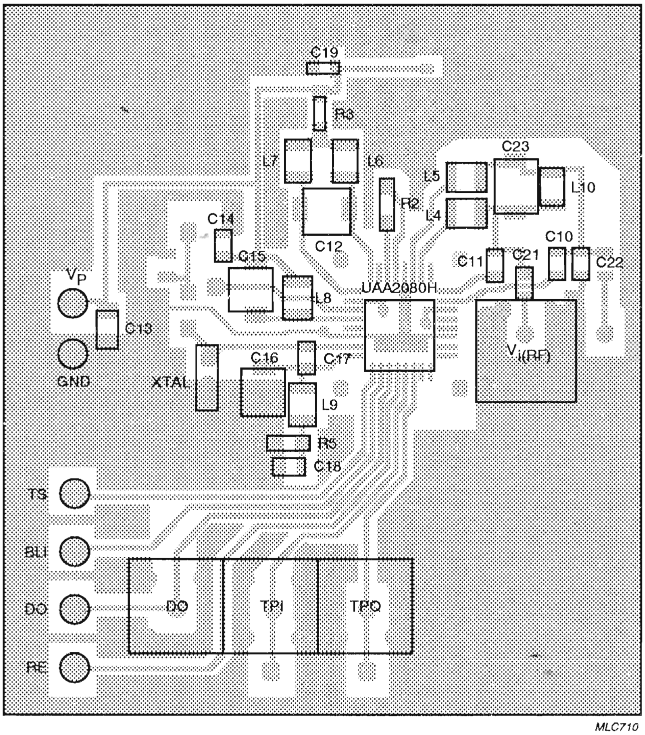


Fig.22 PCB top view with components for TQFP32; test circuit Fig.5.

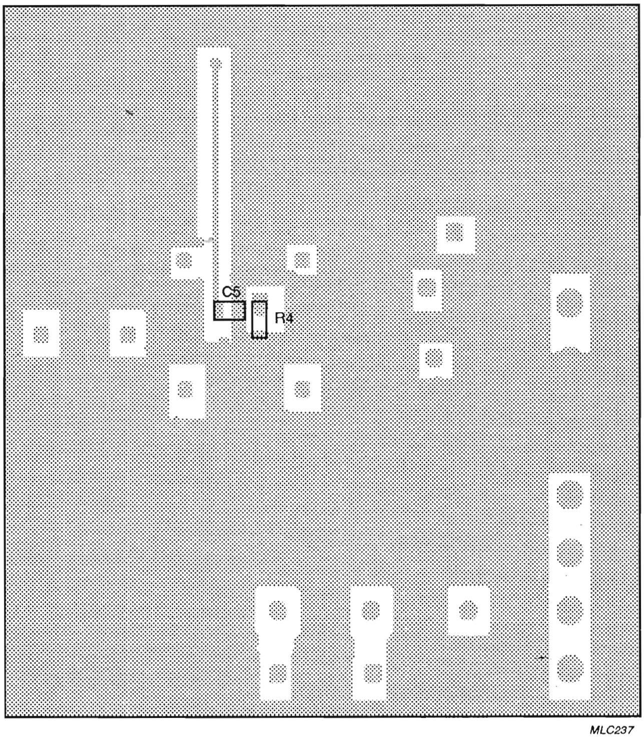


Fig.23 PCB bottom view with components for TQFP32; test circuit Fig.5.

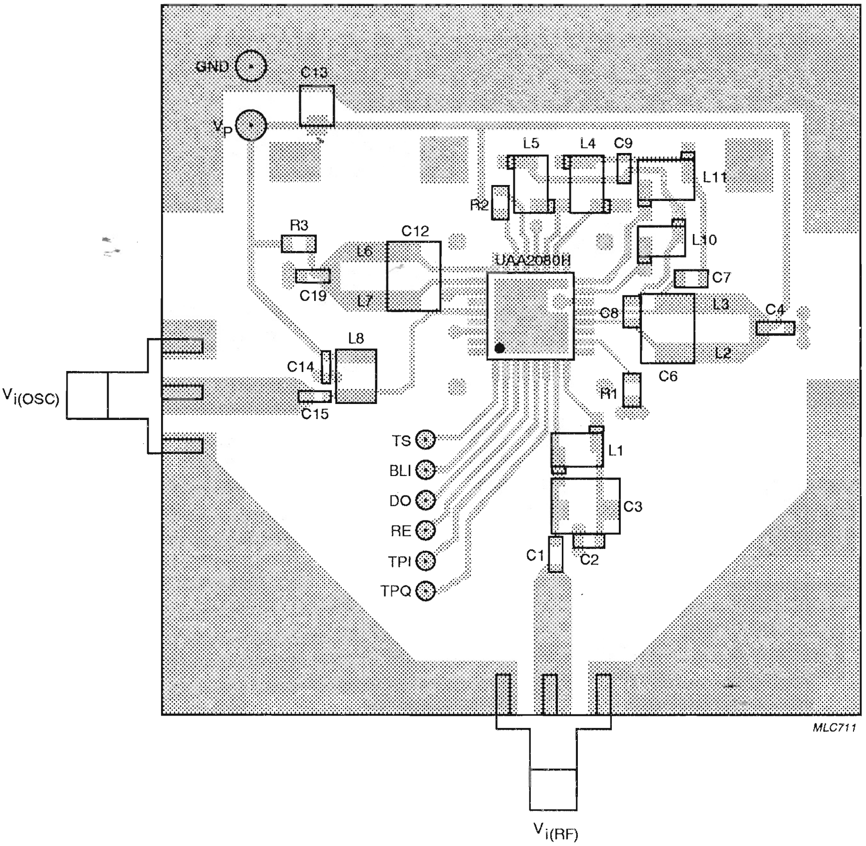


Fig.24 PCB top view with components for TQFP32; test circuit Fig.6.

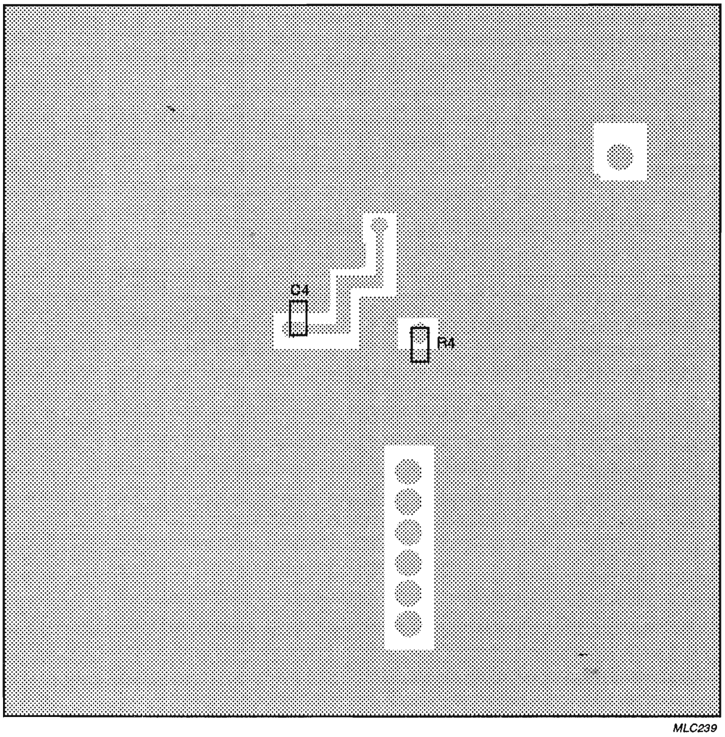


Fig.25 PCB bottom view with components for TQFP32; test circuit Fig.6.

Advanced pager receiver UAA2082

FEATURES

- Wide frequency range: VHF, UHF and 900 MHz bands
- High sensitivity
- High dynamic range
- Electronically adjustable filters on chip
- Suitable for data rates up to 2400 bits/s
- Wide frequency offset and deviation range
- Fully POCSAG compatible FSK receiver
- Power on/off mode selectable by the chip enable input
- Low supply voltage; low power consumption
- 1-cell battery-low detection circuit
- High integration level
- Interfaces directly to the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.

APPLICATIONS

- Wide area paging
- On-site paging
- Telemetry
- RF security systems
- Low bit-rate wireless data links.

GENERAL DESCRIPTION

The UAA2082 is a high-performance low-power radio receiver circuit primarily intended for VHF, UHF and 900 MHz pager receivers for wide area digital paging systems, employing direct FM non-return-to-zero (NRZ) frequency shift keying (FSK).

The receiver design is based on the direct conversion principle where the input signal is mixed directly down to the baseband by a local oscillator on the signal frequency. Two complete signal paths with signals of 90° phase difference are required to demodulate the signal. All channel selectivity is provided by the built-in IF filters. The circuit makes extensive use of on-chip capacitors to minimize the number of external components.

The battery monitoring circuit has an external sense input and a 1.1 V detection threshold for easy operation in a single-cell supply concept.

The UAA2082 was designed to operate together with the PCA5000A, PCF5001 or PCD5003 POCSAG decoders, which contain a digital input filter for optimum call success rate.

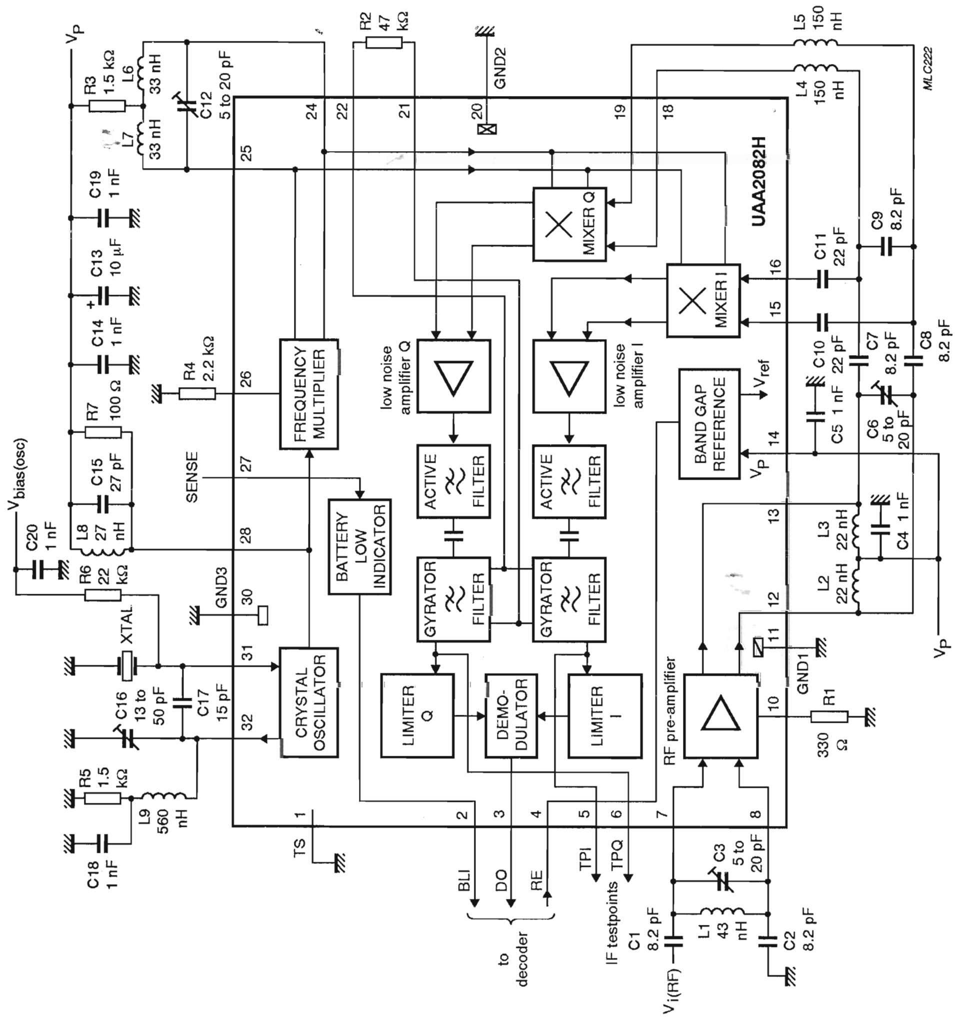
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2082H	TQFP32	plastic thin quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-2
UAA2082U	28 pads	naked die; see Fig.8	

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		1.9	2.05	3.5	V
I_P	supply current		2.3	2.7	3.2	mA
$I_{P(off)}$	stand-by current		–	–	3	μA
$P_{i(ref)}$	RF input sensitivity	BER ≤ $^3/_{100}$; ±4 kHz deviation; data rate 1200 bits/s; T_{amb} = 25 °C				
		$f_{i(RF)}$ = 173 MHz	–	−126.5	−123.5	dBm
		$f_{i(RF)}$ = 470 MHz	–	−124.5	−121.5	dBm
		$f_{i(RF)}$ = 930 MHz	–	−120.0	−114.0	dBm
$P_{i(mix)}$	mixer input sensitivity	BER ≤ $^3/_{100}$; $f_{i(RF)}$ = 470 MHz; ±4 kHz deviation; data rate 1200 bits/s; T_{amb} = 25 °C	–	−115.0	−110.0	dBm
V_{th}	detection threshold for battery LOW indicator	T_{amb} = 25 °C	1.05	1.10	1.15	V
		T_{amb} = −10 to +70 °C	1.03	1.10	1.17	V
T_{amb}	operating ambient temperature		−10	–	+70	°C

BLOCK DIAGRAMS (173 MHz)



Pins 9, 17, 23 and 29 are not connected.

Fig.1 Block, test and application diagram drawn for TQFP32; $f_{i(RF)}$ = 172.941 MHz.

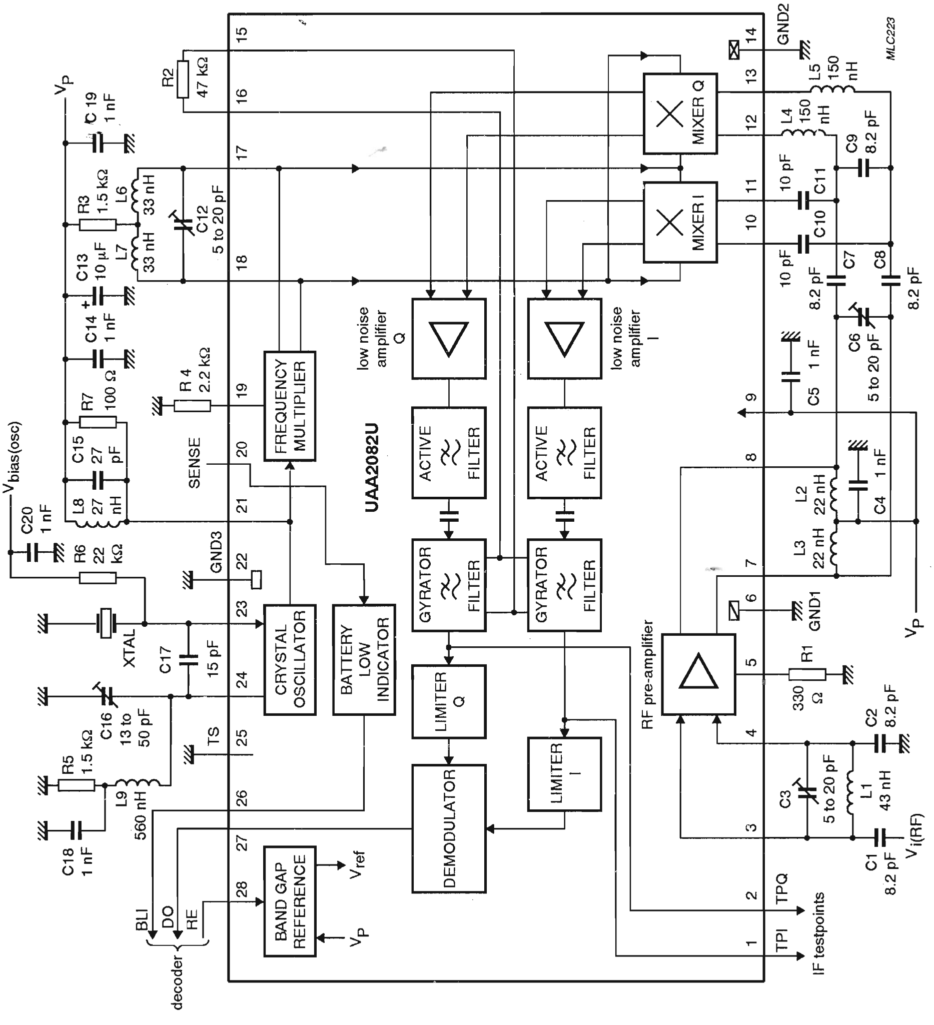


Fig.2 Block, test and application diagram drawn for naked die; $f_{i(RF)} = 172.941$ MHz.

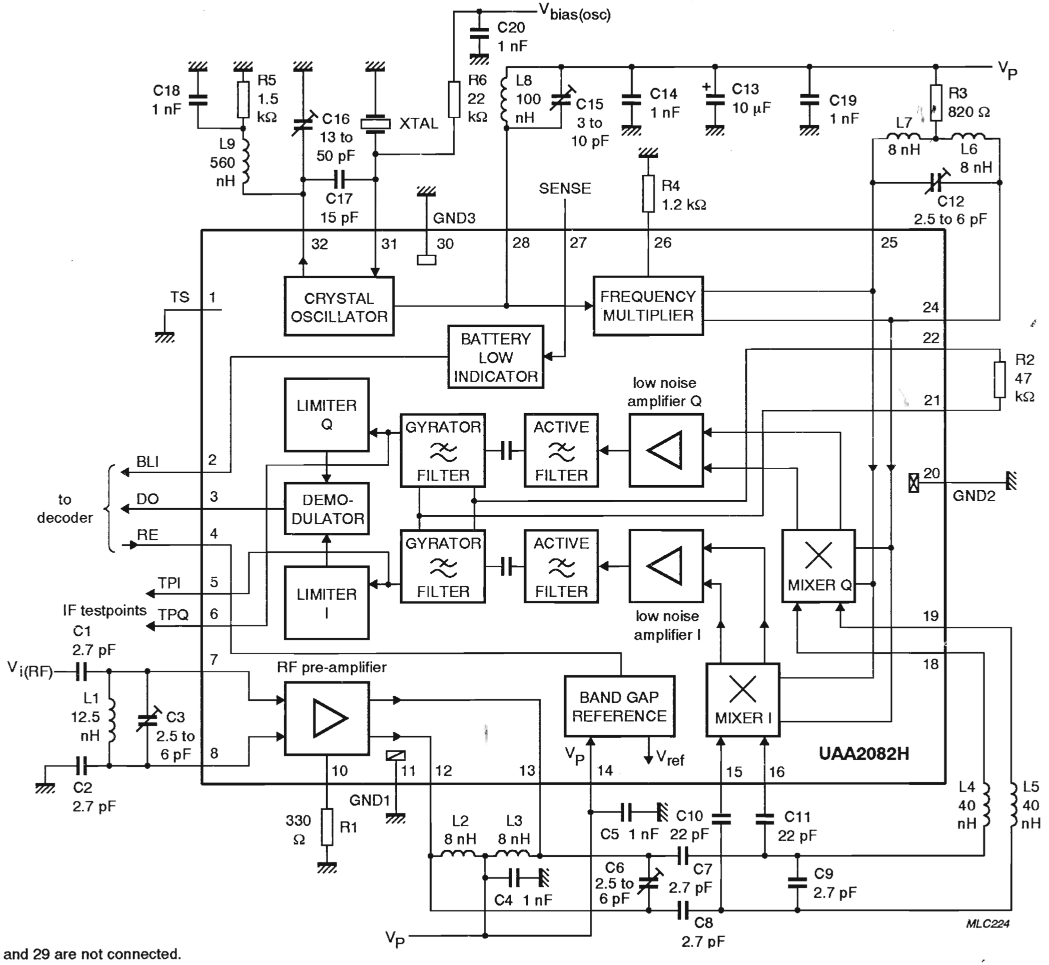
Table 1 Tolerances of components shown in Figs 1 and 2 (notes 1 and 2)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1	±5	Q_{min} = 100 at 173 MHz
L2, L3, L6, L7	±20	Q_{min} = 50 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L4, L5	±10	Q_{min} = 30 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L8	±20	Q_{min} = 30 at 173 MHz; TC = (+25 to +125) × 10^{-6}/K
L9	±10	Q_{min} = 30 at 57 MHz; TC = (+25 to +125) × 10^{-6}/K
Resistors		
R1 to R7	±2	TC = +50 × 10^{-6}/K
Capacitors		
C1, C2, C7, C8, C9, C15	±5	TC = (0 ±30) × 10^{-6}/K; tan $\delta \leq 30 \times 10^{-4}$ at 1 MHz
C3, C6, C12	–	TC = (−750 ±300) × 10^{-6}/K; tan $\delta \leq 50 \times 10^{-4}$ at 1 MHz
C4, C5, C14, C18, C19, C20	±10	TC = (0 ±30) × 10^{-6}/K; tan $\delta \leq 10 \times 10^{-4}$ at 1 MHz
C10, C11	±5	TC = (0 ±30) × 10^{-6}/K; tan $\delta \leq 21 \times 10^{-4}$ at 1 MHz
C13	±20	
C16	–	TC = (−1 700 ±500) × 10^{-6}/K; tan $\delta \leq 50 \times 10^{-4}$ at 1 MHz
C17	±5	TC = (0 ±30) × 10^{-6}/K; tan $\delta \leq 26 \times 10^{-4}$ at 1 MHz

Notes

1. Recommended crystal: f_{XTAL} = 57.647 MHz (crystal with 8 pF load), 3rd overtone, pullability >2.75 × 10^{-6}/pF (change in frequency between series resonance and resonance with 8 pF series capacitor at 25 °C), dynamic resistance R1 < 40 Ω, Δf = ±5 × 10^{-6} for T_{amb} = −10 to +55 °C with 25 °C reference, calibration plus aging tolerance: −5 × 10^{-6} to +15 × 10^{-6}.
2. This crystal recommendation is based on economic aspects and practical experience. Normally the spreads for R1, pullability and calibration do not show their worst case limits simultaneously in one crystal. In such a rare event, the tuning range will be reduced to an insufficient level.

BLOCK AND TEST DIAGRAMS (470 MHz)



Pins 9, 17, 23 and 29 are not connected.

Fig.3 Block, test and application diagram drawn for TQFP32; $f_{i(RF)}$ = 469.95 MHz.

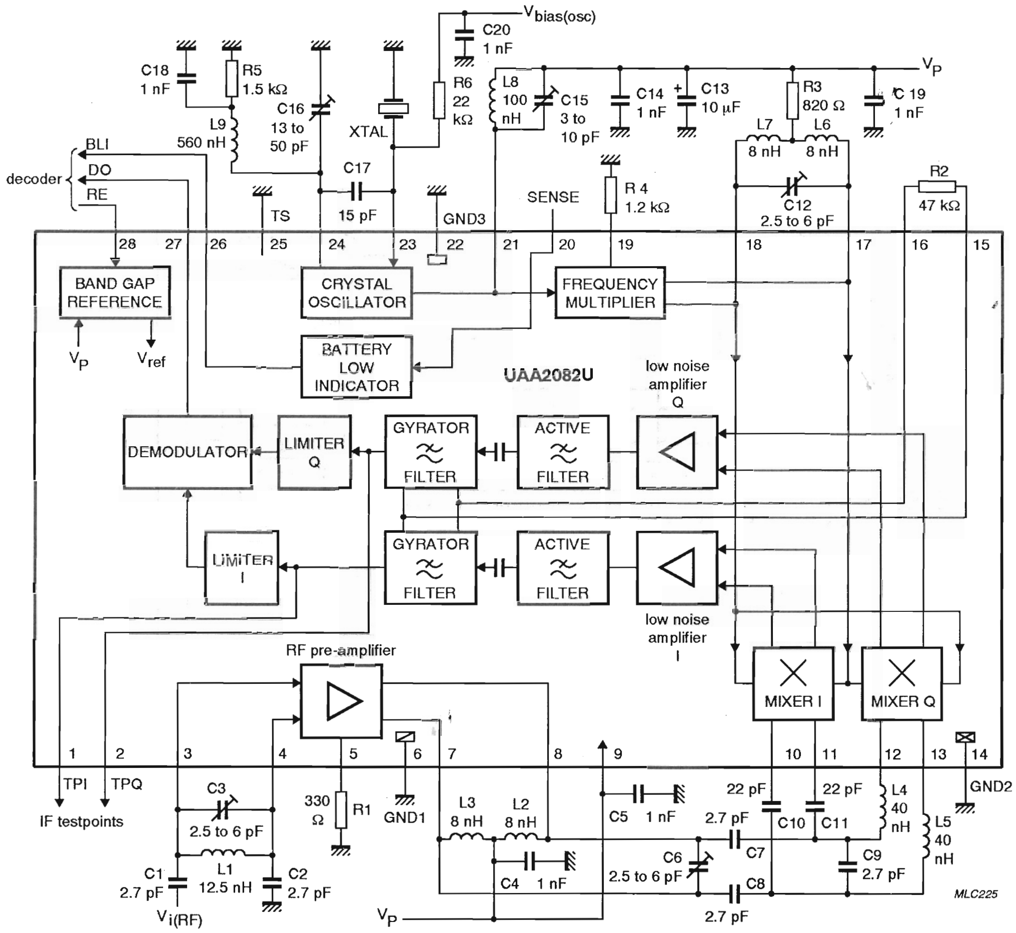


Fig.4 Block, test and application diagram drawn for naked die; $f_{i(RF)}$ = 469.95 MHz.

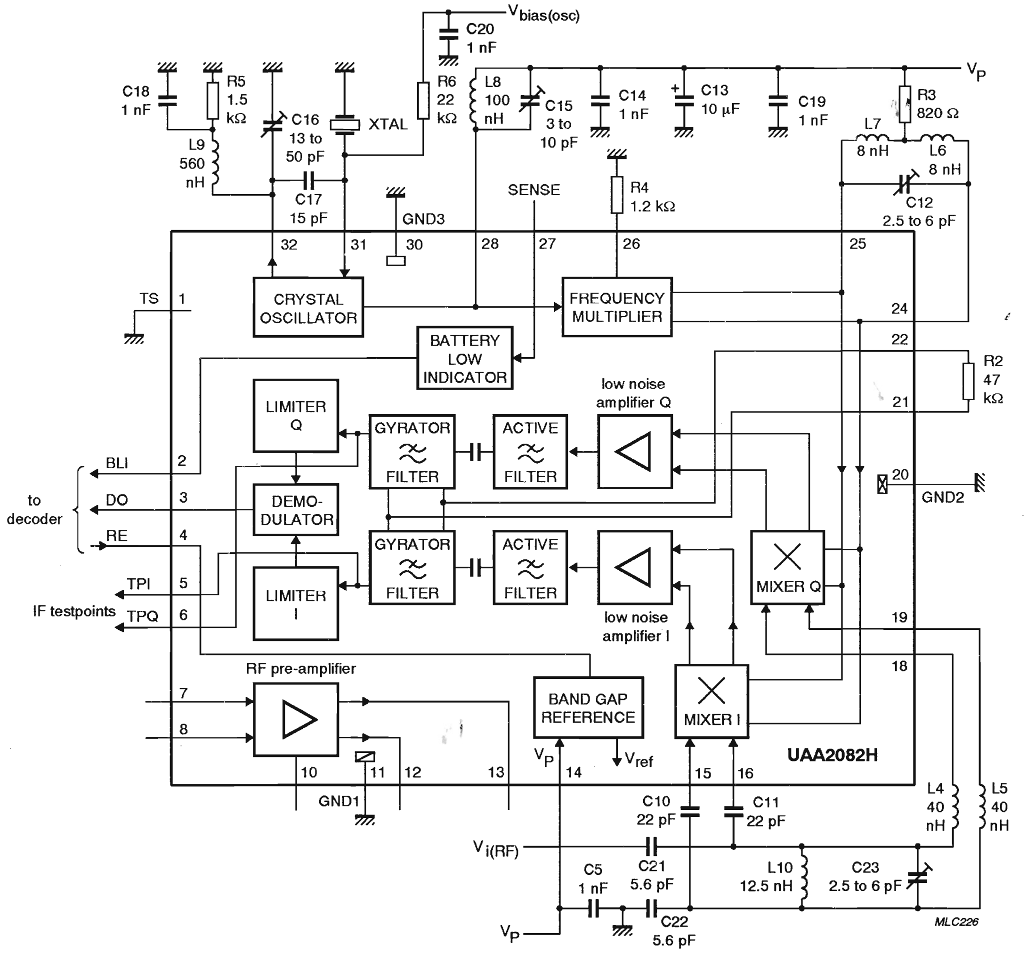


Fig.5 Mixer input sensitivity test circuit; $f_{i(RF)}$ = 469.95 MHz.

Table 2 Tolerances of components shown in Figs 3, 4 and 5 (notes 1 and 2)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1, L10	±5	Q_{min} = 145 at 470 MHz
L2, L3, L6, L7	±20	Q_{min} = 50 at 470 MHz; TC = (+25 to +125) × 10^{-6}/K
L4, L5	±10	Q_{min} = 40 at 470 MHz; TC = (+25 to +125) × 10^{-6}/K
L8	±10	Q_{min} = 30 at 156 MHz; TC = (+25 to +125) × 10^{-6}/K
L9	±10	Q_{min} = 40 at 78 MHz; TC = (+25 to +125) × 10^{-6}/K
Resistors		
R1 to R6	±2	TC = +50 × 10^{-6}/K
Capacitors		
C1, C2, C7, C8, C9	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 30 × 10^{-4} at 1 MHz
C3, C6, C12, C23	–	TC = (−750 ±300) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C4, C5, C14, C18 to C22	±10	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 10 × 10^{-4} at 1 MHz
C10, C11	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 21 × 10^{-4} at 1 MHz
C13	±20	
C16	–	TC = (−1700 ±500) × 10^{-6}/K; tan δ ≤ 50 × 10^{-4} at 1 MHz
C17	±5	TC = (0 ±30) × 10^{-6}/K; tan δ ≤ 26 × 10^{-4} at 1 MHz

Notes

1. Recommended crystal: f_{XTAL} = 78.325 MHz (crystal with 8 pF load), 3rd overtone, pullability >2.75 × 10^{-6}/pF (change in frequency between series resonance and resonance with 8 pF capacitor at 25 °C), dynamic resistance R1 < 30 Ω, Δf = ±5 × 10^{-6} for T_{amb} = −10 to +55 °C with 25 °C reference, calibration plus aging tolerance: −5 × 10^{-6} to +15 × 10^{-6}.
2. This crystal recommendation is based on economic aspects and practical experience. Normally the spreads for R1, pullability and calibration do not show their worst case limits simultaneously in one crystal. In such a rare event, the tuning range will be reduced to an insufficient level.

BLOCK AND TEST DIAGRAM (930 MHz)

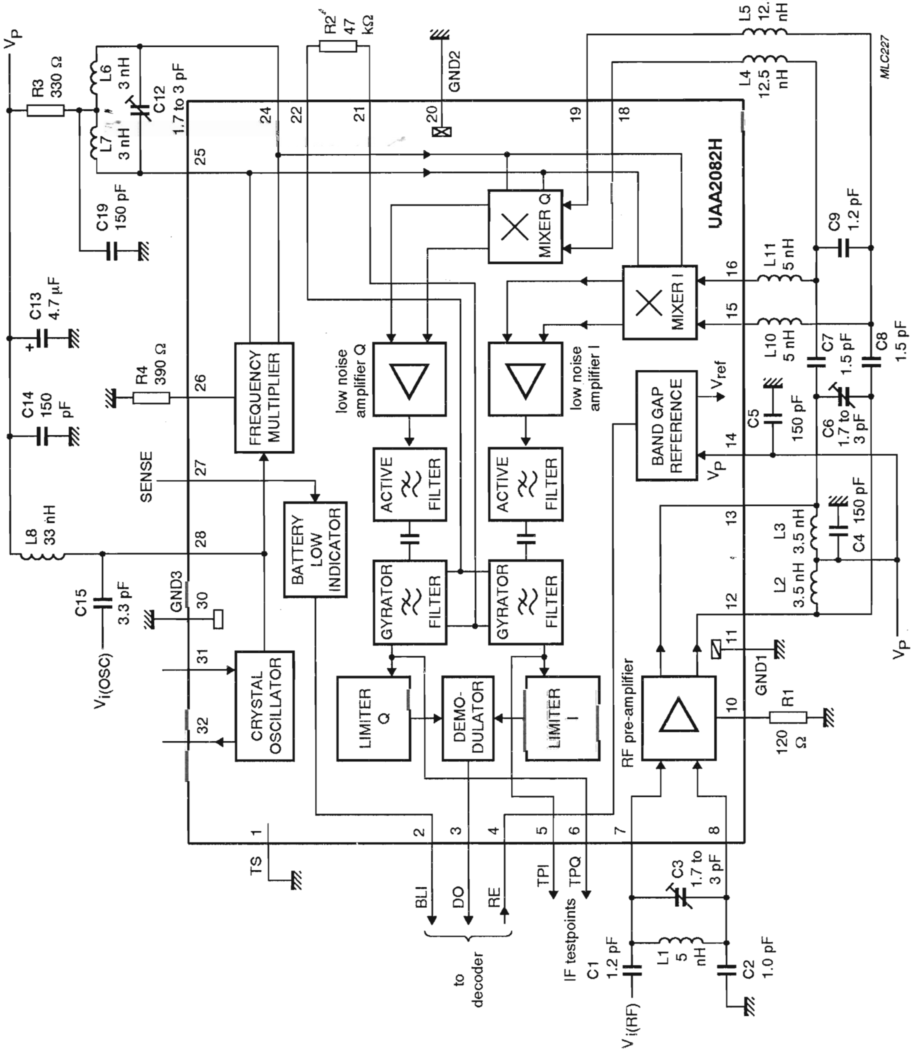


Fig.6 Test circuit; $f_{i(RF)}$ = 930.50 MHz.

Pins 9, 17, 23 and 29 are not connected.

Table 3 Tolerances of components shown in Fig.6 (note 1)

COMPONENT	TOLERANCE (%)	REMARK
Inductances		
L1	±10	Q_{typ} = 150 at 930 MHz
L2, L3, L6, L7	–	microstrip inductor
L4, L5	±5	Q_{typ} = 100 at 930 MHz
L8	±10	Q_{typ} = 65 at 310 MHz
L10, L11	±10	Q_{typ} = 150 at 930 MHz
Resistors		
R1 to R4	±2	TC = (0 ±200) × 10^{-6}/K;
Capacitors		
C1, C2, C7, C8, C9, C15	±5	TC = (0 ±30) × 10^{-6}/K; tan $\delta \leq 30 \times 10^{-4}$ at 1 MHz
C3, C6, C12	–	TC = (0 ±200) × 10^{-6}/K; tan $\delta \leq 30 \times 10^{-4}$ at 1 MHz
C4, C5, C14, C19	±10	TC = (0 ±30) × 10^{-6}/K; tan $\delta \leq 10 \times 10^{-4}$ at 1 MHz
C13	±20	

Note

1. The external oscillator signal $V_{i(OSC)}$ has a frequency of f_{OSC} = 310.1 667 MHz.

PINNING (TQFP32)

SYMBOL	PIN	DESCRIPTION
TS	1	test switch; connection to ground for normal operation
BLI	2	battery LOW indicator output
DO	3	data output
RE	4	receiver enable input
TPI	5	IF test point; I channel
TPQ	6	IF test point; Q channel
VI1RF	7	pre-amplifier RF input 1
VI2RF	8	pre-amplifier RF input 2
n.c.	9	not connected
RRFA	10	external emitter resistor for pre-amplifier
GND1	11	ground 1 (0 V)
VO2RF	12	pre-amplifier RF output 2
VO1RF	13	pre-amplifier RF output 1
V_P	14	supply voltage
VI2MI	15	I channel mixer input 2
VI1MI	16	I channel mixer input 1
n.c.	17	not connected
VI1MQ	18	Q channel mixer input 1
VI2MQ	19	Q channel mixer input 2
GND2	20	ground 2 (0 V)
COM	21	gyrator filter resistor; common line
RGYR	22	gyrator filter resistor
n.c.	23	not connected
VO1MUL	24	frequency multiplier output 1
VO2MUL	25	frequency multiplier output 2
RMUL	26	external emitter resistor for frequency multiplier
SENSE	27	battery LOW detector sense input
OSC	28	oscillator collector
n.c.	29	not connected
GND3	30	ground 3 (0 V)
OSB	31	oscillator base; crystal input
OSE	32	oscillator emitter

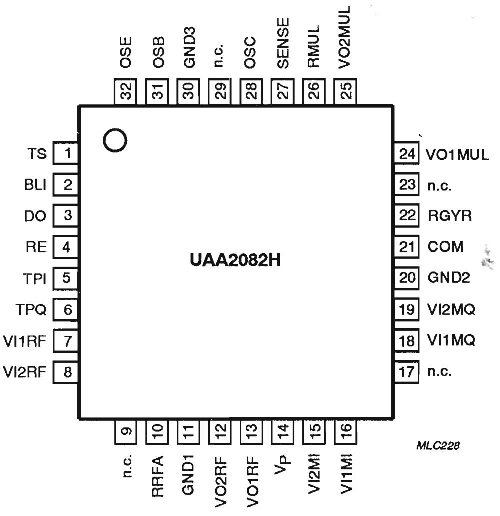
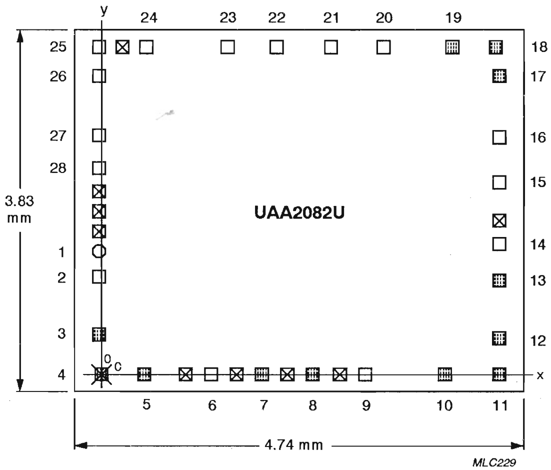


Fig.7 Pin configuration; TQFP32.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

See Table 4 for bonding pad description and locations for x/y co-ordinates.



Where:

- ○ Pad number 1 (diameter 124 μm)
- □ Pad 124 μm x 124 μm
- ☒ Pad not used
- ▦ Pad 100 μm x 100 μm
- ⊠ Pad 100 μm x 100 μm with reference point

Chip area: 18.15 mm^2.
Chip thickness: 380 ±20 μm.
Drawing not to scale.

Fig.8 Bonding pad locations.

Table 4 Bonding pad centre locations (dimensions in μm)

SYMBOL	PAD	DESCRIPTION	x	y
TPI	1	IF test point; I channel	–32	1296
TPQ	2	IF test point; Q channel	–32	1000
VI1RF	3	pre-amplifier RF input 1	–32	360
VI2RF	4	pre-amplifier RF input 2; note 1	0	0
RRFA	5	external emitter resistor for pre-amplifier	472	0
GND1	6	ground 1 (0 V)	1160	0
VO2RF	7	pre-amplifier RF output 2	1688	0
VO1RF	8	pre-amplifier RF output 1	2232	0
V_P	9	supply voltage	2760	0
VI2MI	10	I channel mixer input 2	3608	0
VI1MI	11	I channel mixer input 1	4216	0
VI1MQ	12	Q channel mixer input 1	4216	360
VI2MQ	13	Q channel mixer input 2	4216	960
GND2	14	ground 2 (0 V)	4216	1360
COM	15	gyrator filter resistor; common line	4216	2024
RGYR	16	gyrator filter resistor	4216	2496
VO1MUL	17	frequency multiplier output 1	4216	3136
VO2MUL	18	frequency multiplier output 2	4176	3456
RMUL	19	external emitter resistor for frequency multiplier	3668	3458
SENSE	20	battery LOW detector sense input	2952	3456
OSC	21	oscillator collector	2312	3456
GND3	22	ground 3 (0 V)	1832	3456
OSB	23	oscillator base; crystal input	1328	3456
OSE	24	oscillator emitter	432	3456
TS	25	test switch; connection to ground for normal operation	–32	3456
BLI	26	battery LOW indicator output	–32	3136
DO	27	data output	–32	2512
RE	28	receiver enable input	–32	2152
		lower left corner of chip (typical values)	–278	–186

Note

1. All x/y co-ordinates are referenced to the centre of pad 4 (VI2RF); see Fig.8.

INTERNAL CIRCUITS

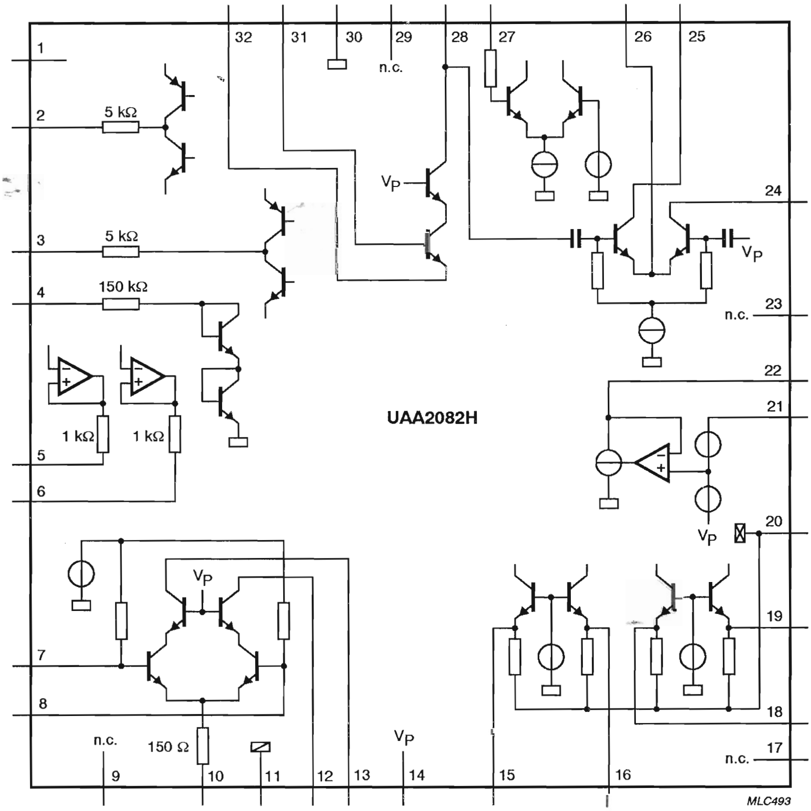


Fig.9 Internal circuits drawn for TQFP32.

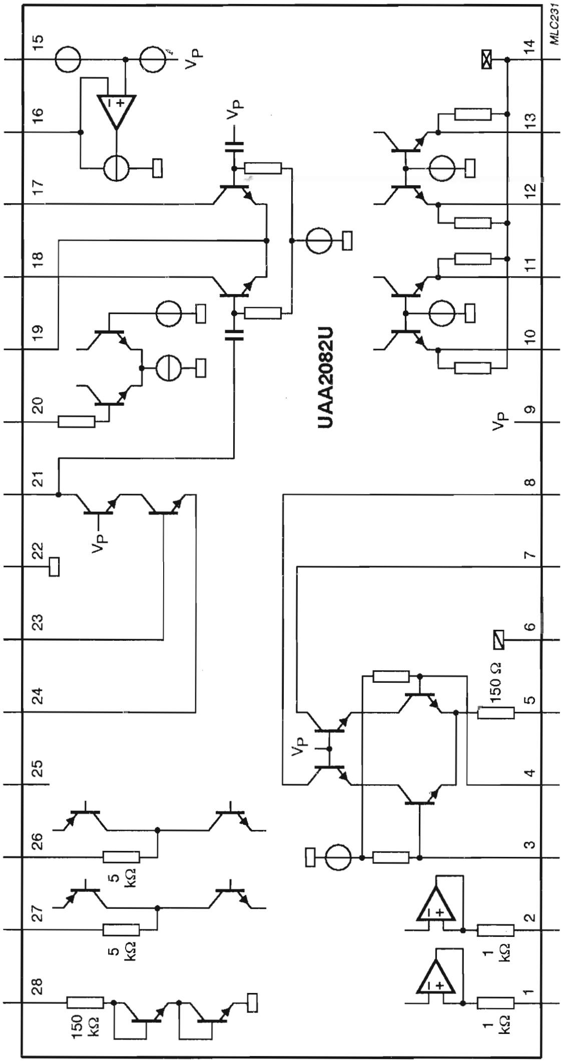


Fig.10 Internal circuits drawn for naked die.

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Figs 1 to 6.

Radio frequency amplifier

The RF amplifier is an emitter-coupled pair driving a balanced cascode stage, which drives an external balanced tuned circuit. Its bias current is set by an external 300 Ω resistor R1 to typically 770 μA. With this bias current the optimum source resistance is 1.3 kΩ at VHF and 1.0 kΩ at UHF. At 930 MHz a higher bias current is required to achieve optimum gain. A value of 120 Ω is used for R1, which corresponds with a bias current of approximately 1.3 mA and an optimum source resistance of approximately 600 Ω.The capacitors C1 and C2 transform a 50 Ω source resistance to this optimum value. The output drives a tuned circuit with capacitive divider (C7, C8 and C9) to provide maximum power transfer to the phase-splitting network and the mixers.

Mixers

The double balanced mixers consist of common base input stages and upper switching stages driven from the frequency multiplier. The 300 Ω input impedance of each mixer acts together with external components (C10, C11; L4, L5 respectively) as phase shifter/power splitter to provide a differential phase shift of 90 degrees between the I channel and the Q channel. At 930 MHz all external phase shifter components are inductive (L10, L11; L4, L5).

Oscillator

The oscillator is based on a transistor in common collector configuration. It is followed by a cascode stage driving a tuned circuit which provides the signal for the frequency multiplier. The oscillator transistor requires an external bias voltage $V_{bias(osc)}$ (1.22 V typ.). The oscillator bias current (typically 250 μA) is determined by the 1.5 kΩ external resistor R5. The oscillator frequency is controlled by an external 3rd overtone crystal in parallel resonance mode. External capacitors between base and emitter (C17) and from emitter to ground (C16) make the oscillator transistor appear as having a negative resistance for small signals; this causes the oscillator to start. Inductance L9 connected in parallel with capacitor C16 to the emitter of the oscillator transistor prevents oscillation at the fundamental frequency of the crystal.

The resonant circuit at output pin OSC selects the second harmonic of the oscillator frequency. In other applications a different multiplication factor may be chosen.

At 930 MHz an external oscillator circuit is required to provide sufficient local oscillator signal for the frequency multiplier.

Frequency multiplier

The frequency multiplier is an emitter-coupled pair driving an external balanced tuned circuit. Its bias current is set by external resistor R4 to typically 190 μA (173 MHz), 350 μA (470 MHz) and 1 mA (930 MHz). The oscillator signal is internally AC coupled to one input of the emitter-coupled pair while the other input is internally grounded via a capacitor. The frequency multiplier output signal between pins VO1MUL and VO2MUL drives the upper switching stages of the mixers. The bias voltage on pins VO1MUL and VO2MUL is set by external resistor R3 to allow sufficient voltage swing at the mixer outputs. The value of R3 depends on the operating frequency: 1.5 kΩ (173 MHz), 820 Ω (470 MHz) and 330 Ω (930 MHz).

Low noise amplifiers, active filters and gyrator filters

The low noise amplifiers ensure that the noise of the following stages does not affect the overall noise figure. The following active filters before the gyrator filters reduce the levels of large signals from adjacent channels. Internal AC couplings block DC offsets from the gyrator filter inputs.

The gyrator filters implement the transfer function of a 7th order elliptic filter. Their cut-off frequencies are determined by the 47 kΩ external resistor R2 between pins RGYR and COM. The gyrator filter output signals are available on IF test pins TPI and TPQ.

Limiters

The gyrator filter output signals are amplified in the limiter amplifiers to obtain IF signals with removed amplitude information.

Demodulator

The limiter amplifier output signals are fed to the demodulator. The demodulator output DO is going LOW or HIGH depending upon which of the input signals has a phase lead.

Battery LOW indicator

The battery LOW indicator senses the supply voltage and sets its output HIGH when the voltage at input SENSE is less than V_{th} (typically 1.10 V). Low battery warning is available at BLI.

Band gap reference

The whole chip except the oscillator section can be powered-up and powered-down by enabling and disabling the band gap reference via the receiver enable pin RE.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).
Ground pins GND1, GND2 and GND3 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	−0.3	+8.0	V
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−10	+70	°C
V_{es}	electrostatic handling (note 1)			
	pins VI1RF and VI2RF	−1500	+2000	V
	pin RRFA	−500	+2000	V
	pins VO1RF and VO2RF	−2000	+250	V
	pins V_P and OSB	−500	+500	V
	pins OSC and OSE	−2000	+500	V
	other pins	−2000	+2000	V

Note

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor.

DC CHARACTERISTICS

V_P = 2.05 V; T_{amb} = −10 to +70 °C (typical values at T_{amb} = 25 °C); measurements taken in test circuit Fig.1, 2, 3 or 4 with crystal at pin OSB disconnected; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		1.9	2.05	3.5	V
I_P	supply current	V_{RE} = HIGH; $f_{i(RF)}$ = 173 and 470 MHz	2.3	2.7	3.2	mA
		V_{RE} = HIGH; $f_{i(RF)}$ = 930 MHz	2.9	3.4	3.9	mA
$I_{P(off)}$	stand-by current	V_{RE} = LOW	–	–	3	μA
$V_{bias(osc)}$	oscillator bias voltage		1.20	1.22	1.24	V
Receiver enable input (pin RE)						
V_{IH}	HIGH level input voltage		1.4	–	V_P	V
V_{IL}	LOW level input voltage		0	–	0.3	V
I_{IH}	HIGH level input current	$V_{IH} = V_P$ = 3.5 V	–	–	20	μA
V_{IL}	LOW level input current	V_{IL} = 0 V	0	–	−1.0	μA
Battery LOW indicator output (pin BLI)						
V_{OH}	HIGH level output voltage	$V_{SENSE} < V_{th}$; I_{BLI} = −10 μA	V_P − 0.5	–	–	V
V_{OL}	LOW level output voltage	$V_{SENSE} > V_{th}$; I_{BLI} = +10 μA	–	–	0.5	V
V_{th}	voltage threshold for battery LOW indicator	V_P = 2.05 V; T_{amb} = 25 °C	1.05	1.10	1.15	V
		V_P = 2.05 to 3.5 V; T_{amb} = −10 to +70 °C	1.03	1.10	1.17	V
Demodulator output (pin DO)						
V_{OH}	HIGH level output voltage	I_{DO} = −10 μA	V_P − 0.5	–	–	V
V_{OL}	LOW level output voltage	I_{DO} = +10 μA	–	–	0.5	V

AC CHARACTERISTICS (173 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Fig.1 or 2; $f_{i(RF)}$ = 172.941 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ±25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 1	–	–126.5	–123.5	dBm
		T_{amb} = –10 to +70 °C; note 2	–	–	–120.5	dBm
		V_P = 1.9 V	–	–	–117.5	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	69	72	–	dB
		T_{amb} = –10 to +70 °C	67	–	–	dB
α_{ci}	IF filter channel imbalance		–	–	2	dB
α_c	co-channel rejection		–	4	7	dB
α_{sp}	spurious immunity		50	60	–	dB
α_{im}	intermodulation immunity		55	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 3	78	85	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 4	–	–	5	ms

Notes

1. The bit error rate BER is measured using the test facility shown in Fig.12. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
2. Capacitor C16 requires re-adjustment to compensate temperature drift.
3. Δf is the frequency offset between the required signal and the interfering signal.
4. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

AC CHARACTERISTICS (470 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Fig.3 or 4; $f_{i(RF)}$ = 469.950 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ± 25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ $^3/_{100}$; note 1	–	–124.5	–121.5	dBm
		T_{amb} = –10 to +70 °C; note 2	–	–	–118.5	dBm
		V_P = 1.9 V	–	–	–115.5	dBm
Mixer input						
$P_{i(mix)}$	input sensitivity	BER ≤ $^3/_{100}$; note 3	–	–115.0	–110.0	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	67	70	–	dB
		T_{amb} = –10 to +70 °C	65	–	–	dB
α_{ci}	IF filter channel imbalance		–	–	2	dB
α_c	co-channel rejection		–	4	7	dB
α_{sp}	spurious immunity		50	60	–	dB
α_{im}	intermodulation immunity		55	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 4	75	82	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 5	–	–	5	ms

Notes

1. The bit error rate BER is measured using the test facility shown in Fig.12. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
2. Capacitor C16 requires re-adjustment to compensate temperature drift.
3. Test circuit Fig.5. $P_{i(mix)}$ is the maximum available power at the input of the test board. The bit error rate BER is measured using the test facility shown in Fig.12.
4. Δf is the frequency offset between the required signal and the interfering signal.
5. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

AC CHARACTERISTICS (930 MHz)

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Fig.6 (note 1); $f_{i(RF)}$ = 930.500 MHz with ±4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ± 25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i(ref)}$	input sensitivity ($P_{i(ref)}$ is the maximum available power at the RF input of the test board)	BER ≤ 3/100; note 2	–	–120.0	–114.0	dBm
		V_P = 1.9 V	–	–	–108.0	dBm
Mixers to demodulator						
α_{acs}	adjacent channel selectivity	T_{amb} = 25 °C	60	69	–	dB
α_c	co-channel rejection		–	5	10	dB
α_{sp}	spurious immunity		40	60	–	dB
α_{im}	intermodulation immunity		53	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 3	65	74	–	dB
f_{offset}	frequency offset range (3 dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2.0	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 4	–	–	5	ms

Notes

1. The external oscillator signal $V_{i(OSC)}$ has a frequency of f_{OSC} = 310.1667 MHz and a level of –15 dBm.
2. The bit error rate BER is measured using the test facility shown in Fig.12. Note that the BER test facility contains a digital input filter equivalent to the one used in the PCA5000A, PCF5001 and PCD5003 POCSAG decoders.
3. Δf is the frequency offset between the required signal and the interfering signal.
4. Turn-on time is defined as the time from pin RE going HIGH to the reception of valid data on output pin DO. Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

TEST INFORMATION

Tuning procedure for AC tests

1. Turn on the signal generator: $f_{gen} = f_{i(RF)} + 4$ kHz, no modulation, $V_{i(RF)} = 1$ mV (RMS).
2. Measure the IF with a counter connected to test pin TPI. Tune C16 to set the crystal oscillator to achieve $f_{IF} = 4$ kHz Change the generator frequency to $f_{gen} = f_{i(RF)} - 4$ kHz and check that f_{IF} is also 4 kHz. For a received input frequency $f_{i(RF)} = 172.941$ MHz the crystal frequency is $f_{XTAL} = 57.647$ MHz, while for $f_{i(RF)} = 469.950$ MHz the crystal frequency is $f_{XTAL} = 78.325$ MHz. For a received input frequency $f_{i(RF)} = 930.500$ MHz an external oscillator signal must be used with $f_{i(OSC)} = 310.1667$ MHz and a level of −15 dBm (for definition of crystal frequency, see Table 1).
3. Set the signal generator to nominal frequency ($f_{i(RF)}$) and turn on the modulation deviation ±4.0 kHz, 600 Hz square wave modulation, $V_{i(RF)} = 1$ mV (RMS). Note that the RF signal should be reduced in the following tests, as the receiver is tuned, to ensure $V_{o(IF)} = 10$ to 50 mV (p-p) on test pins TPI or TPQ.
4. Tune C15 (oscillator output circuit) and C12 (frequency multiplier output) to obtain a peak audio voltage on pin TPI.
5. Tune C3 and C6 (RF input and mixer input) to obtain a peak audio voltage on pin TPI. When testing the mixer input sensitivity tune C23 instead of C3 and C6 (test circuit Fig.5).
6. Check that the output signal on pin TPQ is within 3 dB in amplitude and at 90° (±20°) relative phase of the signal on pin TPI.
7. Check that data signal appears on output pin DO and proceed with the AC test.

AC test conditions

Table 5 Definitions for AC test conditions (see Table 6)

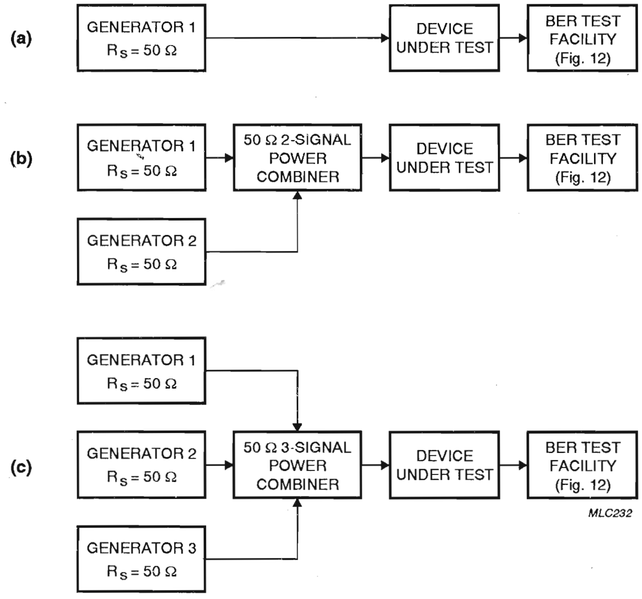
SIGNAL	DESCRIPTION
Modulated test signal 1	
Frequency	172.941, 469.950 or 930.500 MHz
Deviation	±4.0 kHz
Modulation	1200 baud pseudo random bit sequence
Rise time	250 ±25 μs (between 10% and 90% of final value)
Modulated test signal 2	
Deviation	±2.4 kHz
Modulation	400 Hz sine wave
Other definitions	
f_1	frequency of signal generator 1
f_2	frequency of signal generator 2
f_3	frequency of signal generator 3
Δf_{cs}	channel spacing (20 kHz)
P_1	maximum available power from signal generator 1 at the test board input
P_2	maximum available power from signal generator 2 at the test board input
P_3	maximum available power from signal generator 3 at the test board input
$P_{i(ref)}$	maximum available power at the test board input to give a Bit Error Rate (BER) ≤ $^3/_{100}$ for the modulated test signal 1, in the absence of interfering signals and under the conditions as specified in Chapters “AC characteristics (173 MHz)”, “AC characteristics (470 MHz)” and “AC characteristics (930 MHz)”

Table 6 AC test conditions (notes 1 and 2)

SYMBOL	PARAMETER	CONDITIONS	TEST SIGNALS
α_a	adjacent channel selectivity; Fig.11 (b)	$f_2 = f_1 \pm \Delta f_{CS}$ generator 1: modulated test signal 1 generator 2: modulated test signal 2	 $P_1 = P_{i(ref)} + 3$ dB $P_2 = P_1 + \alpha_{a(min)}$
α_c	co-channel rejection; Fig.11 (b)	$f_2 = f_1 \pm$ up to 3 kHz generator 1: modulated test signal 1 generator 2: modulated test signal 2	 $P_1 = P_{i(ref)} + 3$ dB $P_2 = P_1 - \alpha_{c(max)}$
α_{sp}	spurious immunity; Fig.11 (b)	$f_2 = 100$ kHz to 2 GHz generator 1: modulated test signal 1 generator 2: modulated test signal 2	 $P_1 = P_{i(ref)} + 3$ dB $P_2 = P_1 + \alpha_{sp(min)}$
α_{im}	intermodulation immunity; Fig.11 (c)	$f_2 = f_1 \pm \Delta f_{cs}$; $f_3 = f_1 \pm 2\Delta f_{cs}$ generator 1: modulated test signal 1 generator 2: unmodulated generator 3: modulated test signal 2	 $P_1 = P_{i(ref)} + 3$ dB $P_2 = P_1 + \alpha_{im(min)}$ $P_3 = P_2$
α_{bl}	blocking immunity; Fig.11 (b)	$f_2 = f_1 \pm 1$ MHz generator 1: modulated test signal 1 generator 2: modulated test signal 2	 $P_1 = P_{i(ref)} + 3$ dB $P_2 = P_1 + \alpha_{bl(min)}$
f_{offset}	frequency offset range; Fig.11 (a)	deviation = ±4.0 kHz, $f_1 = f_{i(RF)} \pm 2$ kHz ($f_{offset(min)}$) generator 1: modulated test signal 1	 $P_1 = P_{i(ref)} + 3$ dB
Δf_{dev}	deviation range; Fig.11 (a)	deviation = ±2.5 to ±7 kHz; ($\Delta f_{dev(min)}$ to $\Delta f_{dev(max)}$) generator 1: modulated test signal 1	 $P_1 = P_{i(ref)} + 3$ dB
t_{on}	receiver turn-on time; Fig.11 (a)	note 3 generator 1: modulated test signal 1	 $P_1 = P_{i(ref)} + 10$ dB

Notes

1. The tests are executed without load on pins TPI and TPQ.
2. All minimum and maximum values correspond to a bit error rate (BER) ≤ $^3/_{100}$ in the wanted signal (P_1).
3. The BER measurement is started 5 ms ($t_{on(max)}$) after V_{RE} goes HIGH; BER is then measured for 100 bits (BER ≤ $^3/_{100}$).



(a) One generator.
(b) Two generators.
(c) Three generators.

Fig.11 Test configurations.

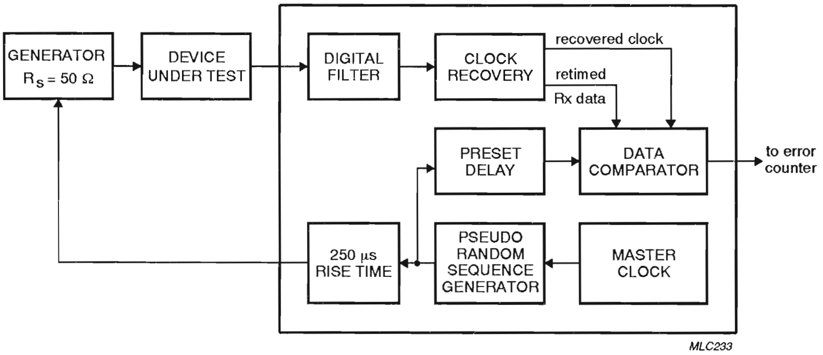


Fig.12 BER test facility.

PRINTED-CIRCUIT BOARDS

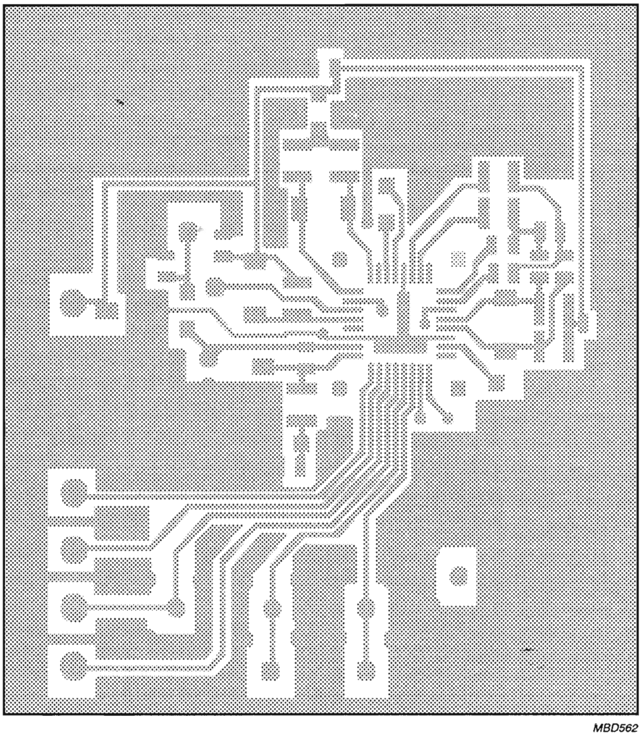


Fig.13 PCB top view for TQFP32; test circuit Figs 1 and 3.

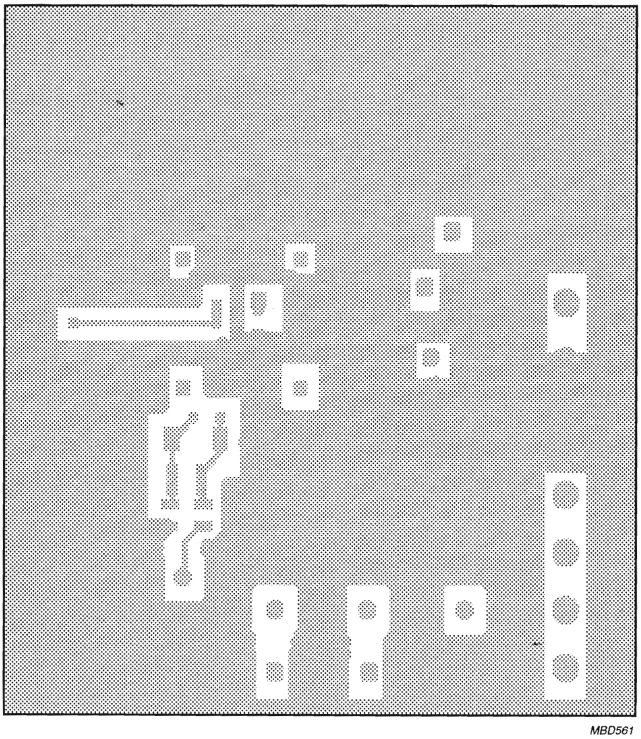
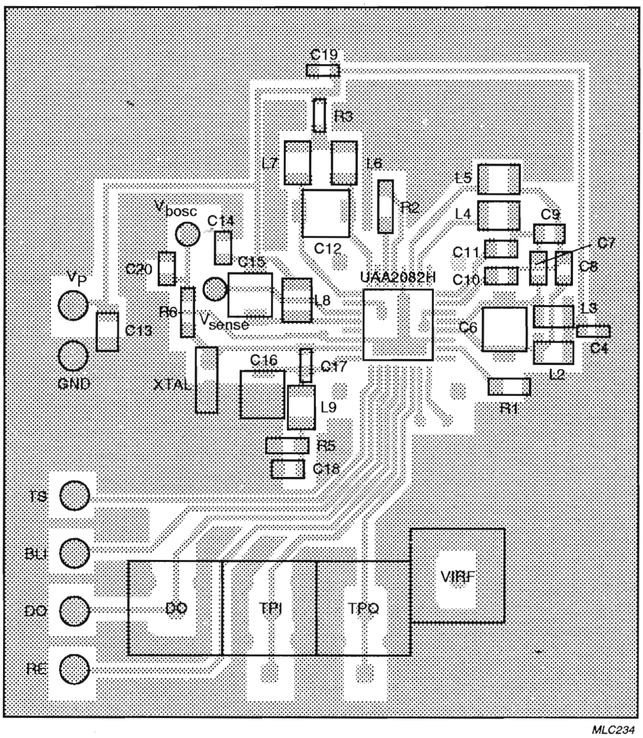


Fig.14 PCB bottom view for TQFP32; test circuit Figs 1 and 3.



V_{EE} = GND; V_C = V_P.

Fig.15 PCB top view with components for TQFP32; test circuit Fig.3.

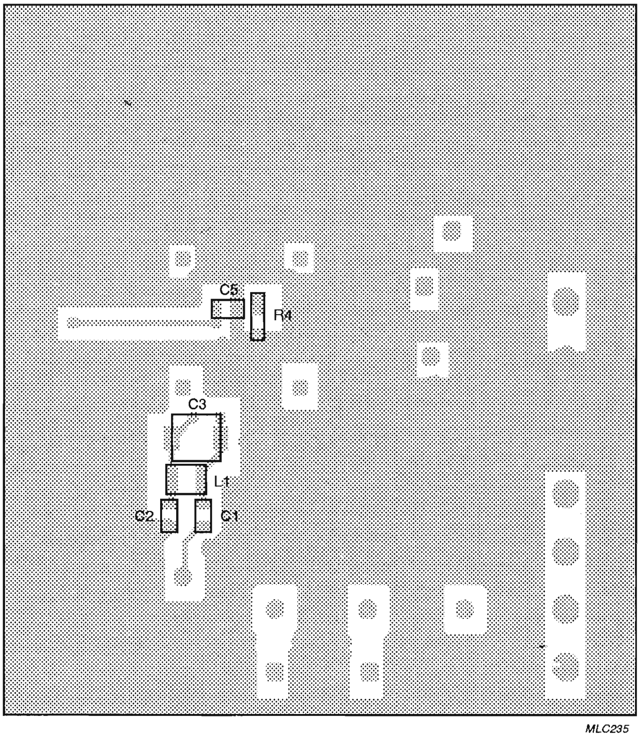


Fig.16 PCB bottom view with components for TQFP32; test circuit Fig.3.

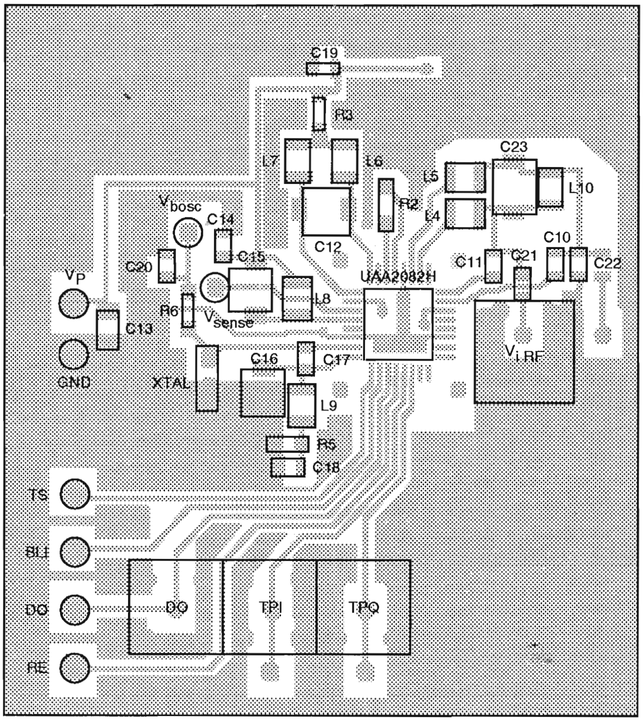


Fig.17 PCB top view with components for TQFP32; test circuit Fig.5.

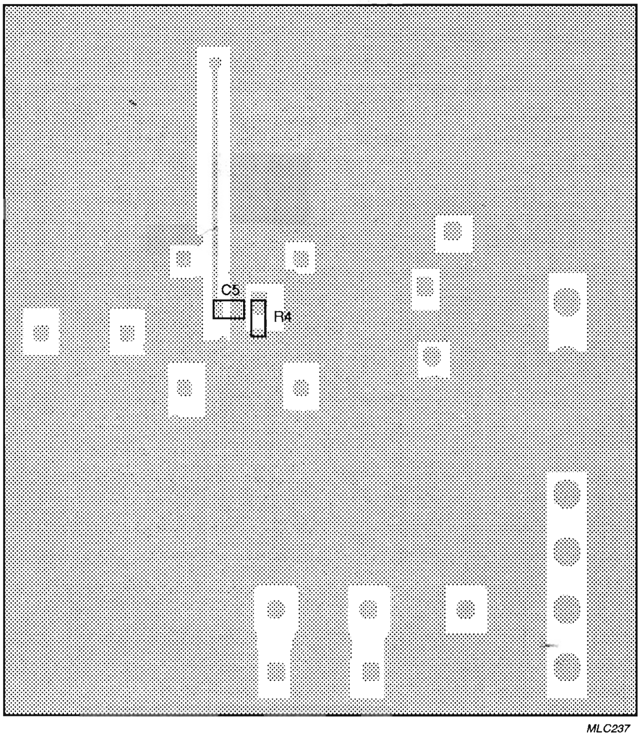


Fig.18 PCB bottom view with components for TQFP32; test circuit Fig.5.

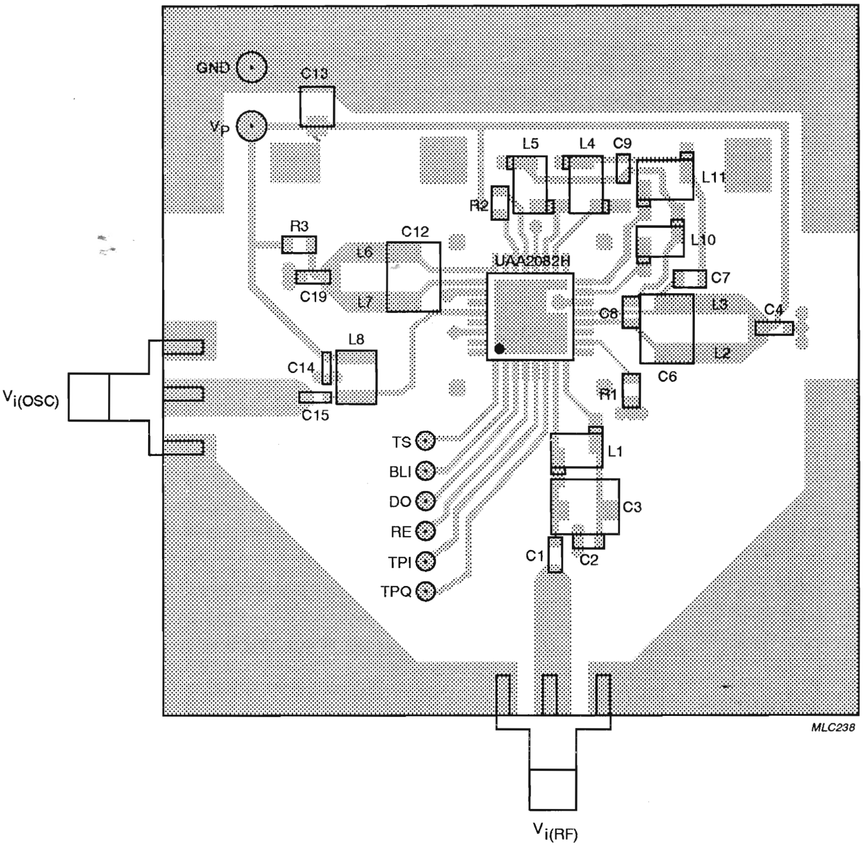


Fig.19 PCB top view with components for TQFP32; test circuit Fig.6.

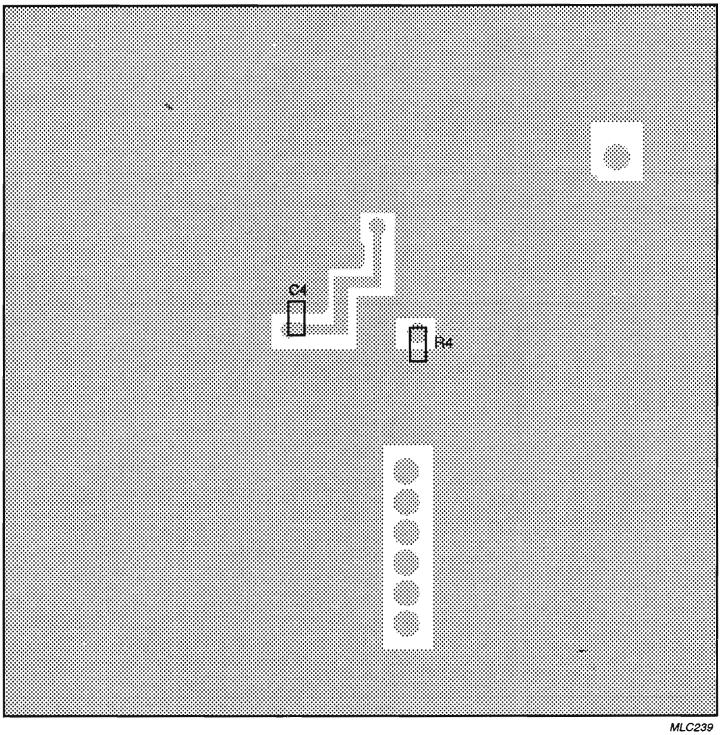


Fig.20 PCB bottom view with components for TQFP32; test circuit Fig.6.

Section 3
Amplifiers

RF/Wireless Communications

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RF Communications

RF AMPLIFIER FAMILY OVERVIEW

	NE/SA5200	NE/SA5204A	NE/SA5205A	NE/SA5209	NE/SA5219
Description	**Dual Gain Stage**	**Wideband Amp**	**Wideband Amp**	**Variable Gain Amp**	**Variable Gain Amp**
V_{CC}	4 – 9V	5 – 8V	5 – 8V	4.5 – 7.0V	4.5 – 7.0V
I_{CC}	4.2mA/95 µA*@5V (per amplifier)	25mA @ 6V	25mA @ 6V	43mA @ 5V	43mA @ 5V
Bandwidth (3dB)	DC - 1.2GHz	DC - 350MHz	DC - 550MHz	DC - 850MHz	700MHz
Gain (power)	7.5dB/–13.5dB* (per amplifier)	19dB	19dB	25dB (voltage)	25dB (voltage)
Noise Figure	3.6dB	6.0dB 50 Ω 4.8dB 75 Ω	6.0dB 50 Ω 4.8dB 75 Ω	9.3dB	9.3dB
1dB Compression	+3.2dBm	+4dBm	+4dBm	–3dBm	–3dBm
3rd Order Intercept (input)	–1.8dBm	–2dBm	–2dBm	+13dBm (output)	+13dBm (output)
Input Impedance	50 Ω	50 Ω	50 Ω	1.2k Ω	1.2k Ω
Output Impedance	50 Ω	50 Ω	50 Ω	60 Ω	60 Ω
Package	SO8	DIP8 SO8	DIP8 SO8	DIP16 SO16	DIP16 SO16
Features	+DC to 1.2GHz operation +Power-Down mode	+DC to 350MHz operation	+DC to 550MHz operation	+DC to 850MHz operation +Gain control pin	+DC to 700MHz operation +Gain control pin

*Amplifier: Enabled/Disabled

RF dual gain-stage

NE/SA5200

DESCRIPTION

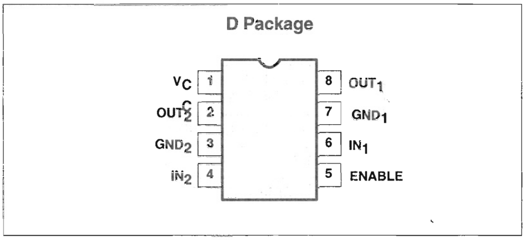
The NE/SA5200 is a dual amplifier with DC to 1200MHz response. Low noise (NF = 3.6dB) makes this part ideal for RF front-ends, and a simple power-down mode saves current for battery operated equipment. Inputs and outputs are matched to 50Ω.

The enable pin allows the designer the ability to turn the amplifiers on or off, allowing the part to act as an amplifier as well as an attenuator. This is very useful for front-end buffering in receiver applications.

FEATURES

- Dual amplifiers
- DC - 1200MHz operation
- Low DC power consumption (4.2mA per amplifier @ V_{CC} = 5V)
- Power-Down Mode (I_{CC} = 95µA typical)
- 3.6dB noise figure at 900MHz
- Unconditionally stable
- Fully ESD protected
- Low cost

PIN CONFIGURATION



- Supply voltage 4-9V
- Gain S_{21} = 7dB at f = 1GHz
- Input and output match S_{11}, S_{22} typically <–14dB

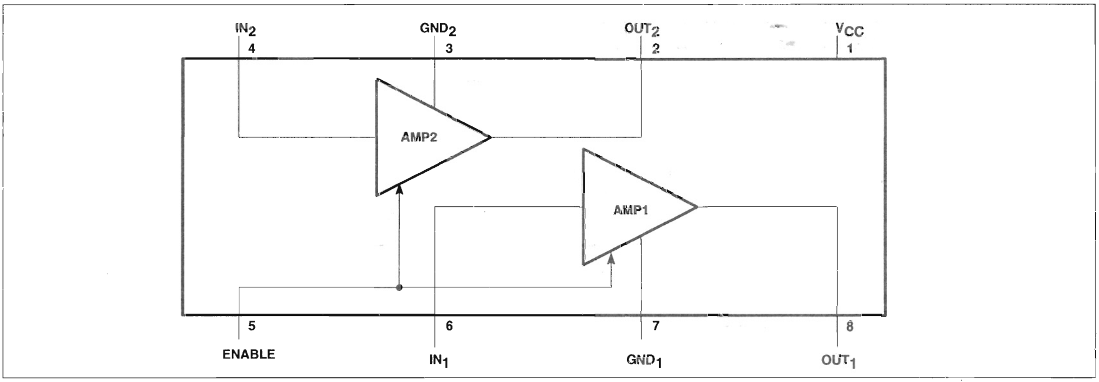
APPLICATIONS

- Cellular radios
- RF IF strips
- Portable equipment

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (Surface–mount)	0-70°C	NE5200D	0174C
8-Pin Plastic Small Outline (Surface–mount)	–40–+85°C	SA5200D	0174C

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	4.0 to 9.0	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[1]	-0.5 to +9	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 8-Pin Plastic SO	780	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 10.5V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   8-Pin SO: θ_{JA} = 158°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4	5.0	9.0	V
I_{CC}	Total supply current	V_{CC} = 5V, ENABLE = High	6.4	8.4	10.4	mA
		V_{CC} = 5V, ENABLE = Low		95	255	μA
		V_{CC} = 9V, ENABLE = High		17.8	22.2	mA
		V_{CC} = 9V, ENABLE = Low		320	960	μA
V_T	TTL/CMOS logic threshold voltage[1]			1.25		V
V_{IH}	Logic 1 level	Power-up mode	2.0		V_{CC}	V
V_{IL}	Logic 0 level	Power-down mode	-0.3		0.8	V
I_{IL}	Enable input current	Enable = 0.4V	-1	0	1	μA
I_{IH}	Enable input current	Enable = 2.4V	-1	0	1	μA
$V_{IDC,ODC}$	Input and output DC levels		0.6	0.83	1.0	V

NOTE:
1. The ENABLE input must be connected to a valid logic level for proper operation of the NE/SA5200.

AC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = +5V, T_A = 25°C, either amplifier, enable = 5V; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
S21	Insertion gain	f = 100MHz	9.2	11	13.2	dB
		f = 900MHz	5.2	7.5		
S22	Output return loss	f = 900MHz		–14.3		dB
S12	Reverse isolation	f = 900MHz		–17.9		dB
S11	Input return loss	f = 900MHz		–16.5		dB
P-1	Output 1dB compression point	f = 900MHz		–4.3		dBm
NF	Noise figure in 50Ω	f = 900MHz		3.6		dB
IP_2	Input second-order intercept point	f = 900MHz		+4.3		dBm
IP_3	Input third-order intercept point	f = 900MHz		–1.8		dBm
ISOL	Amplifier-to-amplifier isolation[2]	f = 900MHz		–25		dB
P_{OUT}	Saturated output power	f = 900MHz		–1.7		dBm
S21	Insertion gain when disabled	f = 100MHz		–13		dB
		f = 900MHz		–13.5		

NOTE:
1. All measurements include the effects of the NE/SA5200 Evaluation Board (see Figure 2). Measurement system impedance is 50Ω.
2. Input applied to one amplifier, output taken at the other output. All ports terminated into 50Ω.

APPLICATIONS

NE/SA5200 is a user-friendly, wide-band, unconditionally stable, low power dual gain amplifier circuit. There are several advantages to using the NE/SA5200 as a high frequency gain block instead of a discrete implementation. First is the simplicity of use. The NE/SA5200 does not need any external biasing components. Due to the higher level of integration and small footprint (SO8) package it occupies less space on the printed circuit board and reduces the manufacturing cost of the system. Also the higher level of integration improves the reliability of the amplifier over a discrete implementation with several components. The power down mode in the NE/SA5200 helps reduce power consumption in applications where the amplifiers can be disabled. And last but not the least is the impedance matching at inputs and outputs. Only those who have toiled through discrete transistor implementations for 50Ω input and output impedance matching can truly appreciate the elegance and simplicity of the NE/SA5200 input and output impedance matching to 50Ω.

A simplified equivalent schematic is shown in 1. Each amplifier is composed of an NPN transistor with an Ft of 13GHz in a classical series-shunt feedback configuration. The two wideband amplifiers are biased from the same bias generator. In normal operation each amplifier consumes about 4mA of quiescent current (at V_{CC} = 5V). In the disable mode the device consumes about 90μA of current, most of it is in the TTL enable buffer and the bias generator. The input impedance of the amplifiers is 50Ω. The amplifiers have typical gain of 11dB at 100MHz and 7dB of gain at 1.2GHz.

It can be seen from 1 that any inductance between Pin 7, 3 and the ground plane will reduce the gain of the amplifiers at higher frequencies. Thus proper grounding of Pins 7 and 3 is essential for maximum gain and increased frequency response. 2 shows the printed circuit board layout and the component placement for the NE/SA5200 evaluation board. The AC coupling capacitors should be selected such that at they are shorts at the desired frequency of operation. Since most low-cost large value surface mount capacitors cease to be simply capacitors in the UHF range and exhibit an inductive behavior, it is recommended that high frequency chip capacitors be utilized in the circuit. A good power supply bypass is also essential for the performance of the amplifier and should be as close to the device as practical.

3 shows the typical frequency response of the two channels of NE/SA5200. The low frequency gain is about 11dB at 100MHz and slowly drops off to 10dB at 500MHz. The gain is about 8dB at 900MHz and 7dB at 1.2 GHz which is typical of NE/SA5200 with a good printed circuit board layout. It can also be seen that both channels have a very well matched frequency response and matched gain to within 0.1dB at 100MHz and 0.2dB at 900MHz.

NE/SA5200 finds applications in many areas of RF communications. It is an ideal gain block for high performance, low cost, low power RF communications transceivers. A typical radio transceiver front-end is shown in 4. This could be the front-end of a cellular phone, a VHF/ UHF hand-held transceiver, UHF cordless telephone or a spread spectrum system. The NE/SA5200 can be used in the receiver path of most systems as an LNA and pre-amplifier. The bandpass filter between the two amplifiers also minimize the noise into the first mixer. In the transmitter path, NE/SA5200 can be used as a buffer to the VCO and isolate the VCO from any load variations due to the power level changes in the power amplifier. This improves the stability of the VCOs. The NE/SA5200 can also be used as a pre-driver to the power amplifier modules.

The two amplifiers in NE/SA5200 can be easily cascaded to have a 13dB gain block at 900MHz. At 100MHz the gain will be 22dB and a noise figure of about 5.5dB. The NE/SA5200 can be operated at a higher voltage up to 9V for much improved 1dB output compression point and higher 3rd order intercept point.

Several stages of NE/SA5200 can also be cascaded and be used as an IF amplifier strip for DBS/TV/GPS receivers. 5 shows a 60dB gain IF strip at 180MHz. The noise figure for the cascaded amplifier chain is given by equation 1.

NF (total) = NF1 + NF2/G1 + NF3/G1*G2 + NF4/G1*G2*G3 + ...
(Equation. 1)

NOTE: The noise figure and gain should not be in dB in the above equation.

Since the noise figure for each stage is about 3.6dB and the gain is about 11dB, the noise figure for the 60dB gain IF strip will be about 6.4dB.

In applications where a single amplifier is required with a 7.5dB gain at 900MHz and current consumption is of paramount importance (battery powered receivers), the amplifier A1 can be used and amplifier A2 can be disabled by leaving GND2 (Pin 3) unconnected. This will reduce the total current consumption for the IC to a meager 4mA.

The ENABLE pin is useful for Time-Division-Duplex systems where the receiver can be disabled for a period of time. In this case the overall system supply current will be decreased by 8mA.

The ENABLE pin can also be used to improve the system dynamic range. For input levels that are extremely high, the NE/SA5200 can be disabled. In this case the input signal is attenuated by 13dB. This prevents the system from being overloaded as well as improves the system's overall dynamic range. In the disabled condition the NE/SA5200 IP_3 increases to nearly +20dBm.

RF dual gain-stage NE/SA5200

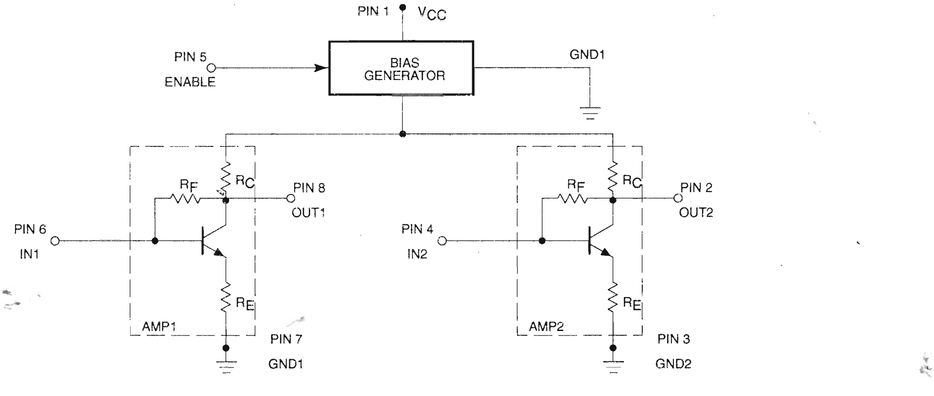
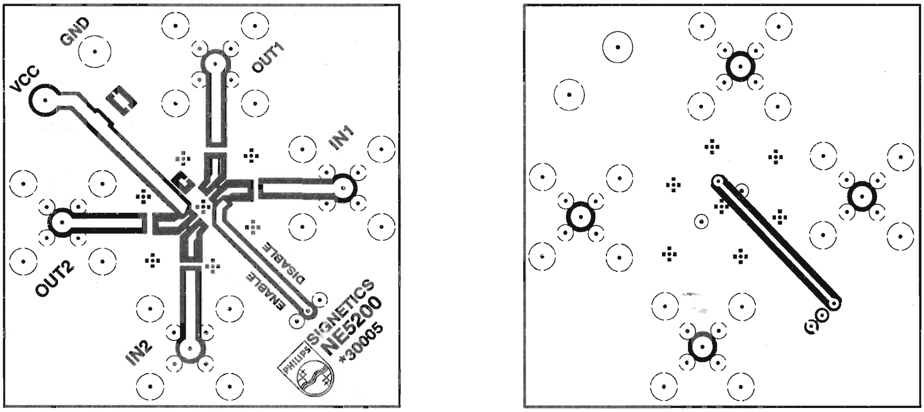
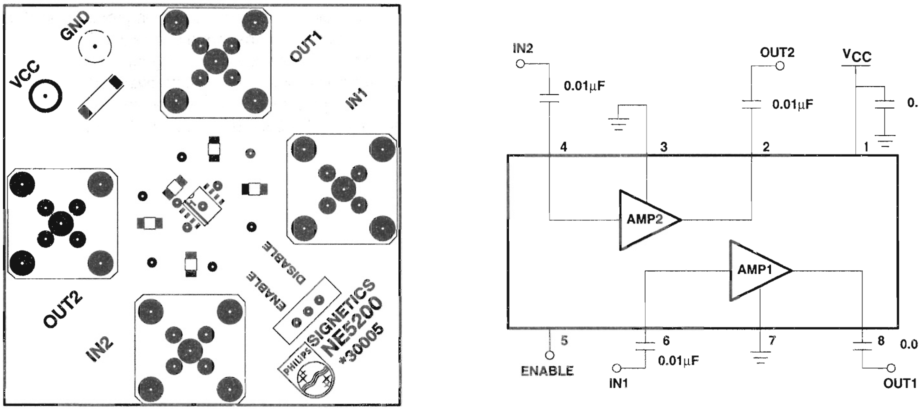


Figure 1. Simplified Equivalent Schematic of NE/SA5200



a. Top Side

b. Bottom Side



c. Top Silk Screen

d. NE/SA5200 Evaluation Board Schematic

Figure 2. Printed Circuit Board Layout of the NE/SA5200 Evaluation Board

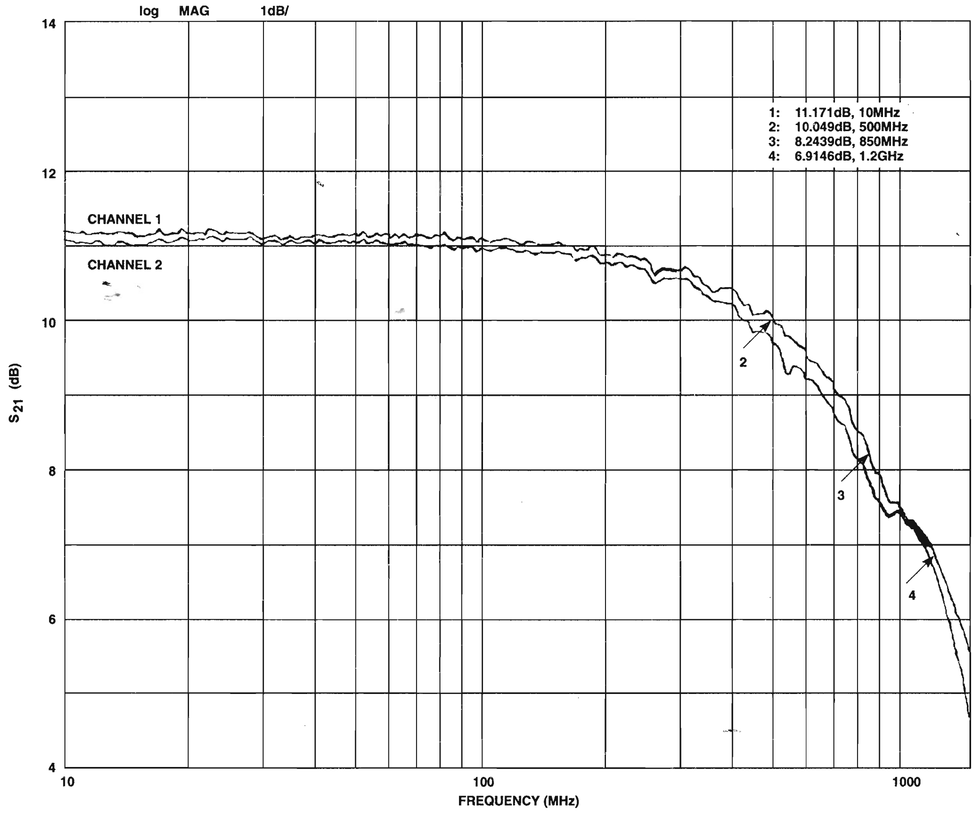


Figure 3. Typical Frequency Response of NE/SA5200 in a 50Ω System

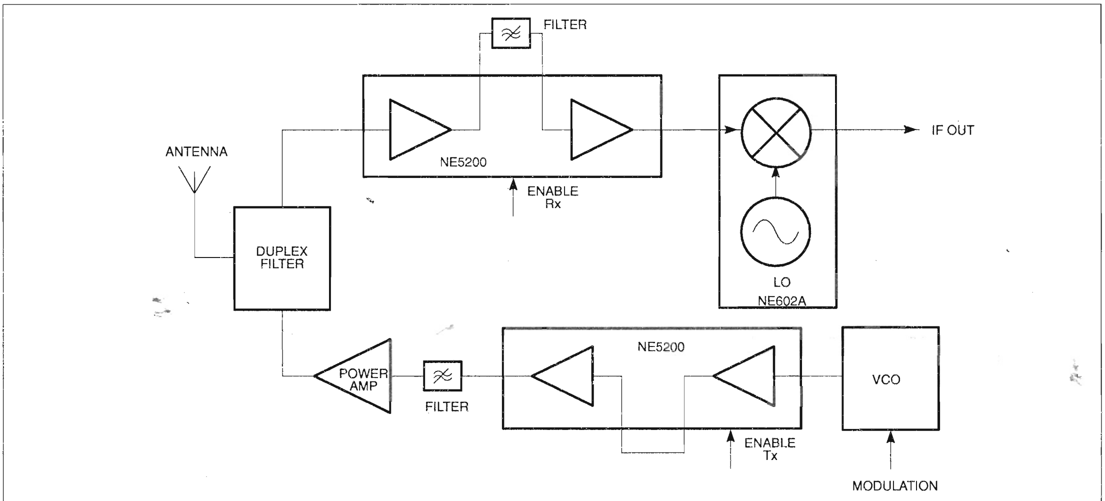


Figure 4. Typical Radio Transceiver Front-End

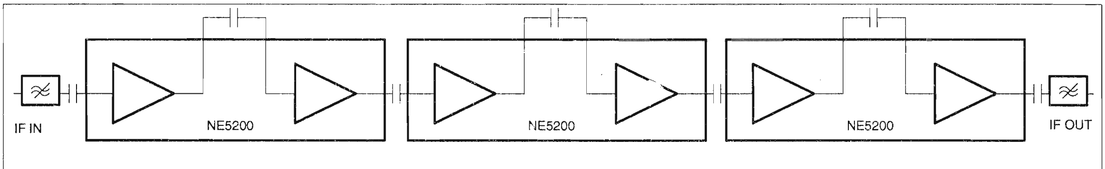


Figure 5. 60dB IF Gain Block for 100-300MHz IF for GPS/DBS Systems

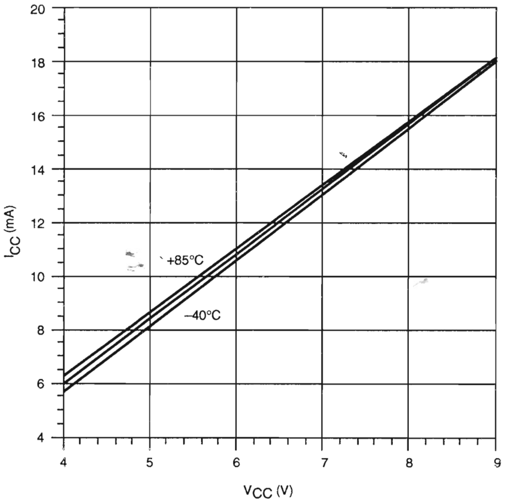


Figure 6. Supply Current vs Supply Voltage and Temperature

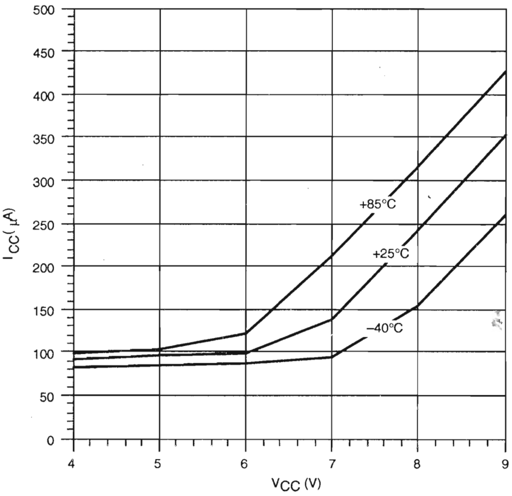


Figure 7. Disabled Supply Current vs V_{CC} and Temperature

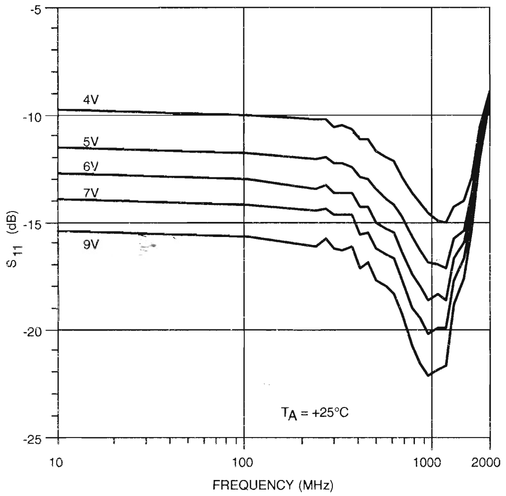


Figure 8. Input Match vs Frequency and V_{CC}

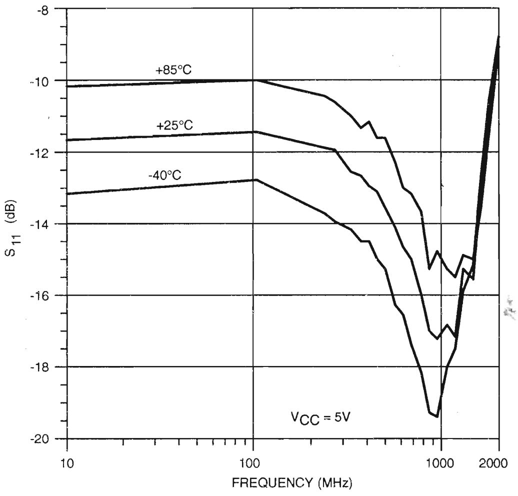


Figure 9. Input Match vs Frequency and Temperature

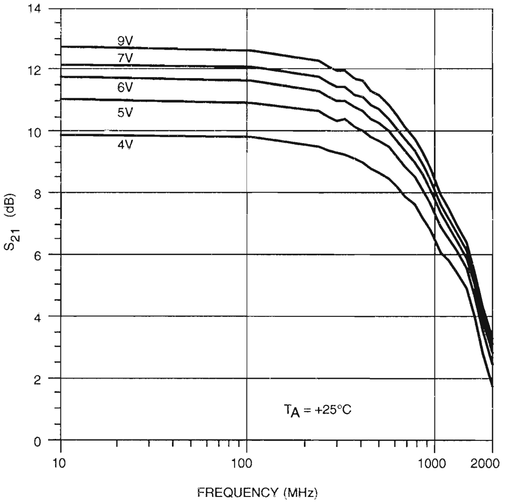


Figure 10. Insertion Gain vs Frequency and V_{CC}

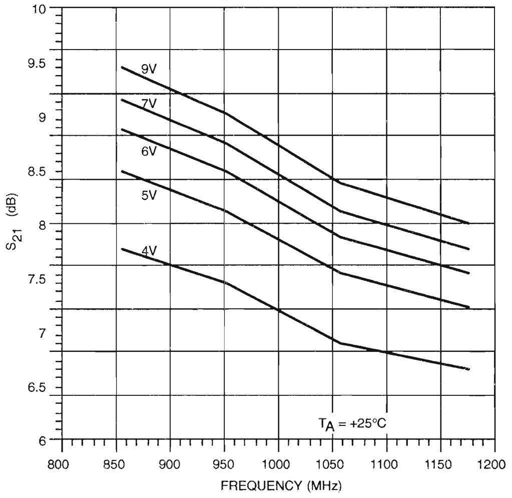


Figure 11. Insertion Gain vs Frequency and V_{CC} — Expanded Detail —

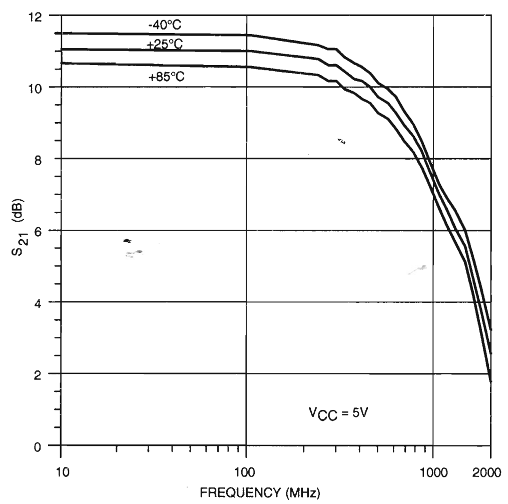


Figure 12. Insertion Gain vs Frequency and Temperature

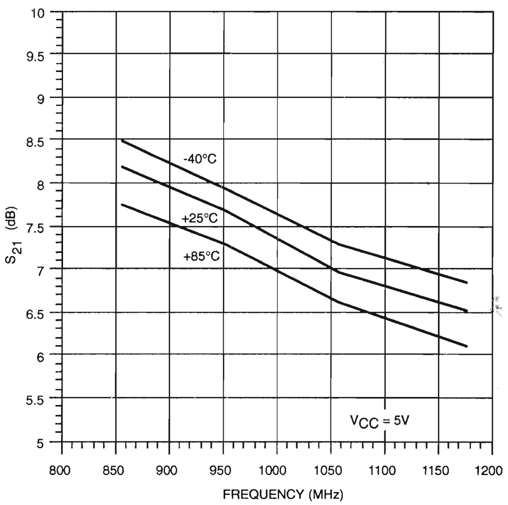


Figure 13. Insertion Gain vs Frequency and Temperature – Expanded Detail –

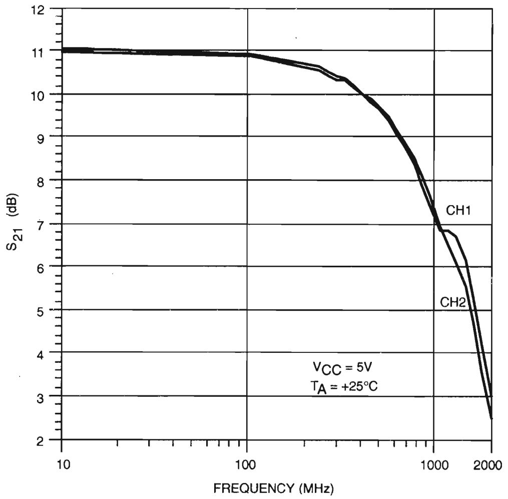


Figure 14. Insertion Gain Matching (CH1 vs CH2) vs Frequency

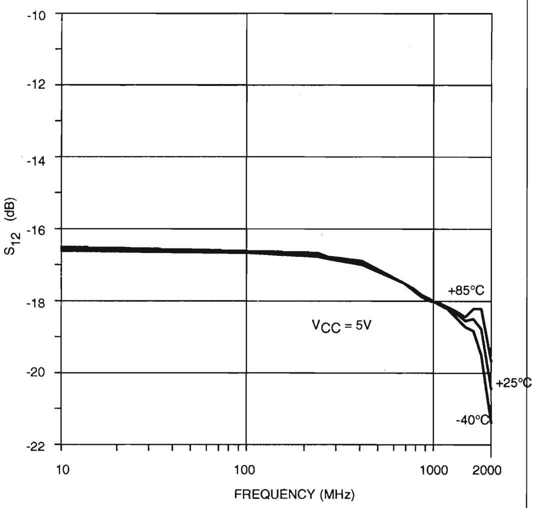


Figure 15. Reverse Insertion Gain vs Frequency and Temperature

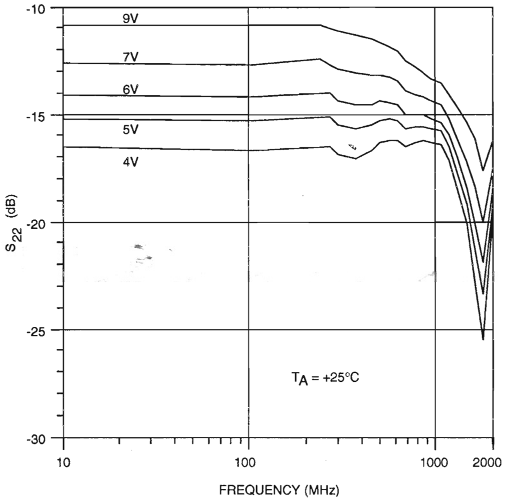


Figure 16. Output Match vs Frequency and V_{CC}

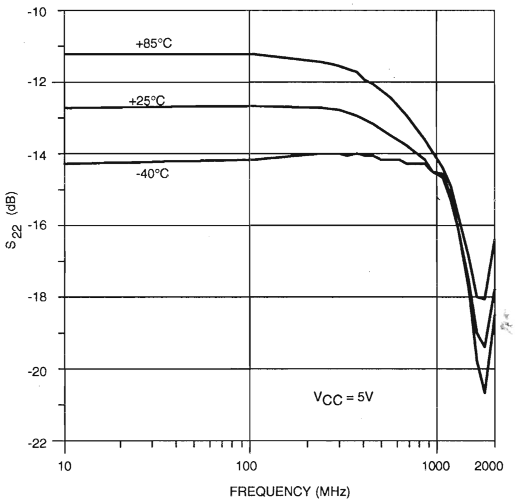


Figure 17. Output Match vs Frequency and Temperature

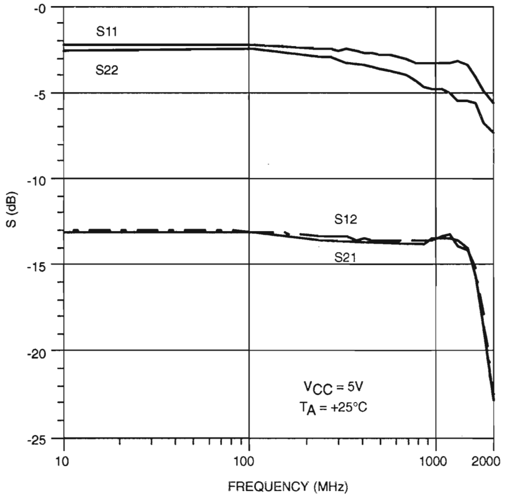


Figure 18. S-parameters vs Frequency for Disabled Amplifier

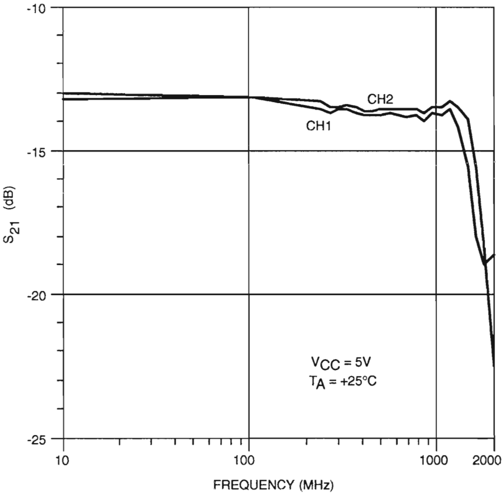


Figure 19. Insertion Gain Matching Disabled (CH1 vs CH2) vs Frequency

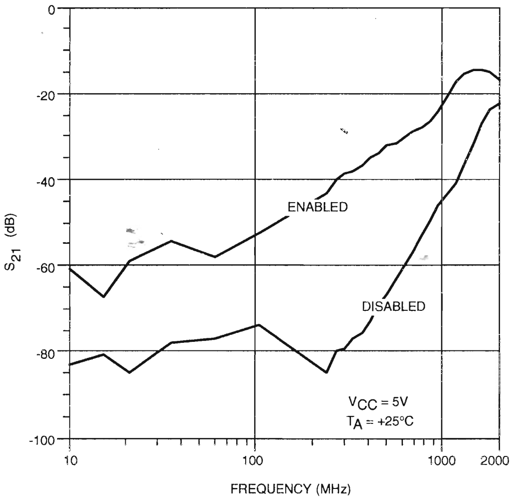


Figure 20. CH1 Input to CH2 Output Isolation vs Frequency

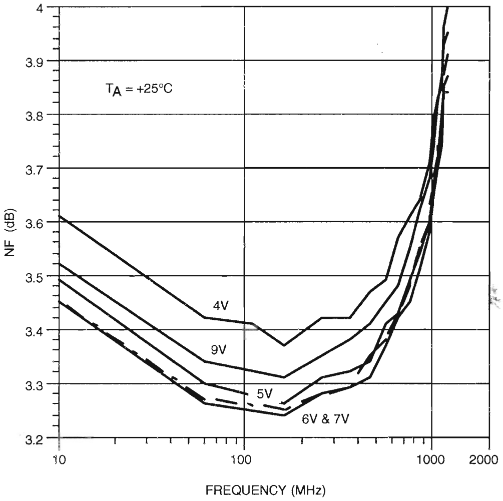


Figure 21. Noise Figure vs Frequency and V_{CC} in a 50Ω System

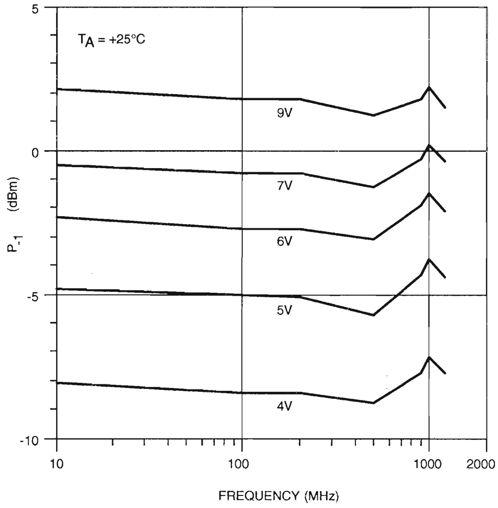


Figure 22. 1dB Output Compression Point vs Frequency and V_{CC}

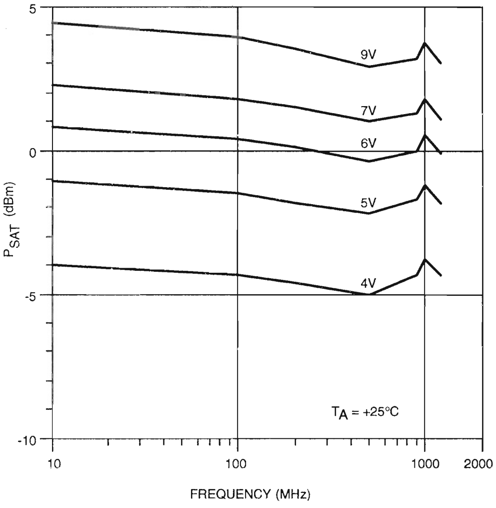


Figure 23. Saturated Output Power vs Frequency and V_{CC}

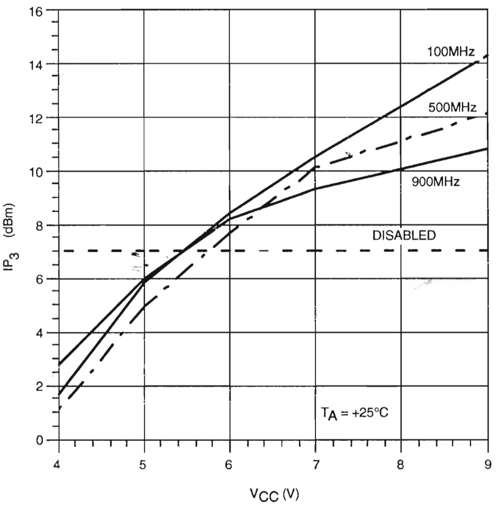


Figure 24. Third-Order Output Intercept vs Frequency and V_{CC}

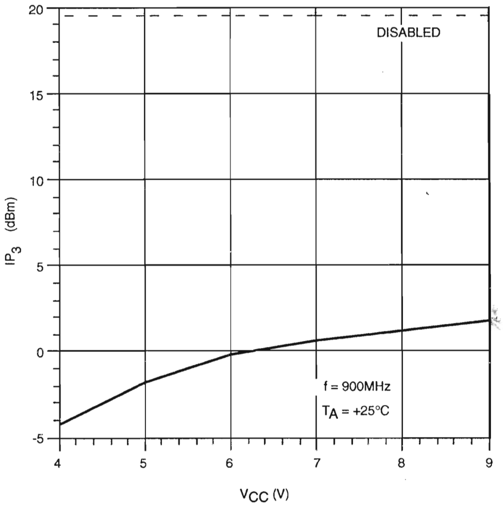


Figure 25. Third-Order Input Intercept vs Frequency and V_{CC}

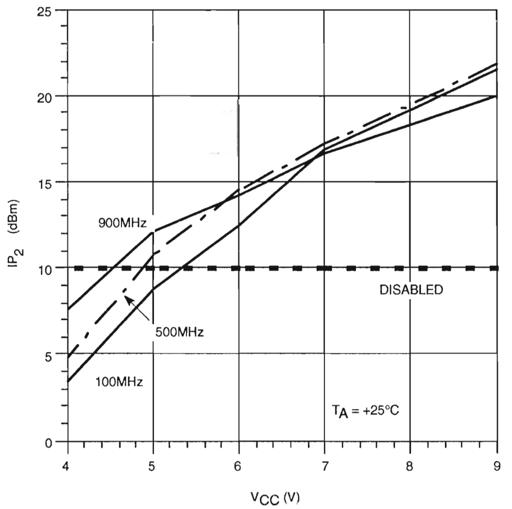


Figure 26. Second-Order Output Intercept vs Frequency and V_{CC}

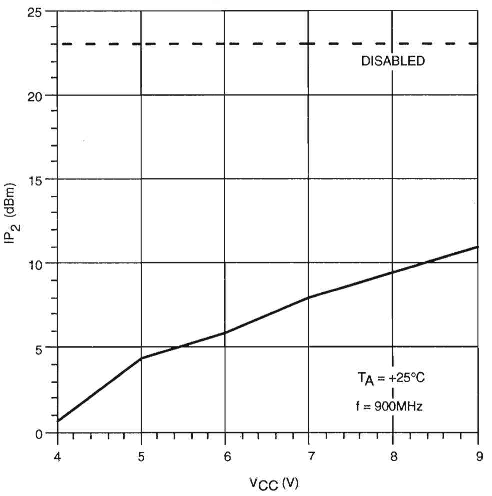


Figure 27. Second-Order Input Intercept vs Frequency and V_{CC}

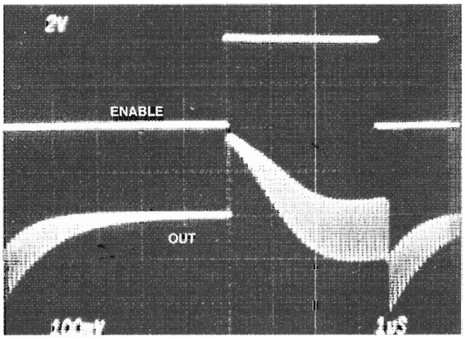


Figure 28. Switching Speed; f_{IN} = 10MHz at –26dBm, V_{DD} = 5V, Coupling Capacitors Set to 0.01µF

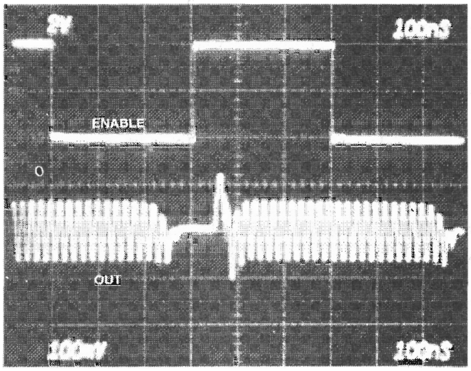


Figure 29. Switching Speed; f_{IN} = 50MHz at –26dBm, V_{DD} = 5V, Coupling Capacitors Set to 100pF

Wide-band high-frequency amplifier

NE/SA5204A

DESCRIPTION

The NE/SA5204A family of wideband amplifiers replaces the NE/SA5204 family. The 'A' parts are fabricated on a rugged 2µm bipolar process featuring excellent statistical process control. Electrical performance is nomically identical to the original parts.

The NE/SA5204A is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 200MHz. The -3dB bandwidth is greater than 350MHz. This performance makes the amplifier ideal for cable TV applications. The NE/SA5204A operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

The NE/SA5204A is a relaxed version of the NE5205. Minimum guaranteed bandwidth is relaxed to 350MHz and the "S" parameter Min/Max limits are specified as typicals only.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA5204A solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The standing wave ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 350MHz operating range.

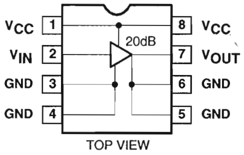
Since the part is a small, monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

No external components are needed other than AC-coupling capacitors because the NE/SA5204A is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm, respectively, at 100MHz.

The part is well matched for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters, and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio, and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA5204As in series as required, without any degradation in amplifier stability.

PIN CONFIGURATION

N, D Packages



FEATURES

- Bandwidth (min.)
  200 MHz, ±0.5dB
  350 MHz, -3dB
- 20dB insertion gain
- 4.8dB (6dB) noise figure Z_O=75Ω (Z_O=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface-mount package available
- Cascadable
- 2000V ESD protection

APPLICATIONS

- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broadband LANs
- Networks
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

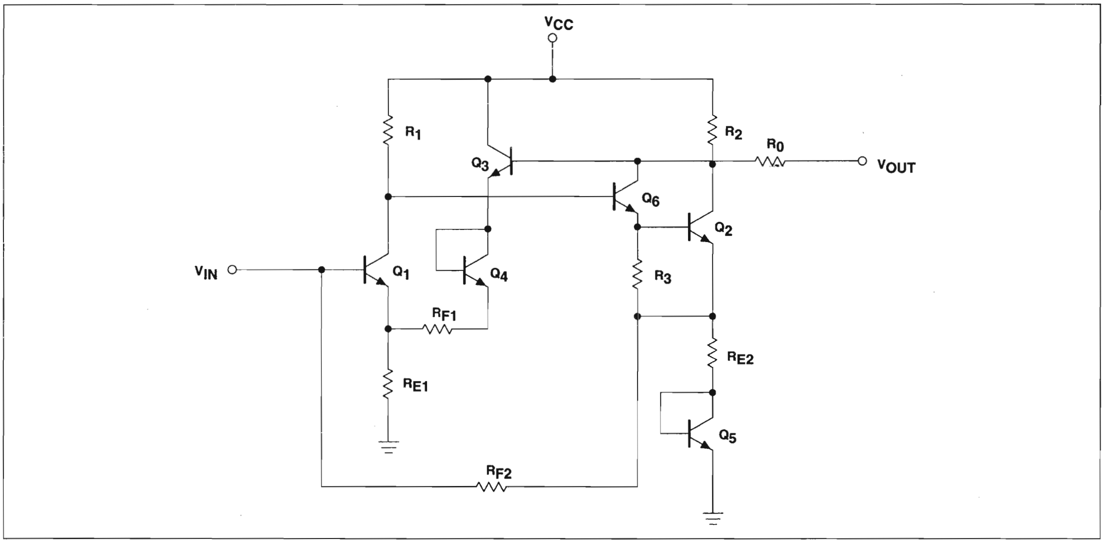
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5204AN	0404B
8-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5204AD	0174C
8-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA5204AN	0404B
8-Pin Plastic Small Outline (SO) package	–40 to +85°C	SA5204AD	0174C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{IN}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	–40 to +85	°C
P_{DMAX}	Maximum power dissipation[1, 2] T_A=25°C(still–air)		
	N package	1160	mW
	D package	780	mW
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	–55 to +150	°C
T_{SOLD}	Lead temperature (soldering 60s)	300	°C

NOTES:
1. Derate above 25°C, at the following rates
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. See “Power Dissipation Considerations” section.

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

V_{CC}=6V, Z_S=Z_L=Z_O=50Ω and T_A=25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage range	Over temperature	5		8	V
I_{CC}	Supply current	Over temperature	19	25	33	mA
S21	Insertion gain	f=100MHz, over temperature	16	19	22	dB
S11	Input return loss	f=100MHz		25		dB
		DC –550MHz		12		
S22	Output return loss	f=100MHz		27		dB
		DC –550MHz		12		
S12	Isolation	f=100MHz		–25		dB
		DC –550MHz		–18		
BW	Bandwidth	±0.5dB	200	350		MHz
BW	Bandwidth	–3dB	350	550		MHz
	Noise figure (75Ω)	f=100MHz		4.8		dB
	Noise figure (50Ω)	f=100MHz		6.0		dB
	Saturated output power	f=100MHz		+7.0		dBm
	1dB gain compression	f=100MHz		+4.0		dBm
	Third–order intermodulation intercept (output)	f=100MHz		+17		dBm
	Second–order intermodulation intercept (output)	f=100MHz		+24		dBm
t_R	Rise time			500		ps
t_P	Propagation delay			500		ps

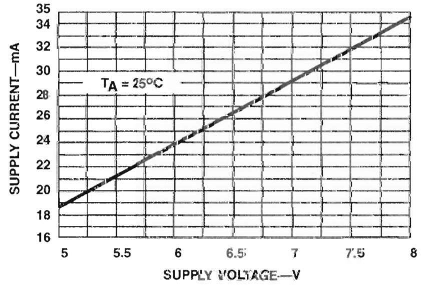


Figure 1. Supply Current vs Supply Voltage

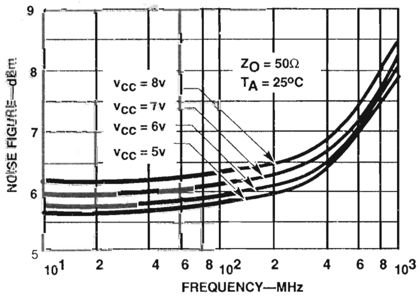


Figure 2. Noise Figure vs Frequency

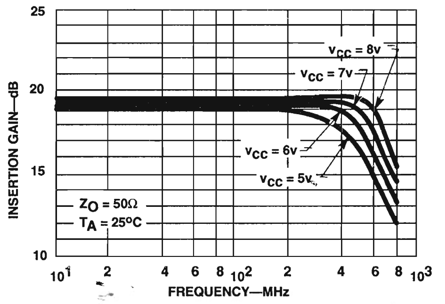


Figure 3. Insertion Gain vs Frequency (S_{21})

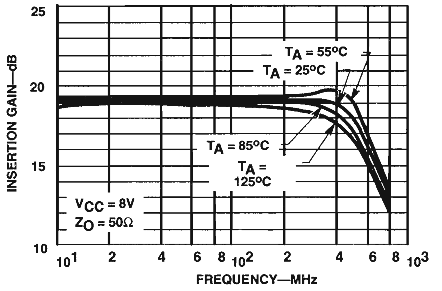


Figure 4. Insertion Gain vs Frequency (S_{21})

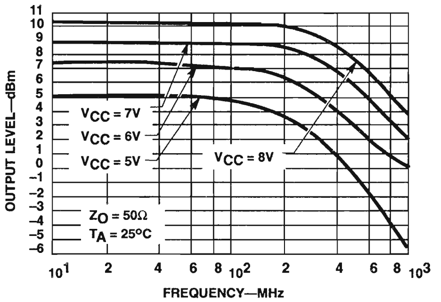


Figure 5. Saturated Output Power vs Frequency

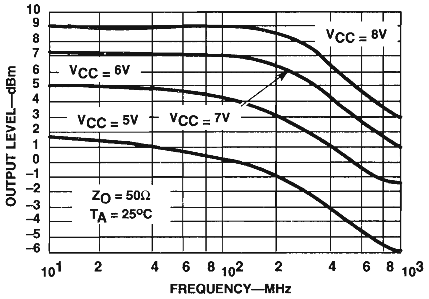


Figure 6. 1dB Gain Compression vs Frequency

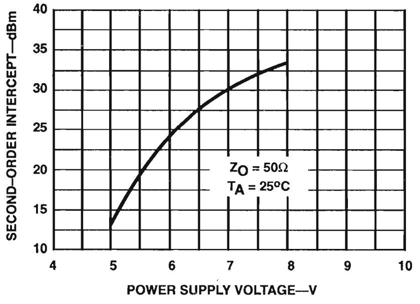


Figure 7. Second-Order Output Intercept vs Supply Voltage

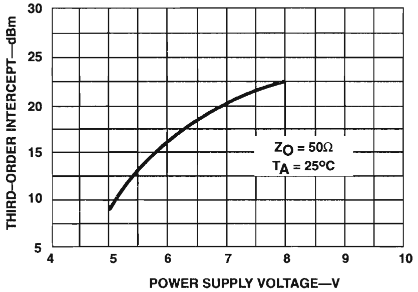


Figure 8. Third-Order Intercept vs Supply Voltage

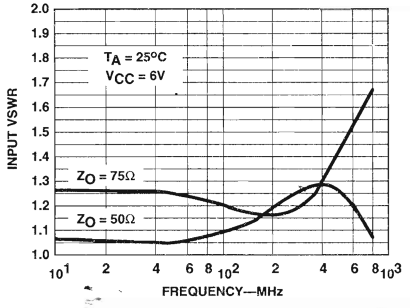


Figure 9. Input VSWR vs Frequency

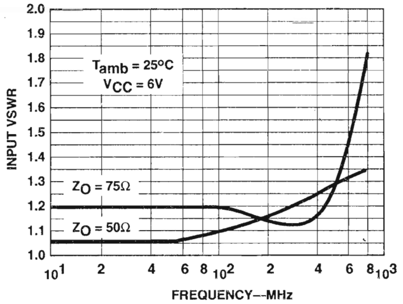


Figure 10. Output VSWR vs Frequency

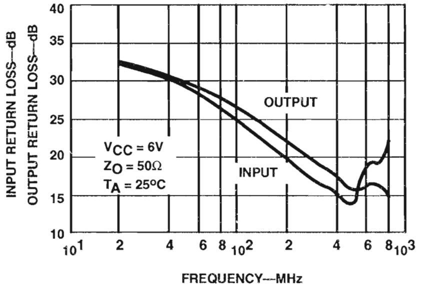


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

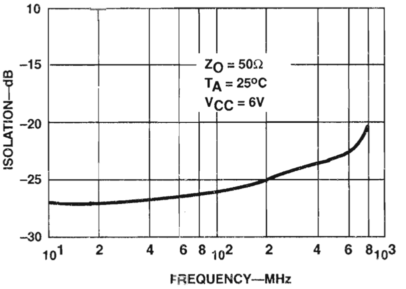


Figure 12. Isolation vs Frequency (S_{12})

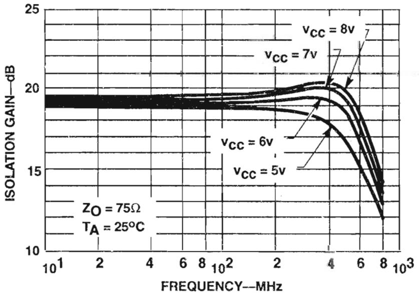


Figure 13. Insertion Gain vs Frequency (S_{21})

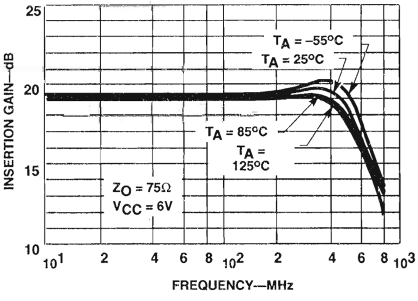


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1}) / R_{E1} \qquad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wide-band terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible, while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10\text{Log}\left(1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}}\right]}{R_O}\right) \text{dB} \qquad (2)$$

where I_{C1}=5.5mA, R_{E1}=12Ω, r_b=130Ω, KT/q=26mV at 25°C and R_0=50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN}=V_{BE1}+(I_{C1}+I_{C3})\ R_{E1} \qquad (3)$$

where R_{E1}=12Ω, V_{BE}=0.8V, I_{C1}=5mA and I_{C3}=7mA (currents rated at V_{CC}=6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4, which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt-feedback loading on the output. The value of R_{F1}=140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT}=V_{CC}-(I_{C2}+I_{C6})R2, \qquad (4)$$

where V_{CC}=6V, R_2=225Ω, I_{C2}=8mA and I_{C6}=5mA.

From here, it can be seen that the output voltage is approximately 3.1V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (32mA max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat-sinking benefits can be realized by mounting the SO and N package bodies against the PC board plane.

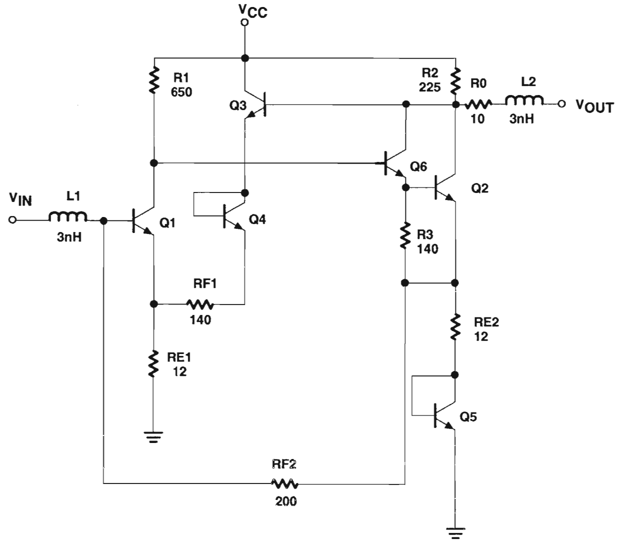


Figure 15. Schematic Diagram

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5204A to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible, and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC-coupled. This is because at V_{CC}=6V, the input is approximately at 1V while the output is at 3.1V. The output must be decoupled into a low-impedance system, or the DC bias on the output of the amplifier will be loaded down, causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high-frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

SCATTERING PARAMETERS

The primary specifications for the NE5204A are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier, and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.

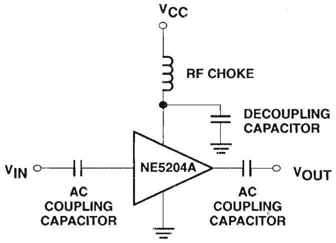
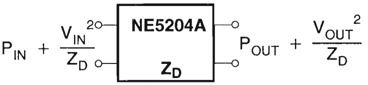


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 18.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5204A to other high-frequency amplifiers.
The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D=Z_{IN}=Z_{OUT}$ for the NE/SA/SE5204A


$P_{IN} + \frac{V_{IN}^2}{Z_D}$
NE5204A
Z_D
$P_{OUT} + \frac{V_{OUT}^2}{Z_D}$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$P_I=V_I^2$

P_I=Insertion Power Gain

V_I=Insertion Voltage Gain

Measured value for the
NE/SA/SE5204A = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

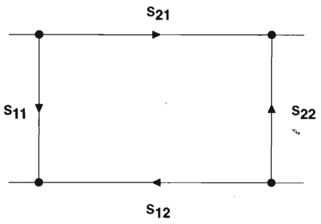
$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20\text{dB}$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20\text{dB}$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:



a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} = \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OSOLATION

$$S_{12} = \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

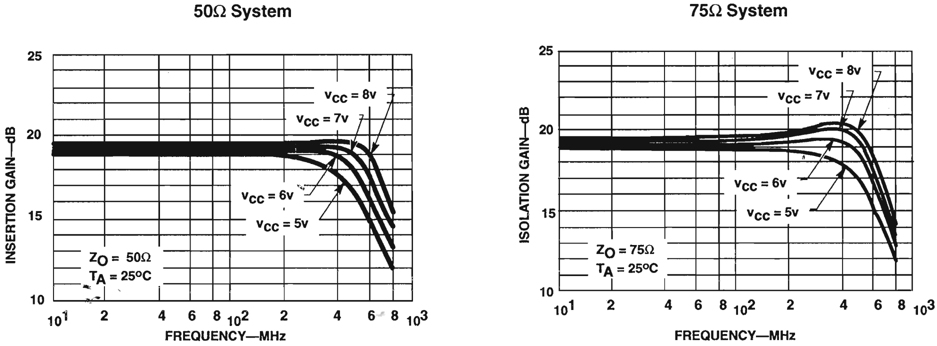
$$S_{21} = \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

$$S_{22} = \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

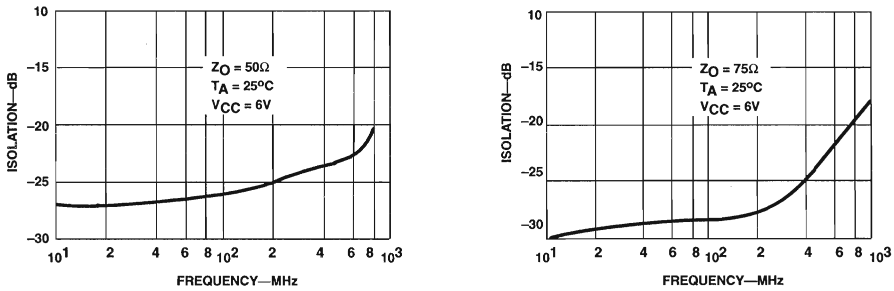
b.

Figure 17.



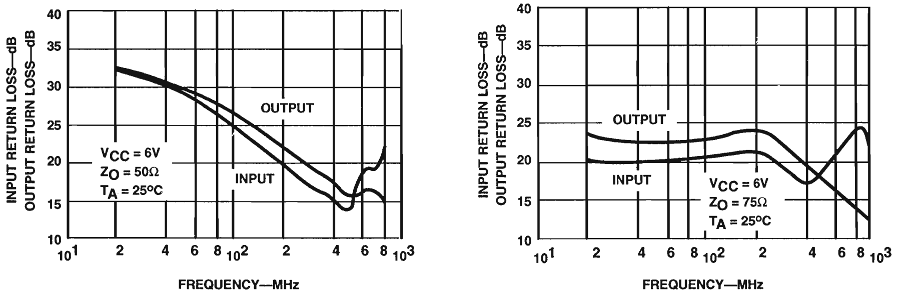
a. Insertion Gain vs Frequency (S_{21})

b. Insertion Gain vs Frequency (S_{21})



c. Isolation vs Frequency (S_{12})

d. S_{12} Isolation vs Frequency



e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 18.

INPUT RETURN LOSS=S_{11}dB
S_{11}dB=20 Log I S_{11} I

OUTPUT RETURN LOSS=S_{22}dB
S_{22}dB=20 Log I S_{22} I

INPUT VSWR=≤1.5

OUTPUT VSWR=≤1.5

1DB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$$IP_2=P_{OUT}+IMR_2$$

$$IP_3=P_{OUT}+IMR_3/2$$

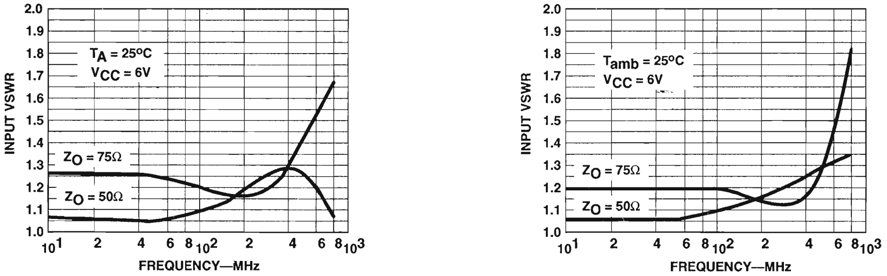
where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA5204A we have chosen an output level of –10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to High-Frequency Amplifiers by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.



a. Input VSWR vs Frequency

b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency

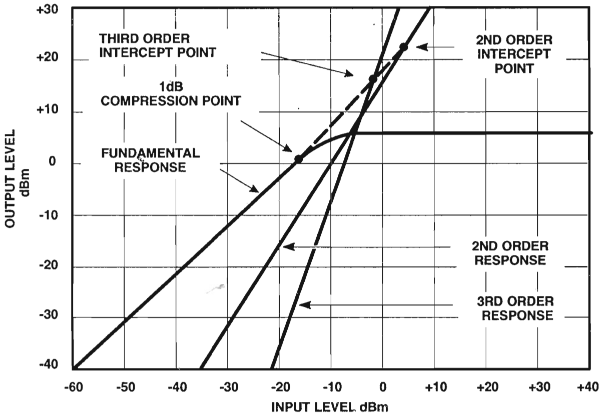

+30
+20
+10
0
-10
-20
-30
-40
OUTPUT LEVEL dBm
THIRD ORDER INTERCEPT POINT
1dB COMPRESSION POINT
FUNDAMENTAL RESPONSE
2ND ORDER INTERCEPT POINT
2ND ORDER RESPONSE
3RD ORDER RESPONSE
-60
-50
-40
-30
-20
-10
0
+10
+20
+30
+40
INPUT LEVEL dBm

Figure 20.

Wide-band high-frequency amplifier

NE/SA/SE5205A

DESCRIPTION

The NE/SA/SE5205A family of wideband amplifiers replace the NE/SA/SE5205 family. The 'A' parts are fabricated on a rugged 2µm bipolar process featuring excellent statistical process control. Electrical performance is nominally identical to the original parts.

The NE/SA/SE5205A is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 450MHz, and the -3dB bandwidth is greater than 600MHz in the EC package. This performance makes the amplifier ideal for cable TV applications. For lower frequency applications, the part is also available in industrial standard dual in-line and small outline packages. The NE/SA/SE5205A operates with a single supply of 6V, and only draws 24mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high-power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA/SE5205A solves these problems by incorporating a wide-band amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output from DC to the -3dB bandwidth limit.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

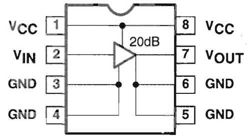
No external components are needed other than AC coupling capacitors because the NE/SA/SE5205A is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA/SE5205As in series as required, without any degradation in amplifier stability.

PIN CONFIGURATIONS

N, D Packages



TOP VIEW

FEATURES

- 600MHz bandwidth
- 20dB insertion gain
- 4.8dB (6dB) noise figure ZO=75Ω (ZO=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface mount package available
- MIL-STD processing available
- 2000V ESD protection

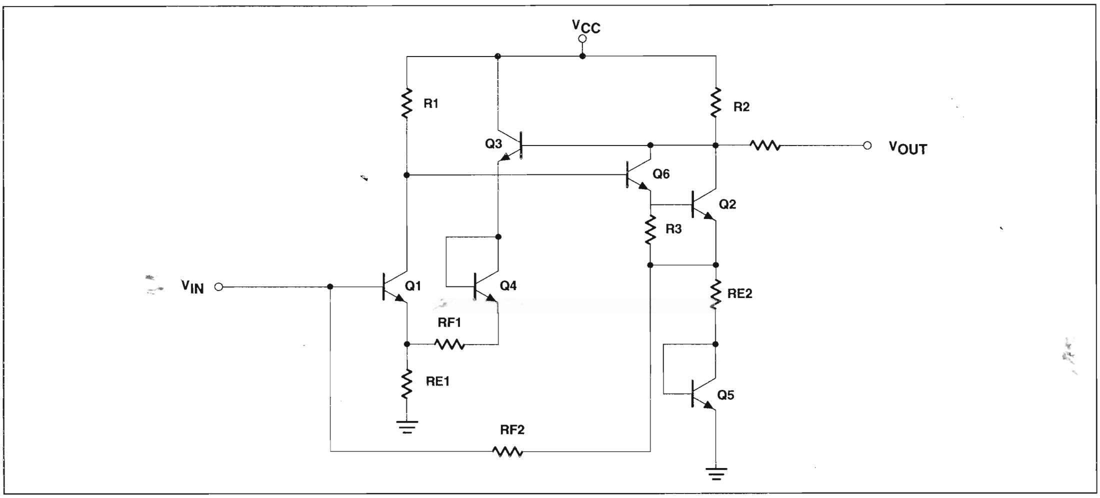
APPLICATIONS

- 75Ω cable TV decoder boxes
- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broad-band LANs
- Fiber-optics
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5205AD	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5205AN	0404B
8-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5205AD	0174C
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5205AN	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-55 to +125°C	SE5205AN	0404B

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{AC}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	-40 to +85	°C
	SE grade	-55 to +125	°C
P_{DMAX}	Maximum power dissipation, T_A=25°C (still-air)$^{1, 2}$		
	N package	1160	mW
	D package	780	mW

NOTES:
1. Derate above 25°C, at the following rates:
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. See “Power Dissipation Considerations” section.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=6V, Z_S=Z_L=Z_O=50Ω and T_A=25°C in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5205A			NE/SA5205A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Operating supply voltage range		5		6.5	5		8	V
		Over temperature	5		6.5	5		8	V
I_{CC}	Supply current		20	25	32	20	25	32	mA
		Over temperature	19	25	33	19	25	33	mA
S21	Insertion gain	f=100MHz	17	19	21	17	19	21	dB
		Over temperature	16.5		21.5	16.5		21.5	
S11	Input return loss	f=100MHz D, N		25			25		dB
		DC - f_{MAX} D, N	12			12			
S22	Output return loss	f=100MHz D, N		27			27		dB
		DC - f_{MAX}	12			12			
S12	Isolation	f=100MHz		-25			-25		dB
		DC - f_{MAX}	-18			-18			
t_R	Rise time			500			500		ps
t_P	Propagation delay			500			500		ps
BW	Bandwidth	±0.5dB D, N		300			450		MHz
f_{MAX}	Bandwidth	-3dB D, N				550			MHz
	Noise figure (75Ω)	f=100MHz		4.8			4.8		dB
	Noise figure (50Ω)	f=100MHz		6.0			6.0		dB
	Saturated output power	f=100MHz		+7.0			+7.0		dBm
	1dB gain compression	f=100MHz		+4.0			+4.0		dBm
	Third-order intermodulation intercept (output)	f=100MHz		+17			+17		dBm
	Second-order intermodulation intercept (output)	f=100MHz		+24			+24		dBm

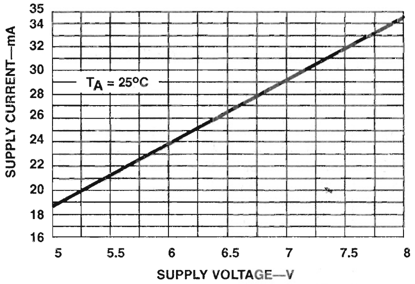


Figure 1. Supply Current vs Supply Voltage

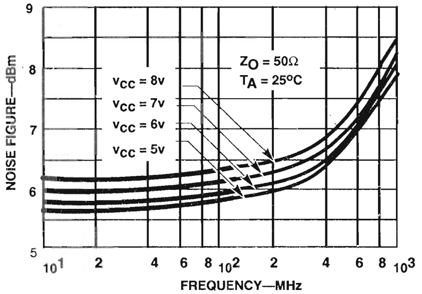


Figure 2. Noise Figure vs Frequency

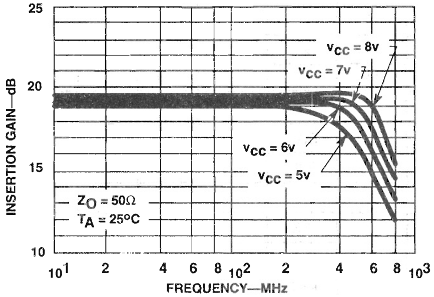


Figure 3. Insertion Gain vs Frequency (S_{21})

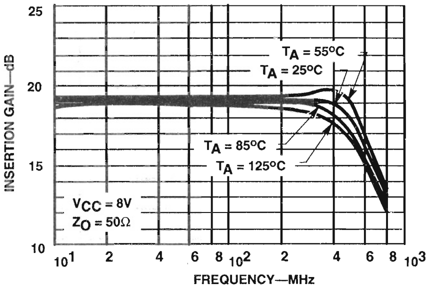


Figure 4. Insertion Gain vs Frequency (S_{21})

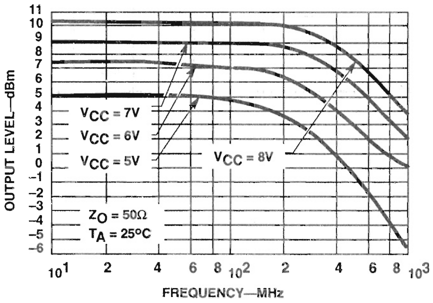


Figure 5. Saturated Output Power vs Frequency

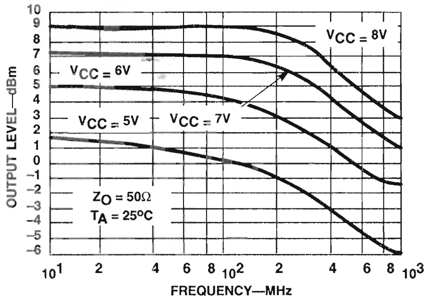


Figure 6. 1dB Gain Compression vs Frequency

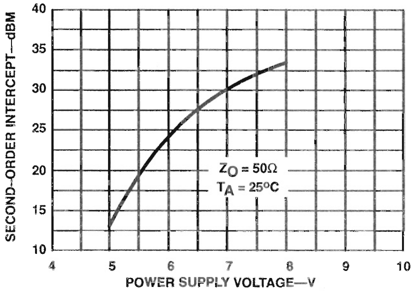


Figure 7. Second-Order Output Intercept vs Supply Voltage

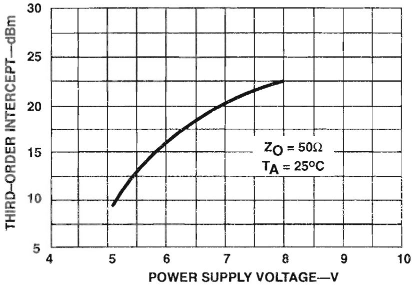


Figure 8. Third-Order Intercept vs Supply Voltage

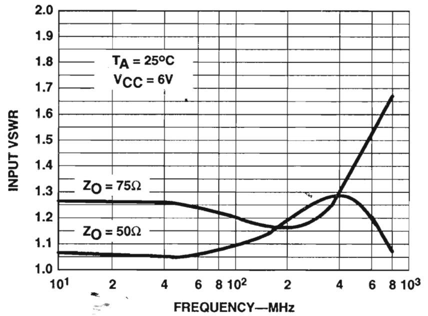


Figure 9. Input VSWR vs Frequency

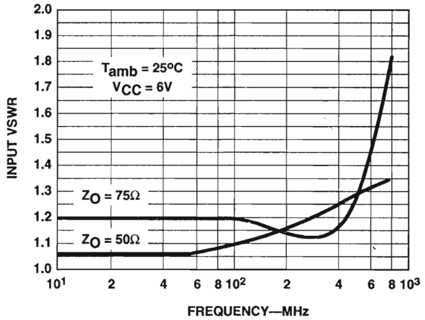


Figure 10. Output VSWR vs Frequency

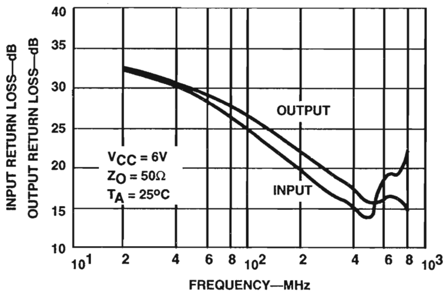


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

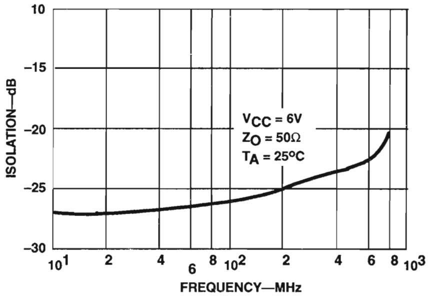


Figure 12. Isolation vs Frequency (S_{12})

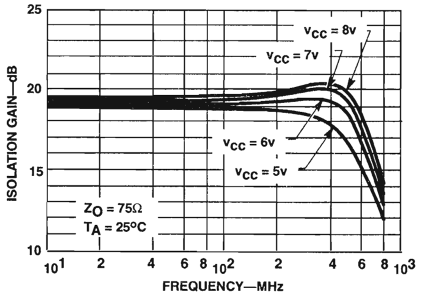


Figure 13. Insertion Gain vs Frequency (S_{21})

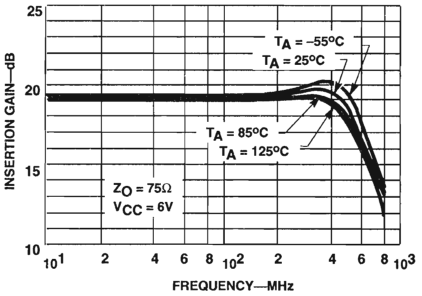


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = \frac{\left(R_{F1} + R_{E1}\right)}{R_{E1}} \qquad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible while R_{F2} is maximized.

The noise figure is given by the following equation:

NF =

$$10 \log \left[1 + \left[\frac{r_b + R_{E1} + \frac{KT}{2qI_{C1}}}{R_O}\right]\right] \text{dB} \qquad (2)$$

where I_{C1}=5.5mA, R_{E1}=12Ω, r_b=130Ω, KT/q=26mV at 25°C and R_0=50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN}=V_{BE1}+(I_{C1}+I_{C3})\ R_{E1}$$

where R_{E1}=12Ω, V_{BE}=0.8V, I_{C1}=5mA and I_{C3}=7mA (currents rated at V_{CC}=6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4 which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. The value of R_{F1}=140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT}=V_{CC}-(I_{C2}+I_{C6})R2,(4)$$

where V_{CC}=6V, R_2=225Ω, I_{C2}=8mA and I_{C6}=5mA.

From here it can be seen that the output voltage is approximately 3.1V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

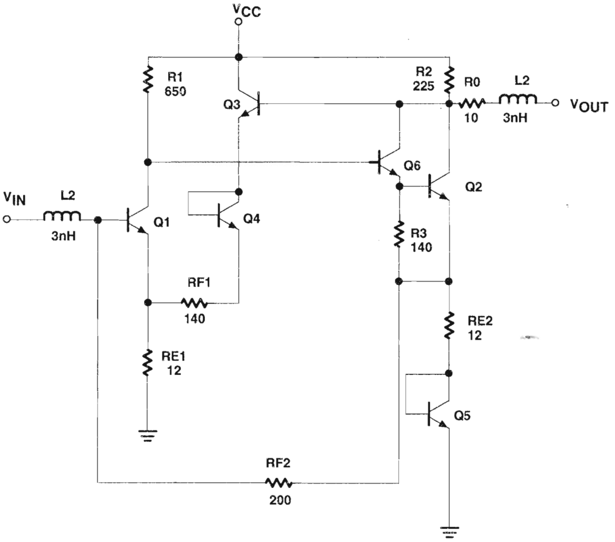


Figure 15. Schematic Diagram

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (32mA Max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat sinking benefits can be realized by mounting the D package body against the PC board plane.

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5205A to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the SO package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection.

Another important consideration is that the input and output should be AC coupled. This is because at V_{CC}=6V, the input is approximately at 1V while the output is at 3.1V. The output must be decoupled into a low impedance system or the DC bias on the output of the amplifier will be loaded down causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

SCATTERING PARAMETERS

The primary specifications for the NE/SA/SE5205A are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 18.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5205A to other high-frequency amplifiers.

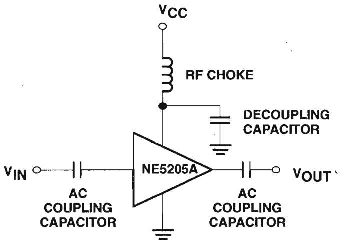
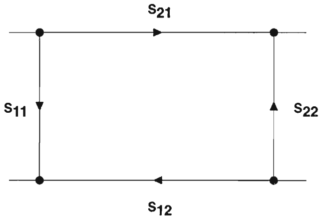


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling



a. Two-Port Network Defined

S11 — INPUT RETURN LOSS $S_{11} = \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$

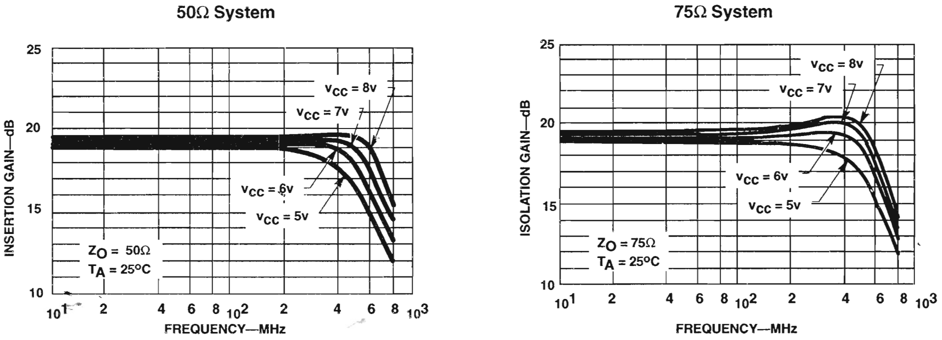
S12 — REVERSE TRANSMISSION LOSS OSOLATION $S_{12} = \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$

S21 — FORWARD TRANSMISSION LOSS OR INSERTION GAIN $S_{21} = \sqrt{\text{TRANSDUCER POWER GAIN}}$

S22 — OUTPUT RETURN LOSS $S_{22} = \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$

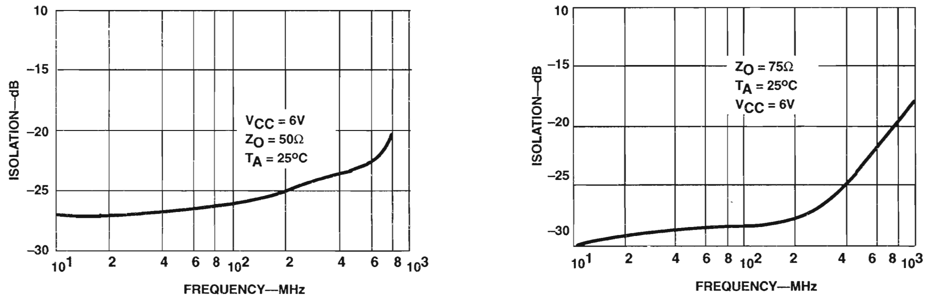
b.

Figure 17.



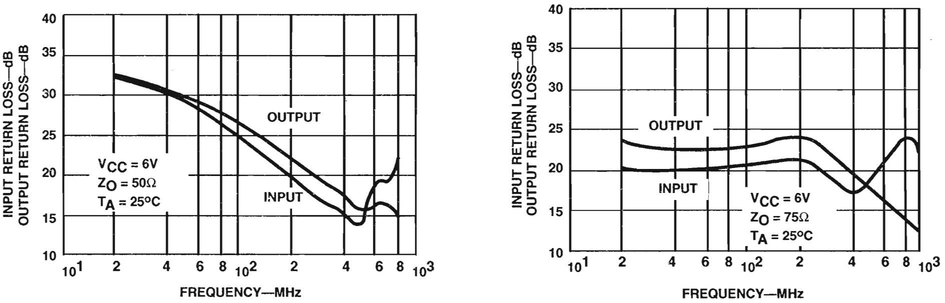
a. Insertion Gain vs Frequency (S_{21})

b. Insertion Gain vs Frequency (S_{21})



c. Isolation vs Frequency (S_{12})

d. S_{12} Isolation vs Frequency



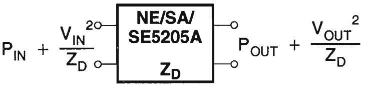
e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 18.

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_{IN} = Z_{OUT}$ for the NE/SA/SE5205A


$P_{IN} + \frac{V_{IN}^2}{Z_D}$
NE/SA/
SE5205A
Z_D
$P_{OUT} + \frac{V_{OUT}^2}{Z_D}$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$P_I = V_I^2$

P_I=Insertion Power Gain

V_I=Insertion Voltage Gain

Measured value for the
NE/SA/SE5205A = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20\text{dB}$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20\text{dB}$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS=S_{11}dB
$S_{11}\text{dB} = 20 \text{ Log } |S_{11}|$

OUTPUT RETURN LOSS=S_{22}dB
$S_{22}\text{dB} = 20 \text{ Log } |S_{22}|$

INPUT VSWR=≤1.5

OUTPUT VSWR=≤1.5

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

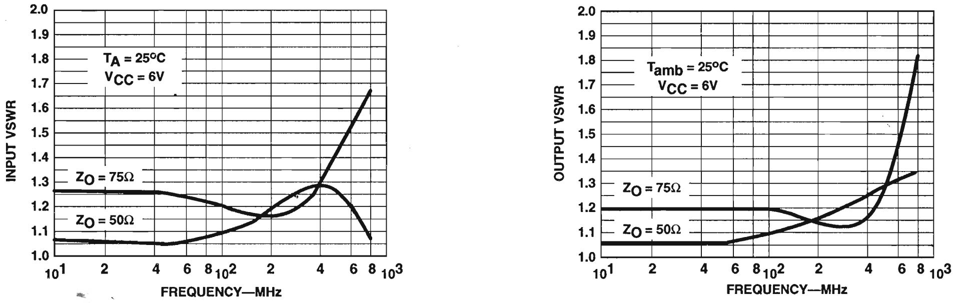
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$IP_2 = P_{OUT} + IMR_2$

$IP_3 = P_{OUT} + IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA/SE5205A we have chosen an output level of -10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.



a. Input VSWR vs Frequency

b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to High-Frequency Amplifiers by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

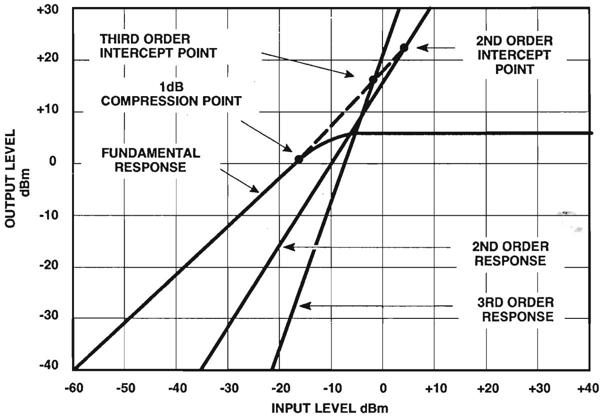


Figure 20.

Wideband variable gain amplifier NE/SA5209

DESCRIPTION

The NE5209 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

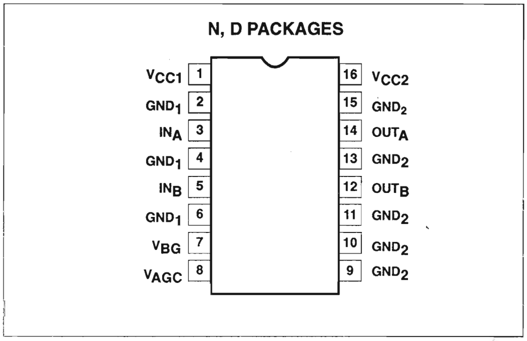
The NE5209 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5209 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

FEATURES

- Gain to 1.5GHz
- 850MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

PIN CONFIGURATION



APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5209D	0005D
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5209N	0406C
16-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5209D	0005D
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5209N	0406C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +8.0	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-Pin Plastic DIP 16-Pin Plastic SO	 1450 1100	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:

   16-Pin DIP: θ_{JA} = 85°C/W

   16-Pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	$V_{CC1} = V_{CC2}$ = 4.5 to 7.0V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, $V_{CC1} = V_{CC2}$ = +5V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{CC}	Supply current	DC tested	38	43	48	mA
		Over temperature[1]	30		55	
A_V	Voltage gain (single-ended in/single-ended out)	DC tested, R_L = 10kΩ	17	19	21	dB
		Over temperature[1]	16		22	
A_V	Voltage gain (single-ended in/differential out)	DC tested, R_L = 10kΩ	23	25	27	dB
		Over temperature[1]	22		28	
R_{IN}	Input resistance (single-ended)	DC tested at ±50μA	0.9	1.2	1.5	kΩ
		Over temperature[1]	0.8		1.7	
R_{OUT}	Output resistance (single-ended)	DC tested at ±1mA	40	60	75	Ω
		Over temperature[1]	35		90	
V_{OS}	Output offset voltage (output referred)			±20	±100	mV
		Over temperature[1]			±250	
V_{IN}	DC level on inputs		1.6	2.0	2.4	V
		Over temperature[1]	1.4		2.6	
V_{OUT}	DC level on outputs		1.9	2.4	2.9	V
		Over temperature[1]	1.7		3.1	
PSRR	Output offset supply rejection ratio (output referred)		20	45		dB
		Over temperature[1]	15			
V_{BG}	Bandgap reference voltage	$4.5V<V_{CC}<7V$ R_{BG} = 10kΩ	1.2	1.32	1.45	V
		Over temperature[1]	1.1		1.55	

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
R_{BG}	Bandgap loading	Over temperature[1]	2	10		kΩ
V_{AGC}	AGC DC control voltage range	Over temperature[1]		0-1.3		V
I_{BAGC}	AGC pin DC bias current	0V<V_{AGC}<1.3V		-0.7	-6	µA
		Over temperature[1]			-10	

NOTES:

1. "Over Temperature Range" testing is as follows:
   NE is 0 to +70°C
   SA is -40 to +85°C
   At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
BW	-3dB bandwidth		600	850		MHz
		Over temperature[1]	500			
GF	Gain flatness	DC - 500MHz		±0.4		dB
		Over temperature[1]		±0.6		
V_{IMAX}	Maximum input voltage swing (single-ended) for linear operation[2]			200		mV_{P-P}
V_{OMAX}	Maximum output voltage swing (single-ended) for linear operation[2]	R_L = 50Ω		400		mV_{P-P}
		R_L = 1kΩ		1.9		V_{P-P}
NF	Noise figure (unmatched configuration)	R_S = 50Ω, f = 50MHz		9.3		dB
V_{IN-EQ}	Equivalent input noise voltage spectral density	f = 100MHz		2.5		nV/√Hz
S12	Reverse isolation	f = 100MHz		-60		dB
$\Delta G/\Delta V_{CC}$	Gain supply sensitivity (single-ended)			0.3		dB/V
$\Delta G/\Delta T$	Gain temperature sensitivity	R_L = 50Ω		0.013		dB/°C
C_{IN}	Input capacitance (single-ended)			2		pF
BW_{AGC}	-3dB bandwidth of gain control function			20		MHz
P_{O-1dB}	1dB gain compression point at output	f = 100MHz		-3		dBm
P_{I-1dB}	1dB gain compression point at input	f = 100MHz, V_{AGC} =0.1V		-10		dBm
$IP3_{OUT}$	Third-order intercept point at output	f = 100MHz, V_{AGC} >0.5V		+13		dBm
$IP3_{IN}$	Third-order intercept point at input	f = 100MHz, V_{AGC} <0.5V		+5		dBm
ΔG_{AB}	Gain match output A to output B	f = 100MHz, V_{AGC} = 1V		0.1		dB

NOTE:

1. "Over Temperature Range" testing is as follows:
   NE is 0 to +70°C
   SA is -40 to +85°C
   At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.
2. With R_L > 1kΩ, overload occurs at input for single-ended gain < 13dB and at output for single-ended gain > 13dB. With R_L = 50Ω, overload occurs at input for single-ended gain < 6dB and at output for single-ended gain > 6dB.

NE5209 APPLICATIONS

The NE5209 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 1. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V_{AGC} input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The NE5209 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 - 7V) that can be used.

The input impedance is about 1kΩ. The main advantage to a differential input configuration is to provide the balun function. Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about 1kΩ. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω. A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output is used and properly matched, nearly 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The NE5209 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5209 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The NE5209 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the NE5209. A maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the NE5209 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path, and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the NE5209 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the NE5209 is shown in Figure 2. Three NE5209s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes BAT17 as shown. The diodes are biased by R1 and R2 to V_{CC} such that a quiescent current of about 2mA in each leg is achieved. An NE5230 low voltage op amp is used as an integrator which drives the V_{AGC} pin on all three NE5209s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three NE5209s will give a dynamic range in excess of 60dB.

The NE5209 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

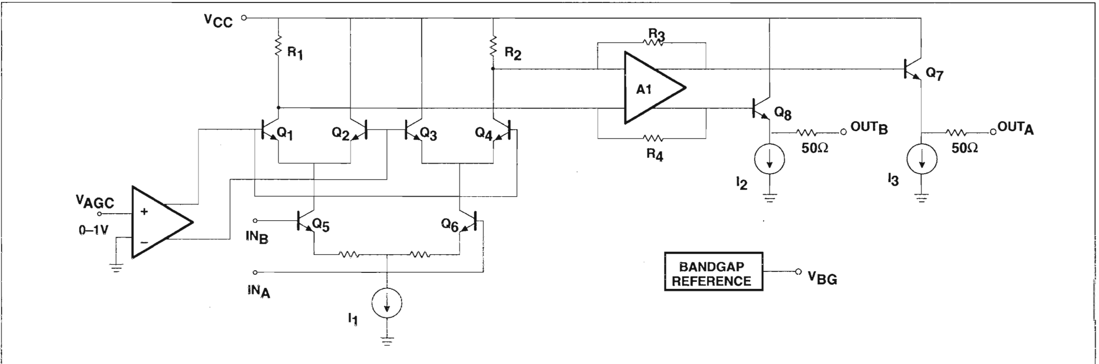


Figure 1. Equivalent Schematic of the VGA

$R_1 = R_2 = 3.9k$
$R_3 = 360\Omega$
$R_4 = 62k$
$R_5 = 100\Omega$
$R_6 = 1k$ pot
$2\pi fL_1 = 10k$
$L_1 = L_2$

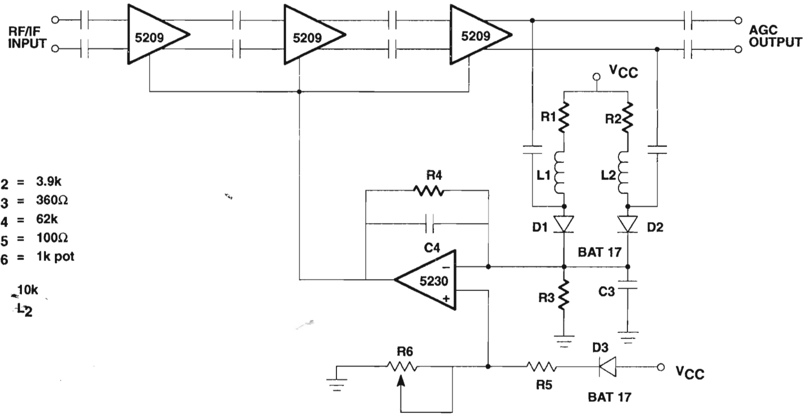


Figure 2. AGC Configuration Using Cascaded NE5209s

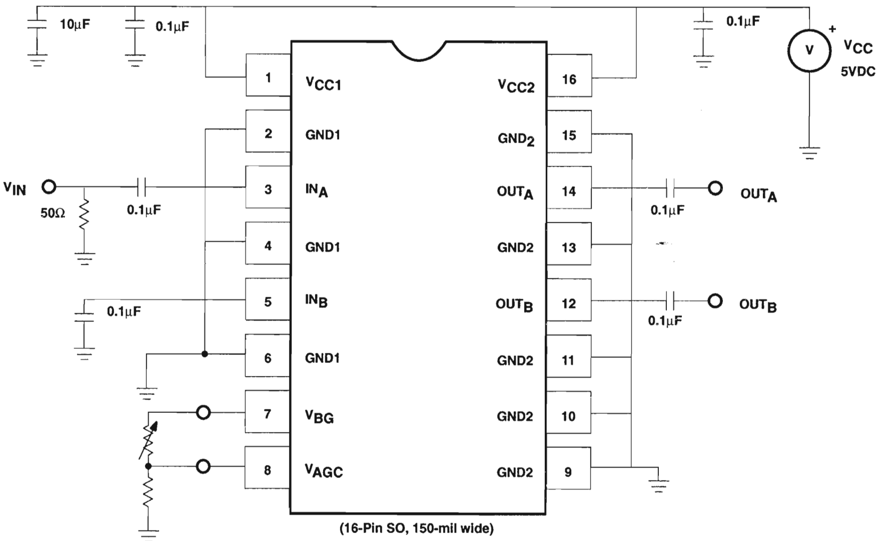
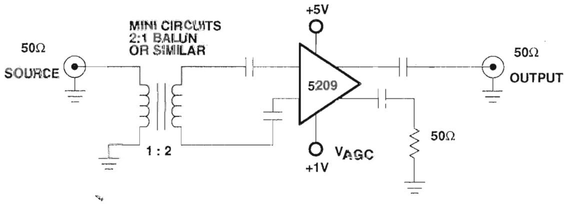
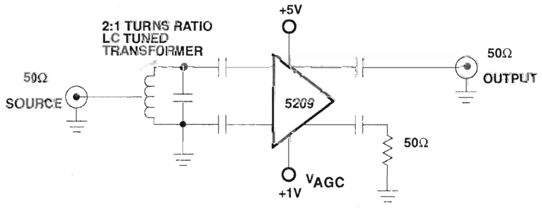


Figure 3. VGA AC Evaluation Board



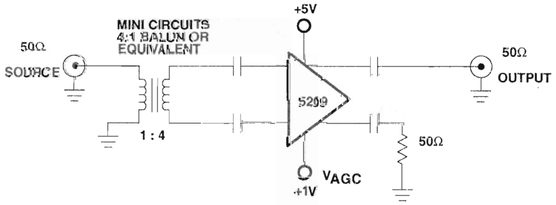
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain.

Figure 4. Broadband Noise Optimization



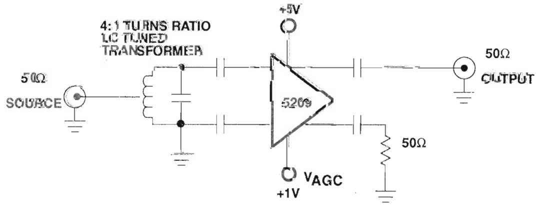
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain. Narrowband circuits have the advantage of greater stability, particularly when multiple devices are cascaded.

Figure 5. Narrowband Noise Optimization



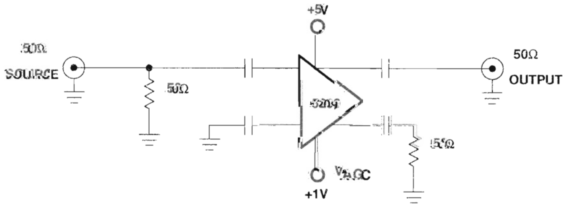
This circuit will exhibit about an 8dB noise figure with 24dB gain.

Figure 6. Broadband Gain Optimization



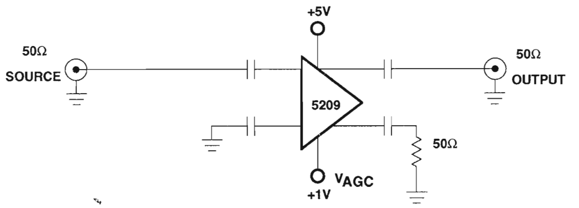
This circuit will exhibit approximately an 8dB noise figure and 25dB gain.

Figure 7. Narrowband Gain Optimization



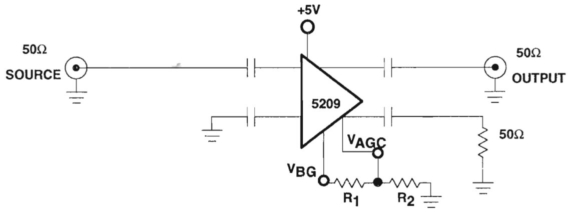
The noise figure of this configuration will be approximately 15dB.

Figure 8. Simple Amplifier Configuration



With the 50Ω source left unterminated, the noise figure is 9dB.

Figure 9. Unterminated Configuration

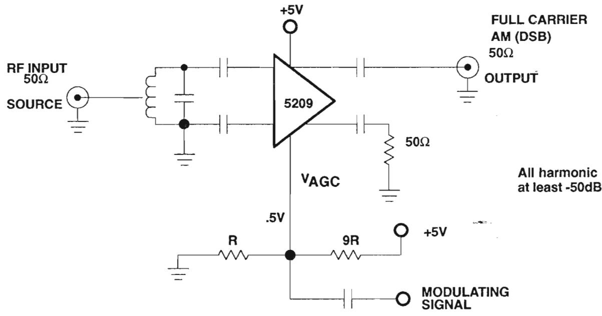


$$\text{Gain} = 19\text{dB} + 20\log_{10} V_{AGC}$$

$$\text{where } V_{AGC} = \left[\frac{R_2}{R_1 + R_2} V_{BG}\right]$$

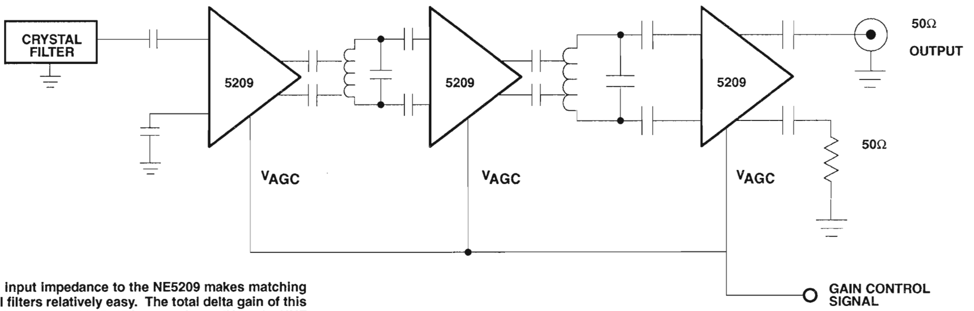
and is in units of Volts, for $V_{AGC} \leq 1V$

Figure 10. User-Programmable Fixed Gain Block



All harmonic distortion products will be at least -50dBc over the audio spectrum.

Figure 11. AM Modulator



The high input impedance to the NE5209 makes matching to crystal filters relatively easy. The total delta gain of this system will approach 80dB. IF frequencies well into the UHF region can be configured with this type of architecture.

Figure 12. Receiver AGC IF Gain

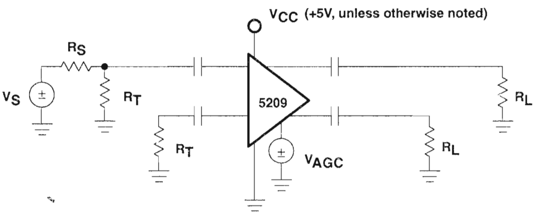


Figure 13. Test Set-up 1 (Used for all Graphs)

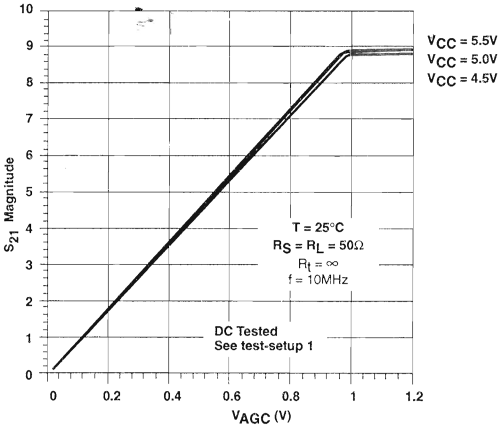


Figure 14. Gain vs V_{AGC} and V_{CC}

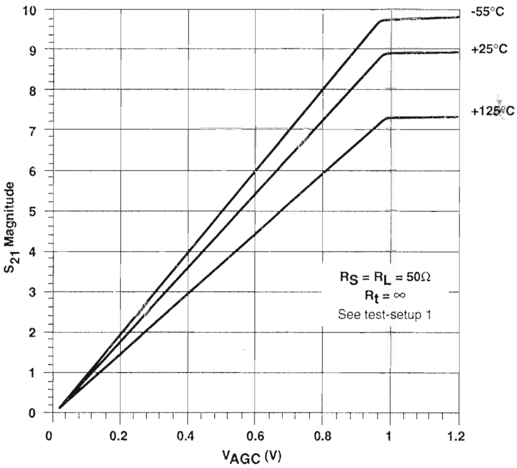


Figure 15. Insertion Gain vs V_{AGC} and Temperature

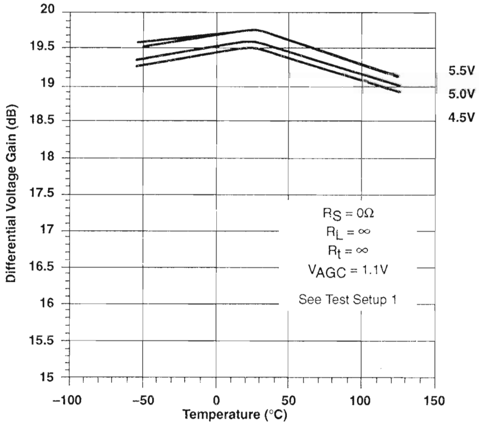


Figure 16. Voltage Gain vs Temperature and V_{CC}

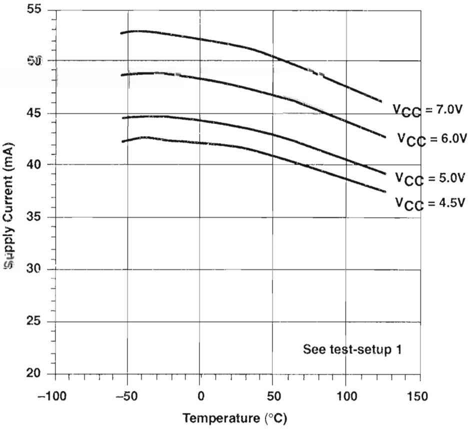


Figure 17. Supply Current vs Temperature and V_{CC}

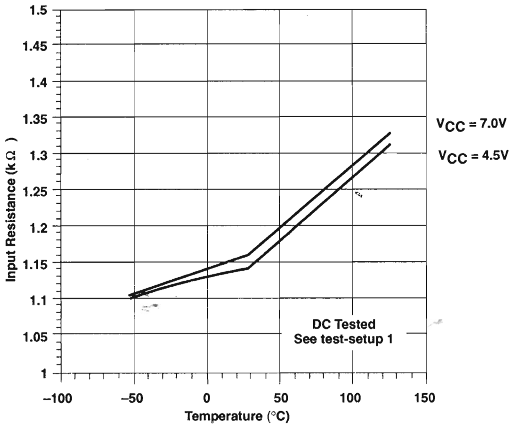


Figure 18. Input Resistance vs Temperature

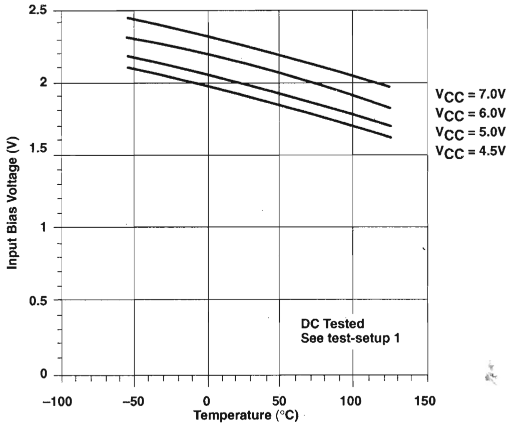


Figure 19. Input Bias Voltage vs Temperature

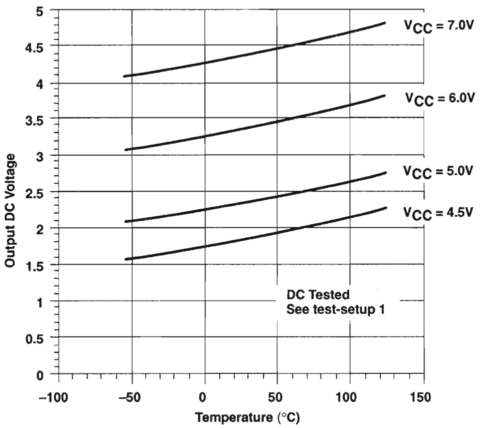


Figure 20. Output Bias Voltage vs Temperature and V_{CC}

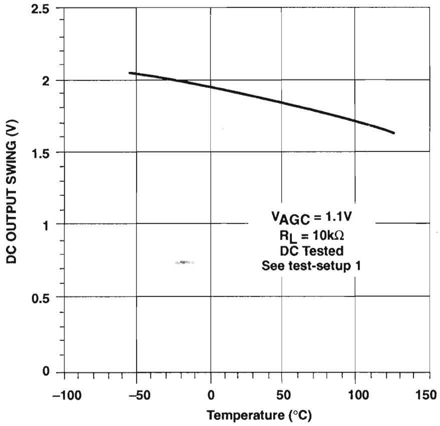


Figure 21. DC Output Swing vs Temperature

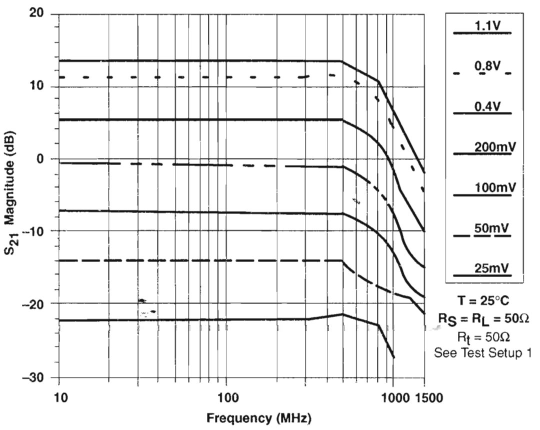


Figure 22. Insertion Gain vs Frequency and V_{AGC}

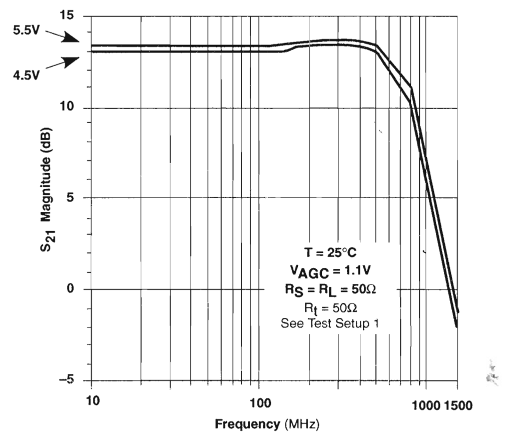


Figure 23. Insertion Gain vs Frequency and V_{CC}

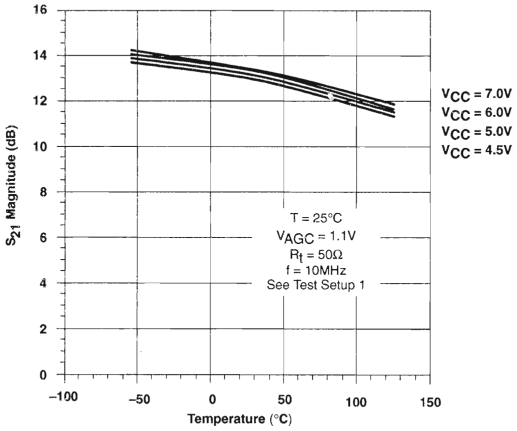


Figure 24. Insertion Gain vs Temperature and V_{CC}

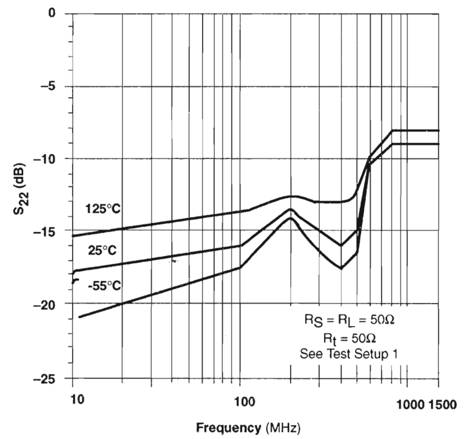


Figure 25. Output Return Loss vs Frequency

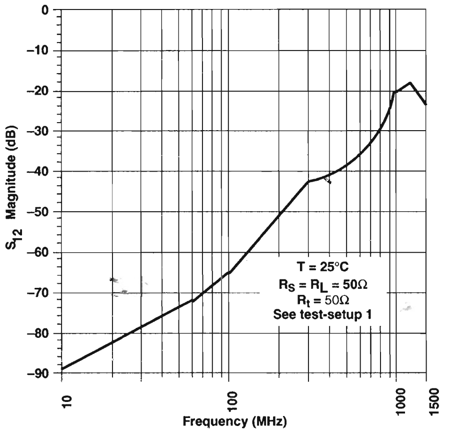


Figure 26. Reverse Isolation vs Frequency

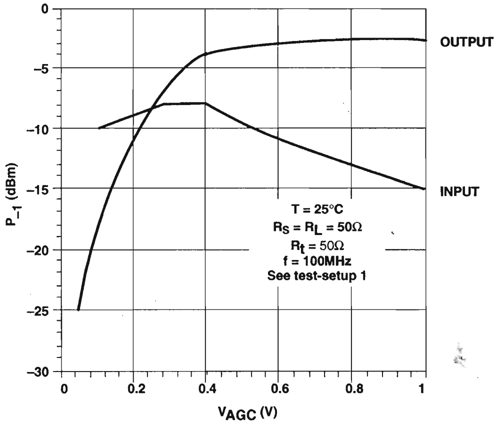


Figure 27. 1dB Gain Compression vs V_{AGC}

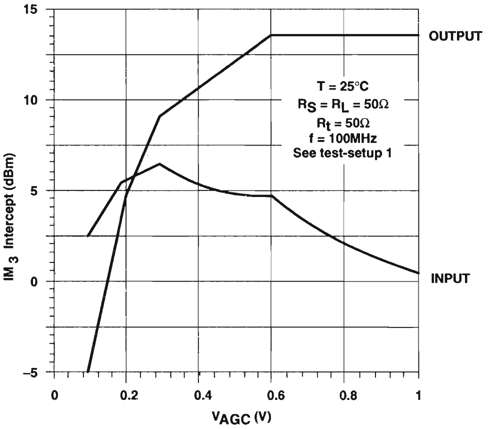


Figure 28. Third-Order Intermodulation Intercept vs V_{AGC}

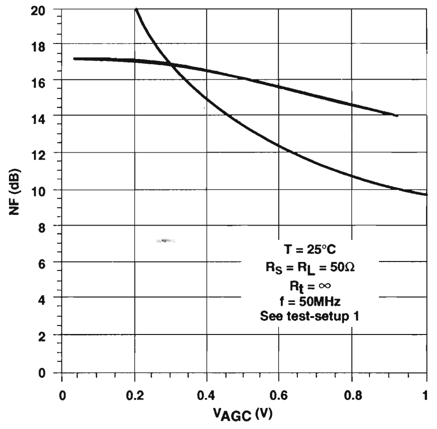


Figure 29. Noise Figure vs V_{AGC}

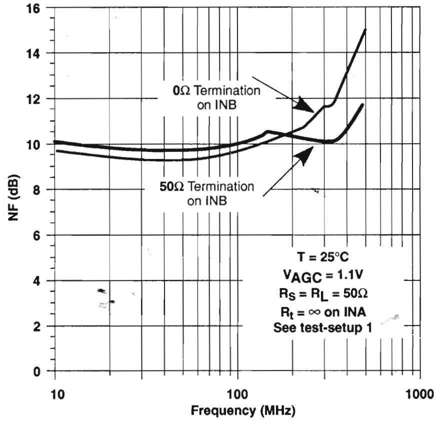


Figure 30. Noise Figure vs Frequency

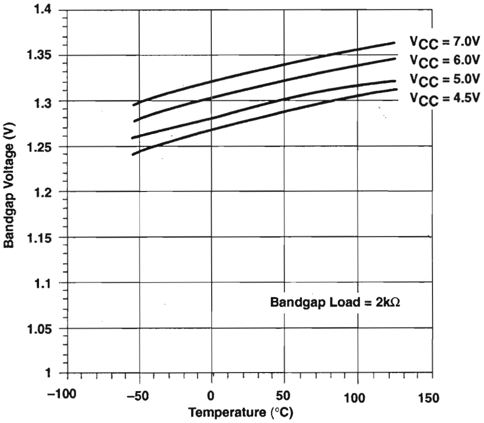


Figure 31. Bandgap Voltage vs Temperature and V_{CC}

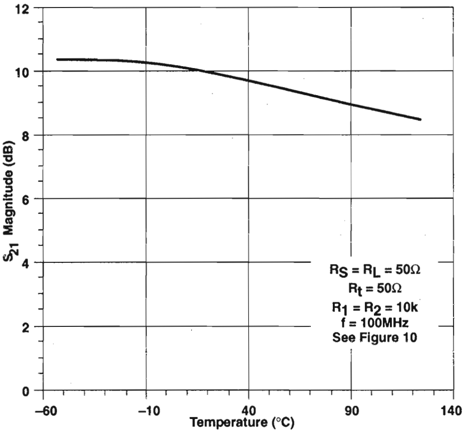
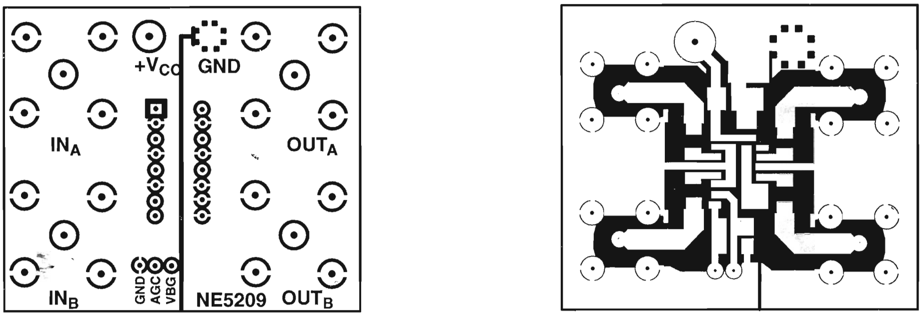


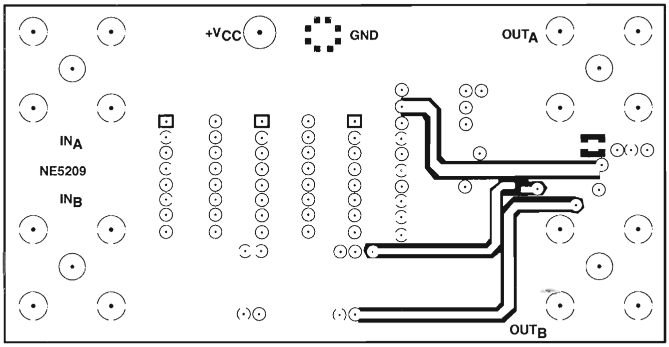
Figure 32. Fixed Gain vs Temperature



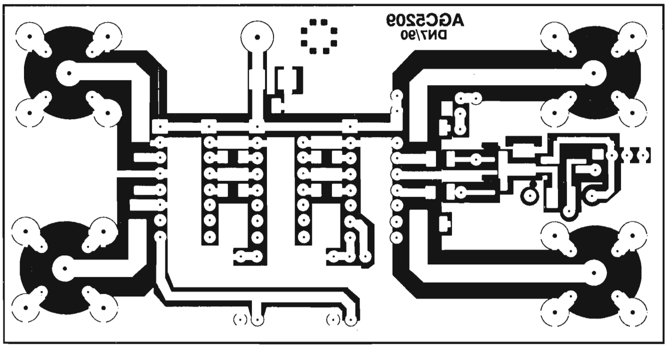
TOP VIEW - COMPONENT SIDE

TOP VIEW - SOLDER SIDE

VGA AC Evaluation Board Layout

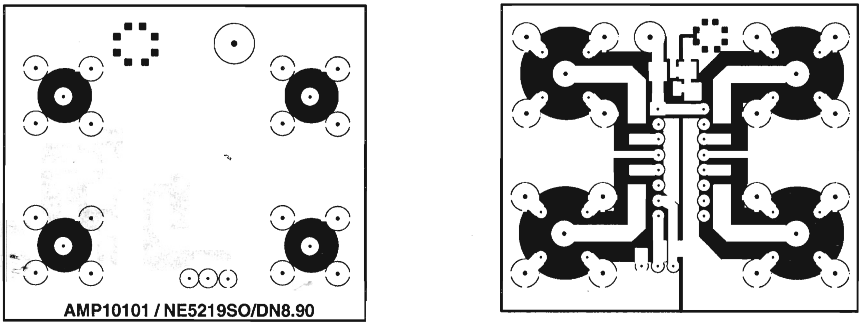


TOP VIEW - COMPONENT SIDE



TOP VIEW - SOLDER SIDE

AGC Configuration Using Cascaded NE5209s - Layout



TOP VIEW - COMPONENT SIDE

TOP VIEW - SOLDER SIDE

VGA AC Evaluation Board Layout (DIP Package)

Wideband variable gain amplifier NE/SA5219

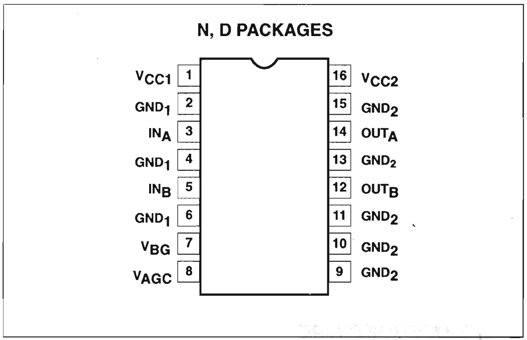
DESCRIPTION

The NE5219 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The NE5219 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5219 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

PIN CONFIGURATION



FEATURES

- 700MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

ORDERING INFORMATION

Description	Temperature Range	Order Code	DWG #
16-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5219D	0005D
16-Pin Plastic Dual In-Line package (DIP)	0 to +70°C	NE5219N	0406C
16-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5219D	0005D
16-Pin Plastic Dual In-Line package (DIP)	-40 to +85°C	SA5219N	0406C

Wideband variable gain amplifier NE/SA5219

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +8.0	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-Pin Plastic DIP 16-Pin Plastic SO	 1450 1100	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   16-Pin DIP: θ_{JA} = 85°C/W
   16-Pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	$V_{CC1} = V_{CC2}$ = 4.5 to 7.0V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, $V_{CC1} = V_{CC2}$ = +5V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{CC}	Supply current	DC tested	36	43	50	mA
A_V	Voltage gain (single-ended in/single-ended out)	DC tested, R_L = 10kΩ	16	19	22	dB
A_V	Voltage gain (single-ended in/differential out)	DC tested, R_L = 10kΩ	22	25	28	dB
R_{IN}	Input resistance (single-ended)	DC tested at ±50μA	0.8	1.2	1.6	kΩ
R_{OUT}	Output resistance (single-ended)	DC tested at ±1mA	35	60	80	Ω
V_{OS}	Output offset voltage (output referred)			±20	±150	mV
V_{IN}	DC level on inputs		1.6	2.0	2.4	V
V_{OUT}	DC level on outputs		1.9	2.4	2.9	V
PSRR	Output offset supply rejection ratio		18	45		dB
V_{BG}	Bandgap reference voltage	$4.5V<V_{CC}<7V$ R_{BG} = 10kΩ	1.2	1.32	1.45	V
R_{BG}	Bandgap loading		2	10		kΩ
V_{AGC}	AGC DC control voltage range			0-1.3		V
I_{BAGC}	AGC pin DC bias current	$0V<V_{AGC}<1.3V$		-0.7	-6	μA

AC ELECTRICAL CHARACTERISTICS

$T_A = 25^oC$, $V_{CC1} = V_{CC2} = +5.0V$, $V_{AGC} = 1.0V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
BW	-3dB bandwidth			700		MHz
GF	Gain flatness	DC - 500MHz		±0.4		dB
V_{IMAX}	Maximum input voltage swing (single-ended) for linear operation[1]			200		mV_{P-P}
V_{OMAX}	Maximum output voltage swing (single-ended) for linear operation[1]	$R_L = 50\Omega$		400		mV_{P-P}
		$R_L = 1k\Omega$		1.9		V_{P-P}
NF	Noise figure (unmatched configuration)	$R_S = 50\Omega$, f = 50MHz		9.3		dB
V_{IN-EQ}	Equivalent input noise voltage spectral density	f = 100MHz		2.5		$nV/\sqrt{Hz}$
S12	Reverse isolation	f = 100MHz		-60		dB
$\Delta G/\Delta V_{CC}$	Gain supply sensitivity (single-ended)			0.3		dB/V
$\Delta G/\Delta T$	Gain temperature sensitivity	$R_L = 50\Omega$		0.013		dB/°C
C_{IN}	Input capacitance (single-ended)			2		pF
BW_{AGC}	-3dB bandwidth of gain control function			20		MHz
P_{O-1dB}	1dB gain compression point at output	f = 100MHz		-3		dBm
P_{I-1dB}	1dB gain compression point at input	f = 100MHz, V_{AGC} =0.1V		-10		dBm
$IP3_{OUT}$	Third-order intercept point at output	f = 100MHz, V_{AGC} >0.5V		+13		dBm
$IP3_{IN}$	Third-order intercept point at input	f = 100MHz, V_{AGC} <0.5V		+5		dBm
ΔG_{AB}	Gain match output A to output B	f = 100MHz, V_{AGC} = 1V		0.1		dB

NOTE:

1. With $R_L > 1k\Omega$, overload occurs at input for single-ended gain < 13dB and at output for single-ended gain > 13dB. With $R_L = 50\Omega$, overload occurs at input for single-ended gain < 6dB and at output for single-ended gain > 6dB.

NE5219 APPLICATIONS

The NE5219 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 1. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V_{AGC} input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The NE5219 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 - 7V) that can be used.

The input impedance is about 1kΩ. The main advantage to a differential input configuration is to provide the balun function. Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about 1kΩ. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω. A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output is used and properly matched, nearly 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The NE5219 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5219 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The NE5219 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the NE5219. A maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the NE5219 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path, and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the NE5219 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the NE5219 is shown in Figure 2. Three NE5219s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes BAT17 as shown. The diodes are biased by R1 and R2 to V_{CC} such that a quiescent current of about 2mA in each leg is achieved. An NE5230 low voltage op amp is used as an integrator which drives the V_{AGC} pin on all three NE5219s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three NE5219s will give a dynamic range in excess of 60dB.

The NE5219 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

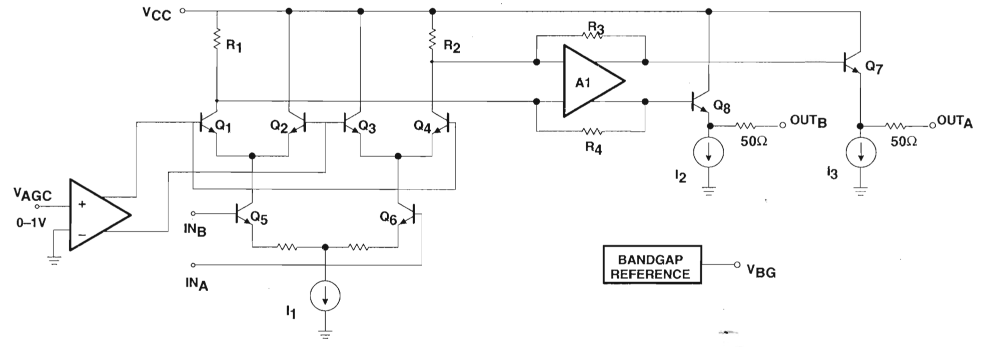


Figure 1. Equivalent Schematic of VGA

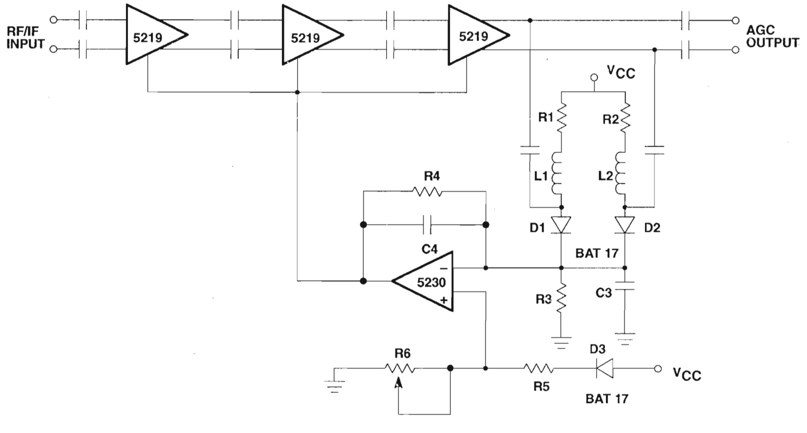


Figure 2. AGC Configuration Using Cascaded NE5219s

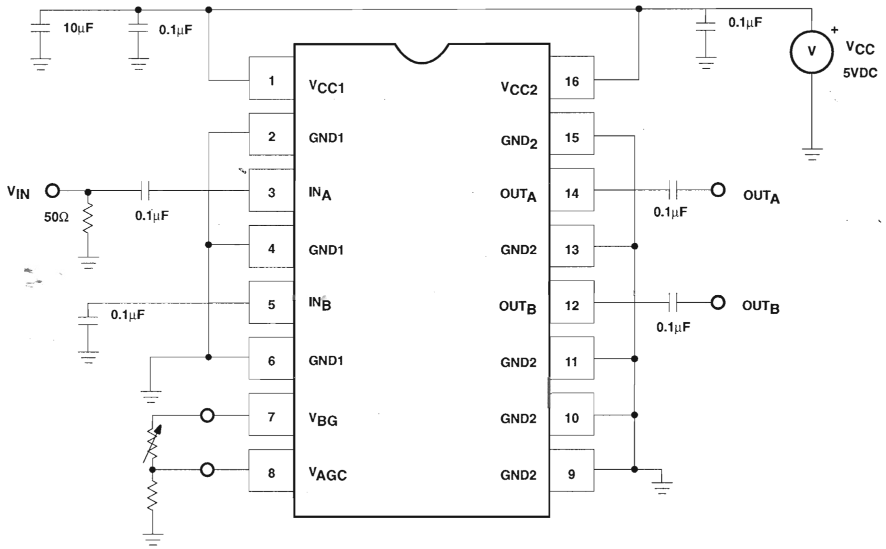
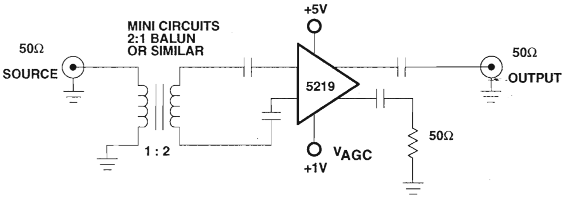
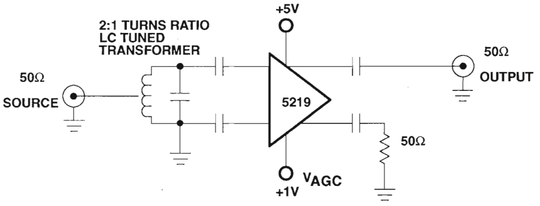


Figure 3. VGA AC Evaluation Board



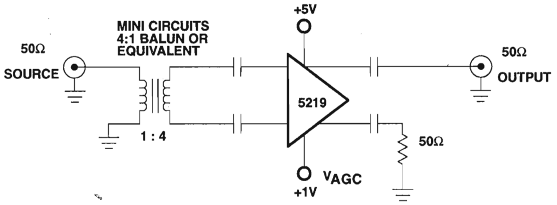
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain.

Figure 4. Broadband Noise Optimization



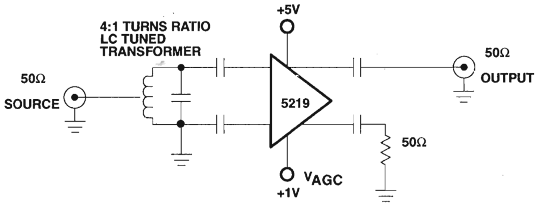
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain. Narrowband circuits have the advantage of greater stability, particularly when multiple devices are cascaded.

Figure 5. Narrowband Noise Optimization



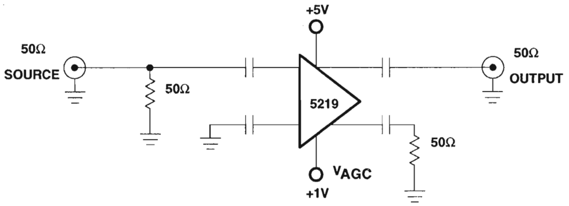
This circuit will exhibit about an 8dB noise figure with 24dB gain.

Figure 6. Broadband Gain Optimization



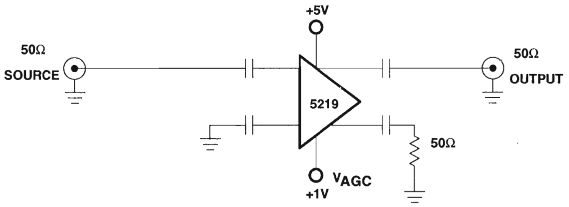
This circuit will exhibit approximately an 8dB noise figure and 25dB gain.

Figure 7. Narrowband Gain Optimization



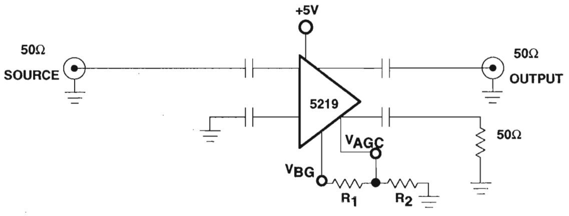
The noise figure of this configuration will be approximately 15dB.

Figure 8. Simple Amplifier Configuration



With the 50Ω source left unterminated, the noise figure is 9dB.

Figure 9. Unterminated Configuration

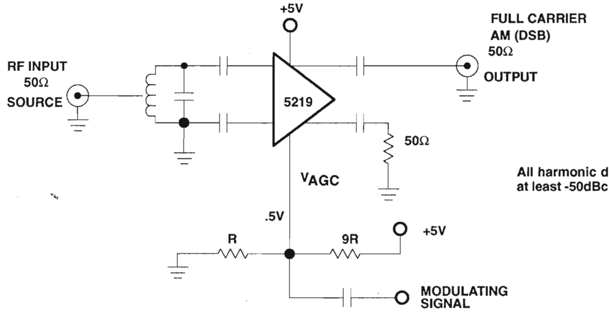


Gain = 19dB + $20\log_{10} V_{AGC}$

where $V_{AGC} = \left[\frac{R_2}{R_1 + R_2} V_{BG} \right]$

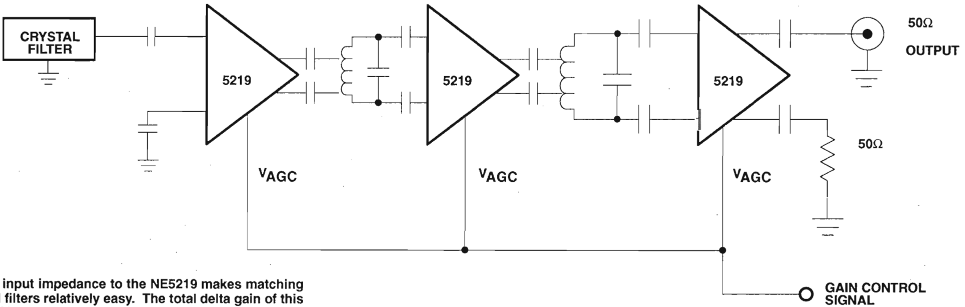
and is in units of Volts, for $V_{AGC} \leq 1V$

Figure 10. User-Programmable Fixed Gain Block



All harmonic distortion products will be at least -50dBc over the audio spectrum.

Figure 11. AM Modulator



The high input impedance to the NE5219 makes matching to crystal filters relatively easy. The total delta gain of this system will approach 80dB. IF frequencies well into the UHF region can be configured with this type of architecture.

Figure 12. Receiver AGC IF Gain

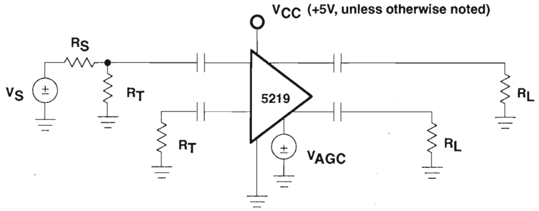


Figure 13. Test Set-up 1 (Used for all Graphs)

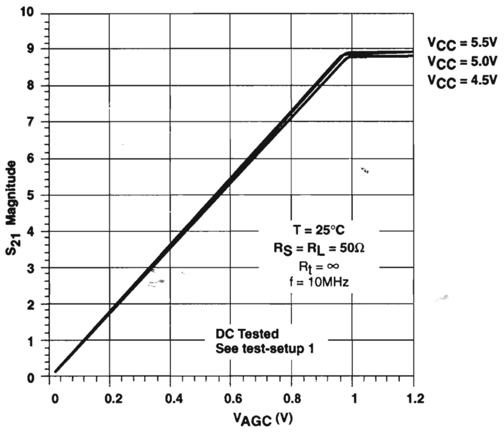


Figure 14. Gain vs V_{AGC} and V_{CC}

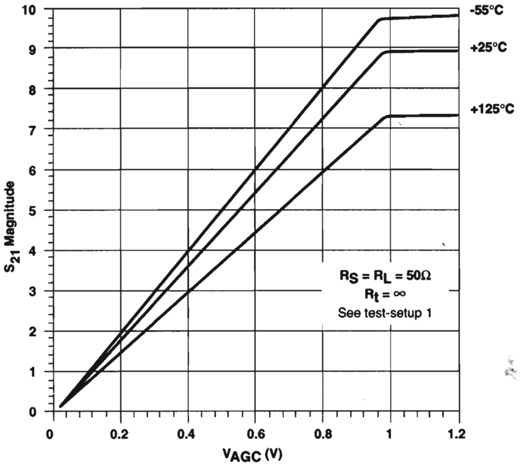


Figure 15. Insertion Gain vs V_{AGC} and Temperature

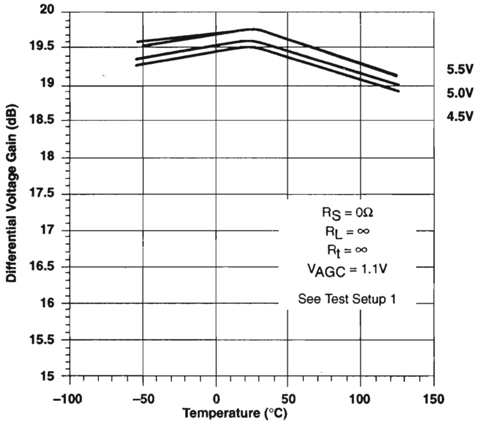


Figure 16. Voltage Gain vs Temperature and V_{CC}

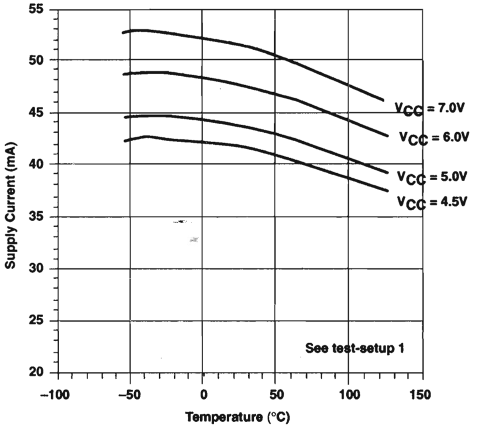


Figure 17. Supply Current vs Temperature and V_{CC}

Wideband variable gain amplifier NE/SA5219

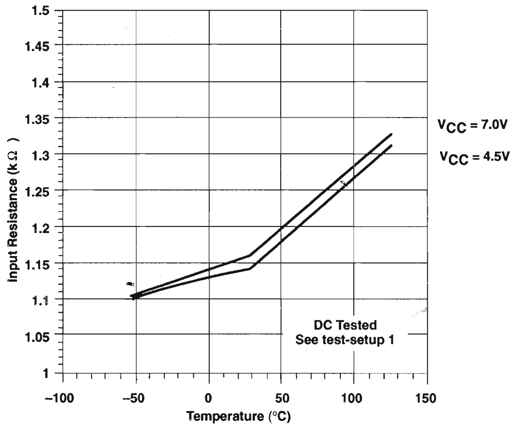


Figure 18. Input Resistance vs Temperature

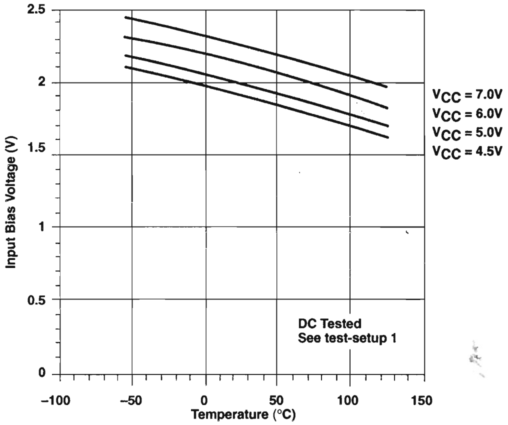


Figure 19. Input Bias Voltage vs Temperature

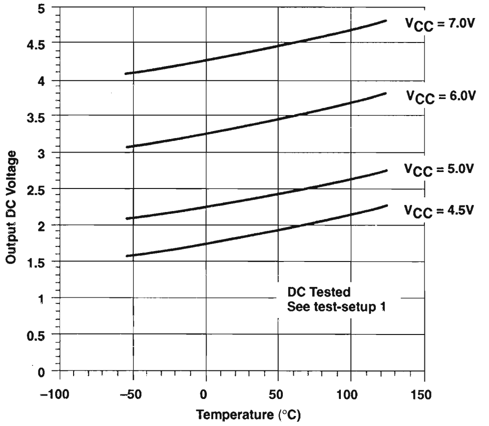


Figure 20. Output Bias Voltage vs Temperature and V_{CC}

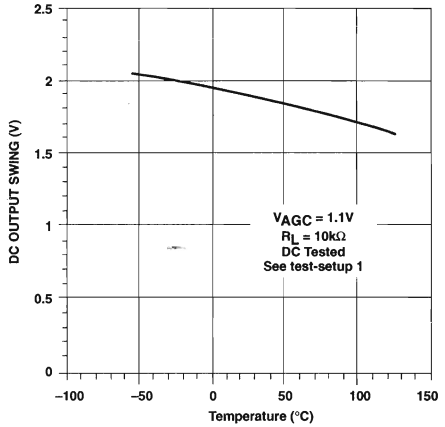


Figure 21. DC Output Swing vs Temperature

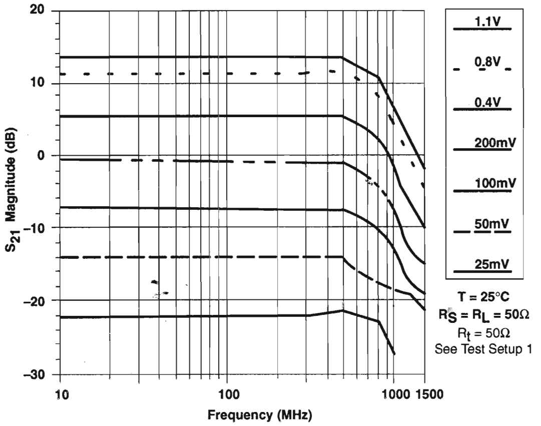


Figure 22. Insertion Gain vs Frequency and V_{AGC}

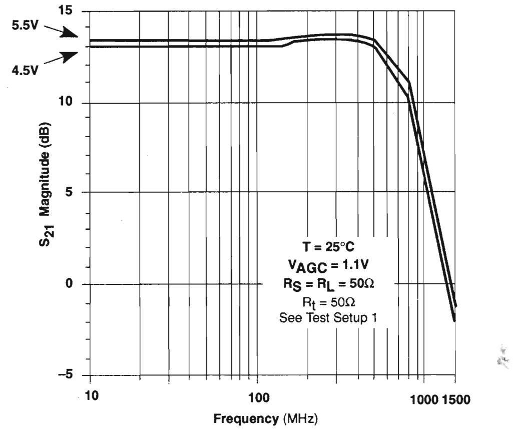


Figure 23. Insertion Gain vs Frequency and V_{CC}

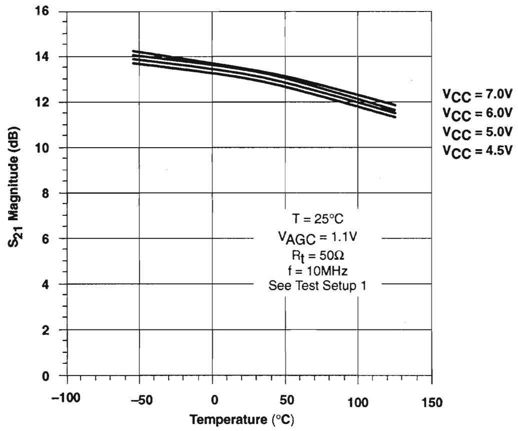


Figure 24. Insertion Gain vs Temperature and V_{CC}

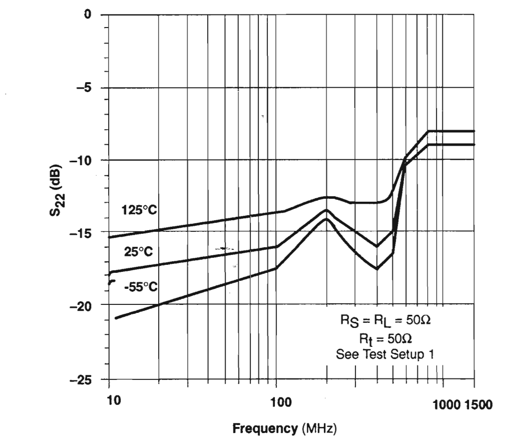


Figure 25. Output Return Loss vs Frequency

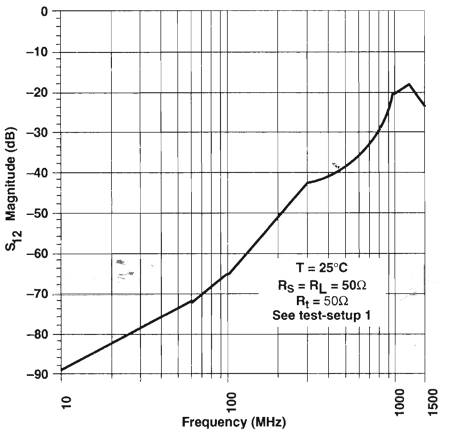


Figure 26. Reverse Isolation vs Frequency

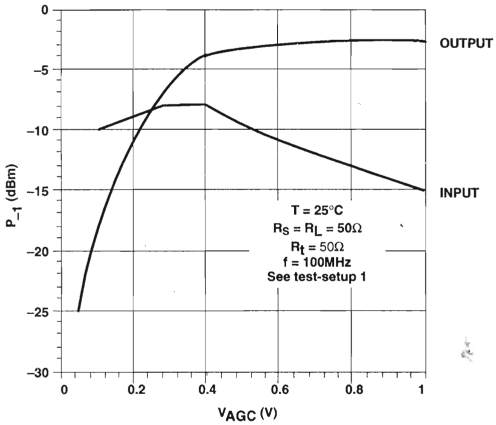


Figure 27. 1dB Gain Compression vs V_{AGC}

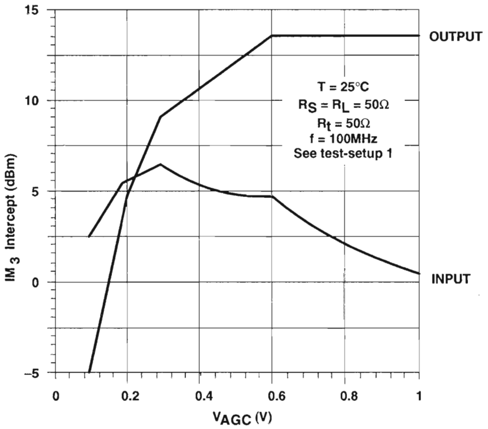


Figure 28. Third-Order Intermodulation Intercept vs V_{AGC}

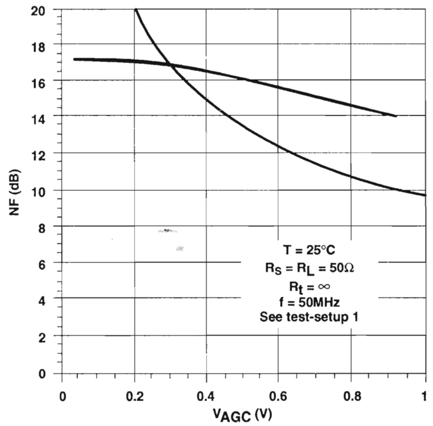


Figure 29. Noise Figure vs V_{AGC}

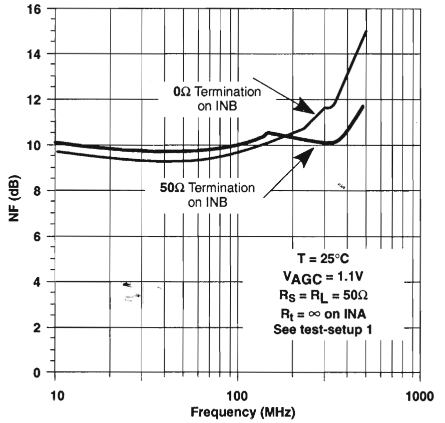


Figure 30. Noise Figure vs Frequency

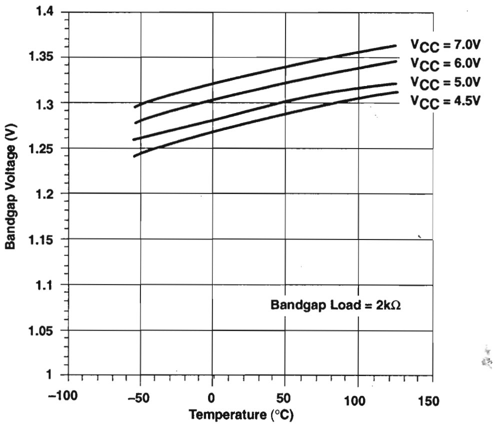


Figure 31. Bandgap Voltage vs Temperature and V_{CC}

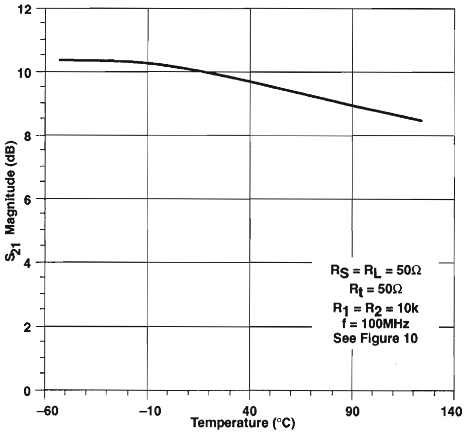
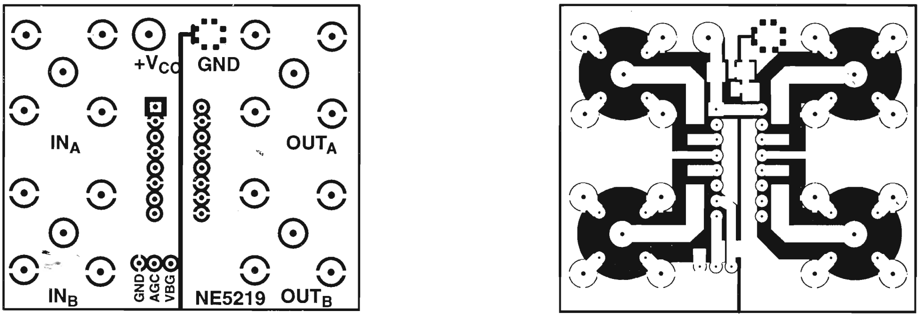


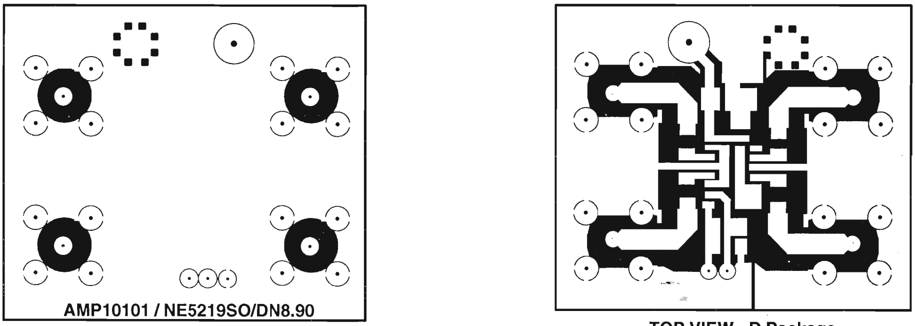
Figure 32. Fixed Gain vs Temperature



TOP VIEW - COMPONENT SIDE

TOP VIEW - SOLDER SIDE

VGA AC Evaluation Board Layout (DIP Package)



BOTTOM VIEW - D Package

TOP VIEW - D Package

VGA AC Evaluation Board Layout (SO Package)

Matched quad high-performance low-voltage operational amplifier

NE/SA5234

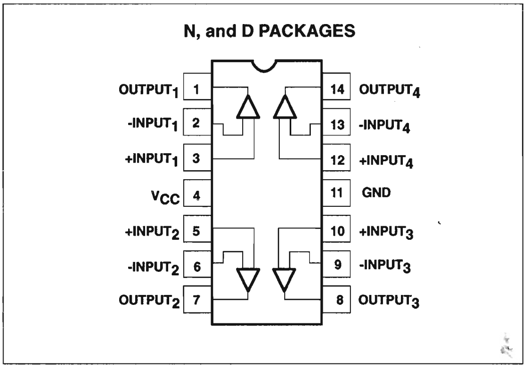
DESCRIPTION

The NE/SA5234 is a matched, low voltage, high performance quad operational amplifier. Among its unique input and output characteristics is the capability for both input and output rail-to-rail operation, particularly critical in low voltage applications. The output swings to less than 50mV of both rails across the entire power supply range. The NE/SA5234 is capable of delivering 5.5V peak-to-peak across a 600Ω load and will typically draw only 700µA per amplifier. The bandwidth is 2.5MHz and the 1% settling time is 1.4µs.

FEATURES

- Wide common-mode input voltage range: 250mV beyond both rails
- Output swing within 50mV of both rails
- Functionality to 1.8V typical
- Low current consumption: 700µA per amplifier
- ±15mA output current capability
- Unity gain bandwidth: 2.5MHz
- Slew rate: 0.8V/µs
- Low noise: 25nV/√Hz
- Electrostatic discharge protection
- Short-circuit protection
- Output inversion prevention

PIN CONFIGURATION



N, and D PACKAGES

APPLICATIONS

- Automotive electronics
- Signal conditioning and sensing amplification
- Portable instrumentation
  - Test and measurement
  - Medical monitors and diagnostics
  - Remote meters
- Audio equipment
- Security systems
- Communications
  - Pagers
  - Cellular telephone
  - LAN
  - 5V Datacom bus
- Error amplifier in motor drives
- Transducer buffer amplifier

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5234D	0175D
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5234N	0405B
14-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5234D	0175D
14-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5234N	0405B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
V_{ESD}	ESD protection voltage at any pin[5]		
	human body model	2000	V
	robot model	200	V
V_S	Dual supply voltage	±3.5	V
V_{DP}	Voltage at any device pin[1]	$V_S \pm 0.5$	V
I_{DP}	Current into any device pin[1]	± 50	mA
V_{IN}	Differential input voltage[2]	0.5	V
V_{CM}	Common-mode input voltage (positive)	$V_{CC} + 0.5$	V
V_{CM}	Common-mode input voltage (negative)	$V_{EE} - 0.5$	V
P_D	Power dissipation[3]	500	mW
T_J	Operating junction temperature[3]	+150	°C
V_{SC}	Supply voltage allowing indefinite output short circuit to either rail[3,4]	7	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C
θ_{JA}	Thermal impedance		
	14 pin Plastic DIP	80	°C/W
	14 pin Plastic SO	115	°C/W

NOTES:

1. Each pin is protected by ESD diodes. The voltage at any pin is limited by the ESD diodes.
2. The differential input of each amplifier is limited by two internal diodes, connected in parallel and opposite to each other. For more differential input range, use differential resistors in series with the input pins.
3. The maximum operating junction temperature is +150°C. At elevated temperatures, devices must be derated according to the package thermal resistance and device mounting conditions. Derates above +25°C: F package at 6.7mW/°C; N package at 9.5mW/°C; D package at 6.25mW/°C.
4. Simultaneous short circuits of two or more amplifiers to the positive or negative rail can exceed the power dissipation ratings and cause eventual destruction of the device.
5. Guaranteed by design.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	+2 to +5.5	V
V_S	Dual supply voltage	±1 to ±2.75	V
V_{CM}	Common-mode input voltage (positive)	$V_{CC} + 0.25$	V
V_{CM}	Common-mode input voltage (negative)	$V_{EE} - 0.25$	V
T_A	Temperature		
	NE	0 to +70	°C
	SA	-40 to +85	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2 to 5.5V, V_{EE} = 0V, T_A = 25°C; $V_{EE} < V_{CM} < V_{CC}$; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE5234			SA5234			
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_{CC} = 5.5V		2.8	4.0		2.8	4.0	mA
		V_{CC} = 5.5V over full temperature range		3.0	4.6		3.2	4.8	
V_{OS}	Offset voltage			±0.2	±4		±0.2	±4	mV
		Over full temperature range		±0.4	±5		±0.6	±5	
$\Delta V_{OS}/\Delta T$	Offset voltage drift with temperature			4			4		μV/°C
ΔV_{OS}	Offset voltage difference between any amplifiers in the same package at the same common mode level[1]			0.4	3		0.4	3	mV
		Over full temperature range		0.8	4		1.2	4	
I_{OS}	Offset current			±3	±20		±3	±30	nA
		Over full temperature range		±4	±30		±6	±60	
$\Delta I_{OS}/\Delta T$	Offset current drift with temperature			0.02	±.3		0.03	±.3	nA/°C
I_B	Input bias current[1]	$V_{EE} < V_{CM} < V_{EE}$ +0.5V	-200	-90		-200	-90		nA
		Over full temperature range	-225	-100		-250	-150		
		V_{EE} +1V < $V_{CM} < V_{CC}$		25	70		25	75	
		Over full temperature range		35	100		35	120	
$\Delta I_B/\Delta T$	Input bias current drift with temperature			0.5			0.5		nA/°C
ΔI_B	Input bias current difference between any amplifier in the same package at the same common mode level.	$V_{EE} < V_{CM} < V_{EE}$ +0.5V		10	30		10	30	nA
		Over full temperature range		25	50		50	70	
		V_{EE} +1V < $V_{CM} < V_{CC}$		5	20		5	20	
		Over full temperature range		15	30		25	50	
V_{CM}	Common-mode input range	$V_{OS} \leq$ 6mV	V_{EE}-0.25		V_{CC}+0.25	V_{EE}-0.25		V_{CC}+0.25	V
		$V_{OS} \leq$ 6mV over full temperature range	V_{EE}-0.1		V_{CC}+0.1	V_{EE}-0.1		V_{CC}+0.1	
CMRR	Common-mode rejection ratio, small signal	$V_{EE} < V_{CM} < V_{EE}$+0.5V, V_{EE}+1V < $V_{CM} < V_{CC}$		100		90	100		dB
		Over full temperature range		100		80	90		
	Common-mode rejection ratio, large signal	$V_{EE} < V_{CM} < V_{CC}$		90			100		
		Over full temperature range		80			90		
PSRR	Power supply rejection ratio	$V_{EE} < V_{CM} < V_{CC}$	80	100		80	100		dB
		Over full temperature range	80	90		80	90		

DC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE5234			SA5234			
			MIN	TYP	MAX	MIN	TYP	MAX	
I_L	Peak load current, sink and source		10	12		10	12		mA
		Over full temperature range	5	8		5	8		
A_{VOL}	Open-loop voltage gain		90	110		90	110		dB
		Over full temperature range		90			90		
V_{OUT}	Output voltage swing	I_{PEAK} = 0.1mA	V_{EE}+0.05		V_{CC}-0.05	V_{EE}+0.1		V_{CC}-0.1	V
		I_{PEAK} = 10mA	V_{EE}+0.25		V_{CC}-0.25	V_{EE}+0.25		V_{CC}-0.25	
		I_{PEAK} = 5mA over full temp range	V_{EE}+0.22		V_{CC}-0.2	V_{EE}+0.2		V_{CC}-0.2	
	Output voltage swing for V_{CC} = 2.75V, V_{EE} = -2.75V	R_L = 2kΩ	V_{EE}+0.2		V_{CC}-0.2	V_{EE}+0.2		V_{CC}-0.2	V
		R_L = 600Ω,	V_{EE}+0.25		V_{CC}-0.25	V_{EE}+0.25		V_{CC}-0.25	

NOTES:

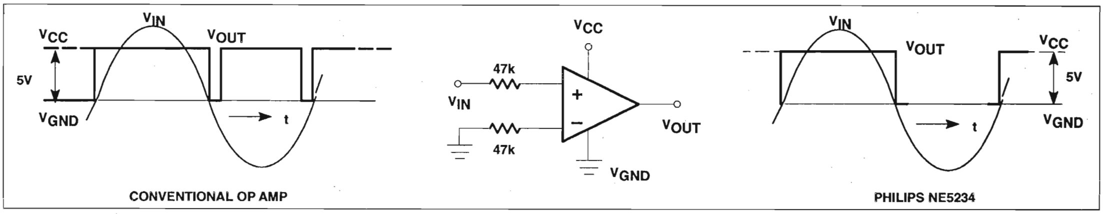
1. These parameters are measured for $V_{EE} < V_{CM} < V_{EE}+.5V$ and for $V_{EE}+1V < V_{CM} < V_{CC}$. By design these parameters are intermediate for common mode ranges between the measured regions.

AC ELECTRICAL CHARACTERISTICS

T_A = +25°C; V_{CC} = 2 to 5.5V; R_L = 10k; C_L = 100pF; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE5234			SA/SE5234			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	Over full temperature range	0.5	0.8		0.5	0.8		V/µs
BW	Unity gain bandwidth: -3dB	Over full temperature range	2	2.5	4.0	2	2.5	4.0	MHz
θ_M	Phase Margin	C_L = 50pF		55			55		deg
t_S	1% settling time	A_V = 1, 1V step		1.4			1.4		µs
V_N	Input referred voltage noise	A_V = 1, R_S = 0Ω, at 1kHz		25			25		nV/Hz 1/2
THD	Total harmonic distortion	10kHz, $1V_{P-P}$, A_V = 1		0.1			0.1		%

OUTPUT INVERSION PREVENTION



Using the NE/SA5234 amplifier

AN1651

Author: L. Hadley

I. SUMMARY

The NE/SA5234 is a unique low-voltage quad operational amplifier specifically designed to operate in a broadly diverse environment. It is an enhanced pin-for-pin replacement for the LM324 category of devices. Supply conditions can range from 1.8V to 6.0V with a resultant current drain of 2.8mA,-700μA per op amp.

Most notable are the input and output dynamic range characteristics of the individual op amps. The common-mode input voltage can actually exceed the positive and negative supply rails by 250mV with no danger of output latching or polarity reversal. In addition, the output of each op amp will swing to within 50mV of the supply rails over the full supply range.

The frequency related characteristics are also above average for low voltage devices in this class. Internal unity gain compensation makes the NE5234 very resistant to any tendency to oscillate in low closed-loop gain configurations. Even so, a unity-gain bandwidth of 2.5MHz is retained. Slew rate is 0.8V/μs and each op amp will settle to a 1% of nominal level within 1.4μs.

II. DETAILED DESCRIPTION

Input Stage

The input differential amplifier consists of a compound transistor structure of parallel NPN and PNP transistors which account for the unique over-drive characteristics of the NE5234. Referring to Figure 1, it is seen that the NPN pair, Q1 and Q2, allow the input to operate in the common-mode input voltage range of 1V above V_{EE}. This region is designated the N-mode region in Figure 3a. Operation in the common-mode range below 1V transfers the input stage into the P-mode of operation.

In the N-mode operating condition, collector current from Q1 and Q2 is summed in the output emitter node of Q10 and Q12 respectively. Q1's base is the non-inverting input and Q2's base the inverting input node for the amplifier.

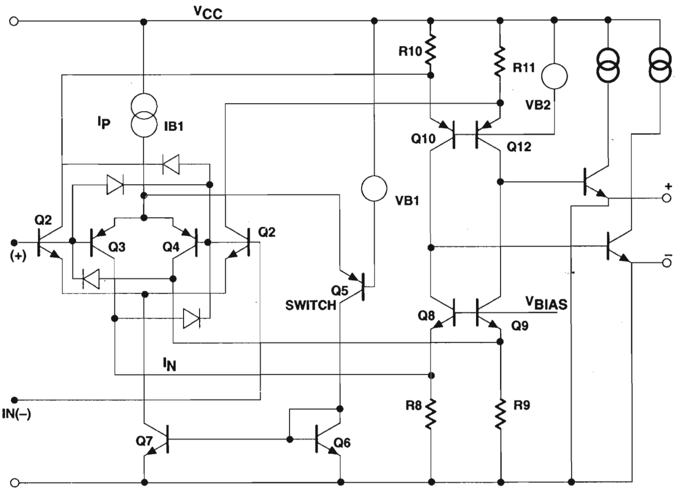


Figure 1. NE5234 Input Stage

Linear operation between the two modes is governed by a current steering circuit consisting of Q5,6 and 7 in conjunction with voltage reference VB1. Operation in the

N-region of the common-mode range will automatically cause Q5 to transfer the IB1 current source to Q7 and the NPN transistor pair Q1 and Q2. Operation below the 1V level at the inputs allows the current from IB1 to be fed directly to Q3 and Q4 emitters giving them priority in processing the signal and linearizing their transfer function. (The sum of the NPN and PNP input pair currents remain constant.)

Operation in the common-mode range near the positive supply rail would normally cause the input stage NPN transistor's base collector junction to become forward biased (base current flow directly to the collector circuit) reversing the collector current flow direction. In a conventional op amp, this would have the adverse effect of reversing the output signal polarity as the operating region is traversed by the input signal. (see Figure 2)

To prevent this from occurring, large geometry diode-connected transistors are cross-connected to the opposite NPN collector, (Q1, Q2). This current, in turn, is summed at the emitter of Q12 pulling it above the V_{CC} rail voltage and preventing polarity reversal. The inverse condition occurs when Q2 is driven above the positive rail, with Q10 emitter being pulled up and signal polarity preserved. (See Figure 1)

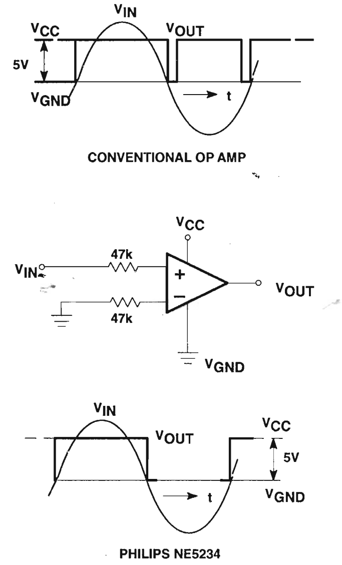
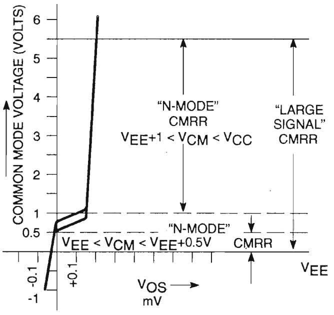


Figure 2. Output Inversion Protection



NE5234 Common-Mode Operating Regions

Figure 3.

For negative going input signals, which drive the inputs toward the V_{EE} rail and below, another set of diode-connected transistors come into operation. These steer the current from the input into Q8 or Q9 emitter circuits again preventing the reversal effect.

Figure 3 shows graphically how the N and P mode transitions relate to the common-mode input voltage and the offset voltage V_{OS}.

Intermediate Amplifier and Output Stage (Figure 4)

The intermediate stage is isolated from the input amplifier by emitter followers to prevent any adverse loading effect. This stage adds gain to the over all amplifier and translates levels for the following class-AB current-control driver. Note that I_2 is the inverting input and I_1 the non-inverting input. The output is taken from multiple collectors on the non-inverting side and provides matching for the following stage.

Class-AB control of the output stage is achieved by Q61 and Q62 with the associated output current regulators. These act to monitor the smallest current of the non-load supporting output transistor to keep it in conduction. Thus, neither Q71 or Q81 is allowed to cutoff but is forced to remain in the proper Class-AB region.

Overload protection is provided by monitor circuits consisting of R76-D2 for sinking and R86-D3 for sourcing condition at the output. When the output current, source or sink, reaches 15 milliamperes, drive current to the stage is shunted away from current sources IB6 or IB9 reducing base current to driver transistors Q72 and Q82 respectively.

The prevention of saturation in the output stage is achieved by saturation detectors Q78 and Q88. When either Q71 or Q81 approaches saturation, current is shunted away from the driver transistors, Q72 or Q83 respectively.

III. CHARACTERISTICS

Internal Frequency Compensation

The use of nested Miller capacitors C2 through C6, in the intermediate and output sections, provides the overall frequency compensation for the amplifier. The dominant pole setting capacitor, C2, provides a constant 6dB/octave roll-off to below the unity gain frequency of 2.5MHz. Figure 5 shows the measured frequency response plot for various values of closed-loop gains.

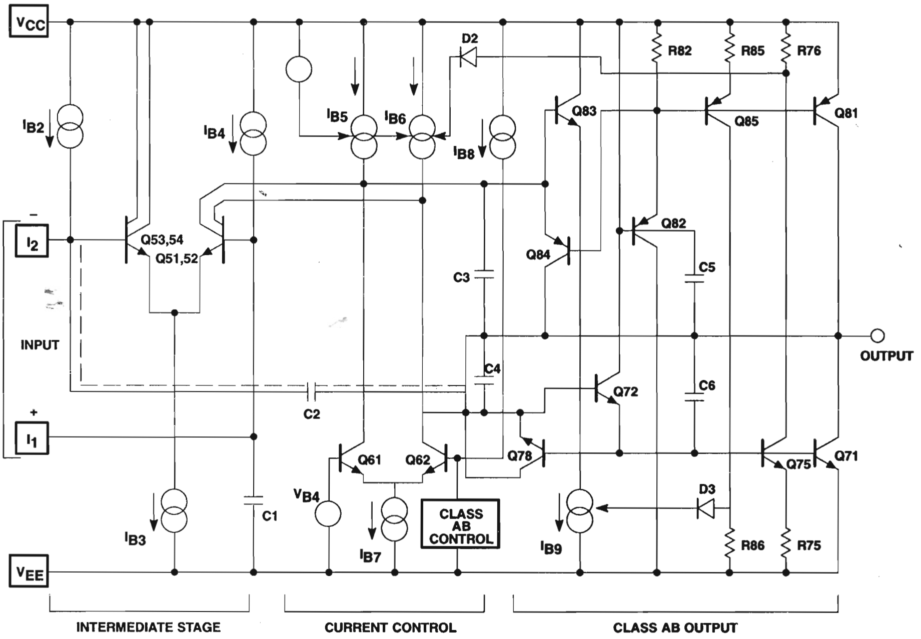


Figure 4.

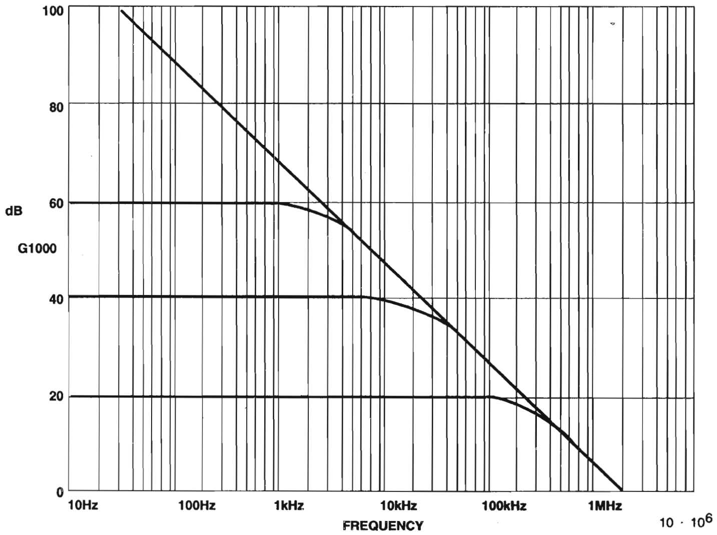


Figure 5. NE5234 Closed Loop Gain vs Frequency

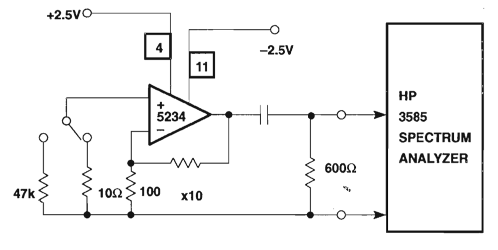


Figure 6. Noise Test Circuit

IV. NOISE REFERRED TO THE INPUT

The typical spectral voltage noise referred to each of the op amps in the NE/SA5234 is specified to be 25nV/√Hz. Current noise is not specified. In the interest of providing a balance of information on the device parameters, a small sample of the standard NE5234s, were tested for input noise current. While this data does not represent a specification, it will give the designer a ball park figure to work with when beginning a particular design with the device. For completeness I have provided the corresponding spectral noise voltage data for the same sample. The data was taken using an HP3585A spectrum analyzer which has the capability of reading noise in nV/√Hz.

The test circuit is shown in Figure 6. As is typical for such measurements the amplifier under test is terminated at its input first with a very low resistance, for the voltage noise reading, followed by the same test with a high value of resistance to register the effect of current noise. The amplifier is set to a non-inverting closed-loop gain of 20dB. Dual supply operation was chosen to allow direct termination of the input resistors to ground.

The measurements were made over the range from 200Hz to 2kHz. Each sample is measured at 200Hz, 500Hz, 1kHz and 2kHz. The data is averaged for each frequency and then the small sample distribution is derived statistically giving the standard deviation relative to the mean.

Referring to the graph in Figure 7a, the equivalent voltage noise is seen to average 18 nV/√Hz. The 95% confidence interval is determined to be approximately one nV/√Hz. The majority of the errors which contribute to this measurement are due to the thermal noise of the parallel combination of the feedback resistor network, in addition to the 10Ω termination resistor on the non-inverting input. At 300° Kelvin a 10Ω resistor generates 0.4 nV/√Hz and the feedback network's equivalent resistance of 90Ω generates 1.2nV/√Hz. Their order-of-magnitude difference from the main noise sources allows them to be neglected in the overall calculation of total stage noise.

Noise current is measured across a 47kΩ resistor and averaged in the same manner. The thermal noise generated by this large resistance is not insignificant. At room temperature it is 28nV/√Hz and must be subtracted from the total noise as measured at the output of the op amp in order to arrive at the equivalent current generated noise voltage. Figure 7b shows the derived current noise distribution for the small sample of 10 NE5234 devices. The result shows that noise current in the 200Hz to 2kHz frequency is typically 0.2pA/√Hz. The 1/f region was not determined for either current or voltage noise.

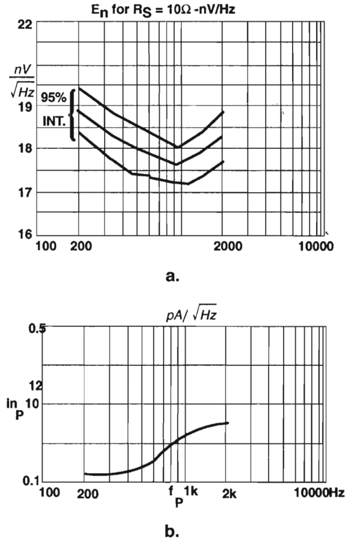


Figure 7. Typical Noise Current and Voltage vs Frequency

V. GUIDE LINES FOR MINIMIZING NOISE

When designing a circuit where noise must be kept to a minimum, the source resistances should be kept low to limit thermally generated degradation in the overall output response. Orders-of-magnitude should be kept in mind when evaluating noise performance of a particular circuit or in planning a new design. For instance, a transducer with a 10kΩ source resistance will generate 2μV of RMS noise over a 20kHz bandwidth. Using the graphical data above, total noise from a gain stage may be calculated.-

Amplifier Noise Voltage (EQ. 1.)

$$25\text{nV}/\sqrt{\text{Hz}} \cdot \sqrt{\text{BW}} = 3.5\mu V_{RMS}$$

$$\text{BW} = 10\text{kHz}$$

Noise from source 10kΩ Resistance –

Noise Voltage from source resistance (EQ. 2.)

$$14\text{nV}/\sqrt{\text{Hz}} \cdot \sqrt{\text{BW}} = 20\mu V_{RMS}$$

Current generated noise (EQ. 3.)

$$0.2\text{pA}/\sqrt{\text{Hz}} \cdot 10^3 \cdot \sqrt{\text{BW}} = 0.28\mu V_{RMS}$$

The total noise is the root-to-sum-of-the-squares of the individual noise voltages –

$$En = \sqrt{(3.5)^2 + (2.0)^2 + (0.28)^2} \quad \text{(EQ. 4.)}$$

$$= 4.04\mu V_{RMS}$$

To determine the signal-to-noise ratio of the stage we must first choose a stage gain, make it 40dB, and a signal voltage magnitude from the transducer which we will set at $10mV_{RMS}$. The resulting signal-to-noise ratio at the output of this stage is determined by first multiplying the gain times the signal which gives $1V_{RMS}$ with a resultant noise of 400mV$_{RMS}$. The signal-to-noise ratio is calculated as

$$S/N \quad 20\log_{10}(1.0/4x10^{-4}) = 68dB \qquad \text{(EQ. 5.)}$$

This is quite adequate for good quality audio applications.

Next assume that the bandwidth is cut to 3.0kHz with an input of 1mV$_{RMS}$. The RMS noise is modified by the ratio of the root of the noise channel bandwidths.

$$\left[\frac{\sqrt{3x10^3}}{\sqrt{20x10^3}}\right] \cdot EN = 1.6\mu V_{RMS} \qquad \text{(EQ. 6.)}$$

Amplified Noise = 160µV$_{RMS}$

$$S/N \quad 20\log_{10}\left[\frac{100x10^{-3}}{1.6x10^{-4}}\right] \qquad \text{(EQ. 7.)}$$

$$= 56dB$$

A 56dB S/N will provide superior voice channel communications .

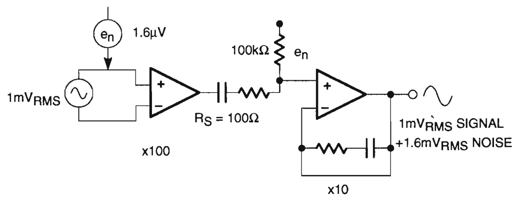


Figure 8.

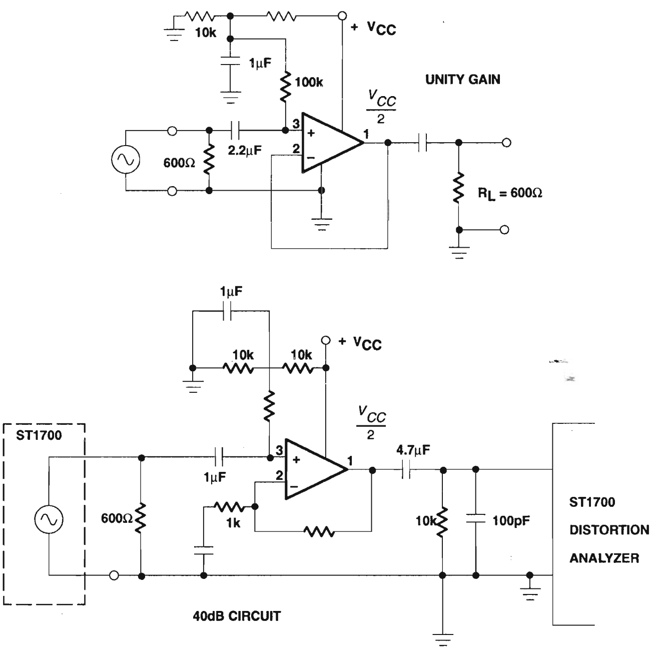


Figure 9. NE5234 THD Test Circuits

VI. MULTIPLE STAGE CONSIDERATIONS

Since multiple noise generators are non-coherent, their total effect is the root-of-the-sum-of-the-squares of the various noise generators at a given amplifier input.

This makes orders-of-magnitude lower noise sources less important than the higher magnitude source. Therefore, when considering the combined signal-to-noise of multiple stages of gain, the first stage in a chain dominates making its design parameters the most critical. For this reason it is good practice to make the preamp stage gain as high as practical to boost signal levels to the second stage allowing at least an order-of-magnitude above the second-stage noise. For instance, a signal input which exceeds the input noise of the following stage by a factor of 10:1 will only be degraded by 0.5% or -46dB, neglecting the first-stage noise. If we use the preceding example with a first-stage output signal of 100mV$_{RMS}$ and a 56dB S/N, and an output noise of 0.16mV. Following this with a 10kHz band limited gain-of-10 second-stage, with a 100kΩ noise source at the non-inverting input, the combined S/N is calculated as follows: (assume a 100Ω source resistance from amplifier #1)

The Second stage output noise is:

$$\left[\sqrt{(0.163x10^{-3})^2 + \left(\sqrt{4KT \cdot 100 \cdot 10{,}000}\right)^2}\right] \cdot 10 \qquad \text{(EQ. 8.)}$$

$$= 1.6mV$$

$$K = \text{Boltzman'sConstant} = 1.38\text{x}10^{-23}\frac{\text{Joule}}{\text{DegKelvin}} \qquad \text{(EQ. 9.)}$$

$$T = 300^{\circ}\text{K} \; ; \; BW = 10\text{kHz}$$

The amplified output signal = $1V_{RMS}$

$$S/N = 20\log_{10}\left(\frac{1}{1.6\text{x}10^{-3}}\right) \qquad \text{(EQ. 10.)}$$

$$= 56\text{dB}$$

Note that there is no effect from the second-stage thermally generated resistor noise due to the dominating effect of the first-stage amplified noise being much greater than the input noise of the second-stage. In addition the equivalent noise resistance of the second-stage is essentially the output resistance of the first-stage plus any series resistance used in coupling the two. This is the parallel combination of source resistance with input terminating or biasing resistance.

VII. LOW HARMONIC DISTORTION

The NE/SA5234 is extremely well adapted to reducing harmonic distortion as it relates to signal level and head room in audio and instrumentation circuits. Its unique internal design limits overdrive induced distortion to a level much below that experienced with other low voltage devices. As will be shown, the device is capable of operating over a wide supply range without causing the typical clipping distortion prevalent in companion operational amplifiers of this class.

A series of tests are shown to allow you to see just how resistant this device is to generating clipping distortion. Two different gain configurations were chosen to demonstrate this particular feature: unity gain non-inverting and 40dB non-inverting. The test set-up was as shown in Figure 9. The Harmonic Distortion analyzer used to make the measurements was a Storage Technology ST1700. The test frequency is 1kHz. For single supply operation, as previously covered, the amplifier should be biased to half the supply voltage to minimize distortion. Operation with dual supplies is simpler from a parts count standpoint as isolation capacitors are not required. Also the time constants associated with charging and discharging these is eliminated . Figure 10a,b and c shows the total harmonic distortion in percent versus input voltage level at 1kHz in V_{RMS} for a non-inverting, unity gain NE5234. The load on the amplifier output is 10kΩ. Beginning with a supply voltage of 1.8V and an input level of $0.1V_{RMS}$, distortion is well below 0.2% ad remains there up to an input level just over $0.5V_{RMS}$ ($1.4V_{P-P}$) and increases to 0.4% for for $0.6V_{RMS}$ ($1.7V_{P-P}$).

For a 2V supply, the input levels increase to $0.65V_{RMS}$ and $0.7V_{RMS}$, respectively for similar levels of distortion. With a supply voltage of 3.0V the input may be increased to $1V_{RMS}$ before THD rises to 0.2% and $1.1V_{RMS}$ for only 0.8% THD. Operation with a 600Ω load will only raise the THD figures slightly . By way of comparison, Figure 10c shows the greatly reduced dynamic range experienced when an LM324 is plugged into the test socket in place of the NE5234. Note that The THD is completely off scale for the case of 1.8 and 2.0V supply, then is barely usable for the low level end of the 3.0V supply example. Figure 11a, b, and c demonstrates the effect on harmonic distortion when closed loop gain is increased to 40dB in the non-inverting mode. It is evident that little increase in THD levels result. The graphs for the 2.0 and 3.0V supply case also include additional information on the effect of a 600Ω load on distortion.

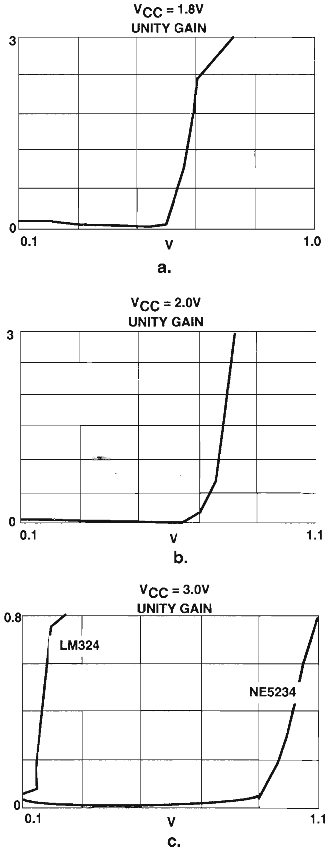


Figure 10. THD vs Supply Voltage for $1V_{RMS}$ Output

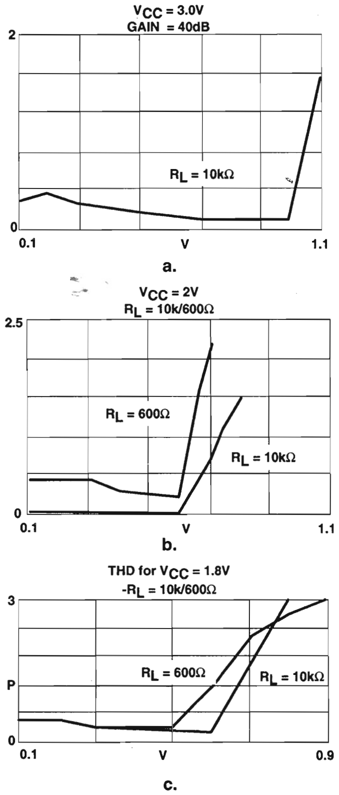


Figure 11. THD vs Load

VIII. GAIN-BANDWIDTH VS CLOSED LOOP FREQUENCY RESPONSE

Figure 5 shows the small signal frequency response of the NE5234 versus closed-loop gain in dB. The test circuit is shown in Figure 6. The plot is taken from measured data and thus shows how each value of closed-loop gain coincides with the open-loop response curve. The NE/SA5234's open-loop gain response has a uniform 6dB/octave roll-off which continues beyond 2.5MHz. This factor guarantees each op amp in the IC a high stability in virtually any gain configuration. In making these measurements, dual supplies of ±2.5V were used in order to allow a grounded reference plane and no coupling capacitors which might cause frequency related errors.

A critical parameter which affects the reproduction quality of complex waveforms is the gain-bandwidth-product of the operational amplifier. Essentially, this is a measure of the maximum frequency handling characteristics of any operational amplifier for a given closed-loop gain. As is evident from the graph, the NE/SA5234 has a 2.5MHz unity gain cross-over frequency — much higher than most other low voltage op amps. For comparison, the µA741 has a gain-bandwidth-product of 1MHz, as do the LM324 and the MC3403.

IX. LOOP-GAIN

The dynamic signal response of any closed-loop amplifier stage is a function of the Loop-gain of that particular stage. Loop-gain is equal to the open-loop gain in dB, at a given frequency, minus the closed-loop gain of the stage. The greater the Loop-gain, the lower the transfer function error of the device. Essentially, any parametric error is reduced by the factor of the Loop-gain. This includes output resistance and output signal voltage accuracy. It is good practice then to maximize Loop-gain to the degree that stage gain may be sacrificed for bandwidth. In some cases it is actually better to use two stages of gain in order to preserve signal quality than to use one high gain stage. Of course, there is a trade-off between the aforementioned factors that affect the signal-to-noise ratio of the stage and optimizing the Loop-gain. For example, a voice-band audio stage which requires 3kHz bandwidth, should be limited to a closed-loop gain of 40dB for lowest distortion in the output signal. For higher quality audio applications requiring a 20kHz bandwidth, the closed-loop gain must be limited to 20dB. This results in a Loop-gain of 20dB at the highest signal frequency.

A second consideration in the list of frequency dependent parameters is the effect of amplifier slew rate. Not only is it frequency dependent but it is also a function of signal amplitude, as we shall see in the next section.

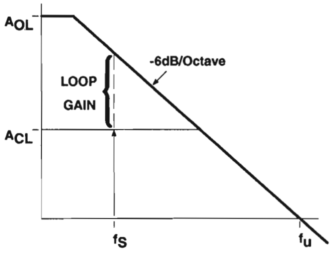


Figure 12.

X. SLEW RATE RESPONSE

The slew rate of an operational amplifier determines how fast it can respond to a signal, and is measured in volts-per-microsecond. The NE5234 has a typical slew rate of 0.8V/µs. Let us see just what this means in terms of signal handling capability. If a sinusoidal input signal, V_S, is used as reference, it is specified by its frequency and peak amplitude, V_P as follows:

$$V_S = V_P \sin(2\pi f t) \tag{EQ. 11.}$$

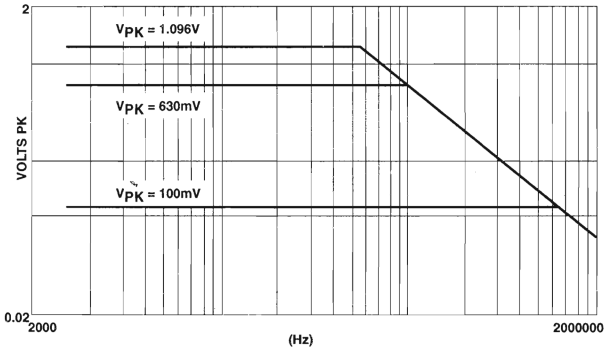


Figure 13. Slew Rate Limiting Amplitude vs Frequency

Slew Rate (SR) is the time-rate-of-change of the signal voltage during any complete cycle, that is over the range of 0 to 2π. This amounts to taking the time derivative of the sine wave which results in multiplying the cosine by the factor '$2\pi f$'.

An example of the trade off between signal amplitude and frequency is shown below for the NE5234 slew rate of 0.8V/µs. As shown in Figure 13, the maximum allowable amplitude signal which can be reproduced is determined by the slew rate response line which gives peak output volts versus frequency in Hertz.

Mathematically, slew rate is determined, by the equation below, as the derivative of the sine wave signal. The resultant slew rate function changes with both frequency and amplitude.

$$\text{Slew Rate} = V_P\,(2\pi\ f)\ \cos\ (2\pi\ f\ t)$$

Note that maximum slew rate occurs where the input sine wave signal crosses the values of 0, π, and 2π on the radian axis. To get a feel for what this means in regards to the typical low voltage circuit, let us consider a $1V_{RMS}$ sinusoidal input to a unity gain amplifier. The peak voltage in the above equation is 1.414V. One can then calculate the required slew rate to faithfully reproduce this signal for various signal frequencies. Or with a given slew rate and a required peak signal amplitude, the maximum frequency before slew rate limiting occurs may be determined. For example using the above amplitude of $1V_{RMS}$, and the slew rate of the NE5234 which is 800,000V/sec, one determines that the highest frequency component which may be reproduced before slew rate distortion occurs is:

800,000 V/sec / $2\pi \bullet 1.414$ volts peak = 90,090Hz. A graphical representation of this relationship is shown in Figure 13. By using this graph along with the information in the preceding Figure 10 and Figure 11, which relate usable signal levels versus power supply voltage, the dynamic behavior of a particular design may be predicted. For instance, given a single supply configuration operating at 2.0V, Figure 10b shows an upper limit to input amplitude of $0.7V_{RMS}$, or about 1V peak for 1% THD. Using this level with the data in Figure 13 leads to a figure of 116kHz as an upper frequency limit for a unity gain amplifier stage operating at 2V DC.

$$\frac{dV_S}{d\,t} = V_P\ \omega\cos\ \omega t = \text{Slew Rate} \qquad \text{(EQ. 12.)}$$

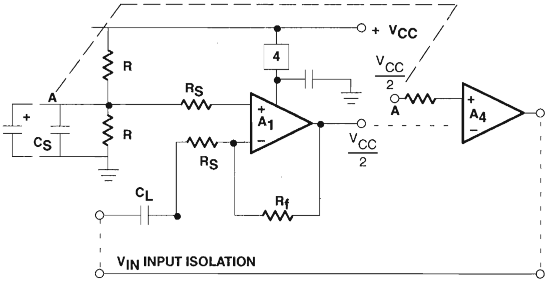


Figure 14. Single Supply Biasing in Cascade

XI. PROCEDURES

Single Supply Operation

When the NE/SA5234 is used in an application where a single supply is necessary, input common-mode biasing to half the supply is recommended for best signal reproduction. Referring to Figure 14, a simplified inverting amplifier input stage is shown with the simplest form of resistive divider biasing. The value of the divider resistance R is not critical and may be increased above the 10kΩ value shown as long as the bias current does not interfere with accuracy due to DC loading error. However the divider junction must be kept at a low AC impedance This is the purpose of bypass

capacitor C_S. Its use provides transient suppression for signals coming from the supply bus. A low cost 0.1µF ceramic disk or chip capacitor is recommended for suppressing fast transients in the microsecond and sub-microsecond region.
Foil capacitors are simply too inductive for any high frequency bypass application and should be avoided. If low frequency noise such as 60Hz or 120Hz ripple is present on the supply bus, an electrolytic capacitor is added in parallel as shown. The common-mode input source resistance, R_S, should also be matched within a reasonable tolerance for maximizing the rejection of induced AC noise.

The output of the first stage is now fixed at the common mode bias voltage and the amplified AC signal is referenced to this constant value. Capacitive coupling to the inverting input is of course required to prevent the bias voltage from being multiplied by the stage gain. Second stage biasing may now be provided by the output voltage of the first stage if non-inverting operation is used in the former. For lowest noise in a high gain input stage, the magnitude of the input source resistance is critical; low values of resistance are preferred over high values to minimize thermally generated noise.

Non-Inverting Stage Biasing

Non-inverting operation of an amplifier stage with single supply is similar to the previous example but the bias resistor R_S must now be sufficiently high to allow the signal to pass
without significant attenuation. The input source resistance reflects the output resistance of the preceding stage or other sourcing device such as a bridge circuit of relatively high impedance. A simple rule of thumb is to make the bias resistor an order of magnitude larger than the generator resistance. Again the feed back network must be terminated capacitively. In this case R1 and the generator resistance should be matched and then R_S is matched to the feedback resistance ,R_F.

In all cases proper bypassing of the NE5234 supply leads (Pins 4 and 11) is very important particularly in a high noise environment. Bypass capacitors must be of ceramic construction with the shortest possible leads to keep inductance low. Chip capacitors are superior in this respect complimenting the increased use of surface mounted integrated devices. Note that both the NE5234D and the automotive grade SA5234D are available and are the surface mount versions of the device.

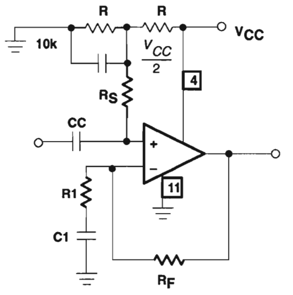


Figure 15. Non-Inverting Biasing

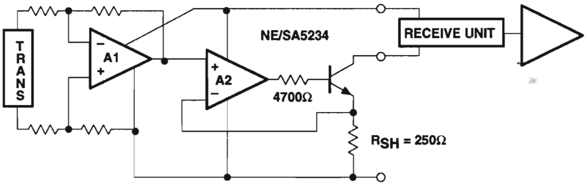
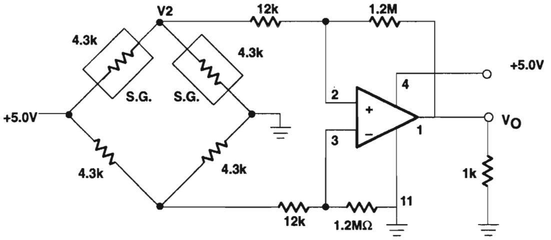


Figure 16. A 4-20mA Current Loop



$\lvert V_2 - V_1 \rvert$	V_O
5.9mV	0.5V
25.6mV	2.50V
46.6mV	4.63V

S.G.: Matched Strain Gauge elements

Figure 17. Strain Gauge Amplifier

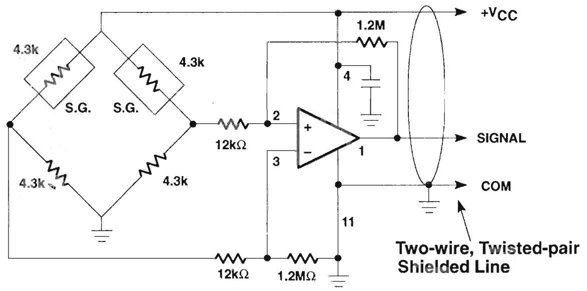


Figure 18. Remote Strain Gauge

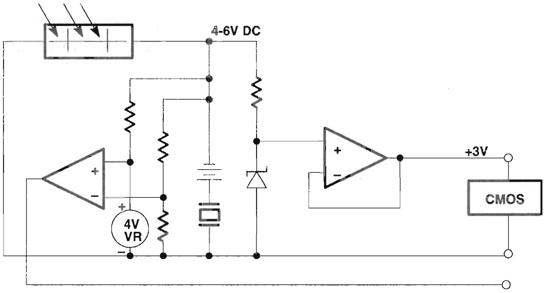


Figure 19. Solar Regulator

APPLICATIONS EXAMPLES

Instrumentation

Strain Gauge Bridge Amplifier

The circuit below shows a simple strain gauge circuit with a gain of 100 (40dB) and operated from a single supply. The chart illustrates the transfer function of the circuit for a single order-of-magnitude signal differential range from the bridge beginning with 5mV up to 50mV. The circuit is operated from a single 5V supply, but could equally as well be configured to use a dual balanced supply. It is immediately evident that the wide common-mode output range of the NE5234 is very advantageous in handling this wide range of signals with good linearity due to this feature.

A variation on this particular idea is the remote strain gauge circuit operating from a three wire line, one of which is the shield. This full-differential input circuit has balanced input resistance to afford good common-mode noise rejection characteristics. Resistors are metal film or deposited carbon. Supply leads must be carefully bypassed close to the NE/SA5234 with ceramic or chip monolithic capacitors to give optimum noise performance. As shown, an auxiliary sub-regulator may be added to improve the overall DC stability of the bridge signal voltage. A regulator capable of providing the necessary few milliamperes at somewhat reduced voltage for the transducer is shown in one of the following examples. This makes use of one of the op amps in the same device package to provide the voltage regulation. Note that the use of multiple op amps within a single package minimizes the possibility of thermal drift and mismatched response from various DC parameters.

Multiple sets of transducers may be constructed from The NE/SA5234 or the NE5234D surface mount device to form a compact and stable instrumentation package. This is useful for transducer applications in the measurement of pressure, strain, position and temperature, which have similar circuit configurations. First order temperature compensation of the transducers such as semiconductor strain gauges, or resistive units may be achieved by using one of the gauges as a reference device only. It is thermally coupled to the same member as the active gauge, as shown in the example. (Figure 18)

A 4 to 20mA Current Loop

Some instrumentation installations require the 4-20mA current loop. This addition to the above bridge transducer circuit examples is demonstrated in Figure 16.

This circuit makes use of the remote transducer bridge previously described and adds current loop signaling capability. The voltage-to-current converter consists of an additional op amp from the same NE/SA5234 package combined with a single transistor to drive the current loop. The sensitivity is actually in mA/V, or transconductance, which is equal to $1/R_{SH}$. This sensitivity in this particular example is set to 4mA/V. Thus, with a bridge amplifier having a differential gain of 100, an input of 10mV will produce a 4mA output current and 50mV will produce a 20mA output. Of course the line resistance plus receiver resistance must be within the voltage compliance range of the supply voltage to guarantee linear operation over the total range. A negative supply may be used if it is preferred to have the current loop referenced to ground.

DC Regulators and Servos

Closely related to DC and low frequency AC linear transducers are DC regulators and servo circuits. The proliferation of many battery, and solar powered remote instrumentation packages results in a need for adaptable circuits which may readily be made up from existing stock ICs. The examples given here are quite simple, but can be very useful to the designer when economy and size are at a premium.

Solar Regulator for 3-Volt CMOS

Working with small instrumentation packages which are to operate from solar photovoltaic cells may bring a need for simple sub-regulators for MOS circuits requiring only a few milliamperes of drain current. Figure 19 shows a simple low voltage regulator making use of the particularly excellent DC characteristics of the NE/SA5234. The regulator becomes an integral part of any functional analog signal processing package such as an environmental data instrumentation unit. The low current drain of the the typical 3V or 5V MOS digital IC allows one sub regulator to serve up to 10 or more such devices. If the instrument package is to be subjected to wide temperature variations, the SA5234 is recommended. A second op amp in the package may serve as a low battery alarm with tone modulator as in radio links, or simple logic level comparator. Overcurrent protection is easily added within the regulator loop to detect short circuit failures and automatically limit the current.

DC Servo-amps

Servo control systems for low voltage motor drives require high gain-accuracy and good DC stability for many applications. Applications such as the position control of air flow vanes, servo valves, and optical lenses or apertures, are typical examples. Figure 20 demonstrates one simple DC motor servo application with position control feedback. The motor is a 3V permanent magnet rotor type used in micro-position applications and is adaptable to battery supply environments.

Position information is received from a multi-turn potentiometer to give adequate resolution. The input voltage may be generated from another potentiometer which is remote from the motor drive unit proper, or from a D/A converter output for micro processor controlled systems. The input voltage range is 1.0 to 3.0V and the supply voltage is 4.5V.

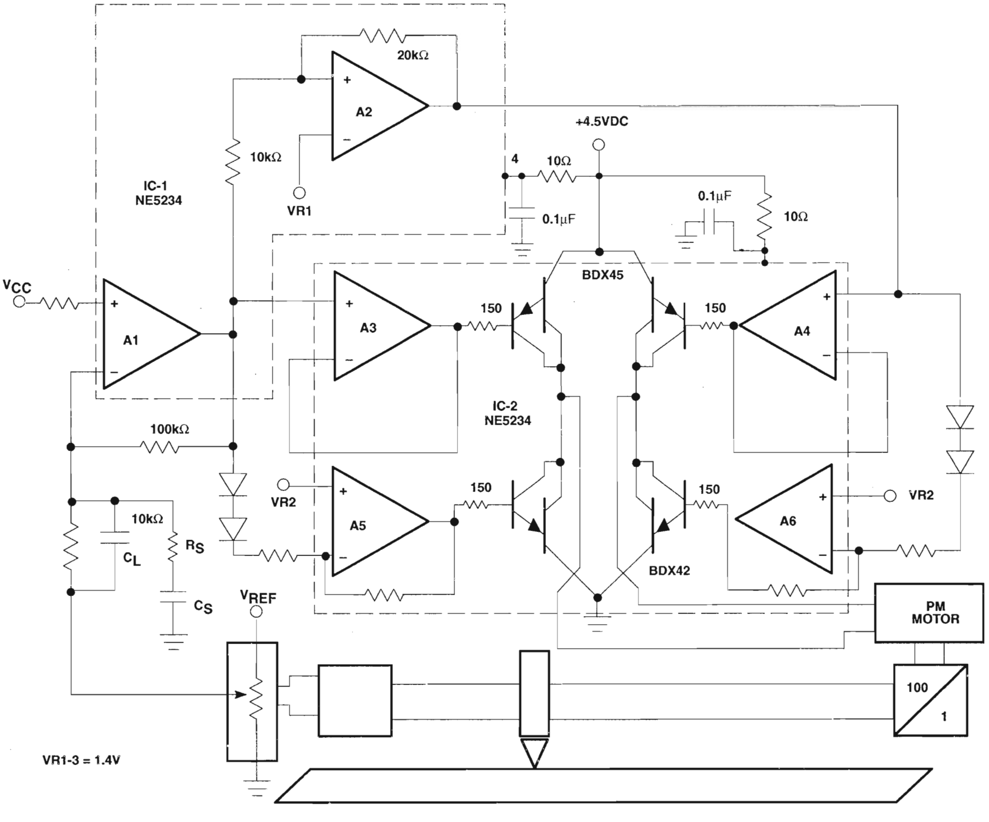


Figure 20. Full Bridge Motor Drive

Active filters

The NE5234 is easily adapted to use in a variety of active filter applications. Its high open-loop gain and excellent unity gain stability make it ideal for high-pass, band-pass and low-pass configurations operated with low voltage single supplies. Its low output impedance also makes it capable of obtaining low noise operation without resorting to separate high current buffers.

Figure 21a shows the circuit for a VCVS low-pass filter with dual supply biasing and 600Ω output termination. Figure 21b is a band-pass filter with AC coupled gain network for single supply operation.

Communications and Audio

Stereo Bridge Amplifier

Figure 22 shows two NE5234 ICs in a bridge amplifier application. The choice of split supplies allows DC coupling, both from the input signal source and to the load. The gain is set to a nominal 20dB. Either inverting or non-inverting operation is available. The inverting input impedance is chosen as 600Ω in order to match standard audio impedance lines within a system. The use of two such amplifiers will provide stereo operation to +10dBm for a 600Ω load.

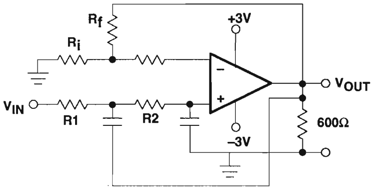
Voice Operated Microphone

The processing of voice transmissions for communications channels is generally coupled with the need for keeping the signal-to-noise ratio high and the intelligibility optimized for a given channel bandwidth. In addition, when a circuit is battery operated and portable, the requirement to obtain maximum battery life becomes important. The circuit example shown here is aimed at filling the need for a portable voice operated transmitter, cordless phone, or tape recorder. It utilizes the Philips Semiconductors NE5234 quad op amp in conjunction with the new low-voltage NE578 compandor to create an audio processor capable of operating in just such an environment. Both devices are operational to a low battery voltage of 2.0V. In addition the design further conserves current by automatically shifting the NE578 compandor to standby during the period when no transmissions are being made. Total current consumption at 3.0V is 2.8mA for the NE5234. In the active mode the NE578 draws 1.4mA and this drops to 170μA in the standby mode. This amounts to reducing the supply current demand by approximately 25% in the 'listen mode'.

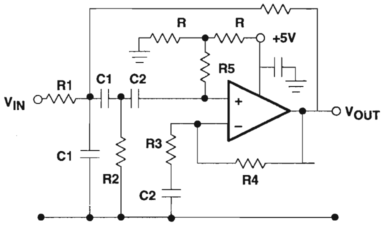
Figure 23 shows the VOX audio circuit example. A description of its operation for voice activated transmission follows.

Audio generated by the electret microphone is fed into the non-inverting input of preamp A1 and the signal amplified by 12dB. The biasing is accomplished by the resistive divider which provides a level of half the supply voltage which is connected through a 100k resistor to the non-inverting terminal of A1. This automatically provides ratiometric common mode biasing set at $V_{CC}/2$ for the device. This level is then transferred directly to the following amplifier, A2, setting its DC operating point. The DC gain of both stage A1 and A2 are unity so the cumulative DC error is not multiplied by stage gain. The peak voice level is approximately $100mV_{RMS}$ at the input to A1 from the microphone and this is boosted to $400mV_{RMS}$. The feedback network gain has a low frequency corner at 160Hz and is flat up to the intersection of the closed loop gain with the open loop gain curve at nearly 500kHz. This would increase the noise bandwidth to an excessive degree unnecessary for voice channel communication. A band limiting network is, therefore, inserted across the feedback resistor to limit response to a nominal 5kHz.

Amplifier stage A2 is used to provide high level audio to the rectifier-filter stage for the rapid generation of a DC control signal for operating the voice activated switch function. Stage A2 gain is set to 20dB in order to allow activation of the voice channel on the rising edge of the first voice syllable. An attack time of 20ms is implemented by adjusting the input charging impedance (R_S) between the rectifier and the A2 amplifier output. AC coupling must be used to isolate the DC common-mode voltage of the amplifier from the rectifier/storage capacitor and to allow only audio frequencies to drive the switching circuit. Amplifier A3 provides a high impedance unity gain buffer to allow a very slow decay rate to be applied to the time constant capacitor, C_T. The output of the storage capacitor reaches approximately 3.2V for a 250ms duration 600Hz burst signal. Diode D1 (1N914) provides a negative clamp action which forces the full peak-to-peak voltage from A2 to charge the storage capacitor. D2 then acts to charge the capacitor to the peak input voltage minus one diode drop, 0.7V. Finally, the buffered DC control signal is fed to A4 which acts as a threshold comparator with extremely high gain and controlled hysteresis. This provides a positive going signal for releasing the NE578 from its inhibit mode when voice input is present. The NE578 is switched from standby mode when voice input is present. The NE578 is switched from standby mode to the active state by raising the voltage on Pin 8 of the device above 2V. Shutting the audio channel off requires this pin to be driven below 100mV. This demands the extremely wide output voltage swing of the NE5234 in order to reach this near to the negative rail voltage. The voltage threshold of the comparator, A4, is adjustable by use of the sensitivity control, R_S. It is used to allow the activation level to be raised or lowered depending upon the ambient audio level in the transmitter vicinity.



a. VCVS Low Pass Filter



b. VCVS Band Pass Filter

Figure 21. Active Filters

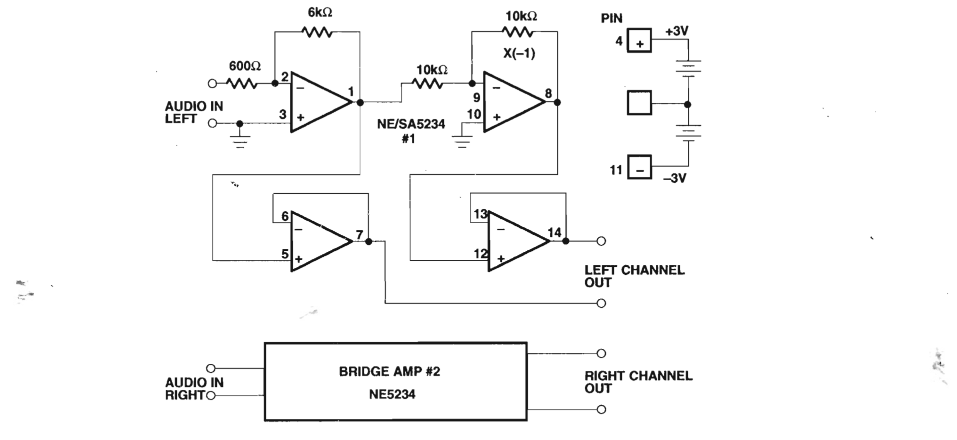


Figure 22. Stereo Bridge Amp

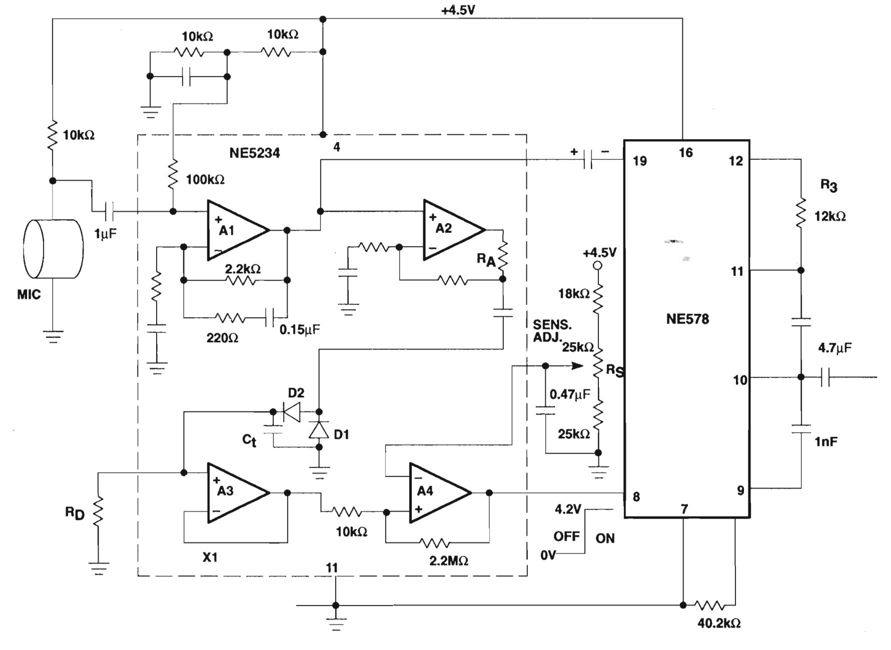


Figure 23. VOX Audio System

Other critical parameters in this type of circuit are the attack and decay times of the RC network which controls the operation of the voice operated switch. Attack time determines how quickly the circuit activates after a quiet period, and the decay time sets how long the transmitter channel stays active between words. It is important to reach an optimum balance between the two time constants in order to allow unbroken transmissions of good quality and no lost syllables. A 100 to 1 attack/decay ratio is used in this particular application and this is primarily set by the value of R_A and R_D. A typical delay of two seconds is easily accomplished. Due to extremely high input impedance of the buffer stage A3, R_D may be in the 1 to 2MΩ range allowing a reasonable value of storage capacitor to be used.

The Audio Channel

Audio input from the preamplifier, A1, is fed directly to Pin 14 of the NE578 compandor. Referring to Figure 24, which shows the internal diagram of the device, it can be seen that this is the compressor portion of the NE578. There is the option in this system to operate either in a 2:1 compressor mode or an automatic level control mode, (ALC). The compressor mode simply makes a 2:1 reduction in the amplitude dynamic range of the input signal and brings it up to the chosen nominal 0dB output level which is programmable from $10mV_{RMS}$ to $1V_{RMS}$. In this particular example it is programmed for a 0dB level of $0.42V_{RMS}$ which is approximately $1V_{P-P}$. This allows for a standardized output level with good characteristics for FM modulation where peak deviation must be controlled. Figure 25 shows the input-output characteristics of the compressor and ALC.

The compressor also has an attack time determined by capacitor C6 on Pin 11. Attack time is 10k * C6, decay time equals four times this value. An auxiliary amplifier stage is used following the NE578 in order to allow bandwidth and special forms of equalization to be implemented. Note that 2:1 compression in a transmission will enhance the channel dynamic range and may be used with no further processing at the receiver, but feeding the received signal through the complimentary 2:1 expandor will achieve even greater enhancement of the recovered audio. The NE578 contains both operations in the same package. Please refer to Philips Semiconductors applications note AN1762 by Alvin K. Wong for complete information on these compandor circuits using the NE578.

Fiber Optic Receiver for Low Frequency Data (Figure 26)

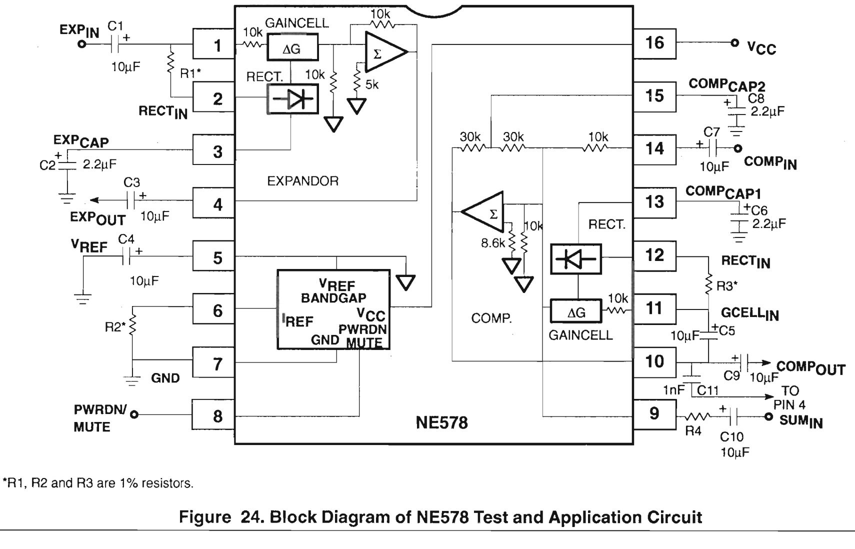
This application makes use of the NE/SA5234 to detect photo-optic signals from either fiber or air transmitted IR (Infra-red) pulses. The signal is digitally encoded for the highest signal-to-noise ratio. The received signal is sensed by an IR photo diode which has its cathode biased to half the supply voltage (2.5V). The first gain stage is configured as a transimpedance amplifier to allow conversion from the microampere diode current signals to a voltage output of approximately $10mV_{0-P}$. The second stage provides a gain-of-ten amplifier to raise this signal level to 1V peak amplitude. This stage is directly coupled from the preamplifier stage in order to provide the necessary common-mode voltage of 2.5V. Its gain control network is capacitively coupled to prevent DC gain as is required in single supply configurations. Since this is essentially a pulse gain stage, low frequency gain below the signal repetition rate is not needed. The third stage acts in a limiting amplifier configuration and its output is squared to swing approximately 5V, the standard TTL level. Again common-mode biasing is passed along from each of the stages up to the last in order minimize parts and simplify circuit layout. The final stage is a simple buffer amplifier to allow the receiver to drive a low impedance long wire line of 600Ω to 900Ω resistance. Some rise time response adjustment may be required. This is easily achieved following stage three by using R_T-C_T to limit the rate of change of the signal voltage prior to the buffer. Note that the last stage acts as a zero-crossing detector. This maximizes noise immunity by allowing a transition only after the third stage output voltage has risen above $2/3V_{CC}$. Phase inversion may be accomplished, if the logic level signals are polarity reversed, by making stage 3 inverting and AC coupling the input signal with a sufficiently large capacitor to reduce droop. Stage 3 must then be biased by connecting its non-inverting node to bias point 'A'. This provides a 2.5V threshold for the proper switching operation of the stage. However, care must be taken not allow the network's time constant to become code dependent as to the average low frequency signal components or errors will result in the output signal.

The advantage of this particular circuit is that it has the simplicity of single supply operation along with the capability of a large output swing making it fully TTL compatible

REFERENCES:

Philips Semiconductors. Linear Data Manual, Volume 2 : Industrial. Sunnyvale: 1988.

Wong, Alvin K. Companding with the NE577 and NE578..Philips Semiconductors Applications Note AN1762 : September 1990.



*R1, R2 and R3 are 1% resistors.

Figure 24. Block Diagram of NE578 Test and Application Circuit

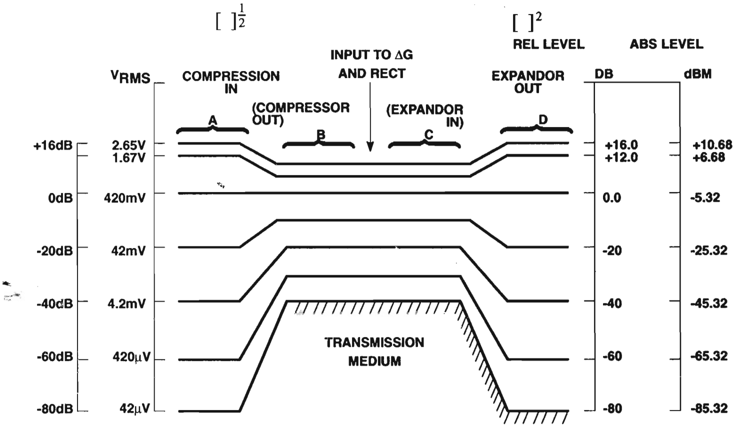


Figure 25. NE570/571/SA571 System Level

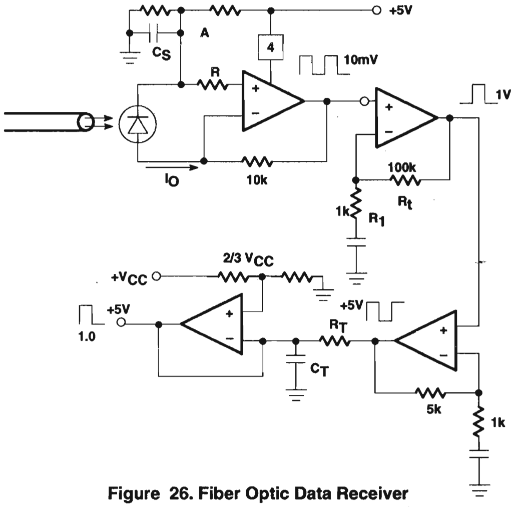


Figure 26. Fiber Optic Data Receiver

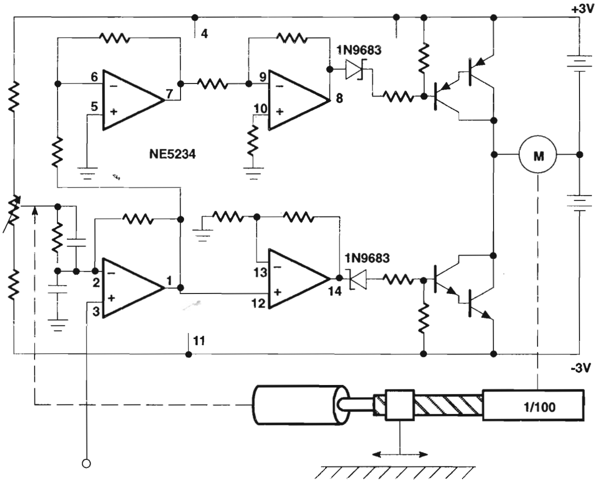


Figure 27. Half Bridge Servo

High frequency operational amplifier NE/SE5539

DESCRIPTION

The NE/SE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter-follower inputs provide a true differential input impedance device. Proper external compensation will allow design operation over a wide range of closed-loop gains, both inverting and non-inverting, to meet specific design requirements.

FEATURES

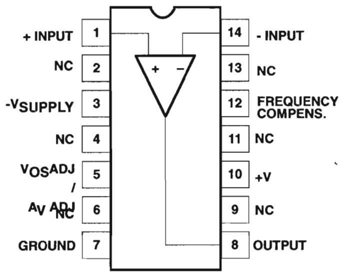
- Bandwidth
  - Unity gain - 350MHz
  - Full power - 48MHz
  - GBW - 1.2GHz at 17dB
- Slew rate: 600/Vμs
- A_{VOL}: 52dB typical
- Low noise - 4nV√Hz typical
- MIL-STD processing available

APPLICATIONS

- High speed datacom
- Video monitors & TV
- Satellite communications
- Image processing
- RF instrumentation & oscillators
- Magnetic storage
- Military communications

PIN CONFIGURATION

D, F, N Packages



Top View

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5539N	0405B
14-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5539D	0175D
14-Pin Ceramic Dual In-Line Package	0 to +70°C	NE5539F	0581B
14-Pin Ceramic Dual In-Line Package	-55 to +125°C	SE5539F	0581B

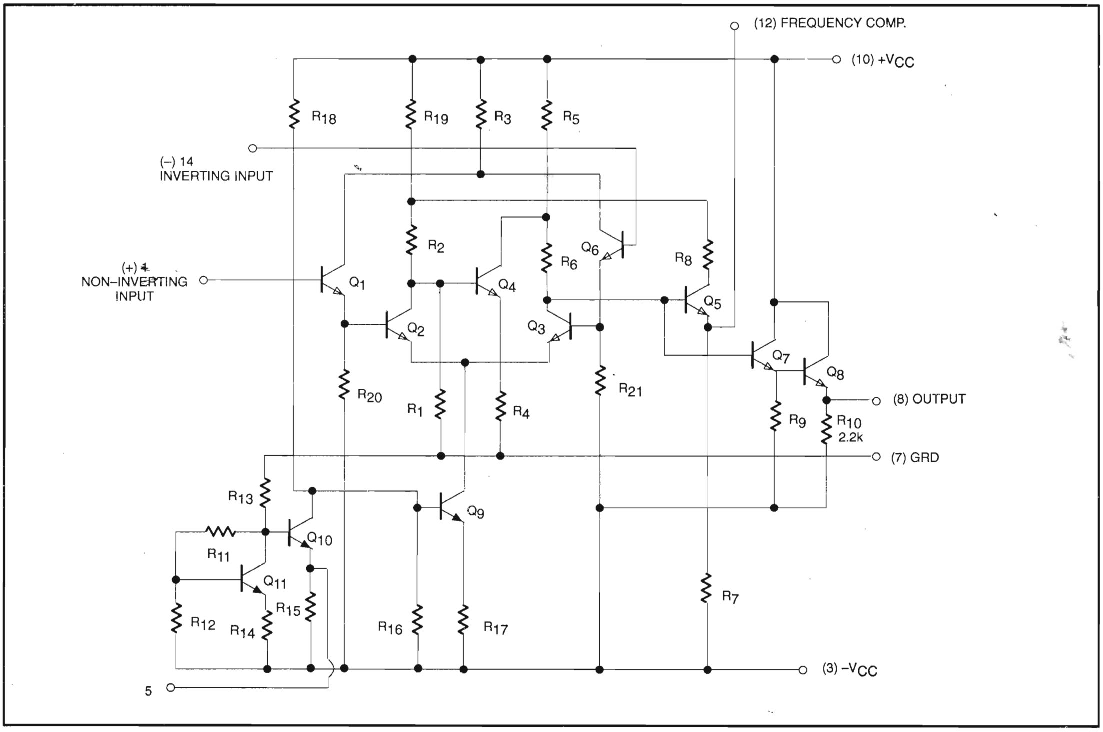
ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	±12	V
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[2]		
	F package	1.17	W
	N package	1.45	W
	D package	0.99	W
T_A	Operating temperature range		
	NE	0 to 70	°C
	SE	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Max junction temperature	150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:

1. Differential input voltage should not exceed 0.25V to prevent excesive input bias current and common-mode voltage 2.5V. These voltage limits may be exceeded if current is limited to less than 10mA.
2. Derate above 25°C, at the following rates:
   F package at 9.3mW/°C
   N package at 11.6mW/°C
   D package at 7.9mW/°C

EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 8V$, $T_A = 25°C$; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539			NE5539			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input offset voltage	$V_O = 0V$, $R_S = 100\Omega$	Over temp		2	5				mV
			$T_A = 25°C$		2	3		2.5	5	
	$\Delta V_{OS}/\Delta T$				5			5		µV/°C
I_{OS}	Input offset current		Over temp		0.1	3				µA
			$T_A = 25°C$		0.1	1			2	
	$\Delta I_{OS}/\Delta T$				0.5			0.5		nA/°C
I_B	Input bias current		Over temp		6	25				µA
			$T_A = 25°C$		5	13		5	20	
	$\Delta I_B/\Delta T$				10			10		nA/°C
CMRR	Common mode rejection ratio	F = 1kHz, $R_S = 100\Omega$, $V_{CM} \pm 1.7V$		70	80		70	80		dB
			Over temp	70	80					
R_{IN}	Input impedance				100			100		kΩ
R_{OUT}	Output impedance				10			10		Ω

DC ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = ±8V, T_A = 25°C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539			NE5539			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OUT}	Output voltage swing	R_L = 150Ω to GND and 470Ω to -V_{CC}	+Swing -Swing				+2.3 -1.7	+2.7 -2.2		V
V_{OUT}	Output voltage swing	R_L = 25Ω to GND Over temp	+Swing -Swing	+2.3 -1.5	+3.0 -2.1					V
		R_L = 25Ω to GND T_A = 25°C	+Swing -Swing	+2.5 -2.0	+3.1 -2.7					
I_{CC+}	Positive supply current	V_O = 0, R_1 = ∞, Over temp			14	18				mA
		V_O = 0, R_1 = ∞, T_A = 25°C			14	17		14	18	
I_{CC-}	Negative supply current	V_O = 0, R_1 = ∞, Over temp			11	15				mA
		V_O = 0, R_1 = ∞, T_A = 25°C			11	14		11	15	
PSRR	Power supply rejection ratio	ΔV_{CC} = ±1V, Over temp			300	1000				µV/V
		ΔV_{CC} = ±1V, T_A = 25°C						200	1000	
A_{VOL}	Large signal voltage gain	V_O = +2.3V, -1.7V, R_L = 150Ω to GND, 470Ω to -V_{CC}					47	52	57	dB
A_{VOL}	Large signal voltage gain	V_O = +2.3V, -1.7V	Over temp							dB
		R_L = 2Ω to GND	T_A = 25°C				47	52	57	
A_{VOL}	Large signal voltage gain	V_O = +2.5V, -2.0V	Over temp	46		60				dB
		R_L = 2Ω to GND	T_A = 25°C	48	53	58				

DC ELECTRICAL CHARACTERISTICS

V_{CC} = ±6V, T_A = 25°C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539			UNITS
					MIN	TYP	MAX	
V_{OS}	Input offset voltage			Over temp		2	5	mV
				T_A = 25°C		2	3	
I_{OS}	Input offset current			Over temp		0.1	3	µA
				T_A = 25°C		0.1	1	
I_B	Input bias current			Over temp		5	20	µA
				T_A = 25°C		4	10	
CMRR	Common-mode rejection ratio	V_{CM} = ±1.3V, R_S = 100Ω			70	85		dB
I_{CC+}	Positive supply current			Over temp		11	14	mA
				T_A = 25°C		11	13	
I_{CC-}	Negative supply current			Over temp		8	11	mA
				T_A = 25°CmA		8	10	
PSRR	Power supply rejection ratio	ΔV_{CC} = ±1V		Over temp		300	1000	µV/V
				T_A = 25°C				
V_{OUT}	Output voltage swing	R_L = 150Ω to GND and 390Ω to –V_{CC}	Over temp	+Swing	+1.4	+2.0		V
				–Swing	–1.1	–1.7		
			T_A = 25°C	+Swing	+1.5	+2.0		
				–Swing	–1.4	–1.8		

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 8V$, $R_L = 150\Omega$ to GND and 470Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
BW	Gain bandwidth product	$A_{CL} = 7$, $V_O = 0.1\ V_{P-P}$		1200			1200		MHz
	Small signal bandwidth	$A_{CL} = 2$, $R_L = 150\Omega^1$		110			110		MHz
t_S	Settling time	$A_{CL} = 2$, $R_L = 150\Omega^1$		15			15		ns
SR	Slew rate	$A_{CL} = 2$, $R_L = 150\Omega^1$		600			600		V/µs
t_{PD}	Propagation delay	$A_{CL} = 2$, $R_L = 150\Omega^1$		7			7		ns
	Full power response	$A_{CL} = 2$, $R_L = 150\Omega^1$		48			48		MHz
	Full power response	$A_V = 7$, $R_L = 150\Omega^1$		20			20		MHz
	Input noise voltage	$R_S = 50\Omega$, 1MHz		4			4		nV/√Hz
	Input noise current	1MHz		6			6		pA/√Hz

NOTES:
1. External compensation.

AC ELECTRICAL CHARACTERISTICS

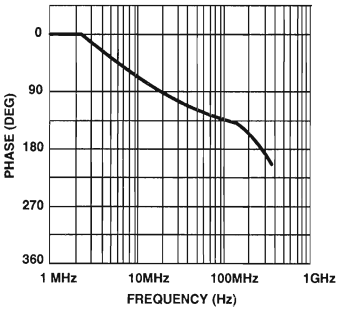
$V_{CC} = \pm 6V$, $R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			UNITS
			MIN	TYP	MAX	
BW	Gain bandwidth product	$A_{CL} = 7$		700		MHz
	Small signal bandwidth	$A_{CL} = 2^1$		120		
t_S	Settling time	$A_{CL} = 2^1$		23		ns
SR	Slew rate	$A_{CL} = 2^1$		330		V/µs
t_{PD}	Propagation delay	$A_{CL} = 2^1$		4.5		ns
	Full power response	$A_{CL} = 2^1$		20		MHz

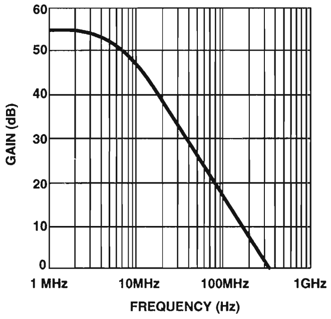
NOTES:
1. External compensation.

TYPICAL PERFORMANCE CURVES

NE5539 Open-Loop Phase

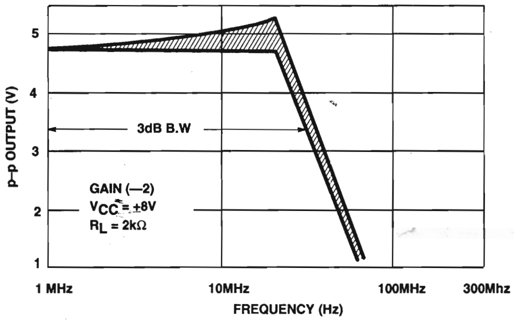


NE5539 Open-Loop Gain

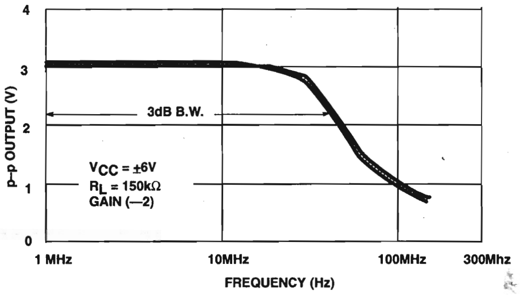


TYPICAL PERFORMANCE CURVES (Continued)

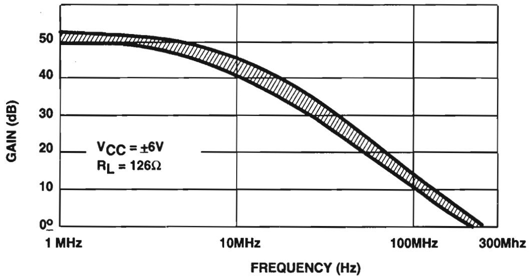
Power Bandwidth (SE)



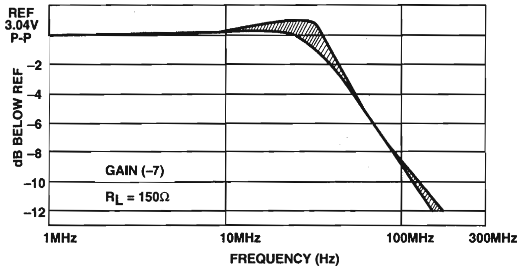
Power Bandwidth (NE)



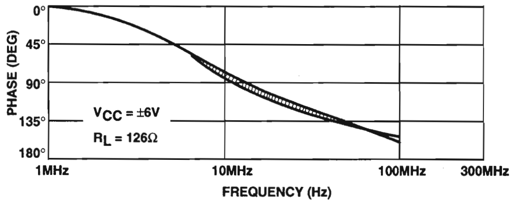
SE5539 Open-Loop Gain vs Frequency



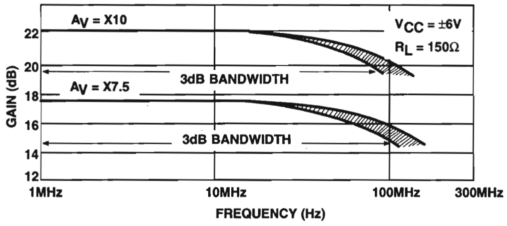
Power Bandwidth



SE5539 Open-Loop Phase vs Frequency



Gain Bandwidth Product vs Frequency

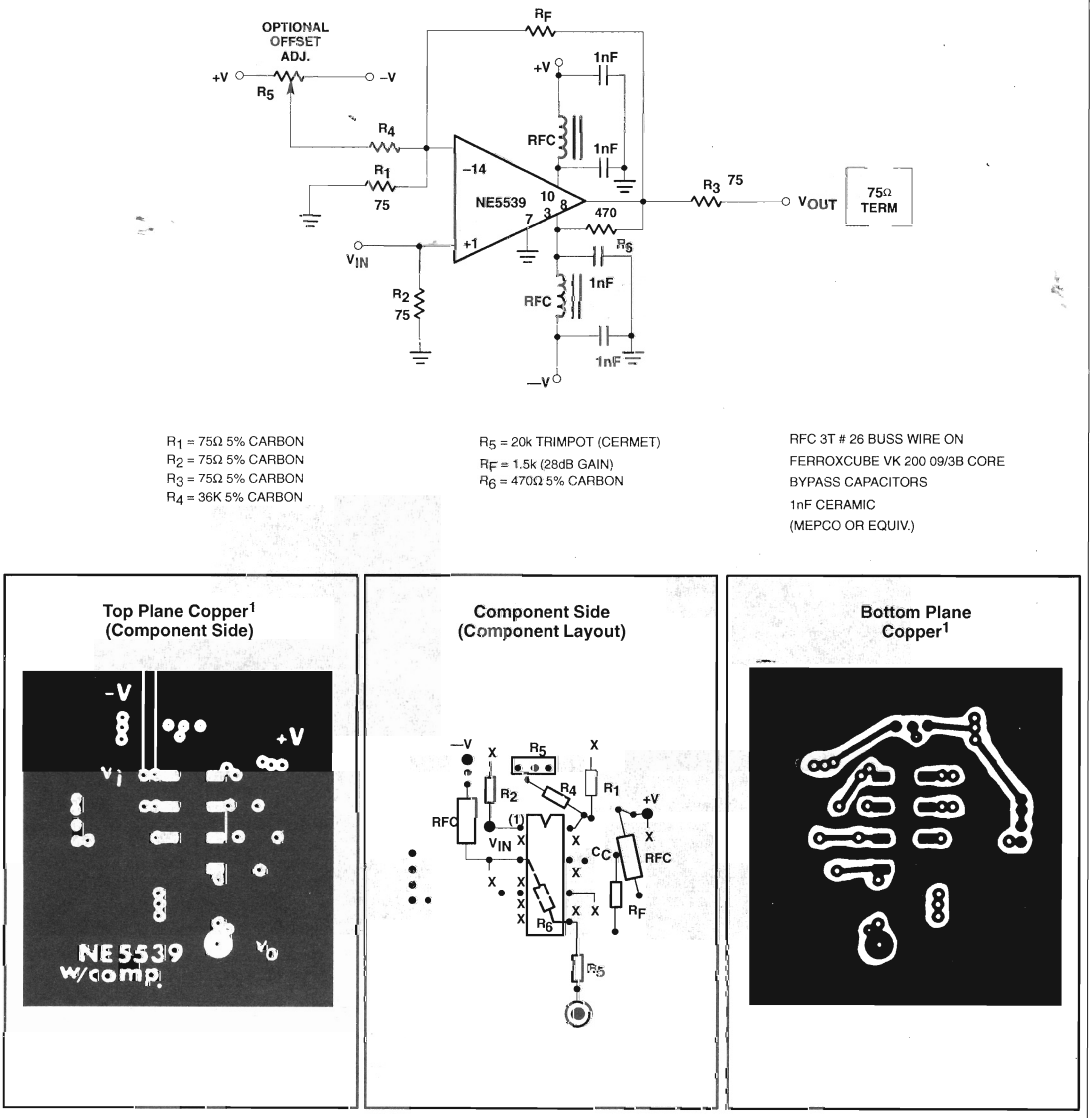


NOTE:

▨ Indicates typical distribution –55°C ≤ T_A ≤ 125°C

CIRCUIT LAYOUT CONSIDERATIONS

As may be expected for an ultra-high frequency, wide-gain bandwidth amplifier, the physical circuit is extremely critical. Bread-boarding is not recommended. A double-sided copper-clad printed circuit board will result in more favorable system operation. An example utilizing a 28dB non-inverting amp is shown in Figure 1.



R1 = 75Ω 5% CARBON
R2 = 75Ω 5% CARBON
R3 = 75Ω 5% CARBON
R4 = 36K 5% CARBON

R5 = 20k TRIMPOT (CERMET)
RF = 1.5k (28dB GAIN)
R6 = 470Ω 5% CARBON

RFC 3T # 26 BUSS WIRE ON
FERROXCUBE VK 200 09/3B CORE
BYPASS CAPACITORS
1nF CERAMIC
(MEPCO OR EQUIV.)

Figure 1. 28dB Non-Inverting Amp Sample PC Layout

NE5539 COLOR VIDEO AMPLIFIER

The NE5539 wideband operational amplifier is easily adapted for use as a color video amplifier. A typical circuit is shown in Figure 2 along with vector-scope1 photographs showing the amplifier differential gain and phase response to a standard five-step modulated staircase linearity signal (Figures 3, 4 and 5). As can be seen in Figure 4, the gain varies less than 0.5% from the bottom to the top of the staircase. The maximum differential phase shown in Figure 5 is approximately +0.1°.

The amplifier circuit was optimized for a 75Ω input and output termionation impedance with a gain of approximately 10 (20dB).

NOTE:

1. The input signal was 200mV and the output 2V. V_{CC} was ±8V.

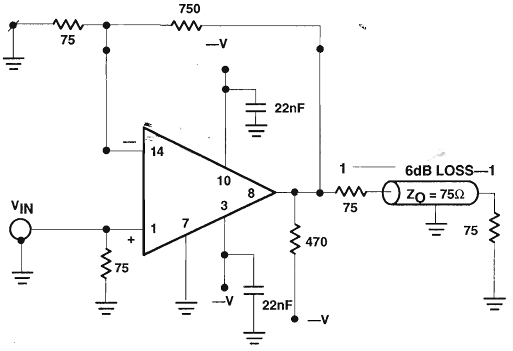


Figure 2. NE5539 Video Amplifier

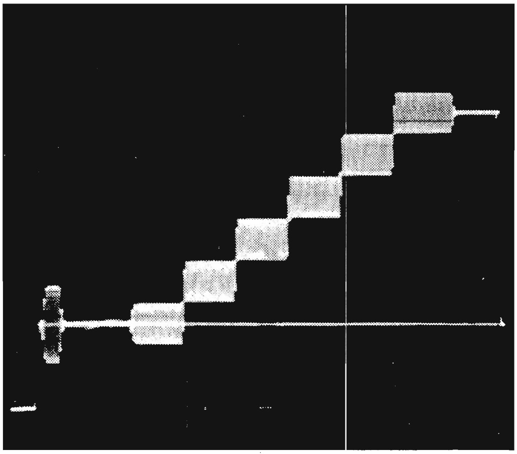


Figure 3. Input Signal

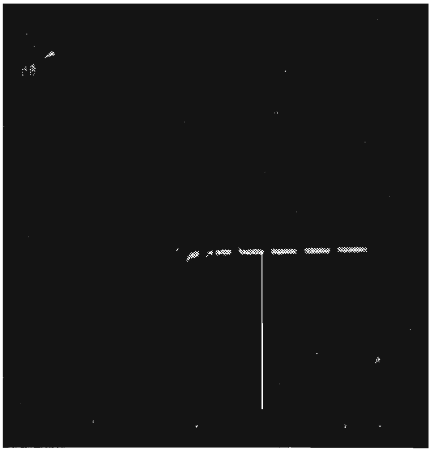


Figure 4. Differential Gain <0.5%

NOTE:

Instruments used for these measurements were Tektronix 146 NTSC test signal generator, 520A NTSC vectorscope, and 1480 waveform monitor.

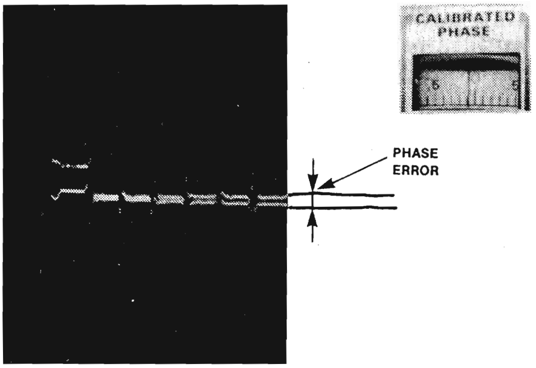


Figure 5. Differential Gain +0.1°

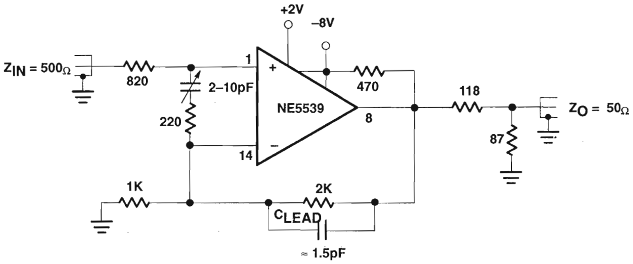


Figure 6. Non-Inverting Follower

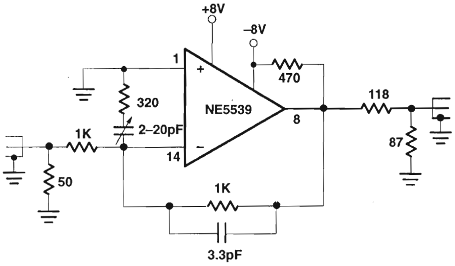


Figure 7. Inverting Follower

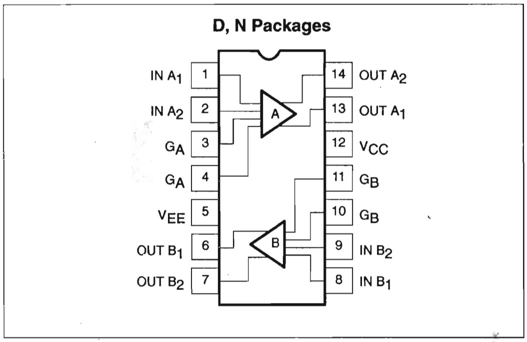
DESCRIPTION

The NE5592 is a dual monolithic, two-stage, differential output, wideband video amplifier. It offers a fixed gain of 400 without external components and an adjustable gain from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers.

FEATURES

- 110MHz unity gain bandwidth
- Adjustable gain from 0 to 400
- Adjustable pass band
- No frequency compensation required
- Wave shaping with minimal external components

PIN CONFIGURATION



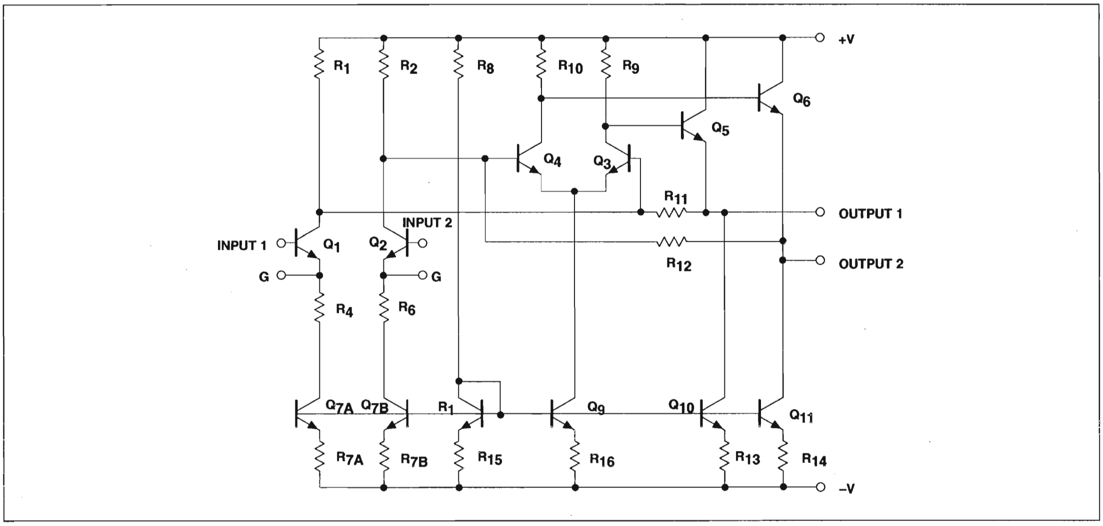
APPLICATIONS

- Floppy disk head amplifier
- Video amplifier
- Pulse amplifier in communications
- Magnetic memory
- Video recorder systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to 70°C	NE5592N	0405B
14-Pin Small Outline (SO) package	0 to 70°C	NE5592D	0175D

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common mode Input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating temperature range NE5592	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
$P_{D\ MAX}$	Maximum power dissipation, T_A=25°C (still air)[1] D package N package	 1.03 1.48	 W W

NOTES:

1. Derate above 25°C at the following rates:
   D package 8.3mW/°C
   N package 11.9mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A=+25°C, V_{SS}=±6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltage is V_S = ±6.0V, and gain select pins are connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
A_{VOL}	Differential voltage gain	R_L=2kΩ, V_{OUT}=3V_{P-P}	400	480	600	V/V
R_{IN}	Input resistance		3	14		kΩ
C_{IN}	Input capacitance			2.5		pF
I_{OS}	Input offset current			0.3	3	µA
I_{BIAS}	Input bias current			5	20	µA
	Input noise voltage	BW 1kHz to 10MHz		4		nV/√Hz
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	V_{CM} ± 1V, f<100kHz V_{CM} ± 1V, f=5MHz	60	93 87		dB dB
PSRR	Supply voltage rejection ratio	ΔV_S= ± 0.5V	50	85		dB
	Channel separation	V_{OUT}=1V_{P-P}; f=100kHz (output referenced) R_L=1kΩ	65	70		dB
V_{OS}	Output offset voltage gain select pins open	R_L=∞ R_L=∞		0.5 0.25	1.5 0.75	V V
V_{CM}	Output common-mode voltage	R_L=∞	2.4	3.1	3.4	V
V_{OUT}	Output differential voltage swing	R_L=2kΩ	3.0	4.0		V
R_{OUT}	Output resistance			20		Ω
I_{CC}	Power supply current (total for both sides)	R_L=∞		35	44	mA

DC ELECTRICAL CHARACTERISTICS

V_{SS}=±6V, V_{CM}=0, 0°C ≤ T_A ≤ 70°C, unless otherwise specified. Recommended operating supply voltage is V_S = ±6.0V, and gain select pins are connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
A_{VOL}	Differential voltage gain	R_L=2kΩ, V_{OUT}=3V_{P-P}	350	430	600	V/V
R_{IN}	Input resistance		1	11		kΩ
I_{OS}	Input offset current				5	μA
I_{BIAS}	Input bias current				30	μA
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	V_{CM} ± 1V, f<100kHz R_S=ϕ	55			dB
PSRR	Supply voltage rejection ratio	ΔV_S= ± 0.5V	50			dB
	Channel separation	V_{OUT}=1V_{P-P}; f=100kHz (output referenced) R_L=1kΩ		70		dB
V_{OS}	Output offset voltage gain select pins connected together gain select pins open	 R_L=∞ R_L=∞			 1.5 1.0	 V V
V_{OUT}	Output differential voltage swing	R_L=2kΩ	2.8			V
I_{CC}	Power supply current (total for both sides)	R_L=∞			47	mA

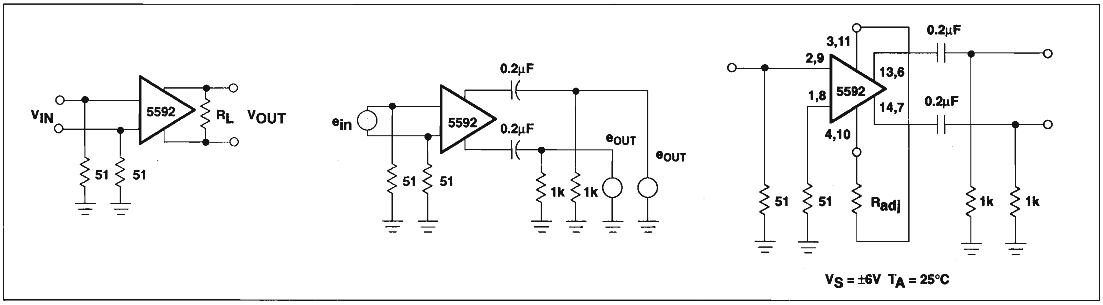
AC ELECTRICAL CHARACTERISTICS

T_A=+25°C V_{SS}=±6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltage V_S=±6.0V. Gain select pins connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
BW	Bandwidth	V_{OUT}=1V_{P-P}		25		MHz
t_R	Rise time			15	20	ns
t_{PD}	Propagation delay	V_{OUT}=1V_{P-P}		7.5	12	ns

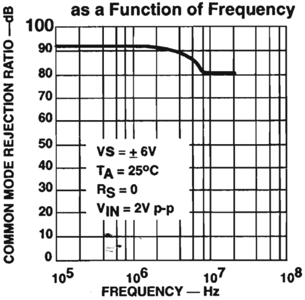
TEST CIRCUITS

T_A=25°C unless otherwise specified.

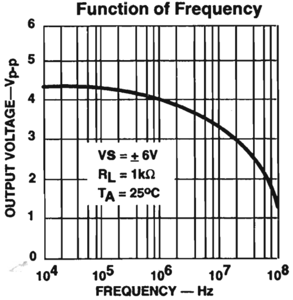


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

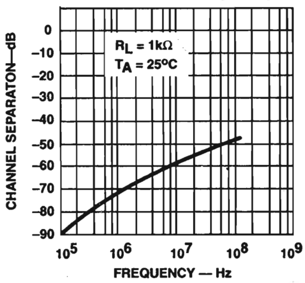
Common-Mode Rejection Ratio as a Function of Frequency



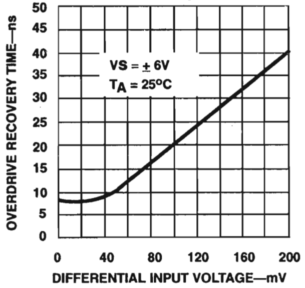
Output Voltage Swing as a Function of Frequency



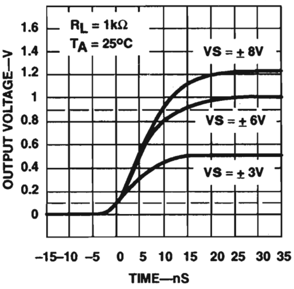
Channel Separation as a Function of Frequency



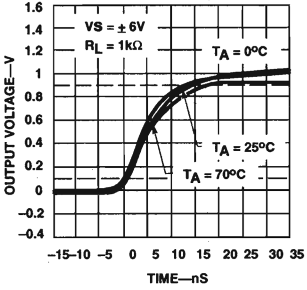
Differential Overdrive Recovery Time



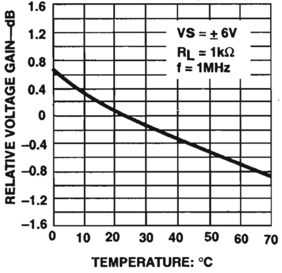
Pulse Response as a Function of Supply Voltage



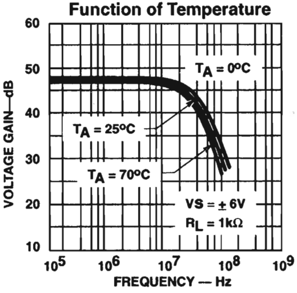
Pulse Response as a Function of Temperature



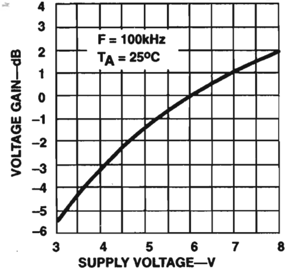
Voltage Gain as a Function of Temperature



Gain vs Frequency as a Function of Temperature

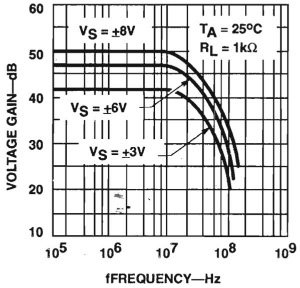


Voltage Gain as a Function of Supply Voltage

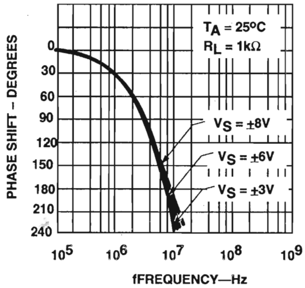


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

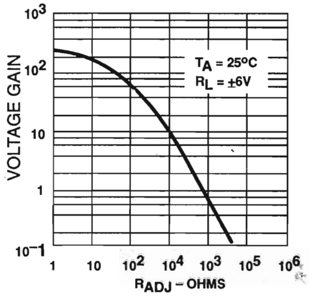
Gain vs Frequency as a Function of Supply Voltage



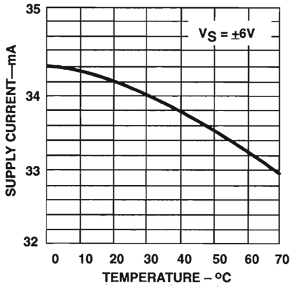
Phase vs Frequency as a Function of Supply Voltage



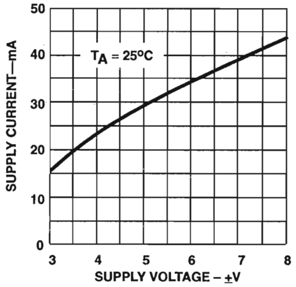
Voltage Gain as a Function of R_{ADJ}



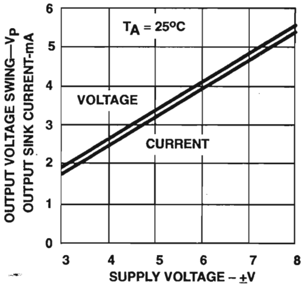
Supply Current as a Function of Temperature



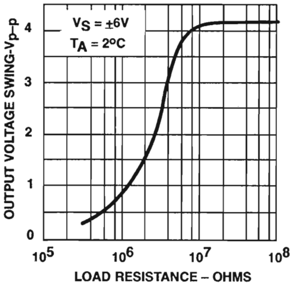
Supply Current as a Function of Supply Voltage



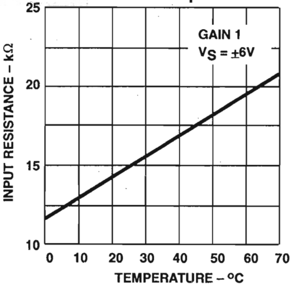
Output Voltage Swing and Sink Current as a Function of Supply Voltage



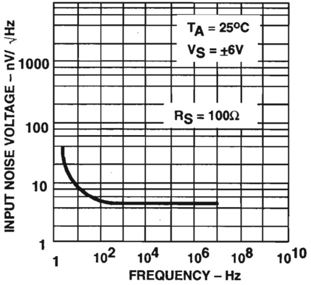
Output Voltage Swing as a Function of Load Resistance



Input Resistance as a Function of Temperature



Input Noise Voltage as a Function of Frequency



Video amplifier NE592

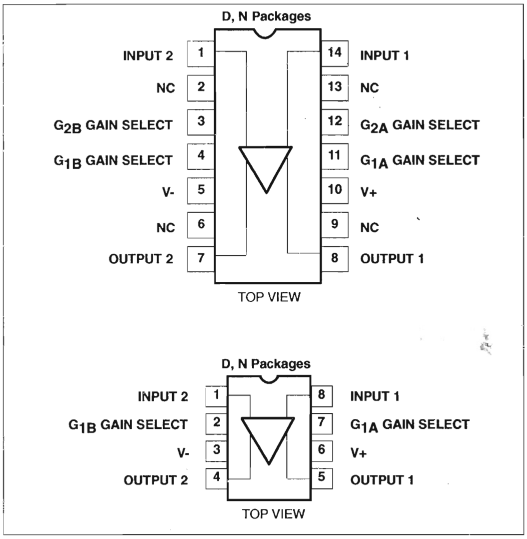
DESCRIPTION

The NE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers. Now available in an 8-pin version with fixed gain of 400 without external components and adjustable gain from 400 to 0 with one external resistor.

FEATURES

- 120MHz unity gain bandwidth
- Adjustable gains from 0 to 400
- Adjustable pass band
- No frequency compensation required
- Wave shaping with minimal external components
- MIL-STD processing available

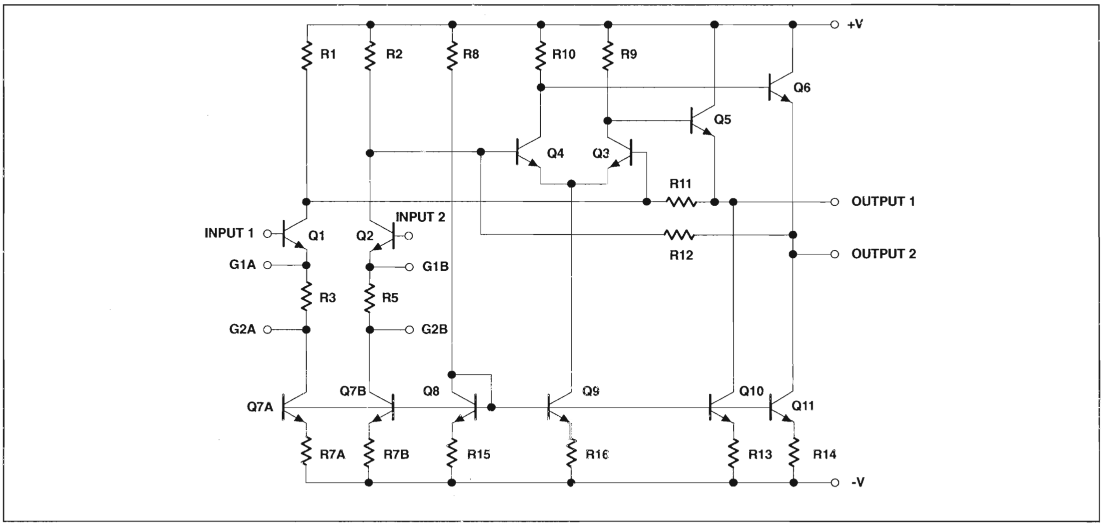
PIN CONFIGURATIONS



APPLICATIONS

- Floppy disk head amplifier
- Video amplifier
- Pulse amplifier in communications
- Magnetic memory
- Video recorder systems

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE592N14	0405B
14-Pin Small Outline (SO) package	0 to +70°C	NE592D14	0175D
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE592N8	0404B
8-Pin Small Outline (SO) package	0 to +70°C	NE592D8	0174C

NOTES:

N8, N14, D8 and D14 package parts also available in "High" gain version by adding "H" before package designation, i.e., NE592HDB

ABSOLUTE MAXIMUM RATINGS

T_A=+25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
$P_{D\ MAX}$	Maximum power dissipation, T_A=25°C (still air)[1]		
	D-14 package	0.98	W
	D-8 package	0.79	W
	N-14 package	1.44	W
	N-8 package	1.17	W

NOTES:

1. Derate above 25°C at the following rates:
   D-14 package at 7.8mW/°C
   D-8 package at 6.3mW/°C
   N-14 package at 11.5mW/°C
   N-8 package at 9.3mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A=+25°C V_{SS}=±6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltages V_S=±6.0V. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE592			UNIT
			Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part					
	Gain 1[1]	R_L=2kΩ, V_{OUT}=3V_{P-P}	250	400	600	V/V
	Gain 2[2, 4]		80	100	120	V/V
R_{IN}	Input resistance					
	Gain 1[1]			4.0		kΩ
	Gain 2[2, 4]		10	30		kΩ
C_{IN}	Input capacitance[2]	Gain 2[4]		2.0		pF
I_{OS}	Input offset current			0.4	5.0	µA
I_{BIAS}	Input bias current			9.0	30	µA
V_{NOISE}	Input noise voltage	BW 1kHz to 10MHz		12		µV_{RMS}
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio					
	Gain 2[4]	V_{CM}±1V, f<100kHz	60	86		dB
	Gain 2[4]	V_{CM}±1V, f=5MHz		60		dB
PSRR	Supply voltage rejection ratio					
	Gain 2[4]	ΔV_S=±0.5V	50	70		dB
V_{OS}	Output offset voltage					
	Gain 1	R_L=∞			1.5	V
	Gain 2[4]	R_L=∞			1.5	V
	Gain 3[3]	R_L=∞		0.35	0.75	V
V_{CM}	Output common-mode voltage	R_L=∞	2.4	2.9	3.4	V
V_{OUT}	Output voltage swing differential	R_L=2kΩ	3.0	4.0		V
R_{OUT}	Output resistance			20		Ω
I_{CC}	Power supply current	R_L=∞		18	24	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 14-pin version only.

DC ELECTRICAL CHARACTERISTICS

DC Electrical CharacteristicsV_{SS}=±6V, V_{CM}=0, 0°C ≤T_A≤70°C, unless otherwise specified. Recommended operating supply voltages V_S=±6.0V. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE592			UNIT
			Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part Gain 1[1] Gain 2[2, 4]	R_L=2kΩ, V_{OUT}=3V_{P-P}	 250 80		 600 120	 V/V V/V
R_{IN}	Input resistance Gain 2[2, 4]		 8.0			 kΩ
I_{OS}	Input offset current				6.0	μA
I_{BIAS}	Input bias current				40	μA
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio Gain 2[4]	V_{CM}±1V, f<100kHz	 50			 dB
PSRR	Supply voltage rejection ratio Gain 2[4]	ΔV_S=±0.5V	 50			 dB
V_{OS}	Output offset voltage Gain 1 Gain 2[4] Gain 3[3]	R_L=∞			 1.5 1.5 1.0	V
V_{OUT}	Output voltage swing differential	R_L=2kΩ	2.8			V
I_{CC}	Power supply current	R_L=∞			27	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 14-pin versions only.

AC ELECTRICAL CHARACTERISTICS

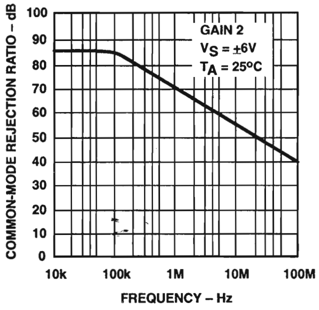
T_A=+25°C V_{SS}=±6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltages V_S=±6.0V. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			UNIT
			Min	Typ	Max	
BW	Bandwidth Gain 1[1] Gain 2[2, 4]			 40 90		 MHz MHz
t_R	Rise time Gain 1[1] Gain 2[2, 4]	V_{OUT}=1V_{P-P}		 10.5 4.5	 12	 ns ns
t_{PD}	Propagation delay Gain 1[1] Gain 2[2, 4]	V_{OUT}=1V_{P-P}		 7.5 6.0	 10	 ns ns

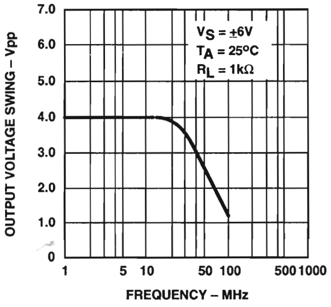
NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 14-pin versions only.

TYPICAL PERFORMANCE CHARACTERISTICS

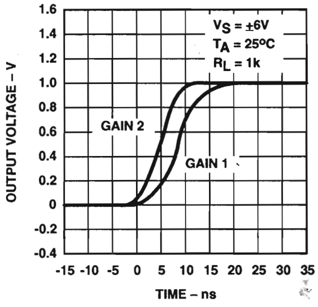
Common-Mode Rejection Ratio as a Function of Frequency



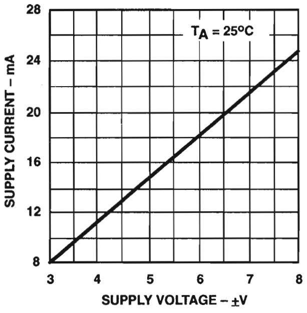
Output Voltage Swing as a Function of Frequency



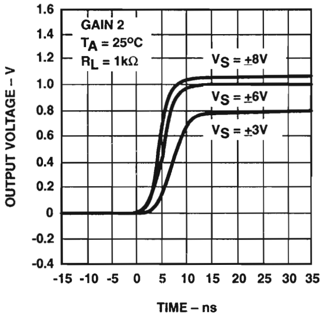
Pulse Response



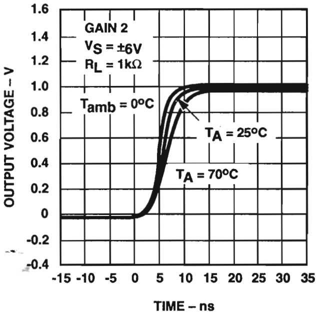
Supply Current as a Function of Temperature



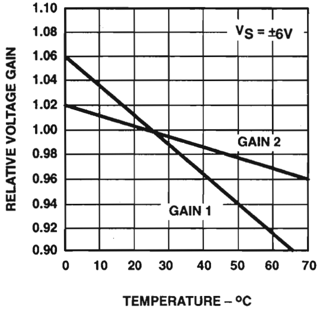
Pulse Response as a Function of Supply Voltage



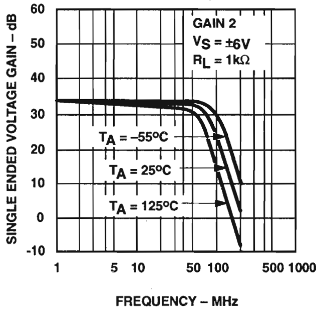
Pulse Response as a Function of Temperature



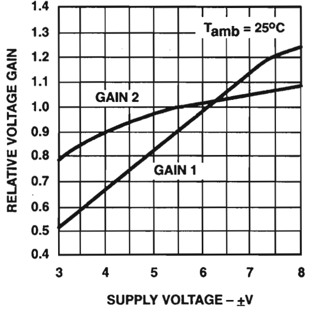
Voltage Gain as a Function of Temperature



Gain vs. Frequency as a Function of Temperature

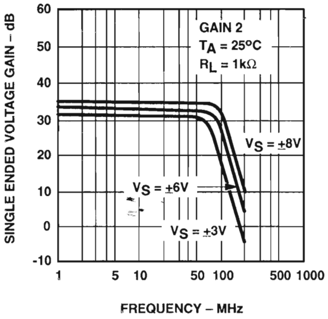


Voltage Gain as a Function of Supply Voltage

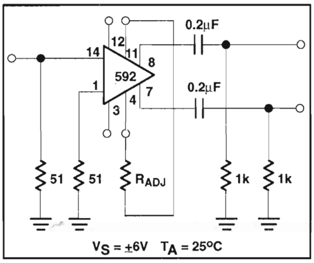


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

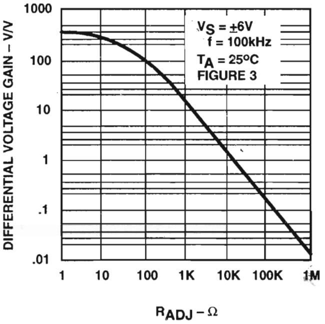
Gain vs. Frequency as a Function of Supply Voltage



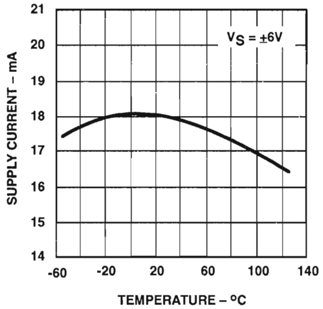
Voltage Gain Adjust Circuit



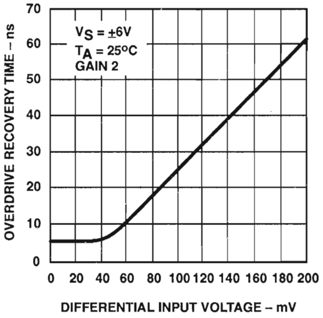
Voltage Gain as a Function of RADJ (Figure 3)



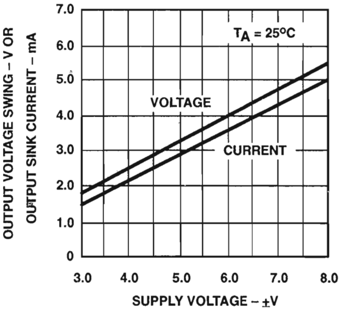
Supply Current as a Function of Temperature



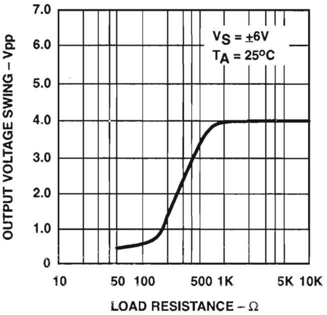
Differential Overdrive Recovery Time



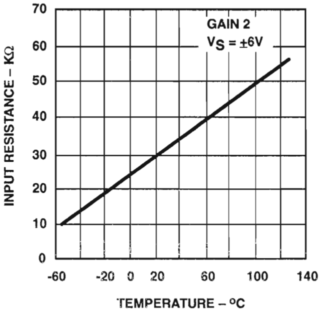
Output Voltage and Current Swing as a Function of Supply Voltage



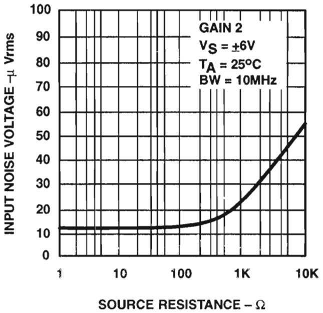
Output Voltage Swing as a Function of Load Resistance

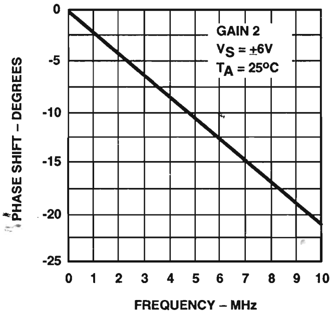


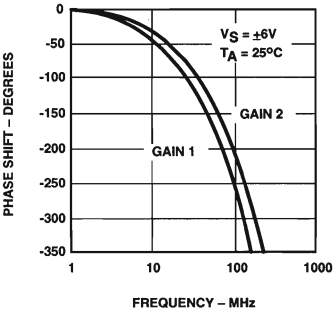
Input Resistance as a Function of Temperature

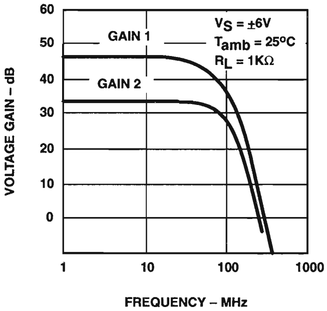


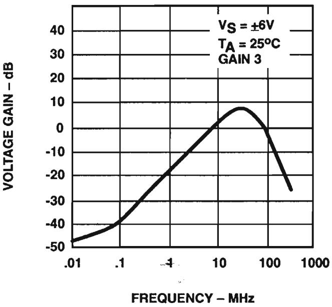
Input Noise Voltage as a Function of Source Resistance



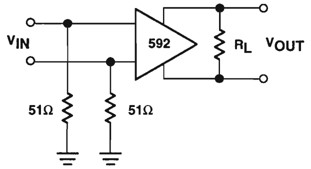

Phase Shift as a Function of Frequency

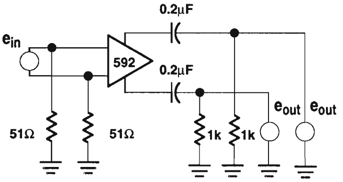

Phase Shift as a Function of Frequency


Voltage Gain as a Function of Frequency


Voltage Gain as a Function of Frequency

TEST CIRCUITS T$_A$ = 25°C, unless otherwise specified.



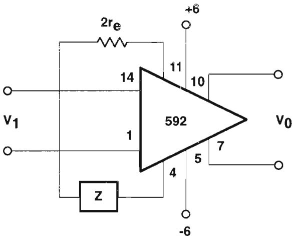


TYPICAL APPLICATIONS

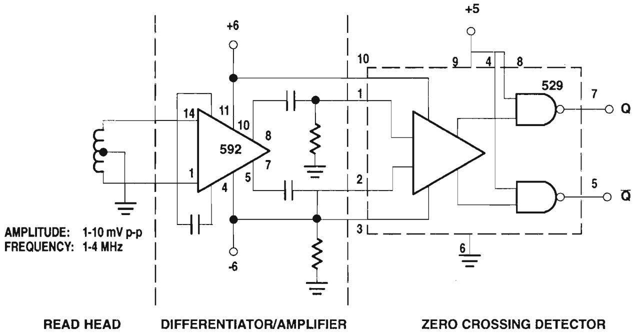
NOTE:

$$\frac{V_O(s)}{V_1(s)} \approx \frac{1.4 \cdot 10^4}{Z(S) + 2r_e}$$

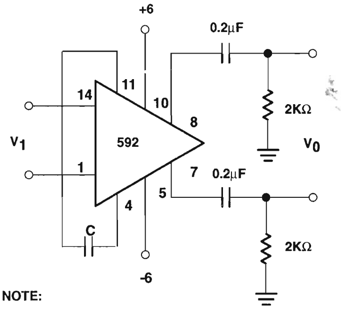
$$\approx \frac{1.4 \cdot 10^4}{Z(S) + 32}$$



Basic Configuration



Disc/Tape Phase-Modulated Readback Systems



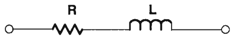
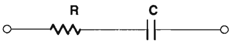
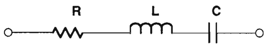
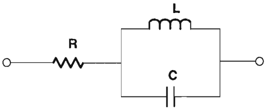
NOTE:

For frequency $F_1 << 1/2\pi(32)C$

$$V_O \approx 1.4 \times 10^4 C \frac{dV_i}{dT}$$

Differentiation with High Common-Mode Noise Rejection

FILTER NETWORKS

Z NETWORK	FILTER TYPE	$\frac{V_O(s)}{V_1(s)}$ TRANSFER FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/Ls + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTES:

In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.

$S = j\omega$

$\omega = 2\pi f$

6W audio amplifier with preamplifier

TDA1010A

The TDA1010A is a monolithic integrated class-B audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a 6 W car radio amplifier for use with 4 Ω and 2 Ω load impedances. The wide supply voltage range and the flexibility of the IC make it an attractive proposition for record players and tape recorders with output powers up to 10 W.

Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- low-cost external components
- good ripple rejection
- thermal protection

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 24	V
Repetitive peak output current	I_{ORM}	max.	3	A
Output power at pin 2; d_{tot} = 10%				
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	6,4	W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	6,2	W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3,4	W
V_P = 14,4 V; R_L = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_o	typ.	9	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2	%
Input impedance				
preamplifier (pin 8)	$\lvert Z_i \rvert$	typ.	30	kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ.	20	kΩ
Total quiescent current at V_P = 14,4 V	I_{tot}	typ.	31	mA
Sensitivity for P_o = 5,8 W; R_L = 4 Ω	V_i	typ.	10	mV
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

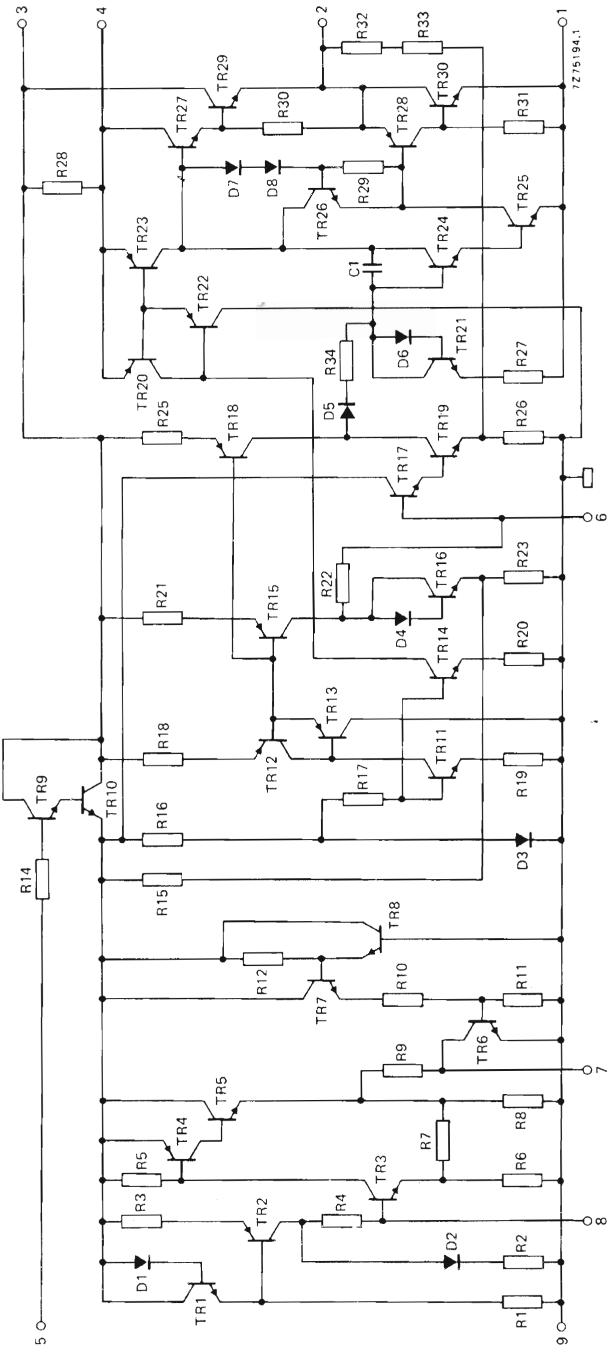


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24	V
Peak output current	I_{OM}	max.	5	A
Repetitive peak output current	I_{ORM}	max.	3	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−25 to + 150	°C
A.C. short-circuit duration of load during sine-wave drive; without heatsink at V_P = 14,4 V	t_{sc}	max.	100	hours

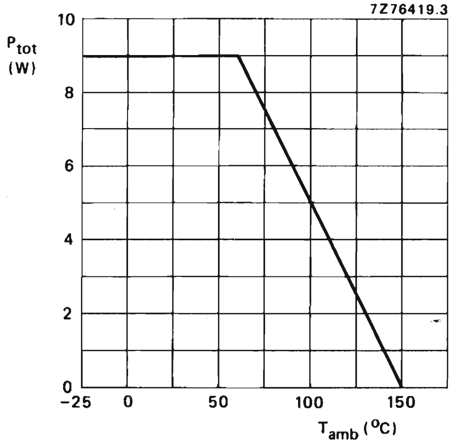


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 14,4 V; R_L = 2 Ω; T_{amb} = 60 °C maximum; thermal shut-down starts at T_j = 150 °C. The maximum sine-wave dissipation in a 2 Ω load is about 5,2 W. The maximum dissipation for music drive will be about 75% of the worst-case sine-wave dissipation, so this will be 3,9 W. Consequently, the total resistance from junction to ambient

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{3{,}9} = 23\ \text{K/W}.$$

Since $R_{th\ j\text{-}tab} = 10$ K/W and $R_{th\ tab\text{-}h} = 1$ K/W,

$$R_{th\ h\text{-}a} = 23 - (10 + 1) = 12\ \text{K/W}.$$

D.C. CHARACTERISTICS

Supply voltage range	V_P		6 to 24	V
Repetitive peak output current	I_{ORM}	<	3	A
Total quiescent current at $V_P = 14{,}4$ V	I_{tot}	typ.	31	mA

A.C. CHARACTERISTICS

$T_{amb} = 25\ ^{o}C$; $V_P = 14{,}4$ V; $R_L = 4\ \Omega$; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power (see Fig. 4) at $d_{tot} = 10\%$; measured at pin 2; with bootstrap				
$V_P = 14{,}4$ V; $R_L = 2\ \Omega$ (note 1)	P_o	typ.	6,4	W
$V_P = 14{,}4$ V; $R_L = 4\ \Omega$ (note 1 and 2)	P_o	>	5,9	W
		typ.	6,2	W
$V_P = 14{,}4$ V; $R_L = 8\ \Omega$ (note 1)	P_o	typ.	3,4	W
$V_P = 14{,}4$ V; $R_L = 4\ \Omega$; without bootstrap	P_o	typ.	5,7	W
$V_P = 14{,}4$ V; $R_L = 2\ \Omega$; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_o	typ.	9	W
Voltage gain				
preamplifier (note 3)	G_{v1}	typ.	24	dB
			21 to 27	dB
power amplifier	G_{v2}	typ.	30	dB
			27 to 33	dB
total amplifier	$G_{v\,tot}$	typ.	54	dB
			51 to 57	dB
Total harmonic distortion at $P_o = 1$ W	d_{tot}	typ.	0,2	%
Efficiency at $P_o = 6$ W	η	typ.	75	%
Frequency response (−3 dB)	B		80 Hz to 15	kHz
Input impedance				
preamplifier (note 4)	$\lvert Z_i \rvert$	typ.	30	kΩ
			20 to 40	kΩ
power amplifier (note 5)	$\lvert Z_i \rvert$	typ.	20	kΩ
			14 to 26	kΩ
Output impedance of preamplifier; pin 7 (note 5)	$\lvert Z_o \rvert$	typ.	20	kΩ
			14 to 26	kΩ
Output voltage preamplifier (r.m.s. value) $d_{tot} < 1\%$ (pin 7) (note 3)	$V_{o(rms)}$	>	0,7	V
Noise output voltage (r.m.s. value; note 6)				
$R_S = 0\ \Omega$	$V_{n(rms)}$	typ.	0,3	mV
$R_S = 8{,}2$ kΩ	$V_{n(rms)}$	typ.	0,7	mV
		<	1,4	mV
Ripple rejection at f = 1 kHz to 10 kHz (note 7)	RR	>	42	dB
at f = 100 Hz; C2 = 1 μF	RR	>	37	dB
Sensitivity for $P_o = 5{,}8$ W	V_i	typ.	10	mV
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ.	30	mA

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Up to $P_o \leqslant 3$ W : $d_{tot} \leqslant 1\%$.
3. Measured with a load impedance of 20 kΩ.
4. Independent of load impedance of preamplifier.
5. Output impedance of preamplifier ($|Z_o|$) is correlated (within 10%) with the input impedance ($|Z_i|$) of the power amplifier.
6. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
7. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude: 2 V).
8. The tab must be electrically floating or connected to the substrate (pin 9).

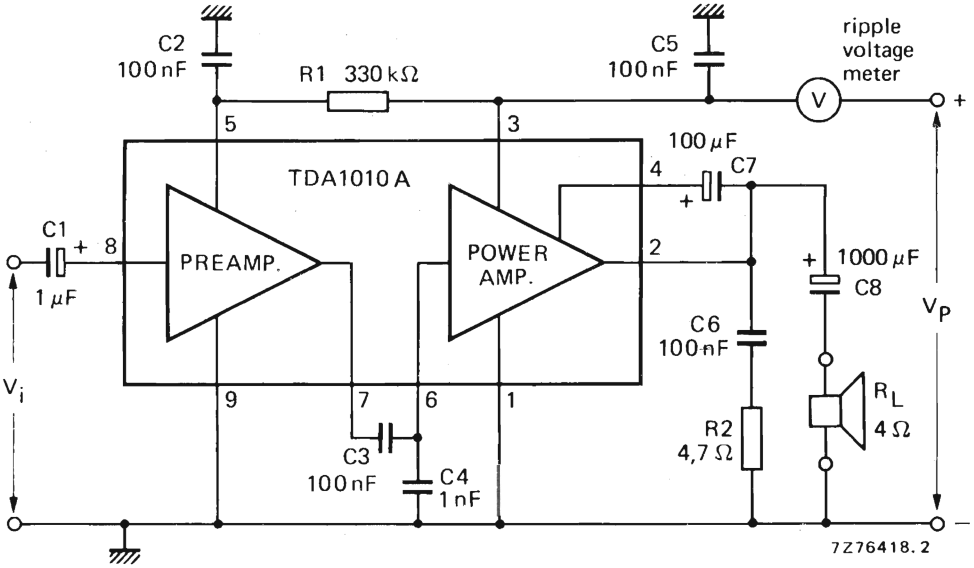


Fig. 3 Test circuit.

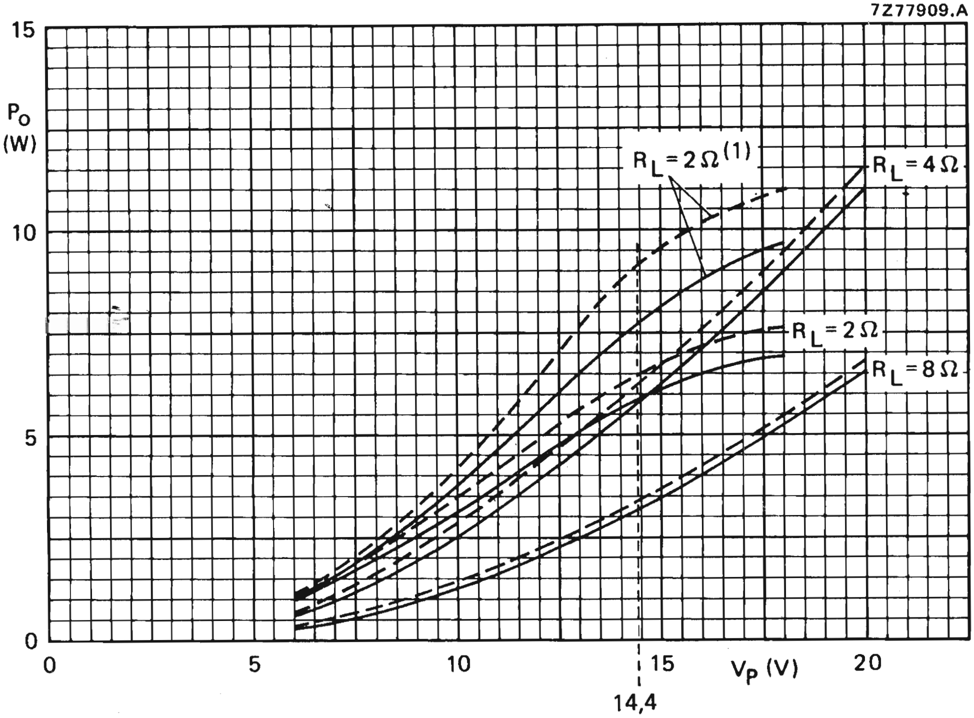


Fig. 4 Output power of the circuit of Fig. 3 as a function of the supply voltage with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\,\Omega^{(1)}$ has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, d_{tot} = 10%, T_{amb} = 25 °C.

Fig. 5 See next page.
Total harmonic distortion in the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\,\Omega^{(1)}$ has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, V_P = 14,4 V.

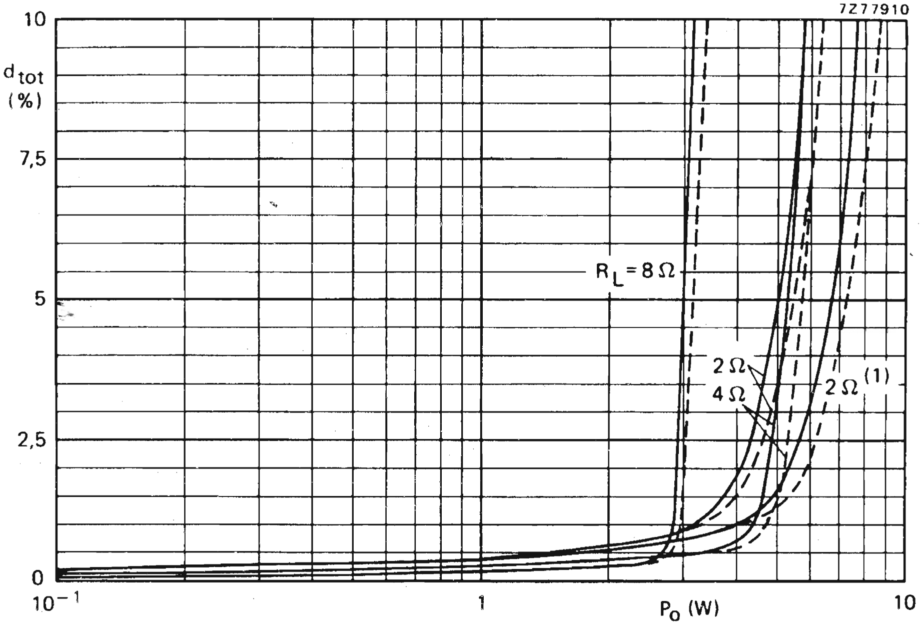


Fig. 5 For caption see preceding page.

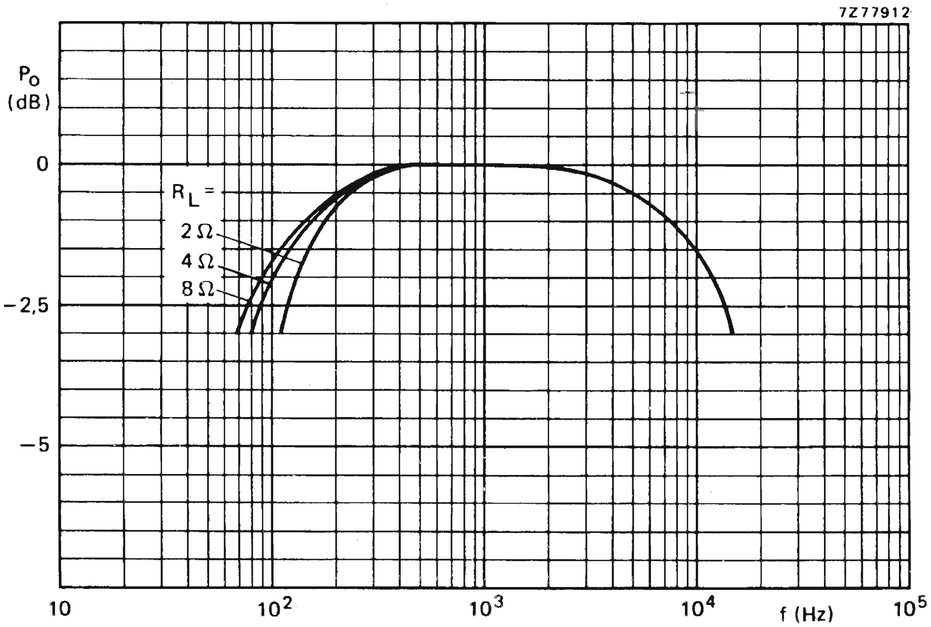


Fig. 6 Frequency characteristics of the circuit of Fig. 3 for three values of load impedance; typical values. P_o relative to 0 dB = 1 W; V_P = 14,4 V.

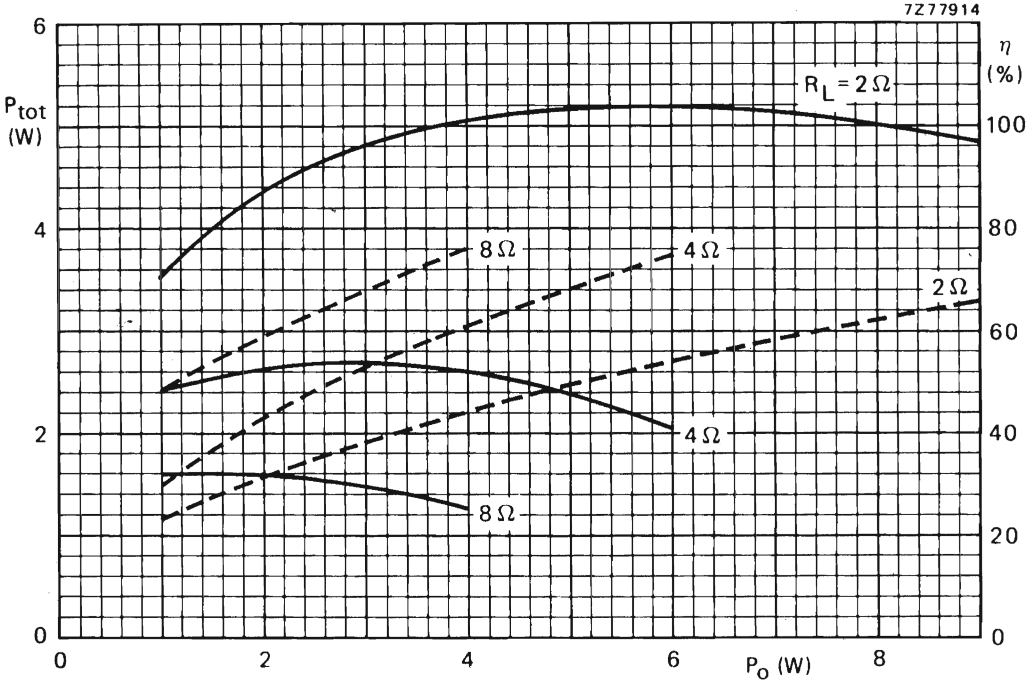


Fig. 7 Total power dissipation (solid lines) and the efficiency (dashed lines) of the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter (for $R_L = 2\ \Omega$ an external bootstrap resistor of 220 Ω has been used); typical values. $V_P = 14{,}4$ V; f = 1 kHz.

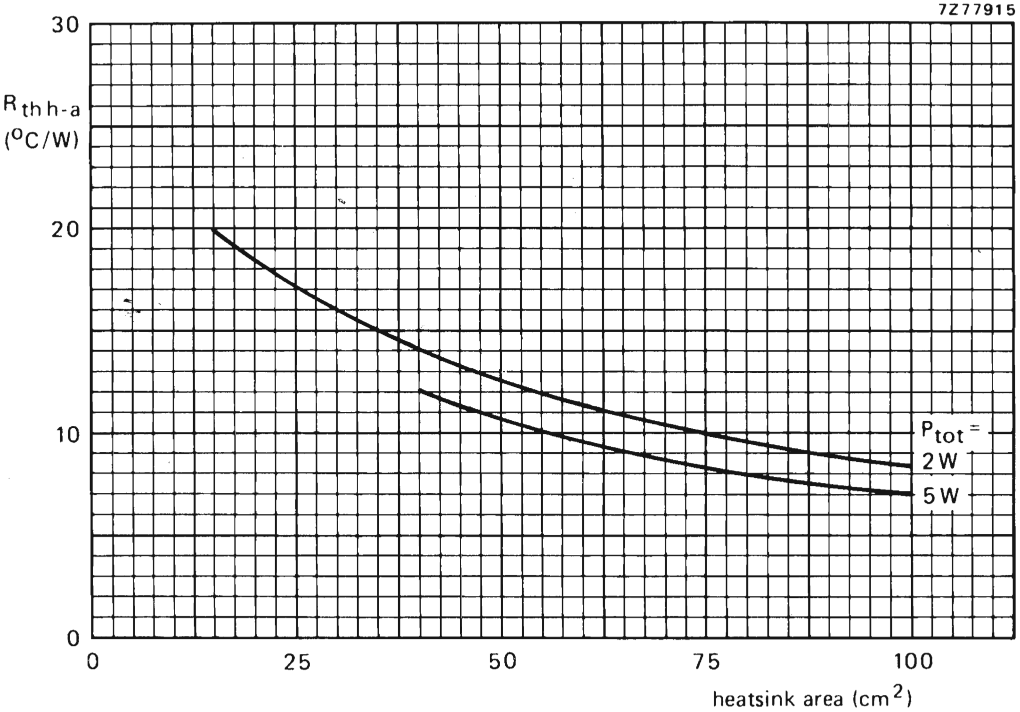


Fig. 8 Thermal resistance from heatsink to ambient of a 1,5 mm thick bright aluminium heatsink as a function of the single-sided area of the heatsink with the total power dissipation as a parameter.

APPLICATION INFORMATION

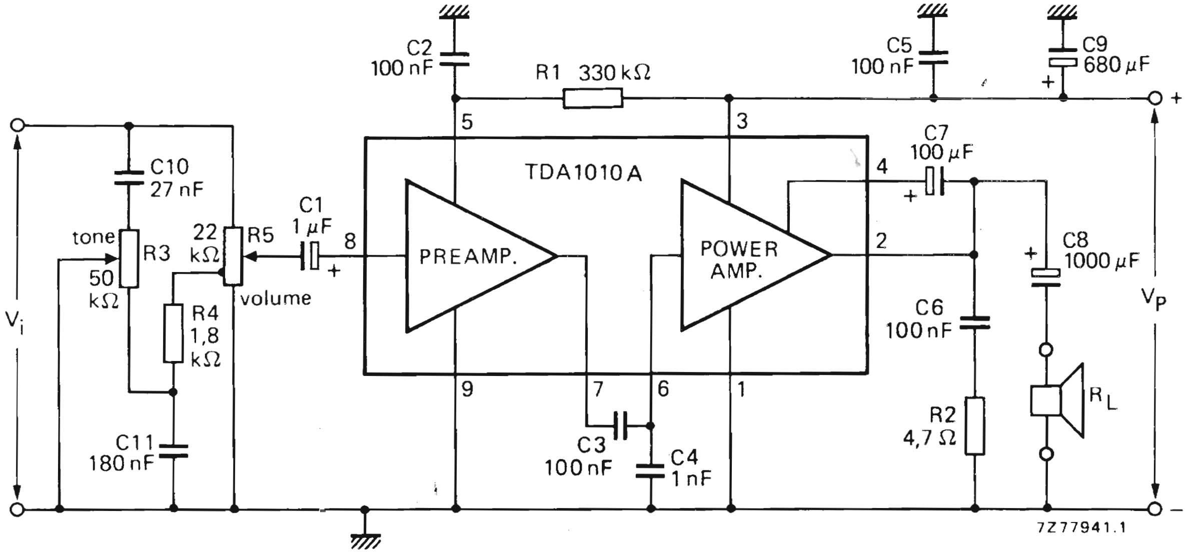


Fig. 9 Complete mono audio amplifier of a car radio.

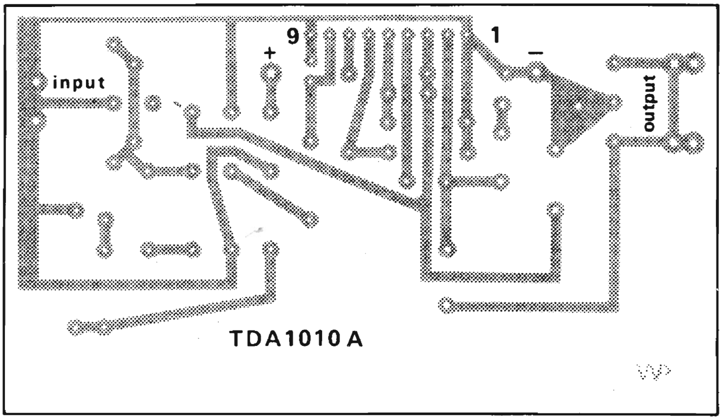


Fig. 10 Track side of printed-circuit board used for the circuit of Fig. 9; p.c. board dimensions 92 mm x 52 mm.

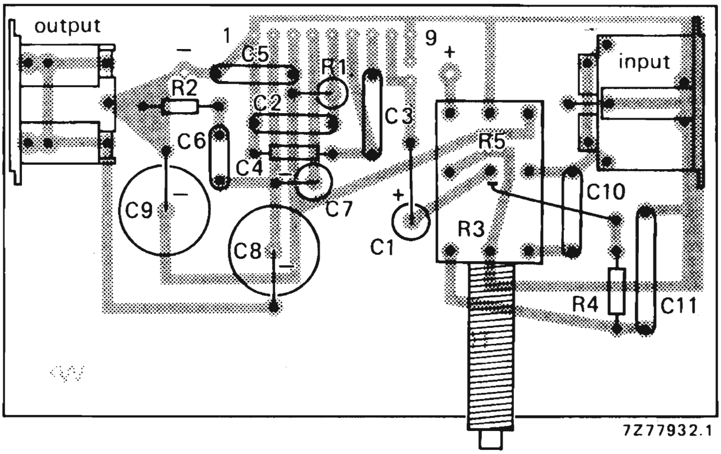


Fig. 11 Component side of printed-circuit board showing component layout used for the circuit of Fig. 9.

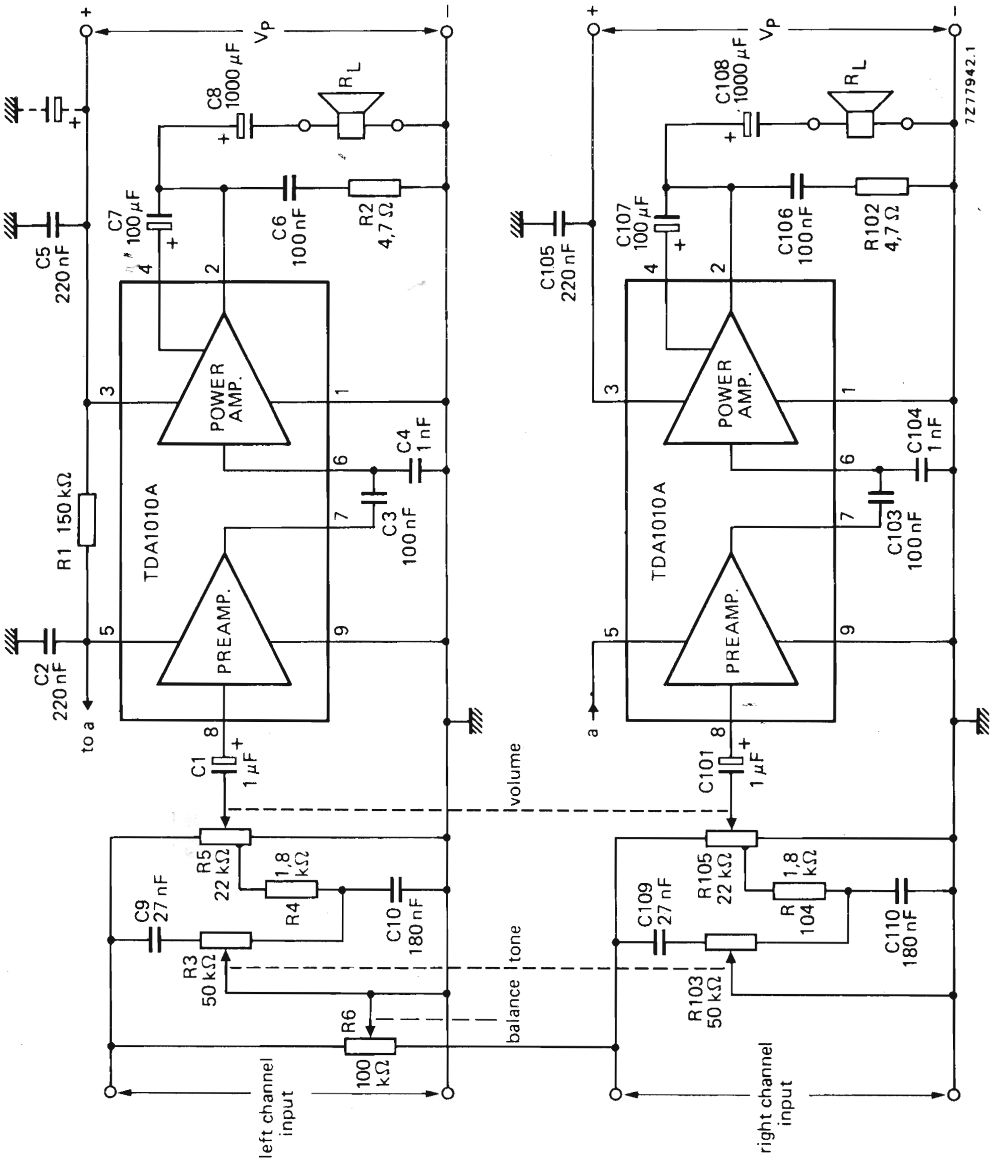


Fig. 12 Complete stereo car radio amplifier.

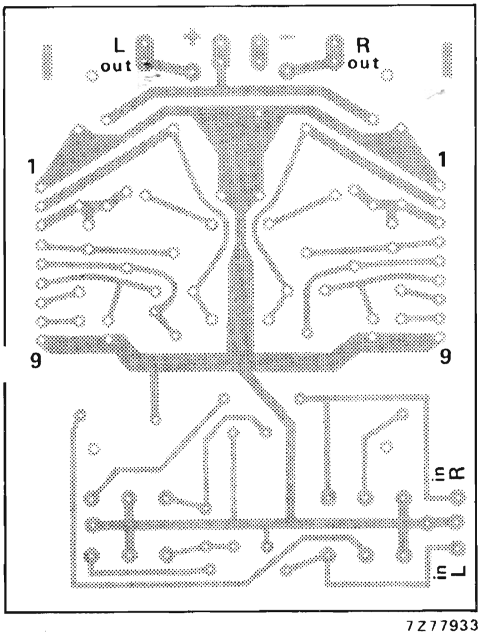


Fig. 13 Track side of printed-circuit board used for the circuit of Fig. 12; p.c. board dimensions 83 mm x 65 mm.

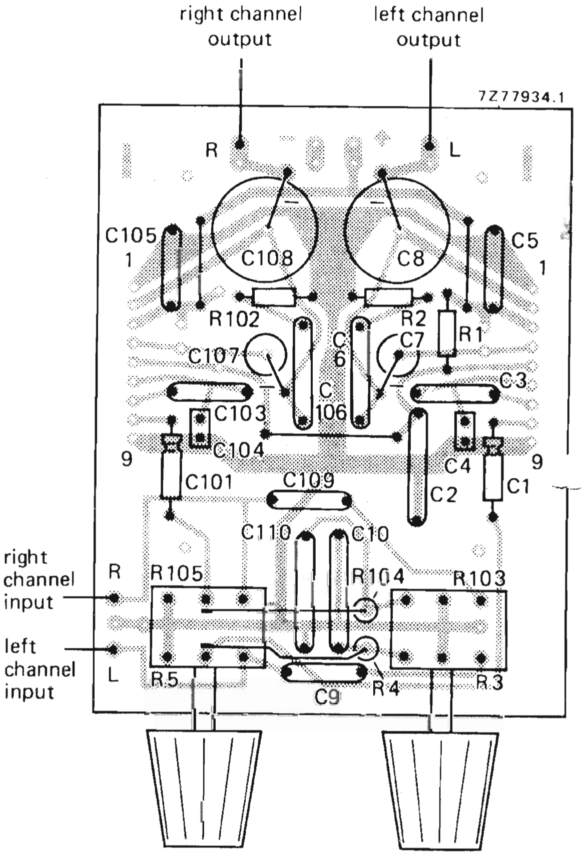


Fig. 14 Component side of printed-circuit board showing component layout used for the circuit of Fig. 12. Balance control is not on the p.c. board.

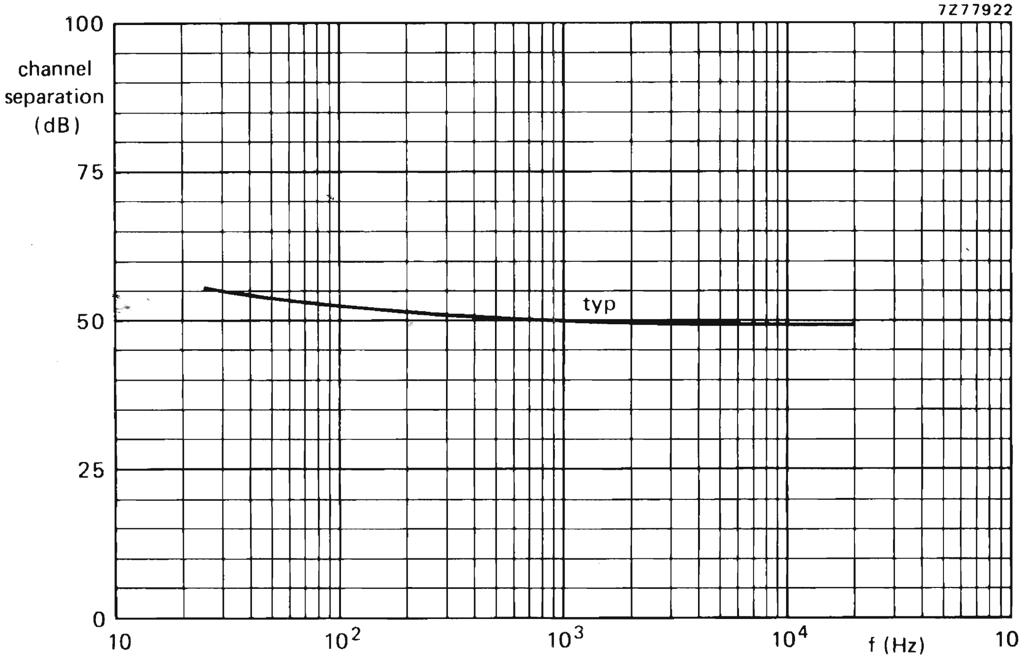


Fig. 15 Channel separation of the circuit of Fig. 12 as a function of the frequency.

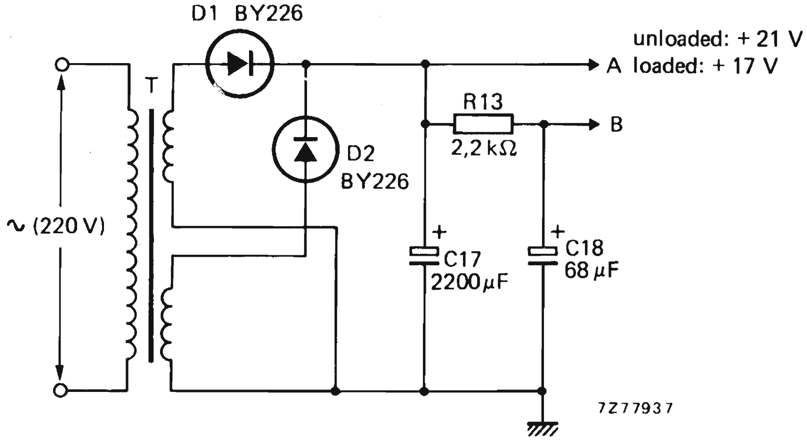


Fig. 16 Power supply of circuit of Fig. 17.

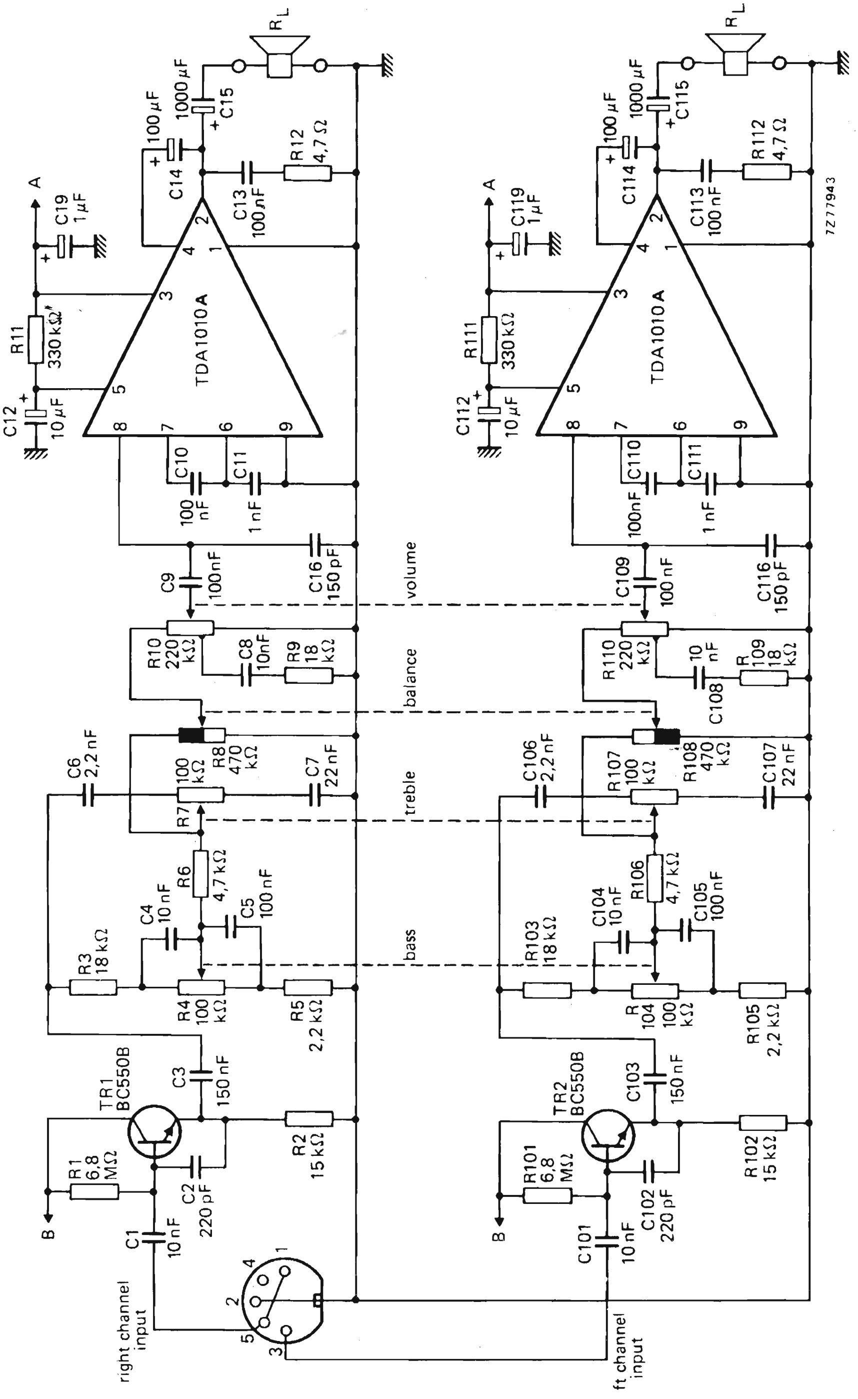


Fig. 17 Complete mains-fed ceramic stereo pick-up amplifier; for power supply see Fig. 16.

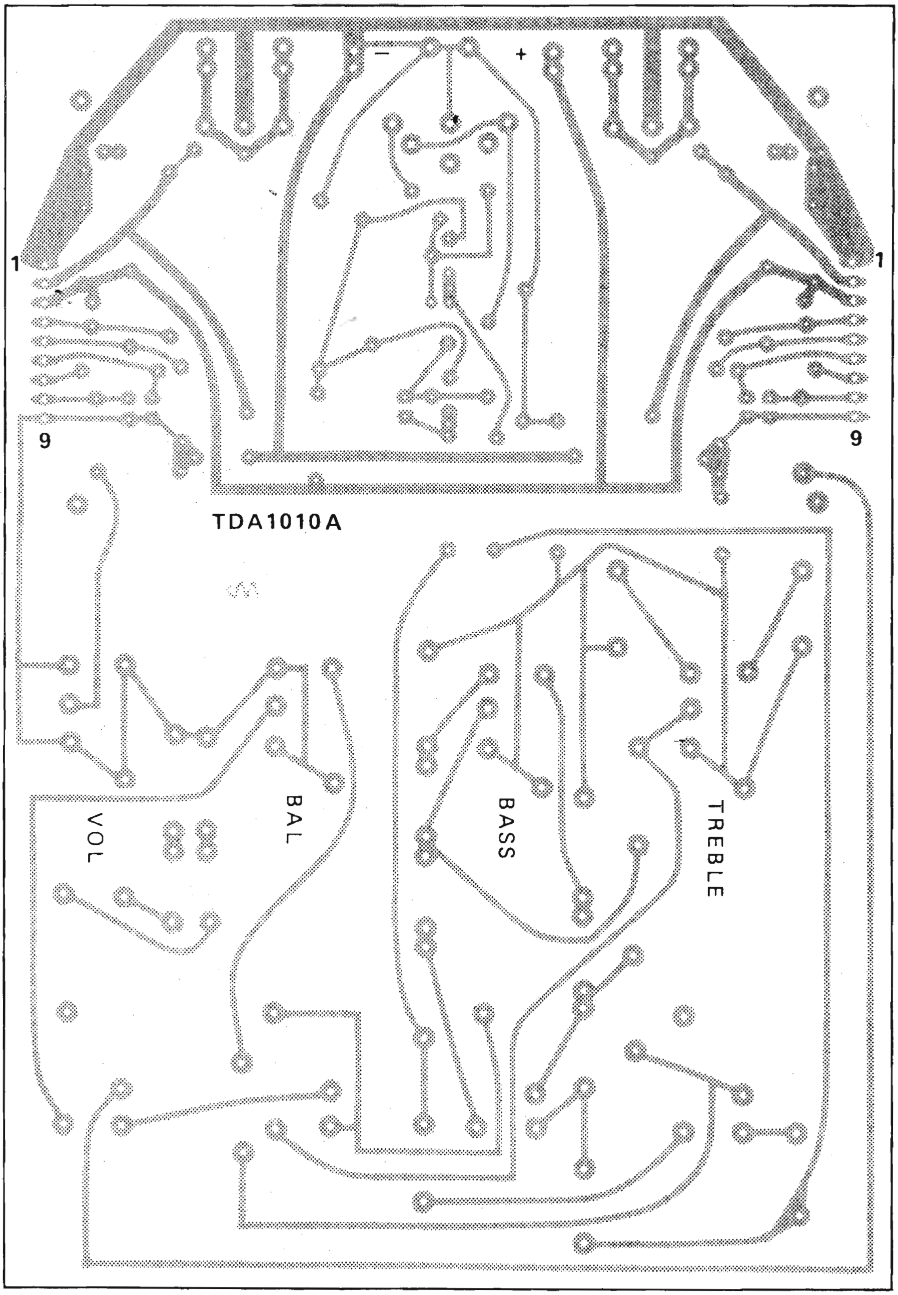


Fig. 18 Track side of printed-circuit board used for the circuit of Fig. 17 (Fig. 16 partly); p.c. board dimensions 169 mm x 118 mm.

7Z77935

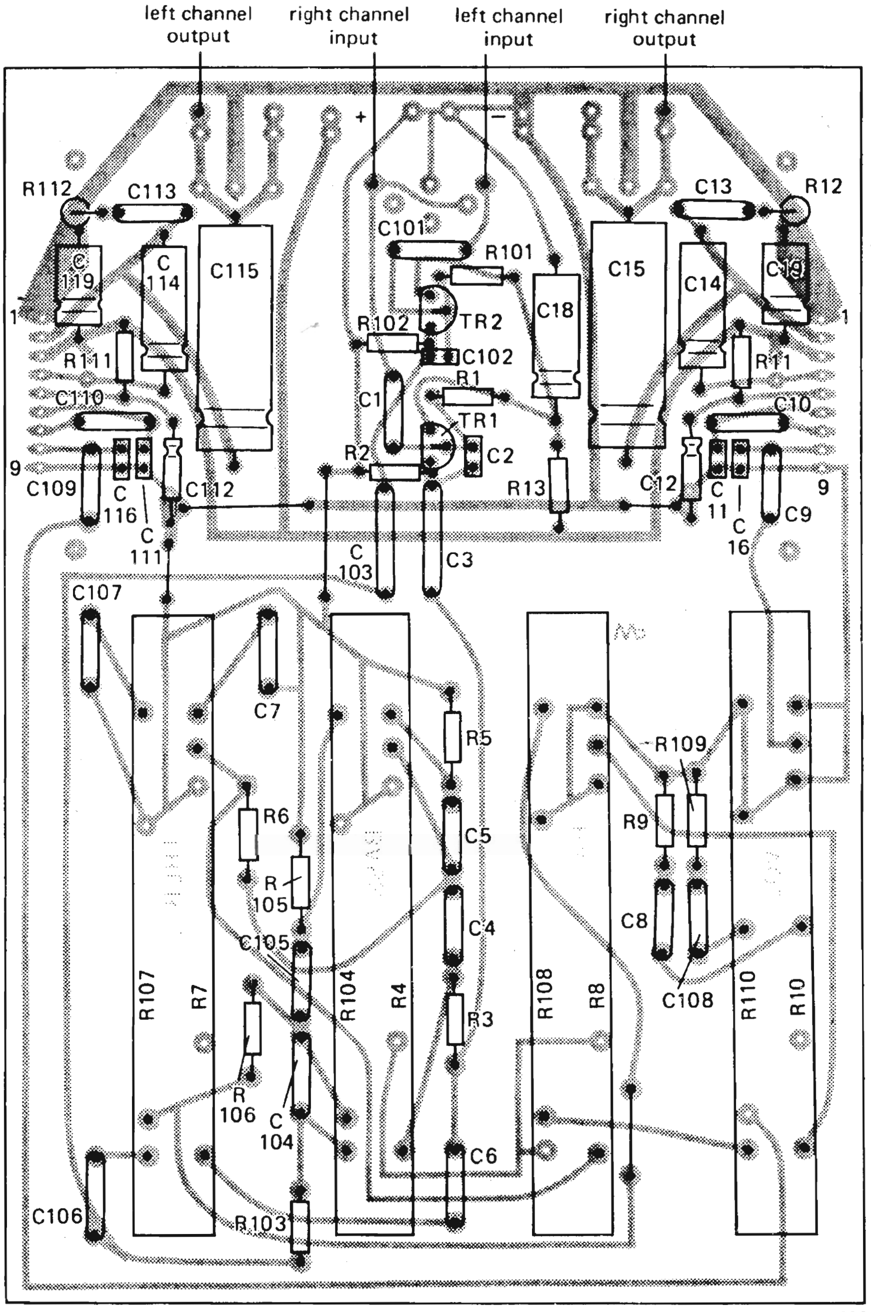


Fig. 19 Component side of printed-circuit board showing component layout used for the circuit of Fig. 17 (Fig. 16 partly).

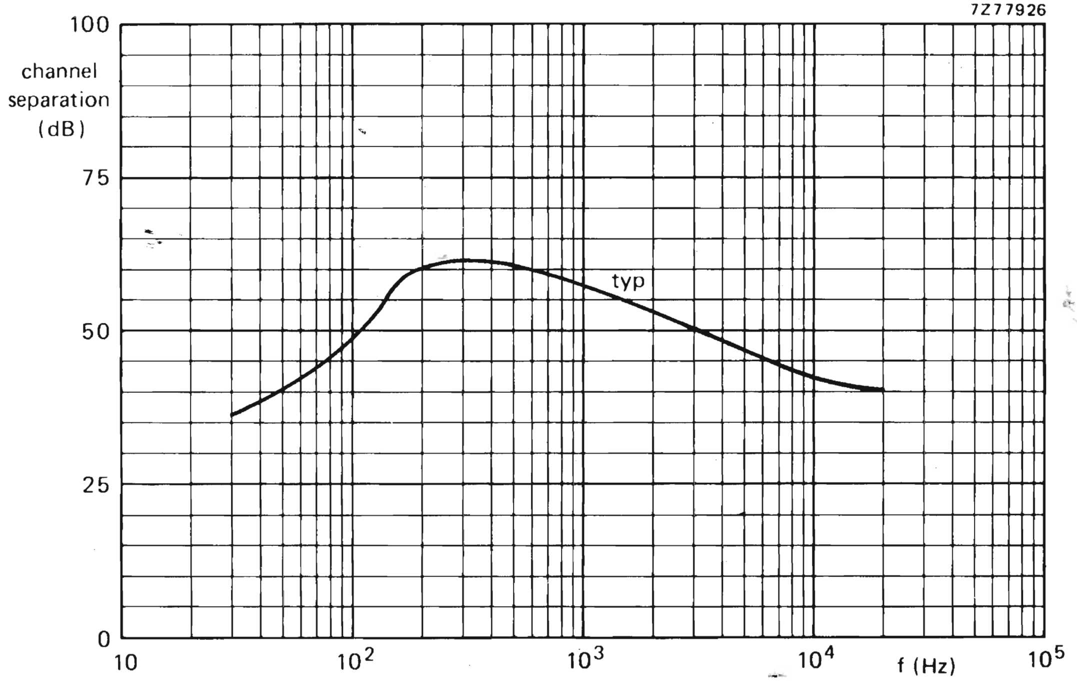


Fig. 20 Channel separation of the circuit of Fig. 17 as a function of frequency.

2 to 6W audio power amplifier with preamplifier TDA1011A

The TDA1011A is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The device can deliver up to 6 W into 4 Ω at 16 V loaded supply in mains-fed applications. The maximum permissible supply voltage of 24 V makes this circuit very suitable for d.c. and a.c. apparatus, while the low applicable supply voltage of 5,4 V permits 9 V applications. The power amplifier has an inverted input/output which makes the circuit optimal for applications with active tone control and spatial stereo. Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P		5,4 to 20	V
Peak output current	I_{OM}	max.	3	A
Output power at d_{tot} = 10%				
V_P = 16 V; R_L = 4 Ω	P_o	typ.	6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2	%
Input impedance				
preamplifier (pin 8)	$\lvert Z_i \rvert$	>	100	kΩ
Total quiescent current	I_{tot}	typ.	14	mA
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

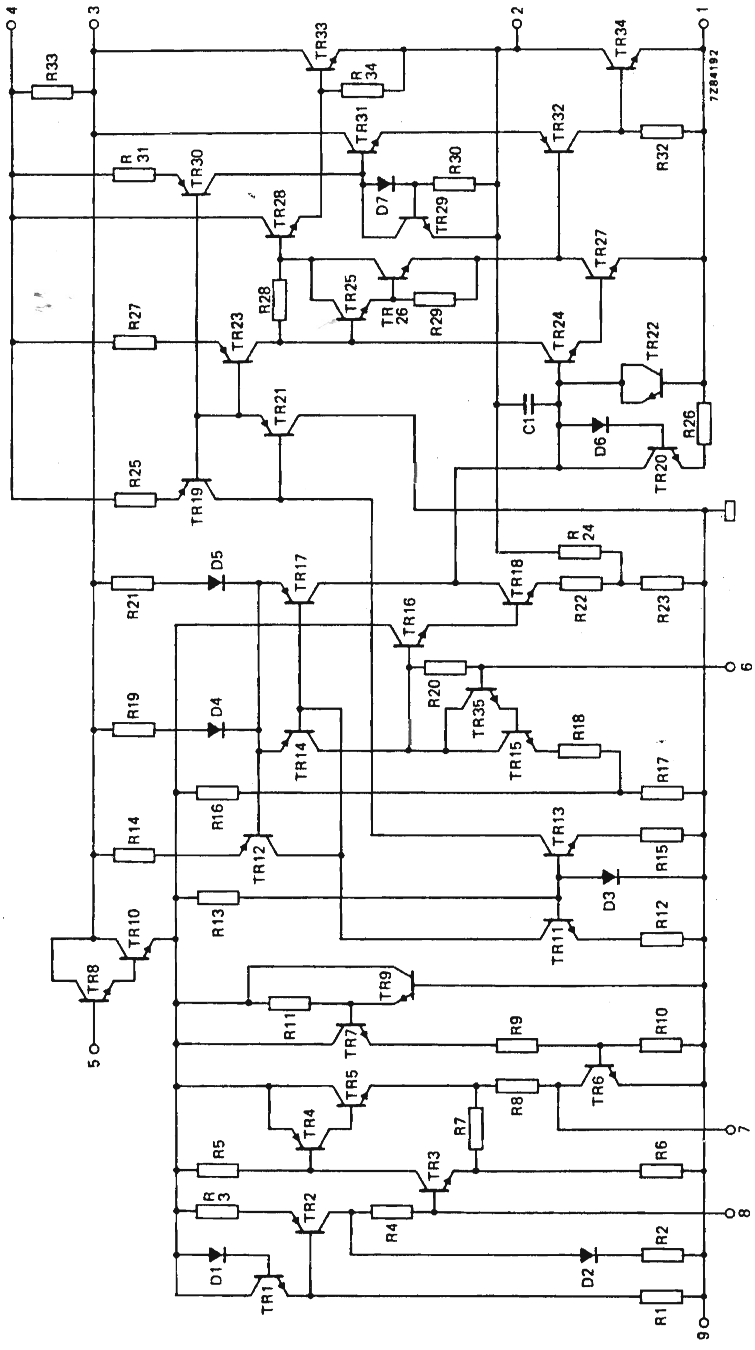


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24 V
Peak output current	I_{OM}	max.	3 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150 °C	
Operating ambient temperature	T_{amb}	−25 to + 150 °C	
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100 hours

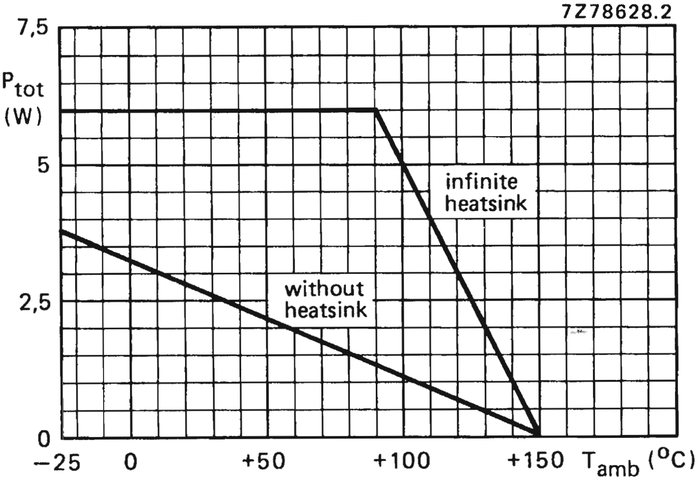


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume $V_P = 12$ V; $R_L = 4\ \Omega$; $T_{amb} = 60$ °C maximum; $P_o = 3{,}8$ W.

The maximum sine-wave dissipation is 1,8 W.

The derating of 10 K/W of the package requires the following external heatsink (for sine-wave drive):

$$R_{th\,j\text{-}a} = R_{th\,j\text{-}tab} + R_{th\,tab\text{-}h} + R_{th\,h\text{-}a} = \frac{150-60}{1{,}8} = 50\ \text{K/W}.$$

Since $R_{th\,j\text{-}tab} = 10$ K/W and $R_{th\,tab\text{-}h} = 1$ K/W, $R_{th\,h\text{-}a} = 50 - (10 + 1) = 39$ K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P		5,4 to 20	V
Repetitive peak output current	I_{ORM}	<	2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ.	14	mA
		<	22	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)				
with bootstrap:				
V_P = 16 V; R_L = 4 Ω	P_o	typ.	6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	>	3,6	W
		typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
without bootstrap:				
V_P = 12 V; R_L = 4 Ω	P_o	typ.	3,5	W
Voltage gain:				
preamplifier (note 2)	G_{v1}	typ.	23	dB
			21 to 25	dB
power amplifier (note 3)	G_{v2}	typ.	29	dB
total amplifier (note 3)	$G_{v\,tot}$	typ.	52	dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ.	0,3	%
		<	1	%
Frequency response; −3 dB (note 4)	B		60 Hz to 15	kHz
Input impedance:				
preamplifier (note 5)	$\lvert Z_{i1} \rvert$	>	100	kΩ
		typ.	200	kΩ
Output impedance preamplifier	$\lvert Z_{o1} \rvert$	typ.	1	kΩ
Output voltage preamplifier (r.m.s. value)				
d_{tot} < 1% (note 2)	$V_{o(rms)}$	>	1,2	V
Noise output voltage (r.m.s. value; note 6)				
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,5	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0,8	mV
Noise output voltage at f = 500 kHz (r.m.s. value)				
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ.	8	μV
Ripple rejection (note 6)				
f = 1 to 10 kHz	RR	typ.	42	dB
f = 100 Hz; C2 = 1 μF	RR	>	35	dB
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ.	35	mA
Stand-by current at maximum V_P (note 8)	I_{sb}	<	100	μA

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured with R2 = 20 kΩ.
4. Measured at P_o = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
5. Independent of load impedance of preamplifier.
6. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
7. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude: 2 V).
8. The total current when disconnecting pin 5 or short-circuited to ground (pin 9).
9. The tab must be electrically floating or connected to the substrate (pin 9).

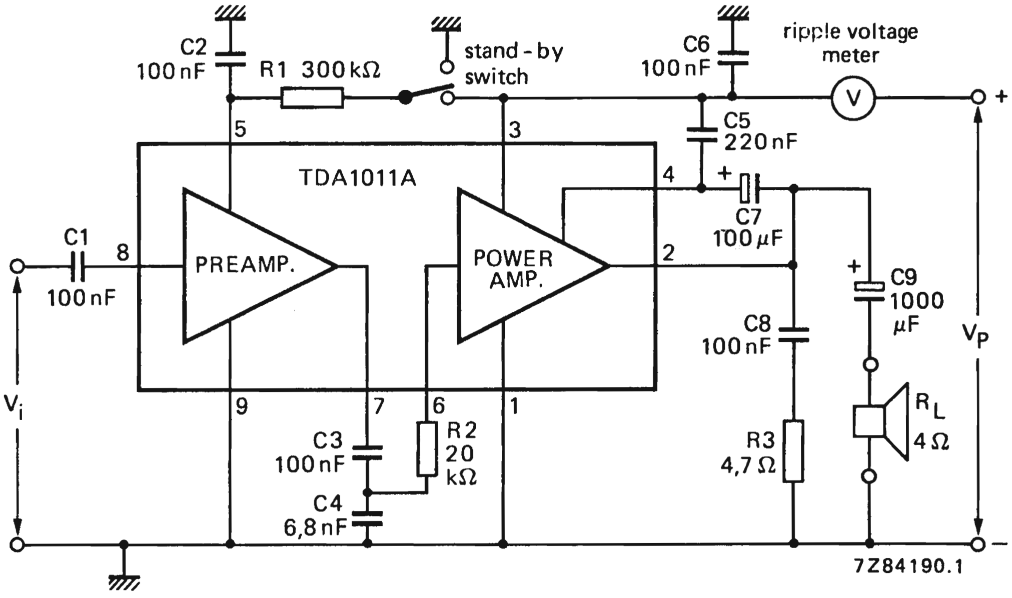


Fig. 3 Test circuit.

APPLICATION INFORMATION

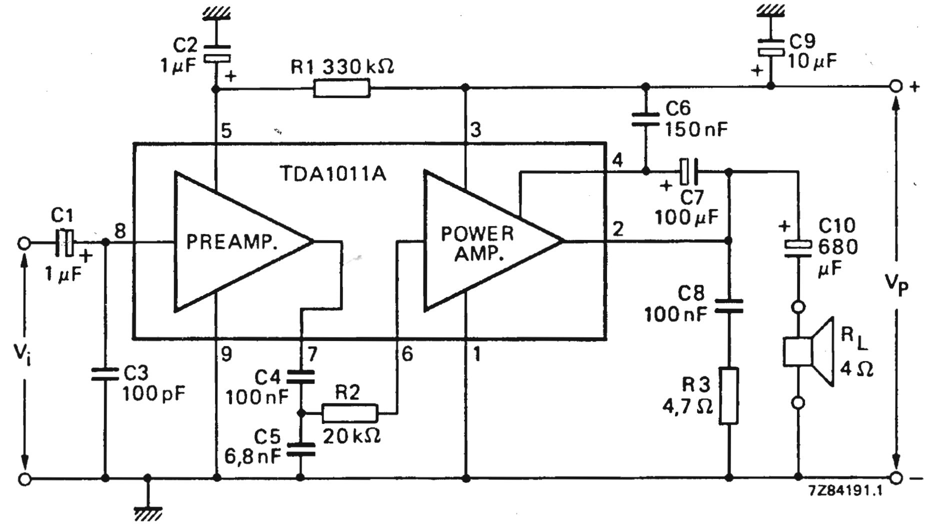


Fig. 4 Circuit diagram of a 4 W amplifier.

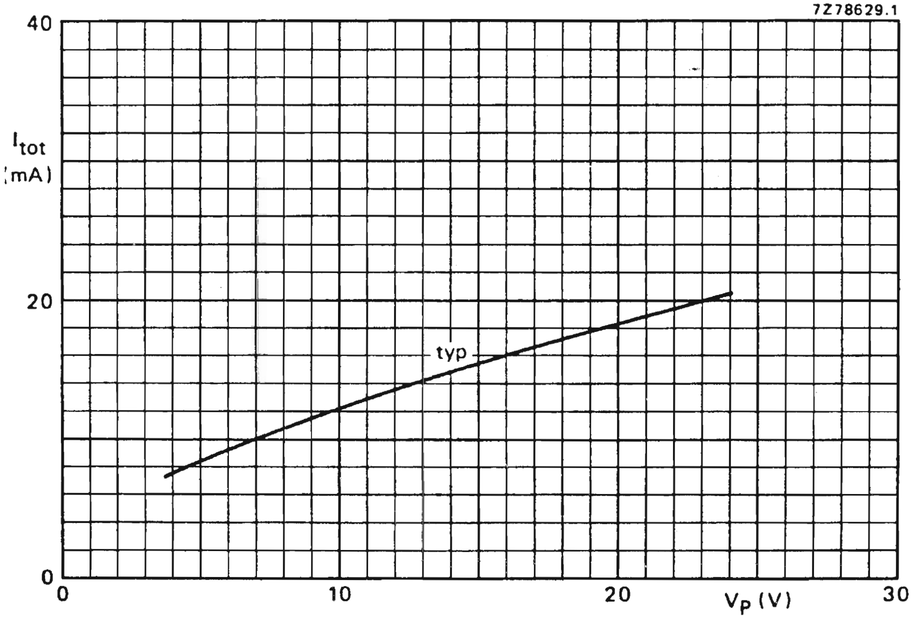


Fig. 5 Total quiescent current as a function of supply voltage.

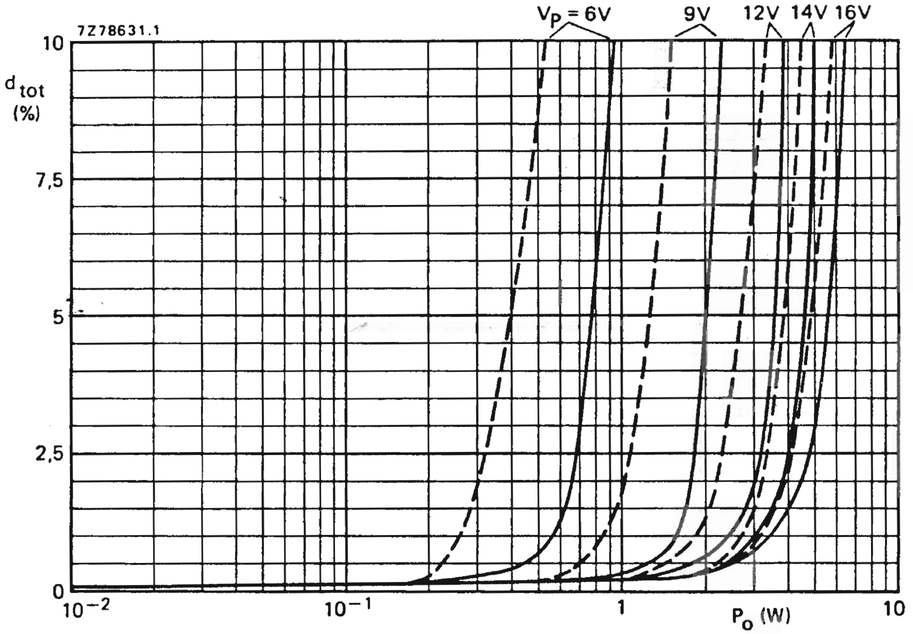


Fig. 6 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; – – – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

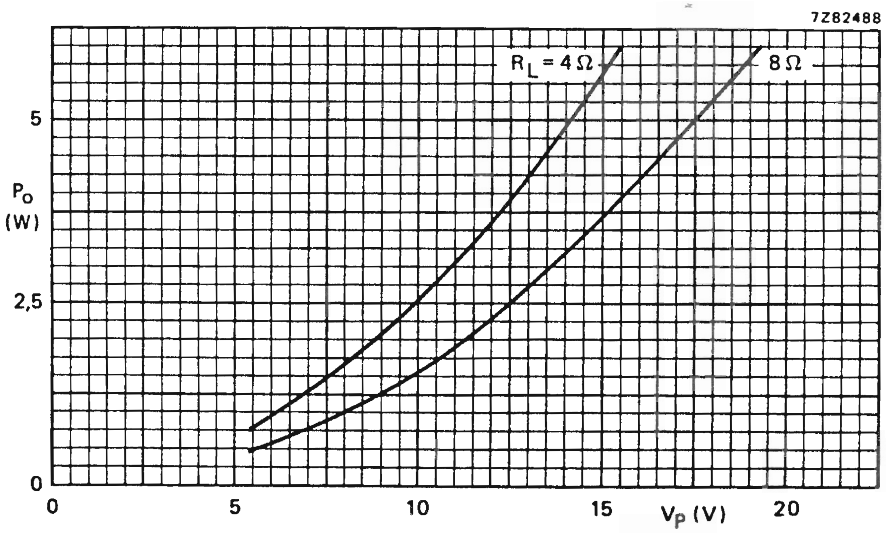


Fig. 7 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C1

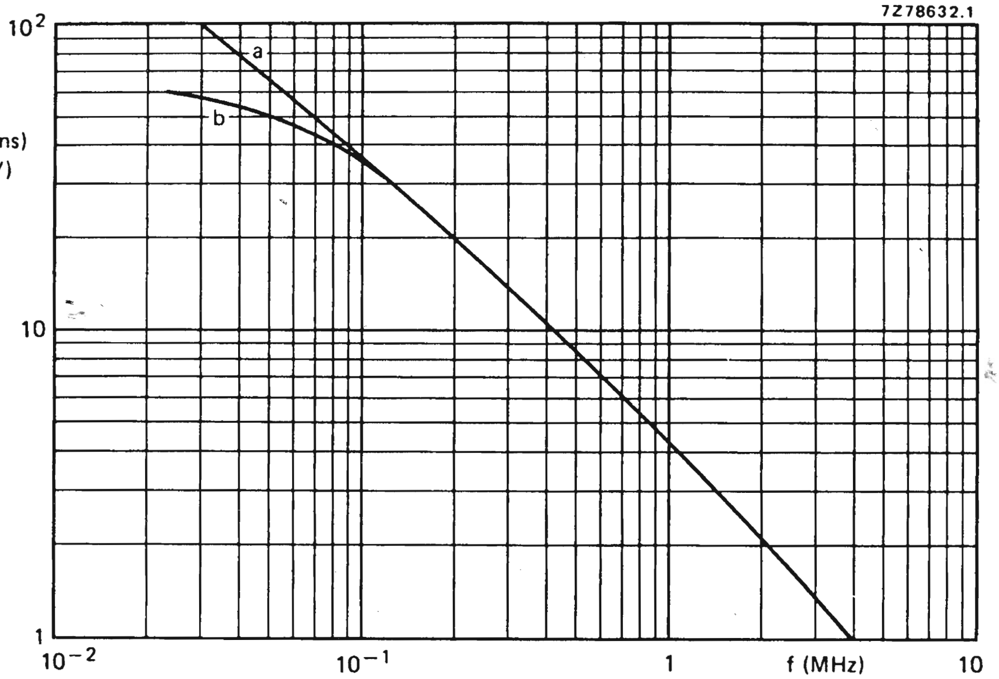


Fig. 8 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

4W amplifier with DC volume control

TDA1013B

GENERAL DESCRIPTION

The TDA1013B is an integrated audio amplifier circuit with DC volume control, encapsulated in a 9-lead single in-line (SIL) plastic package. The wide supply voltage range makes this circuit ideal for applications in mains and battery-fed apparatus such as television receivers and record players.

The DC volume control stage has a logarithmic control characteristic with a range of more than 80 dB; control is by means of a DC voltage variable between 2 and 6.5 V.

The audio amplifier has a well defined open loop gain and a fixed integrated closed loop. This device requires only a few external components and offers stability and performance.

Features

- Few external components
- Wide supply voltage range
- Wide control range
- Pin compatible with TDA1013A
- Fixed gain
- High signal-to-noise ratio
- Thermal protection

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10	18	40	V
Repetitive peak output current		I_{ORM}	–	–	1.5	A
Total sensitivity	P_o = 2.5 W; DC control at max. gain	V_i	44	55	69	mV
Audio amplifier						
Output power	THD = 10%; R_L = 8 Ω	P_o	4.0	4.2	–	W
Total harmonic distortion	P_o = 2.5 W; R_L = 8 Ω	THD	–	0.15	0.1	%
Sensitivity	P_o = 2.5 W	V_i	100	125	160	mV
DC volume control unit						
Gain control range		$\lvert\Delta G_v\rvert$	80	–	–	dB
Signal handling	THD < 1%; DC control = 0 dB	V_i	1.2	1.7	–	V
Sensitivity (pin 6)	V_o = 125 mV; max. voltage gain	V_i	39	45	55	mV
Input impedance (pin 8)		$\lvert Z_i\rvert$	23	29	35	kΩ

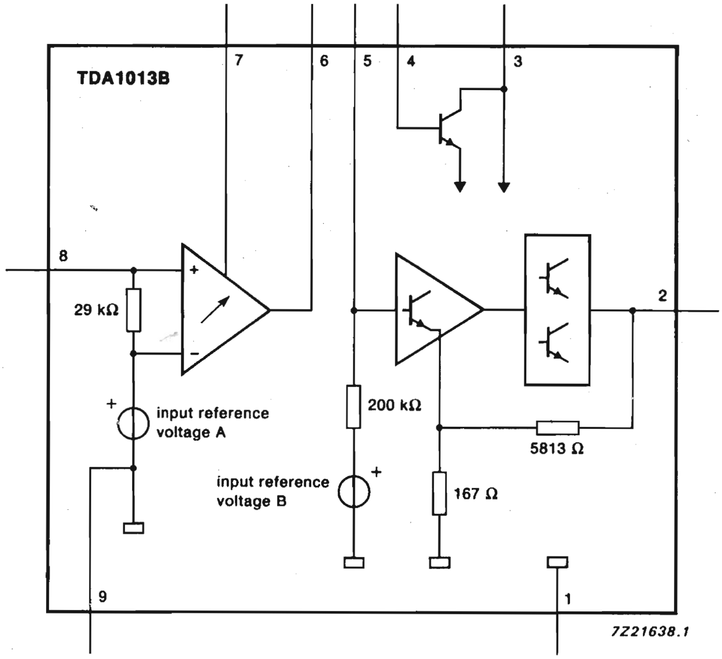


Fig.1 Block diagram.

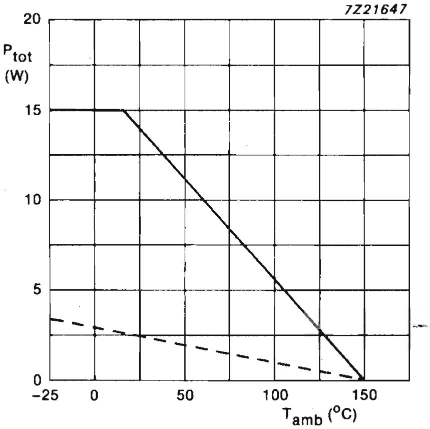
PINNING

1	signal ground
2	amplifier output
3	supply voltage
4	electronic filter
5	amplifier input
6	control unit output
7	control voltage
8	control unit input
9	power ground

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	40	V
Non-repetitive peak output current	I_{OSM}	–	3	A
Repetitive peak output current	I_{ORM}	–	1.5	A
Storage temperature range	T_{stg}	–65	+ 150	°C
Crystal temperature	T_c	–	+ 150	°C
Total power dissipation	P_{tot}	see Fig. 2		



———— infinite heatsink
– – – – – without heatsink

Fig.2 Power derating curve.

HEATSINK DESIGN EXAMPLE

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C; T_c = 150 °C (max.); for a 4 W application, the maximum dissipation is approximately 2.5 W. The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} =$$

$$\frac{T_{j\ max} - T_{amb\ max}}{P_{max}} = \frac{150 - 60}{2.5} = 36\ \text{K/W}$$

Since $R_{th\ j\text{-}tab}$ = 9 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 36 – (9 + 1) = 26 K/W.

CHARACTERISTICS

V_P = 18 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; see Fig. 10; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	10	18	40	V
Total quiescent current		I_{tot}	–	25	60	mA
Noise output voltage	note 1					
at maximum gain	$R_S = 0\ \Omega$	V_n	–	0.5	–	mV
at maximum gain	$R_S = 5\ k\Omega$	V_n	–	0.6	1.4	mV
at minimum gain	$R_S = 0\ \Omega$	V_n	–	0.25	–	mV
Total sensitivity	P_o = 2.5 W; DC control at max. gain	V_i	44	55	69	mV
Audio amplifier						
Repetitive peak output current		I_{ORM}	–	–	1.5	A
Output power	THD = 10%; R_L = 8 Ω	P_o	4.0	4.2	–	W
Total harmonic distortion	P_o = 2.5 W; R_L = 8 Ω	THD	–	0.15	1.0	%
Sensitivity	P_o = 2.5 W	V_i	100	125	160	mV
Input impedance (pin 5)		$\|Z_i\|$	100	200	500	kΩ
Power bandwidth		B_P	–	30 to 40 000	–	Hz
DC volume control unit						
Gain control range		$\|\Delta G_v\|$	80	90	–	dB
Signal handling	THD < 1%; DC control = 0 dB	V_i	1.2	1.7	–	V
Sensitivity (pin 6)	V_o = 125 mV; max. voltage gain	V_i	39	44	55	mV
Input impedance (pin 8)		$\|Z_i\|$	23	29	35	kΩ
Output impedance (pin 6)		$\|Z_o\|$	45	60	75	Ω

Note to the characteristics

1. Measured in a bandwidth in accordance with IEC 179, curve ‘A’.

APPLICATION INFORMATION

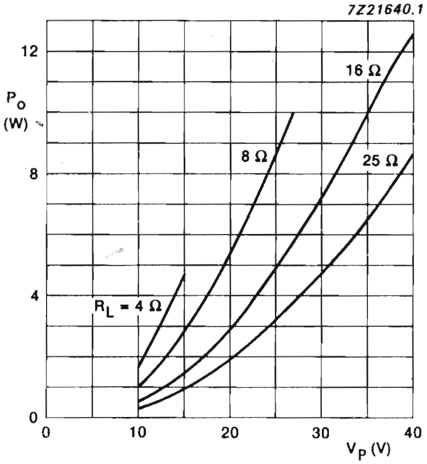


Fig.3 Output power as a function of supply voltage; f = 1 kHz; THD = 10% and control voltage (V_7) = 6.5 V.

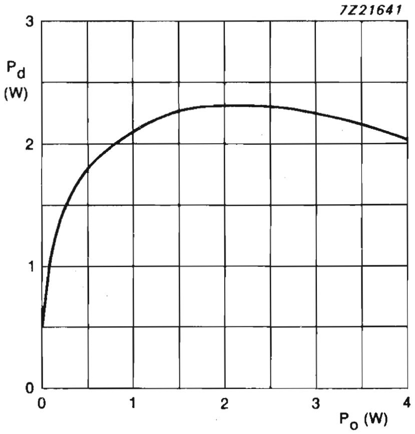


Fig.4 Power dissipation as a function of output power; V_P = 18 V; f = 1 kHz; R_L = 8 Ω and control voltage (V_7) = 6.5 V.

APPLICATION INFORMATION (continued)

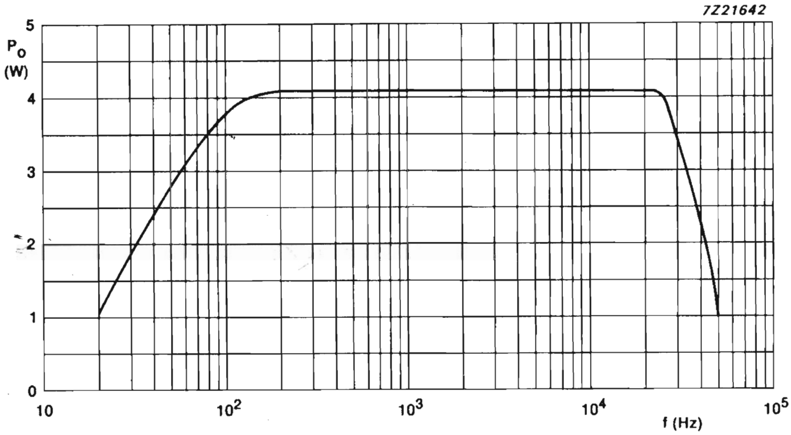


Fig.5 Power bandwidth; $V_P = 18$ V; $R_L = 8\ \Omega$; THD = 10% and control voltage (V_7) = 6.5 V.

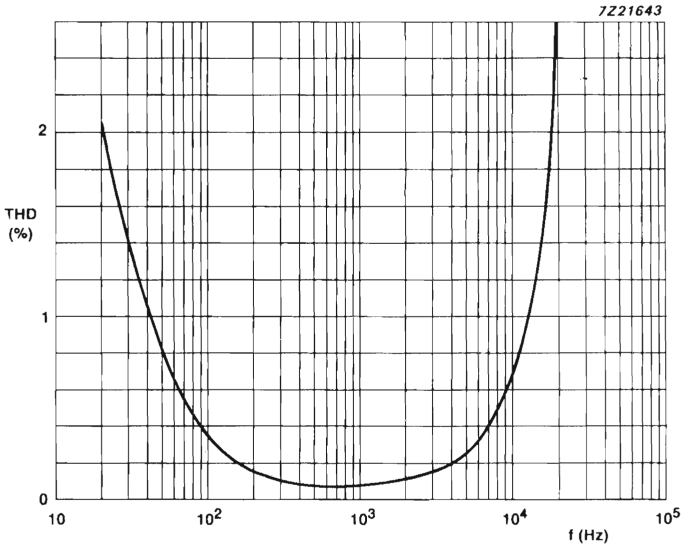
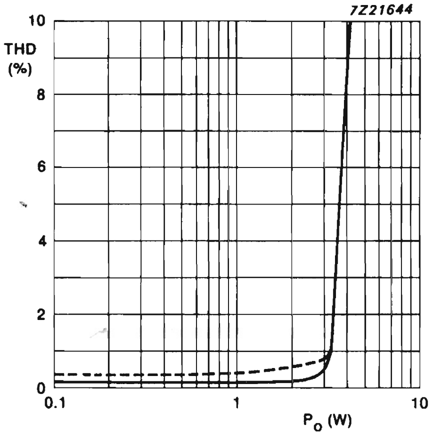


Fig.6 Total harmonic distortion as a function of frequency; $V_P = 18$ V; $R_L = 8\ \Omega$; $P_o = 2.5$ W and control voltage = 6.5 V.



------- 10 kHz
——— 1 kHz

Fig.7 Total harmonic distortion as a function of output power; V_P = 18 V; R_L = 8 Ω and control voltage = 6.5 V.

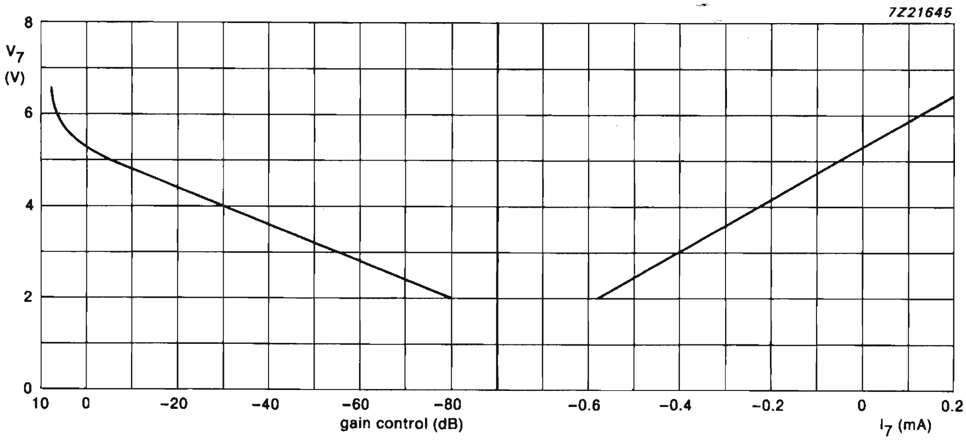


Fig.8 Typical control curve.

APPLICATION INFORMATION (continued)

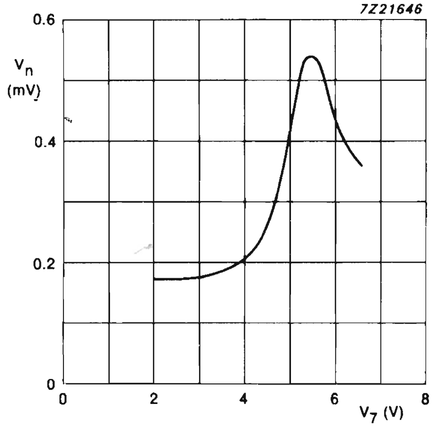
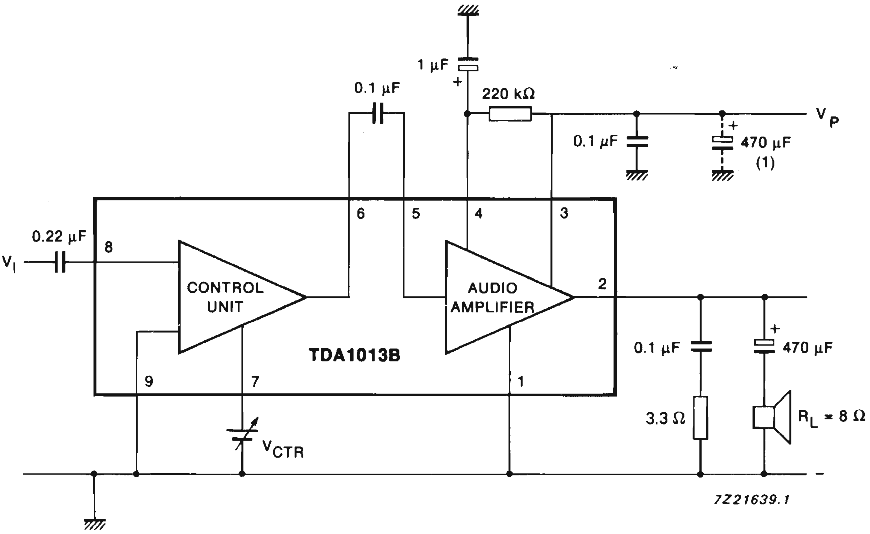


Fig.9 Noise output voltage as a function of the control voltage; V_P = 18 V; R_L = 8 Ω (in accordance with IEC 179, curve 'A').



(1) Belongs to power supply circuitry.

Fig.10 Application diagram.

1 to 4W audio amplifier with preamplifier

TDA1015

The TDA1015 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The very low applicable supply voltage of 3,6 V permits 6 V applications. Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 18	V
Peak output current	I_{OM}	max.	2,5	A
Output power at d_{tot} = 10%				
V_P = 12 V; R_L = 4 Ω	P_o	typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,3	%
Input impedance				
preamplifier (pin 8)	$\lvert Z_i \rvert$	>	100	kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ.	20	kΩ
Total quiescent current	I_{tot}	typ.	14	mA
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

1 to 4W audio amplifier with preamplifier TDA1015

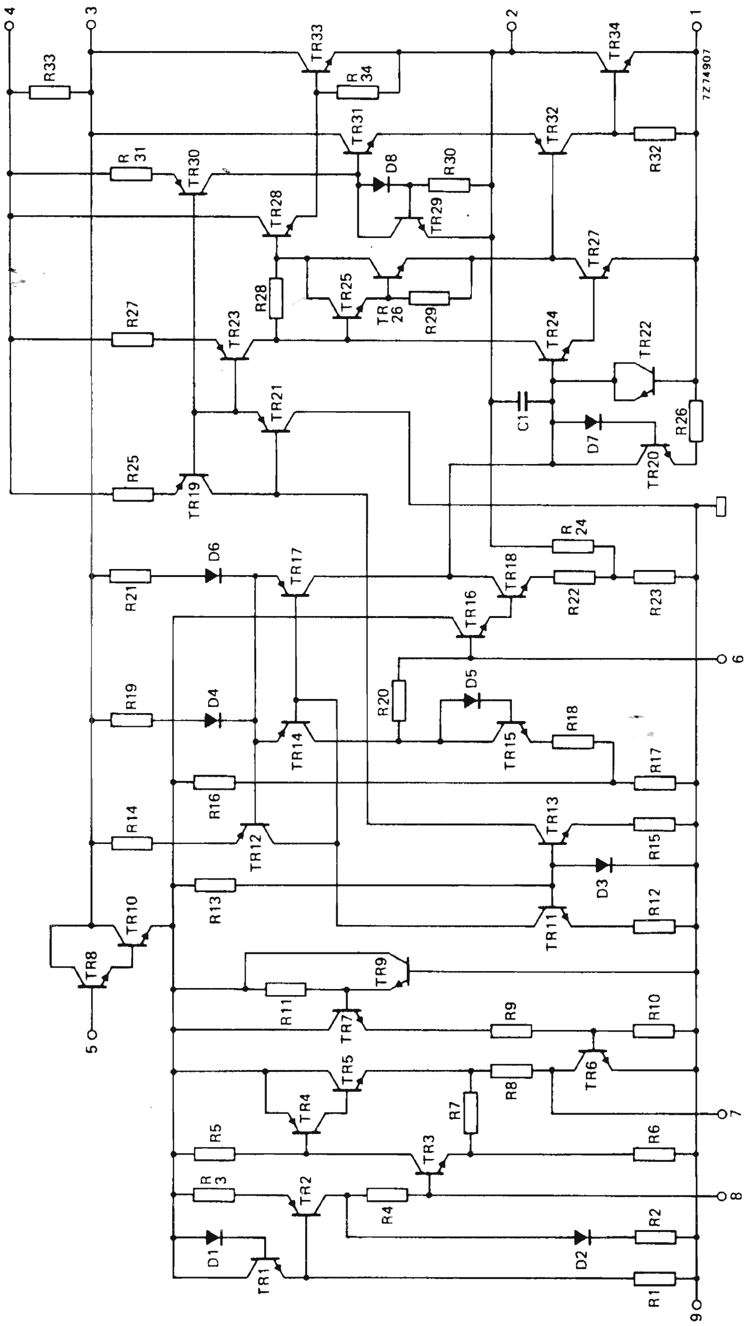


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Peak output current	I_{OM}	max.	2,5	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}	−55 to + 150		°C
Operating ambient temperature	T_{amb}	−25 to + 150		°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100	hours

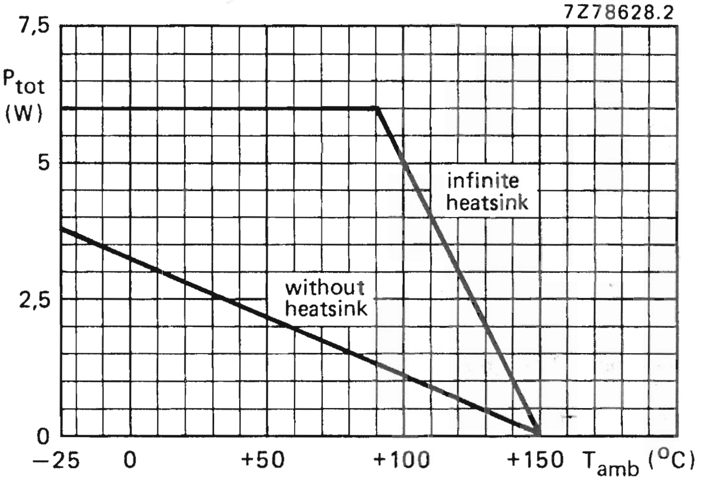


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 12 V; R_L = 4 Ω; T_{amb} = 45 °C maximum.

The maximum sine-wave dissipation is 1,8 W.

$$R_{th\,j\text{-}a} = R_{th\,j\text{-}tab} + R_{th\,tab\text{-}h} + R_{th\,h\text{-}a} = \frac{150-45}{1,8} = 58\ \text{K/W}.$$

Where $R_{th\,j\text{-}a}$ of the package is 45 K/W, so no external heatsink is required.

D.C. CHARACTERISTICS

Supply voltage range	V_P		3,6 to 18	V
Repetitive peak output current	I_{ORM}	<	2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ.	14	mA
		<	25	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)				
with bootstrap:				
V_P = 12 V; R_L = 4 Ω	P_o	typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
without bootstrap:				
V_P = 12 V; R_L = 4 Ω	P_o	typ.	3,0	W
Voltage gain:				
preamplifier (note 2)	G_{v1}	typ.	23	dB
power amplifier	G_{v2}	typ.	29	dB
total amplifier	$G_{v\,tot}$	typ.	52	dB
			49 to 55	dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ.	0,3	%
		<	1,0	%
Frequency response; –3 dB (note 3)	B		60 Hz to 15	kHz
Input impedance:				
preamplifier (note 4)	$\|Z_{i1}\|$	>	100	kΩ
		typ.	200	kΩ
power amplifier	$\|Z_{i2}\|$	typ.	20	kΩ
Output impedance preamplifier	$\|Z_{o1}\|$	typ.	1	kΩ
Output voltage preamplifier (r.m.s. value)				
d_{tot} < 1% (note 2)	$V_{o(rms)}$	typ.	0,8	V
Noise output voltage (r.m.s. value; note 5)				
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,2	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0,5	mV
Noise output voltage at f = 500 kHz (r.m.s. value)				
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ.	8	μV
Ripple rejection (note 6)				
f = 100 Hz	RR	typ.	38	dB

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at P_O = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

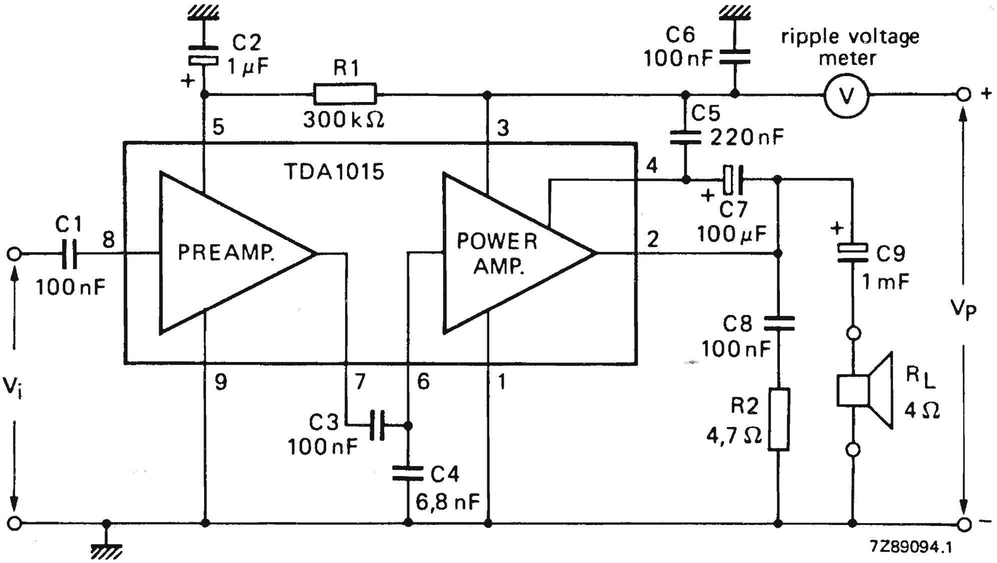


Fig. 3 Test circuit.

APPLICATION INFORMATION

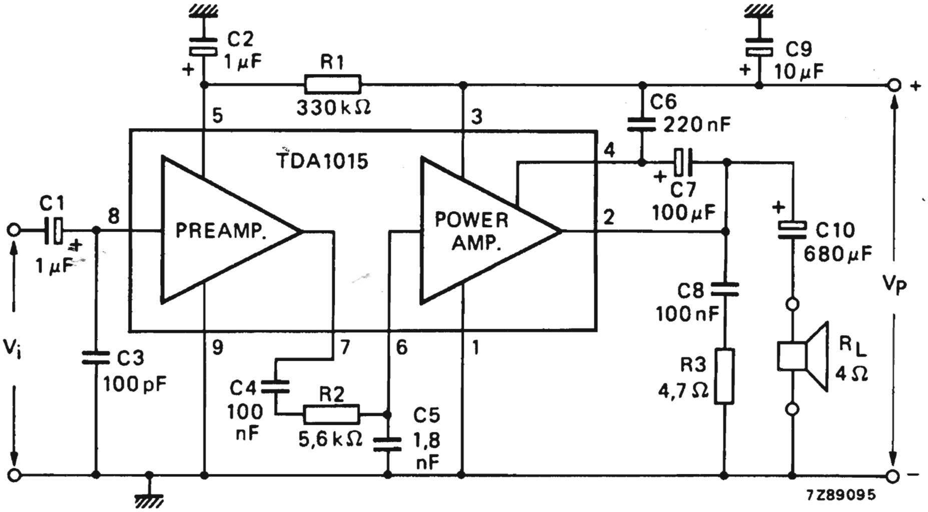


Fig. 4 Circuit diagram of a 1 to 4 W amplifier.

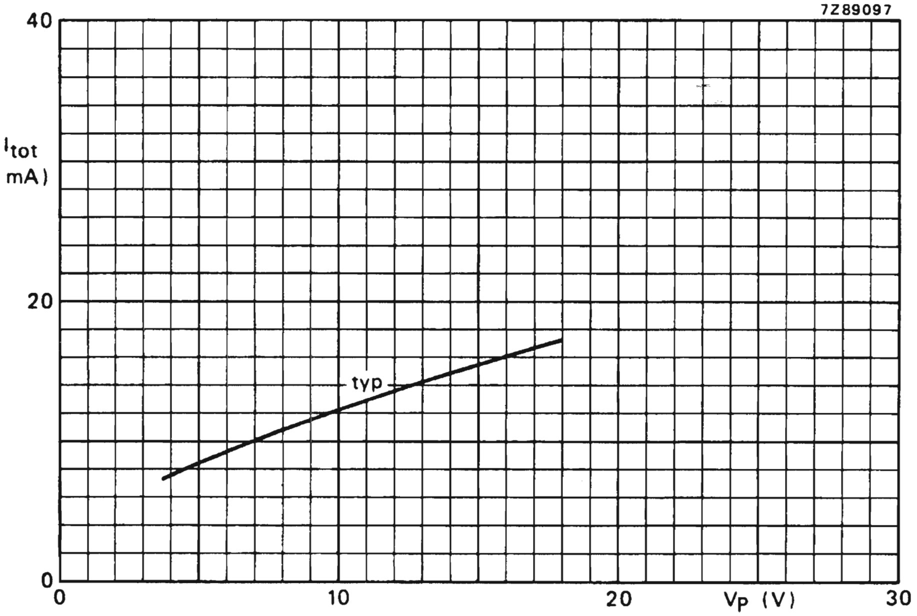


Fig. 5 Total quiescent current as a function of supply voltage.

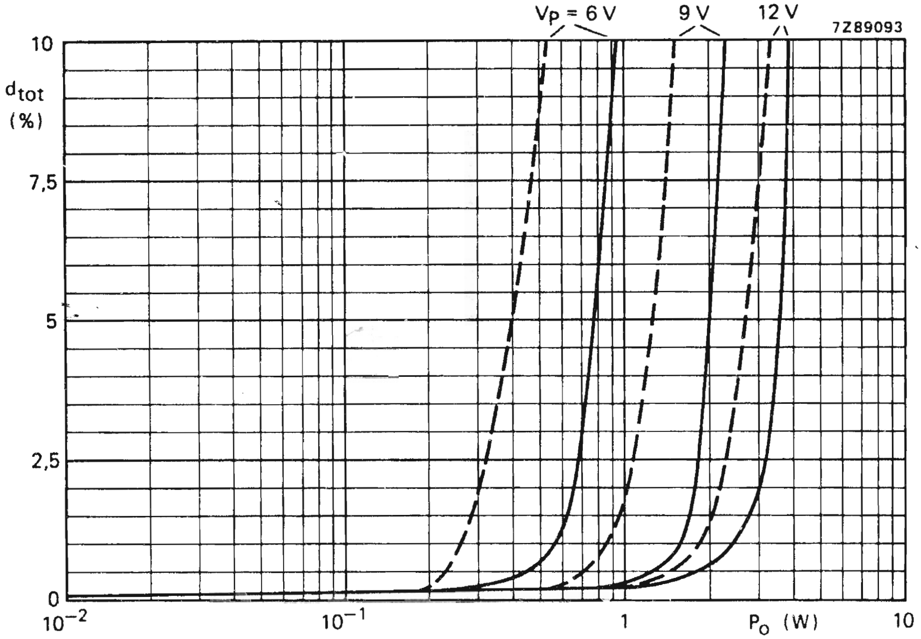


Fig. 6 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; – – – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

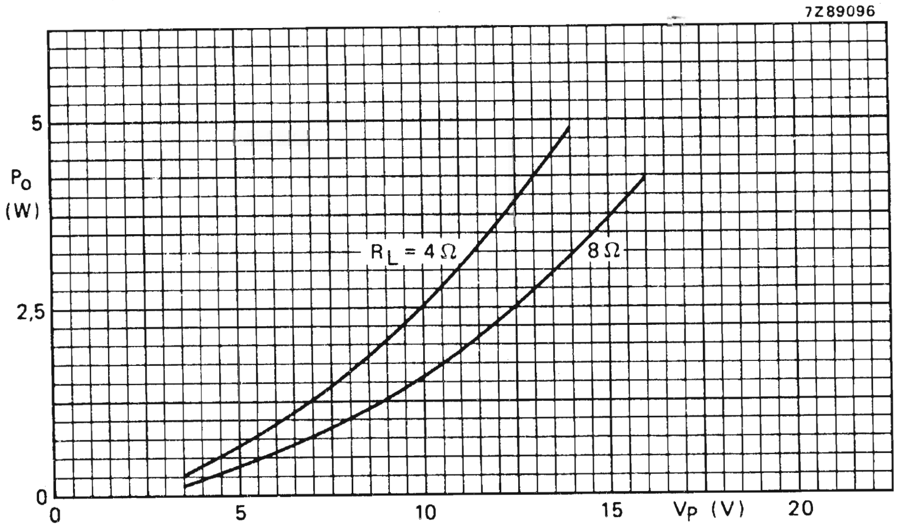


Fig. 7 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

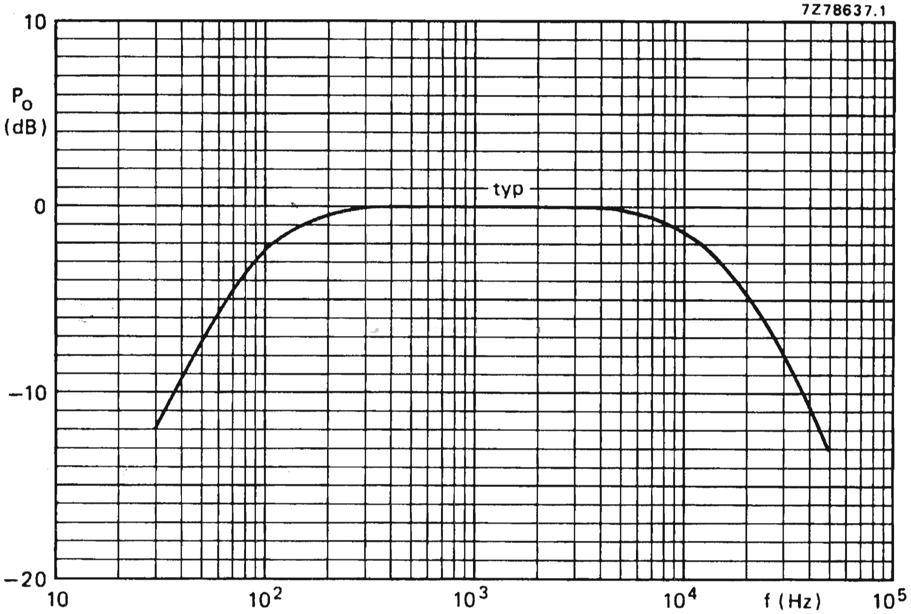


Fig. 8 Voltage gain as a function of frequency; P_o relative to 0 dB = 1 W; V_P = 12 V; R_L = 4 Ω.

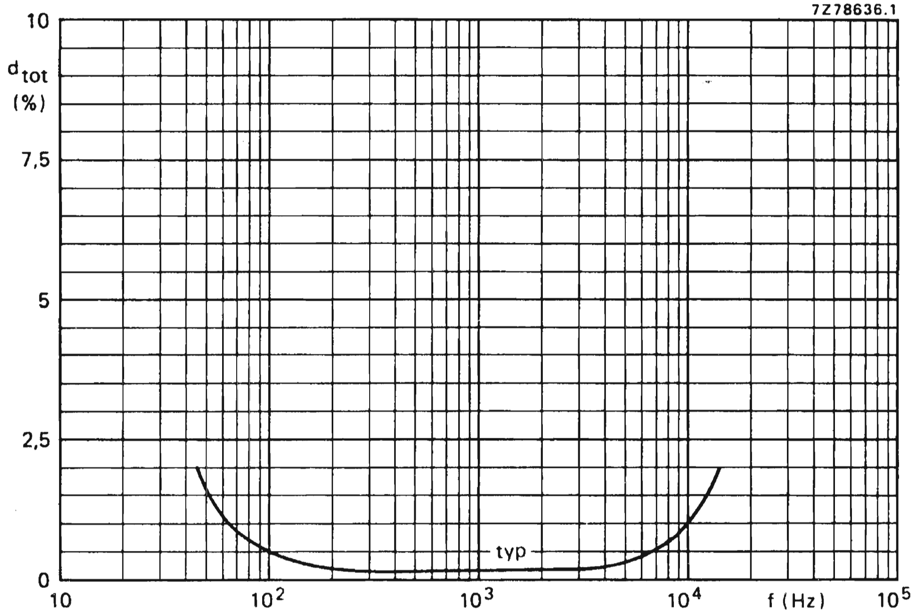


Fig. 9 Total harmonic distortion as a function of frequency; P_o = 1 W; V_P = 12 V; R_L = 4 Ω.

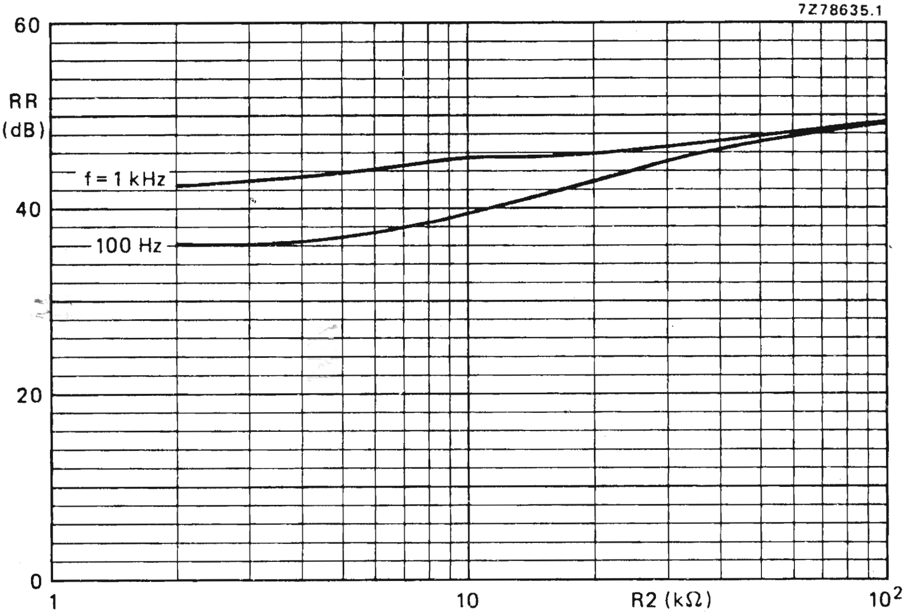


Fig. 10 Ripple rejection as a function of R2 (see Fig. 4); $R_S = 0$; typical values.

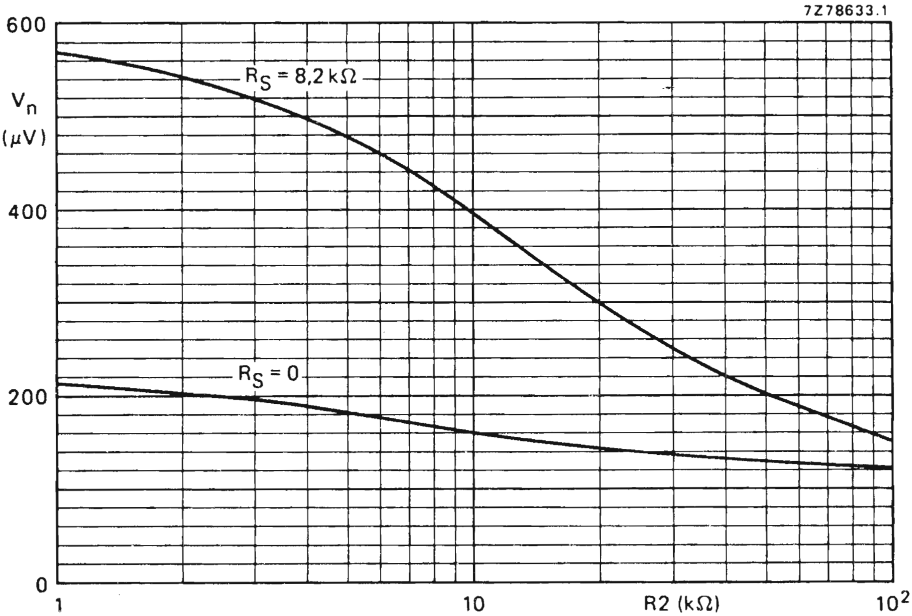


Fig. 11 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

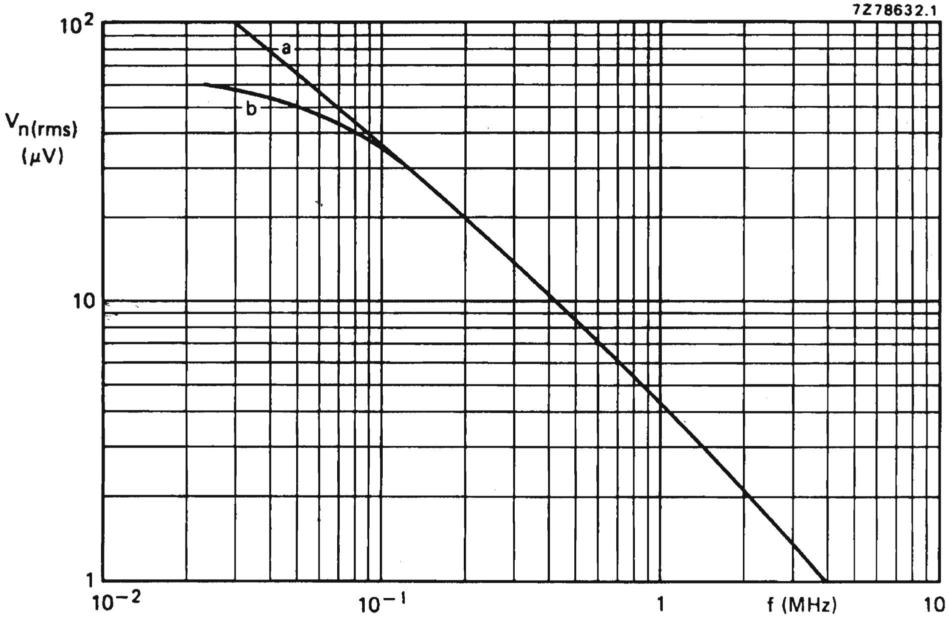


Fig. 12 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

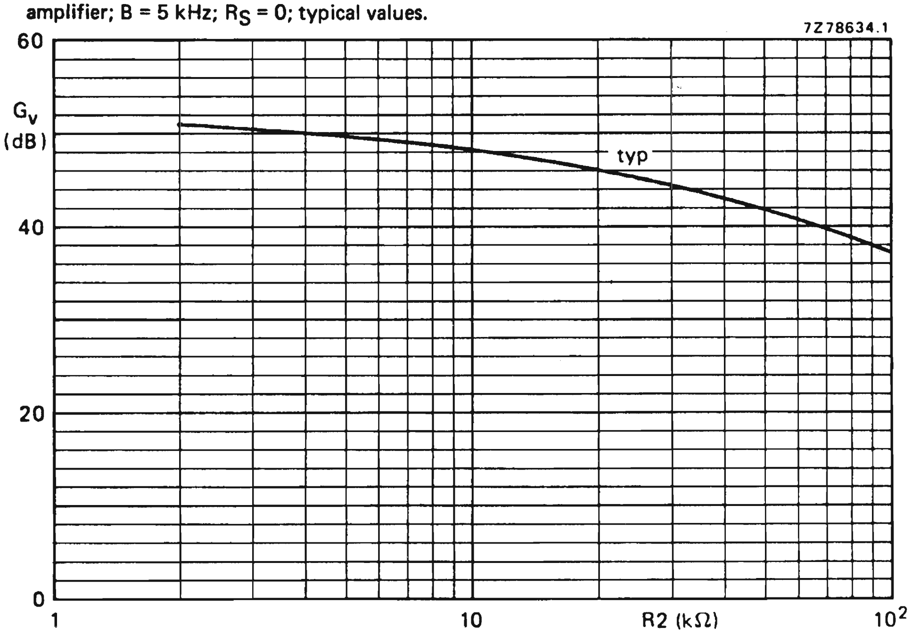


Fig. 13 Voltage gain as a function of R2 (see Fig. 4).

1 Watt low voltage audio power amplifier TDA7052

GENERAL DESCRIPTION

The TDA7052 is a mono output amplifier in a 8-lead dual-in-line (DIL) plastic package. The device is designed for battery-fed portable audio applications.

Features:

- No external components
- No switch-on or switch-off clicks
- Good overall stability
- Low power consumption
- No external heatsink required
- Short-circuit proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	39	40	41	dB
Output power	THD = 10%; 8 Ω	P_o	–	1,2	–	W
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%

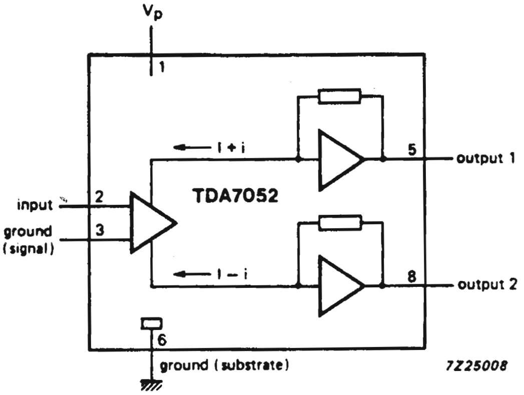


Fig. 1 Block diagram.

PINNING

1	V_P	supply voltage	5	OUT1	output 1
2	IN	input	6	GND2	ground (substrate)
3	GND1	ground (signal)	7	n.c.	not connected
4	n.c.	not connected	8	OUT2	output 2

FUNCTIONAL DESCRIPTION

The TDA7052 is a mono output amplifier designed for battery-fed portable audio applications, such as tape recorders and radios.
The gain is fixed internally at 40 dB. A large number of tape recorders and radios are still designed for mono sound, plus a space-saving trend by reduction of the number of battery cells. This means a decrease in supply voltage which results in an reduction of output power. To compensate for this reduction, the TDA7052 uses the Bridge-Tied-Load principle (BTL) which can deliver an output power of 1,2 W (THD = 10%) into an 8 Ω load with a power supply of 6 V. The load can be short-circuited at each signal excursion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	18	V
Non-repetitive peak output current	I_{OSM}	–	1,5	A
Total power dissipation	P_{tot}	see Fig. 2		
Crystal temperature	T_c	–	150	°C
Storage temperature range	T_{stg}	–65	+ 150	°C

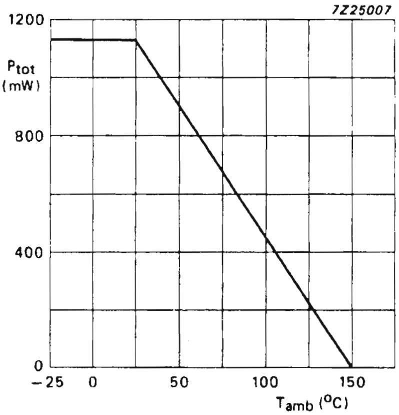


Fig. 2 Power derating curve.

POWER DISSIPATION

Assume V_P = 6 V; R_L = 8 Ω; T_{amb} = 50 °C maximum.

The maximum sinewave dissipation is 0,9 W.

$$R_{th\,j\text{-}a} = \frac{150 - 50}{0,9} \approx 110 \text{ K/W}.$$

Where $R_{th\,j\text{-}a}$ of the package is 110 K/W, so no external heatsink is required.

CHARACTERISTICS

V_P = 6 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	39	40	41	dB
Output power	THD = 10%	P_o	•	1,2	–	W
Noise output voltage (RMS value)						
	note 1	$V_{no(rms)}$	–	150	300	µV
	note 2	$V_{no(rms)}$	–	60	–	µV
Frequency response		f_r	–	20 Hz to 20 kHz	–	Hz
Supply voltage ripple rejection	note 3	SVRR	40	50	–	dB
DC output offset voltage pin 5 to 8	R_S = 5 kΩ	$\Delta V_{5\text{-}8}$	–	–	100	mV
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%
Input impedance		$\|Z_I\|$	–	100	–	kΩ
Input bias current		I_{bias}	–	100	300	nA

Notes to the characteristics

1. The unweighted RMS noise output voltage is measured at a bandwidth of 60 Hz to 15 kHz with a source impedance (R_S) of 5 kΩ.
2. The RMS noise output voltage is measured at a bandwidth of 5 kHz with a source impedance of 0 Ω and a frequency of 500 kHz. With a practical load (R = 8 Ω; L = 200 µH) the noise output current is only 100 nA.
3. Ripple rejection is measured at the output with a source impedance of 0 Ω and a frequency between 100 Hz and 10 kHz. The ripple voltage = 200 mV (RMS value) is applied to the positive supply rail.

APPLICATION INFORMATION

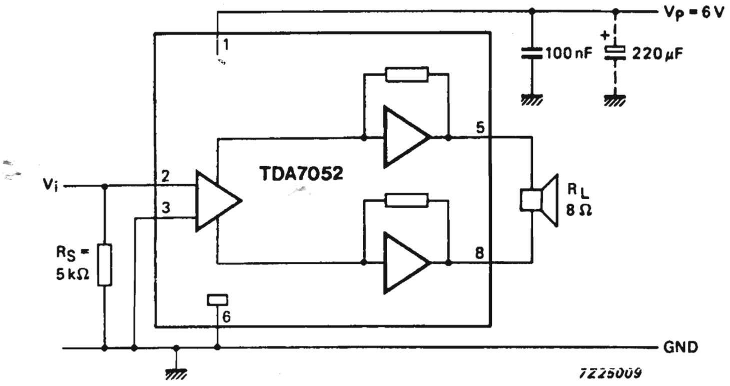


Fig. 3 Application diagram.

1-Watt low voltage audio power amp with DC volume control

TDA7052A/AT

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch on and off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins

GENERAL DESCRIPTION

The TDA7052A/AT are mono BTL output amplifiers with DC volume control. They are designed for use in TV and monitors, but also suitable for battery-fed portable recorders and radios.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7052A	8	DIL	plastic	SOT97
TDA7052AT	8	mini-pack	plastic	SOT96A

QUICK REFERENCE DATA

SYMBOL	PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range		4.5	–	18	V
P_O	output power in 8 Ω (TDA7052A) in 16 Ω (TDA7052AT)	 $V_P = 6$ V $V_P = 6$ V	 1 0.5	 1.1 0.55	 – –	 W W
G_v	maximum total voltage gain		35	36	37	dB
ϕ	gain control range		75	80	–	dB
I_P	total quiescent current	$V_P = 6$ V; $R_L = \infty$	–	6	12	mA
THD	total harmonic distortion	$P_O = 0.5$ W	–	0.2	1	%

FUNCTIONAL DESCRIPTION

The TDA7052A/AT are mono BTL output amplifiers with DC volume control, designed for use in TV and monitors but also suitable for battery fed portable recorders and radios. In conventional DC volume circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low. In the TDA7052A/AT the DC volume control stage is integrated into the input stage so that no coupling capacitors are required and yet a low offset voltage is maintained. At the same time the minimum supply remains low.

The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Thus a reduced power supply with smaller capacitors can be used which results in cost savings.

For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 36 dB. The DC volume control stage has a logarithmic control characteristic.

The total gain can be controlled from 36 dB to –44 dB. If the DC volume control voltage is below 0.3 V, the device switches to the mute mode. The amplifier is short-circuit proof to ground and V_P. Also a thermal protection circuit is implemented. If the crystal temperature rises above 150 °C the gain will be reduced, so the output power is reduced. Special attention is given to switch on and off clicks, low HF radiation and a good overall stability.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage range		–	18	V
I_{ORM}	repetitive peak output current		–	1	A
I_{OSM}	non-repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\%$			
	TDA7052A		–	1.25	W
	TDA7052AT		–	0.64	W
T_{amb}	operating ambient temperature range		–40	85	°C
T_{stg}	storage temperature range		–55	150	°C
T_{vj}	virtual junction temperature		–	150	°C
T_{sc}	short-circuit time		–	1	hr
V_2	input voltage pin 2		–	8	V
V_4	input voltage pin 4		–	8	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air			
	TDA7052A	–	100	K/W
	TDA7052AT	–	155	K/W

Note

TDA7052A: V_P = 6 V; R_L = 8 Ω.
The maximum sine-wave dissipation is 0.9 W.
Therefore $T_{amb(max)}$ = 150 - 100 x 0.9 = 60 °C.
TDA7052AT: V_P = 6 V; R_L = 16 Ω.
The maximum sine-wave dissipation is 0.46 W.
Therefore $T_{amb(max)}$ = 150 - 155 x 0.46 = 78 °C.

CHARACTERISTICS

$V_P = 6$ V; $T_{amb} = 25$ °C; f = 1 kHz; unless otherwise specified (see Fig.6).
TDA7052A: $R_L = 8\ \Omega$;
TDA7052AT: $R_L = 16\ \Omega$;

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range		4.5	–	18	V
I_P	total quiescent current	$V_P = 6$ V; $R_L = \infty$ note 1	–	6	12	mA
Maximum gain; $V_4 = 1.4$ V						
P_O	output power TDA7052A TDA7052AT	THD = 10%	 1 0.5	 1.1 0.55	 – –	 W W
THD	total harmonic distortion TDA7052A TDA7052AT	 $P_O = 0.5$ W $P_O = 0.25$ W	 – –	 0.2 0.2	 1 1	 % %
G_v	voltage gain		35	36	37	dB
V_I	input signal handling	$V_4 = 1$ V; THD < 1%	0.6	–	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	f = 500 kHz; note 2	–	tbf	–	µV
B	bandwidth		–	20 Hz to 20 kHz	–	
RR	ripple rejection	note 3	40	–	–	dB
$\lvert V_{off}\rvert$	DC output offset voltage		–	tbf	150	mV
Z_I	input impedance (pin 2)		15	20	25	kΩ
Minimum gain; $V_4 = 0.5$ V						
G_v	voltage gain		–	–44	–	dB
$V_{no(rms)}$	noise output voltage RMS value)	note 4	–	20	30	µV
Mute position						
V_O	output voltage in mute position	$V_4 \leq 0.3$ V; $V_I = 600$ mV	–	–	30	µV
DC volume control						
ϕ	gain control range		75	80	–	dB
I_4	control current	$V_4 = 0.4$ V	tbf	65	tbf	µA

Notes to the characteristics

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage dividend by R_L.
2. The noise output voltage (RMS value) at f = 500 kHz is measured with $R_S = 0\ \Omega$ and bandwidth = 5 kHz.
3. The ripple rejection is measured with $R_S = 0\ \Omega$ and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV, (RMS value) is applied to the positive supply rail.
4. The noise output voltage (RMS-value) is measured with $R_S = 5$ kΩ unweighted.

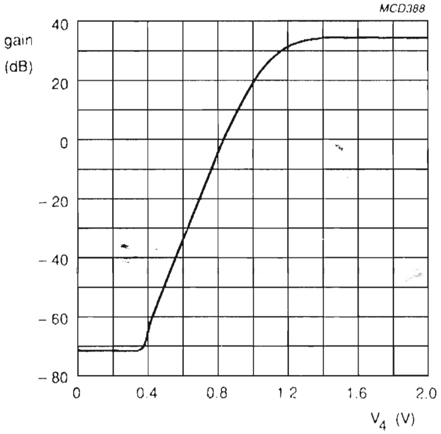


Fig.3 Gain control as a function of DC volume control.

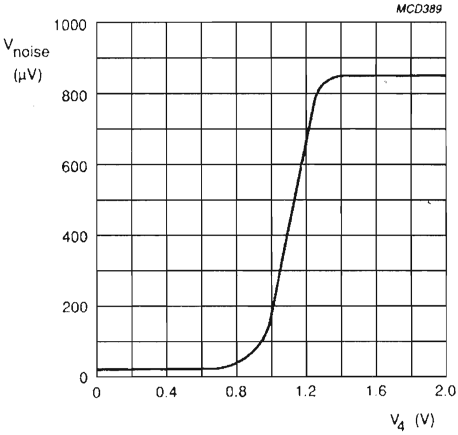


Fig.4 Noise output voltage as a function of DC volume control.

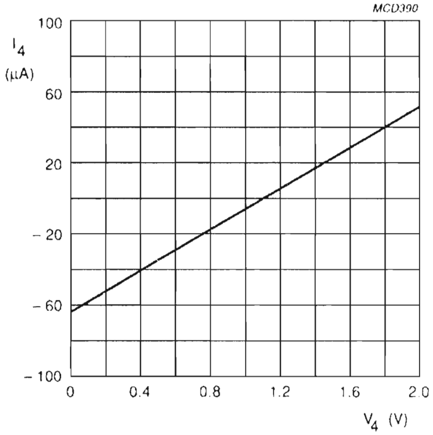
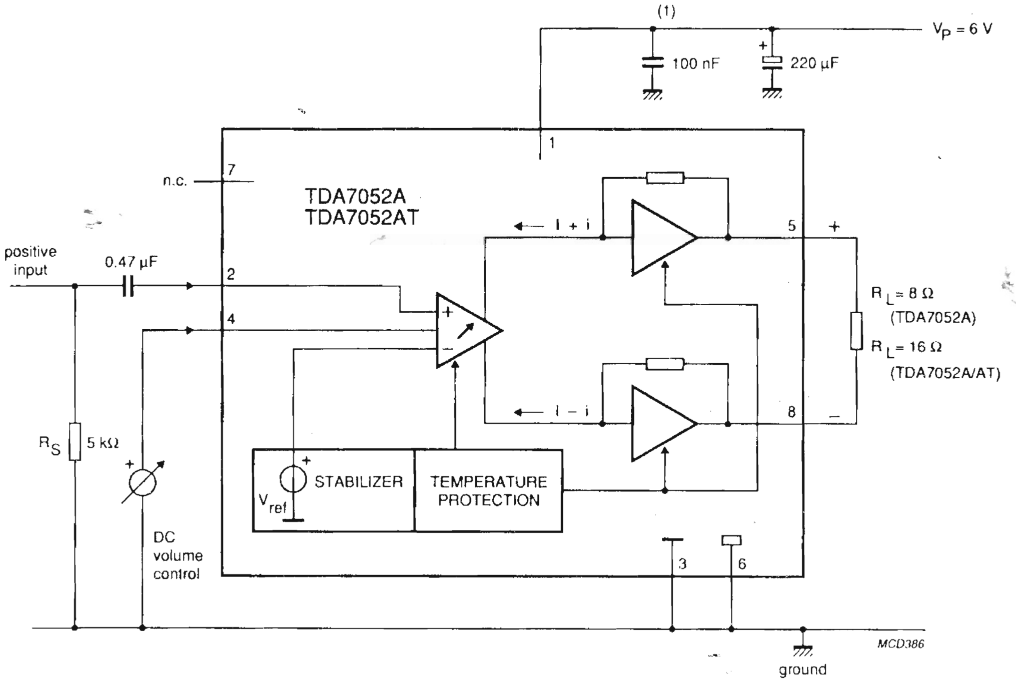


Fig.5 Control current as a function of DC volume control.

APPLICATION INFORMATION



(1) This capacitor can be omitted if the 220 μF electrolytic capacitor is connected close to pin 1.

Fig.6 Test and application diagram.

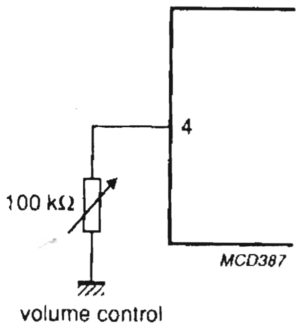


Fig.7 Application with potentiometer as volume control; maximum gain = 30 dB.

3-Watt mono BTL audio output amplifier TDA7056A

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7056A is a mono BTL output amplifier with DC volume control. It is designed for use in TV and monitors, but also suitable for battery-fed portable recorders and radios.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7056A	9	SIL	plastic	SOT110BE

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range		4.5	–	18	V
P_O	output power in 16 Ω	$V_P = 12$ V	3	3.4	–	W
G_v	voltage gain		35	36	37	dB
ϕ	gain control range		75	80	–	dB
I_p	total quiescent current	$V_P = 12$ V; $R_L = \infty$	–	8	16	mA
THD	total harmonic distortion	$V_P = 0.5$ W	–	0.2	1	%

3-Watt mono BTL audio output amplifier TDA7056A

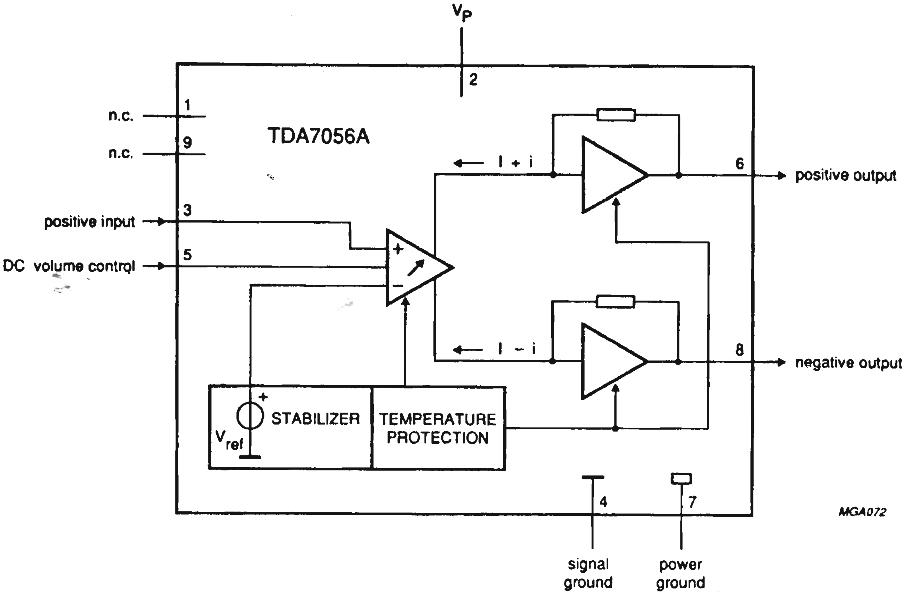


Fig.1 Block diagram.

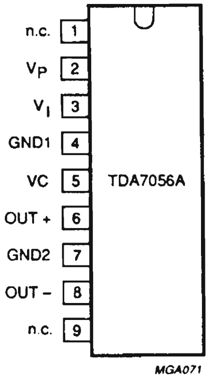


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
V_P	2	positive supply voltage
V_I	3	voltage input
GND1	4	signal ground
VC	5	DC volume control
OUT+	6	positive output
GND2	7	power ground
OUT−	8	negative output
n.c.	9	not connected

FUNCTIONAL DESCRIPTION

The TDA7056A is a mono BTL output amplifier with DC volume control, designed for use in TV and monitor but also suitable for battery-fed portable recorders and radios.
In conventional DC volume circuits the control or input stage is AC coupled to the output stage via external capacitor to keep the offset voltage low.
In the TDA7056A the DC volume stage is integrated into the input stage so that coupling capacitors are not required and a low offset voltage is maintained.
At the same time the minimum supply voltage remains low.
The BTL principle offers the following advantages:

- lower peak value of the supply current
- the frequency of the ripple on the supply voltage is twice the signal frequency

Thus, a reduced power supply and smaller capacitors can be used which results in cost savings.
For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 36 dB. The DC volume control stage has a logarithmic control characteristic.
The total gain can be controlled from 36 dB to −44 dB.
If the DC volume control voltage is below 0.3 V, the device switches to the mute mode.
The amplifier is short-circuit proof to ground and V_P. Also a thermal protection circuit is implemented. If the crystal temperature rises above 150 °C the gain will be reduced, so the output power is reduced.
Special attention is given to switch-on and off clicks, low HF radiation and a good overall stability.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage range		−	18	V
I_{ORM}	repetitive peak output current		−	1	A
I_{OSM}	non repetitive peak output current		−	1.5	A
P_{tot}	total power dissipation	$T_{case} < 60$ °C	−	9	W
T_{amb}	operating ambient temperature range		−40	85	°C
T_{stg}	storage temperature range		−55	150	°C
T_{vj}	virtual junction temperature		−	150	°C
T_{sc}	short-circuit time		−	1	hr
V_3	input voltage pin 3		−	8	V
V_5	input voltage pin 5		−	8	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}c}$	from junction to case	−	10	K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air	−	55	k/W

Note

$V_P = 12$ V; $R_L = 16\ \Omega$; The maximum sine-wave dissipation is ≈ 1.8 W. The $R_{th\ vj\text{-}a}$ of the package is 55 K/W;
$T_{amb\ (max)} = 150 - 55 \times 1.8 \approx 51$ °C

CHARACTERISTICS

$V_P = 12$ V; $f = 1$ kHz; $R_L = 16\ \Omega$; $T_{amb} = 25$ °C; unless otherwise specified (see Fig.6)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range		4.5	–	18	V
I_P	total quiescent current	$V_P = 6$ V; $R_L = \infty$; note 1	–	8	16	mA
Maximum gain ($V_5 = 1.4$ V)						
P_O	output power	THD = 10%	3	3.4	–	W
THD	total harmonic distortion	$P_O = 0.5$ W	–	0.2	1	%
G_v	voltage gain		35	36	37	dB
V_I	input signal handling	$V_5 = 1$ V;THD < 1%	0.6	–	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	f = 500 kHz; note 2	–	tbf	–	μV
B	bandwidth		–	20 Hz to 20 kHz	–	
RR	ripple rejection	note 3	40	–	–	dB
$\lvert V_{off}\rvert$	DC output offset voltage		–	tbf	150	mV
Z_I	input impedance pin 3		15	20	25	kΩ
Minimum gain ($V_5 = 0.5$ V)						
G_v	voltage gain		–	−44	–	dB
$V_{no(rms)}$	noise output voltage (RMS value)	note 4	–	20	30	μV
Mute position						
V_O	output voltage in mute position	$V_5 \leq 0.3$ V; $V_I = 600$ mV	–	–	30	μV
DC volume control						
ϕ	gain control range		75	80	–	dB
I_5	control current	$V_5 = 0$ V	tbf	65	tbf	μA

Notes to the characteristics

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.
2. The noise output voltage (RMS value) at f = 500 kHz is measured with $R_s = 0\ \Omega$ and bandwidth = 5 kHz.
3. The ripple rejection is measured with $R_S = 0\ \Omega$ and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV (RMS value) is applied to the positive supply rail.
4. The noise output voltage (RMS value) is measured with $R_S = 5$ kΩ unweighted.

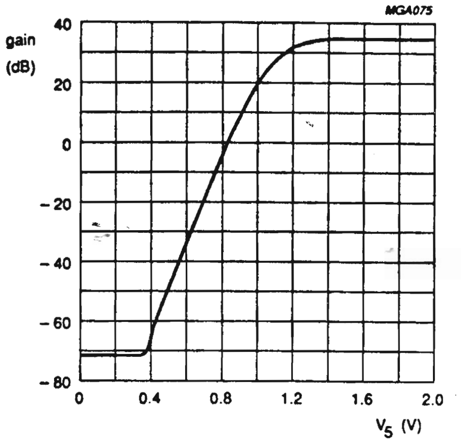


Fig.3 Gain as a function of DC volume control.

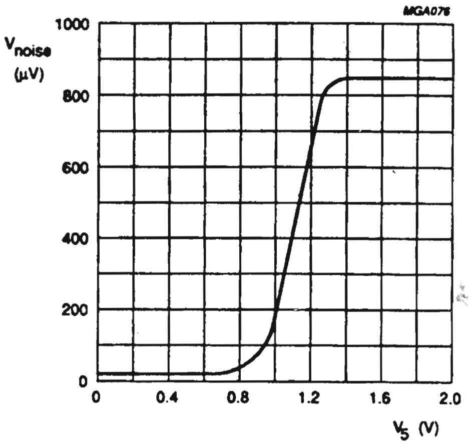


Fig.4 Noise output voltage as a function of DC volume control.

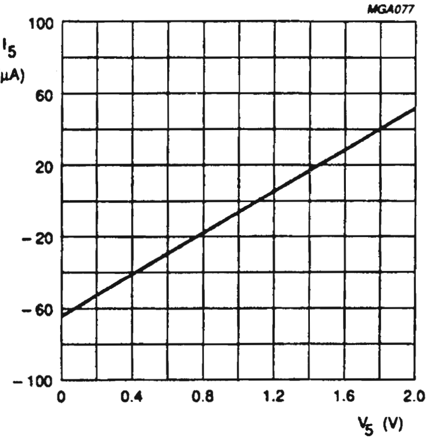
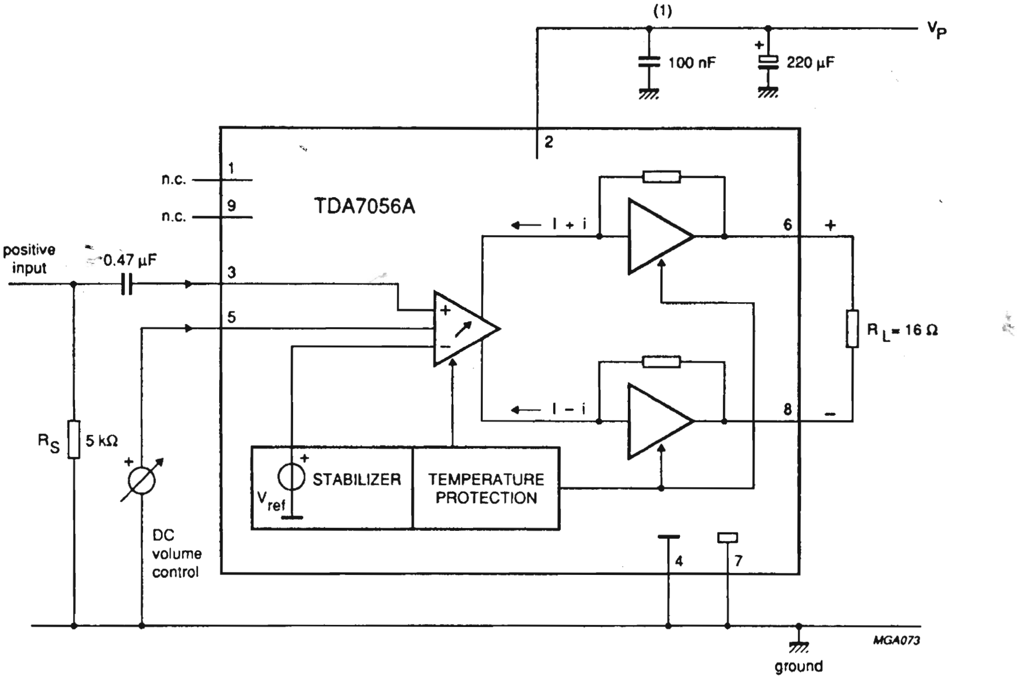


Fig.5 Control current as a function of DC volume control.

APPLICATION INFORMATION



(1) This capacitor can be omitted if the 220 μF electrolytic capacitor is connected close to pin 2.

Fig.6 Test and application diagram.

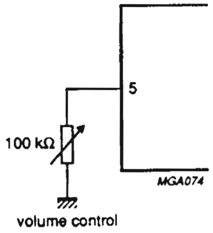


Fig.7 Application using a potentiometer for volume control; $G_v = 30$ dB.

True logarithmic amplifier

TDA8780M

FEATURES

- 72 dB true logarithmic dynamic range
- Small-signal gain-adjustment facility
- Constant limiting output voltage
- Temperature and DC power supply voltage independent
- Easy interfacing to analog-to-digital converters
- Output DC level shift facility.

APPLICATIONS

- Dynamic range compression
- IF signal dynamic range reduction in GSM900 and DCS1 800 receivers
- Compression receivers.

GENERAL DESCRIPTION

The TDA8780M is a true logarithmic amplifier intended for dynamic range reduction of IF signals at 10.7 MHz in GSM900 and DCS1 800 receivers. It offers true logarithmic characteristics over a 72 dB input dynamic range, has a small-signal gain-adjustment facility and a constant limiting output voltage for large input levels.

The device is manufactured in an advanced BiCMOS process which enables high performance being obtained with low DC power supply consumption. The true logarithmic amplifier can be driven by single-ended or differential inputs. The DC operating point is set by overall on-chip feedback decoupled by two off-chip capacitors, which define the low-frequency cut-off point.

The performance of the amplifier is stabilized against temperature and DC power supply variations. The differential output is converted internally to a single-ended output by an on-chip operational amplifier arrangement in which the DC output level is set by an externally-supplied reference voltage. A power-down facility allows the circuit to be disabled from a control input.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	DC power supply voltage	4.5	5.0	5.5	V
I_P	DC power supply current	–	–	10	mA
$I_{P(PD)}$	DC power supply current in power-down mode	–	–	250	µA
f_i	operating input frequency	–	–	15	MHz
$V_{i(M)}$	dynamic logarithmic input voltage (peak value)	0.06	–	300	mV
T_{amb}	operating ambient temperature	–20	–	+75	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8780M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

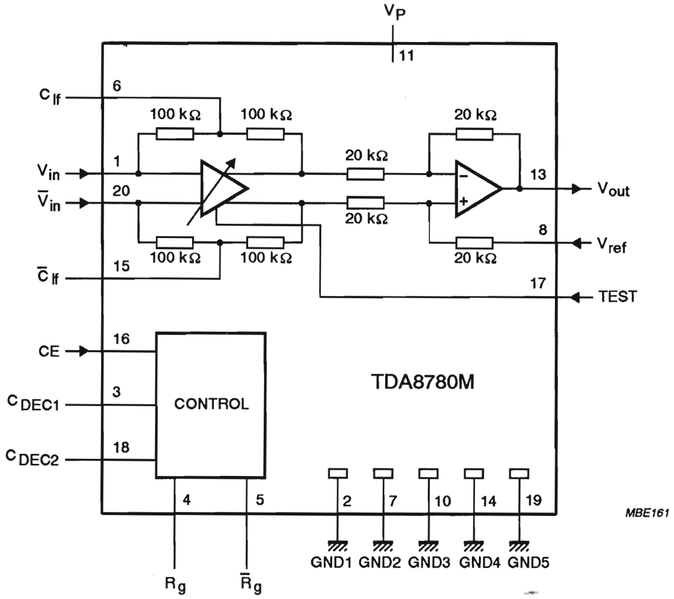


Fig.1 Block diagram.

True logarithmic amplifier TDA8780M

PINNING

SYMBOL	PIN	DESCRIPTION
V_{in}	1	signal voltage input
GND1	2	ground 1
C_{DEC1}	3	control circuit first decoupling and optional start-up capacitor connection
R_g	4	small-signal gain-setting resistor
$\overline{R}_g$	5	small-signal complementary gain-setting resistor
C_{lf}	6	low-frequency cut-off point setting capacitor
GND2	7	ground 2
V_{ref}	8	external reference voltage input
n.c.	9	not connected
GND3	10	ground 3 (main ground)
V_P	11	DC power supply
n.c.	12	not connected
V_{out}	13	true logarithmic voltage output
GND4	14	ground 4
$\overline{C}_{lf}$	15	complementary low-frequency cut-off point setting capacitor
CE	16	TTL-level-compatible circuit enable input (active HIGH)
TEST	17	test input; connected to ground in normal operation
C_{DEC2}	18	control circuit second decoupling and optional start-up capacitor
GND5	19	ground 5
$\overline{V}_{in}$	20	complementary signal voltage input

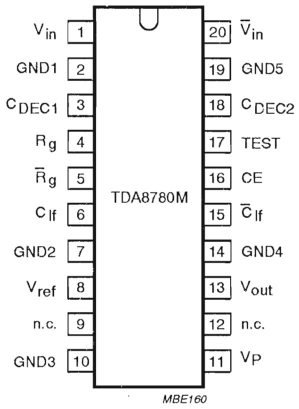


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

A true logarithmic amplifier can be realized from a cascade of similar stages each stage consisting of a pair of amplifiers whose inputs and outputs are connected in parallel. One of these amplifiers can be formed by an undegenerated long-tailed pair which provides high gain but limited linear input signal-handling capability. The other amplifier can be formed by a degenerated long-tailed pair which provides a gain of unity and a much larger linear input signal-handling capability.

The overall cascade amplifies very small input signals but, once these reach the level at which the undegenerated long-tailed pair in the last stage is at the limit of its linear signal-handling capability, the output voltage becomes logarithmically dependent on the input signal level. This behaviour continues until the input signal reaches the level at which undegenerated long-tailed pair in the first stage is at the limit of its linear input signal-handling capability. The transfer characteristic beyond this point then depends on the exact configuration of the degenerated long-tailed pair in the first stage.

Five stages are used in the TDA8780M to provide a 72 dB true logarithmic dynamic range. The DC bias current in the undegenerated long-tailed pair in the first stage is made externally adjustable, using an off-chip resistor, to provide a small-signal gain adjustment facility. A high-level limiter is inserted between the first and second stages to provide a constant limiting output voltage which is essentially independent of the value of the gain setting resistor. These stages can be driven by single-ended or differential inputs. The DC operating point is set by overall on-chip feedback decoupled by two off-chip capacitors which define the low-frequency cut-off point. The performance is stabilized against temperature and DC power supply variations. The input to the true logarithmic amplifier is protected against damage due to excessive differential input signals by diodes.

The differential output from the true logarithmic amplifier is converted internally to a single-ended output by an on-chip operational amplifier arrangement in the which the DC output level is set by an externally-supplied reference voltage. The output is capable of driving loads down to 10 kΩ. The limiting output voltage and the output drive capability have been chosen to facilitate interfacing to analog-to-digital converters. A major part of the DC power supply current consumption of the device is associated with provision of this output drive capability. The DC power supply consumption is significantly less when the device is driving smaller loads.

A power-down facility allows the circuit to be disabled from a TTL-level compatible control input.

True logarithmic amplifier TDA8781T

FEATURES

- 55 dB true logarithmic dynamic range
- Small-signal gain-adjust facility
- Constant limiting output voltage
- Temperature and DC power supply voltage compensation
- Easy interfacing to TDA8703 analog-to-digital converter
- Output DC level shift facility
- Additional received signal-strength indication (RSSI) output.

APPLICATIONS

- Dynamic range compression
- IF signal dynamic range reduction in GSM900 and DCS1800 receivers
- Compressive receivers.

GENERAL DESCRIPTION

The TDA8781T is a true logarithmic amplifier intended for dynamic range reduction of IF signals at 10.7 MHz in GSM900 and DCS1800 receivers. It offers true logarithmic characteristics over a 55 dB input dynamic range and has a small-signal gain-adjust facility and a constant limiting output voltage for large input levels. It is manufactured in an advanced BICMOS process which enables high performance to be obtained with low DC power supply consumption. The true logarithmic amplifier can be driven by single-ended or differential inputs and the DC operating point is set by overall on-chip feedback decoupled by two off-chip capacitors which define the low-frequency cut-off point. The performance of the true logarithmic amplifier is stabilized against temperature and DC power supply voltage variations. The differential output is converted internally to a single-ended output by an on-chip operational amplifier arrangement in which the DC output level is set by an externally-supplied reference voltage. An additional received signal-strength indication (RSSI) output is available and a power-down facility allows the circuit to be disabled from a TTL-level compatible control input.

The device can be used to compress IF signals prior to being digitized in digital radio systems. It allows the usage of low-cost, low-power 8-bit DACs instead of the 10 or 12-bit types. In GSM systems decompression is performed by the digital signal processor such as the PCD5080. The TDA8781T interfaces directly with the ADC which is integrated on the Base Band Interface PCD5070.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC power supply voltage	4.5	5.0	5.5	V
I_{CC}	DC power supply current	–	–	10	mA
I_{OFF}	I_{CC} in power-down mode	–	250	400	μA
f_i	operating input frequency	0.1	10.7	15.0	MHz
T_{amb}	operating ambient temperature	−20	–	+75	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8781T	14	SO14	plastic	SOT108A

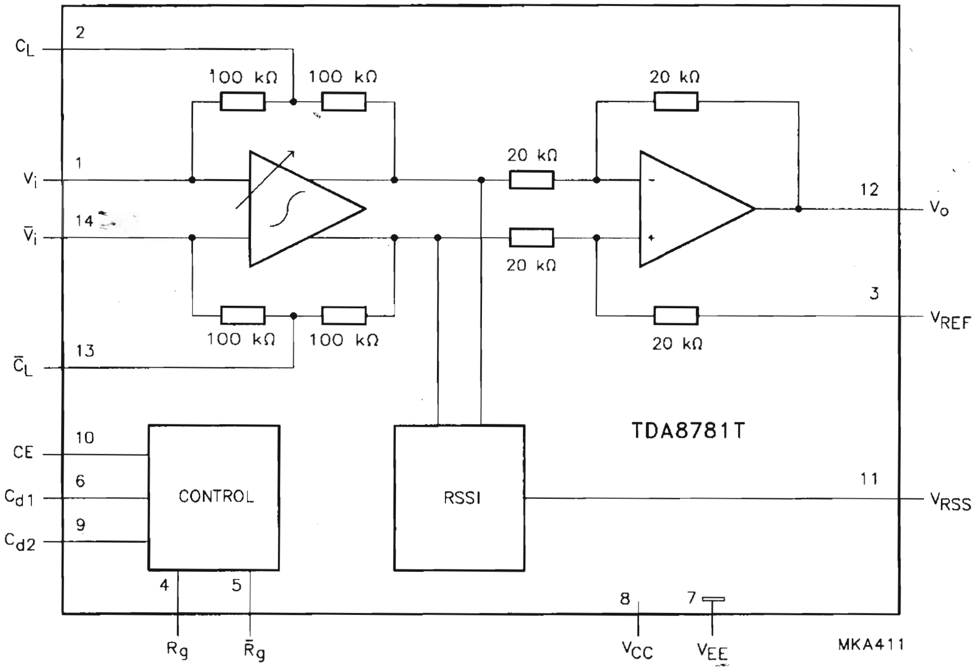


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_i	1	signal input
C_L	2	low-frequency cut-off point setting capacitor connection
V_{REF}	3	external reference voltage input
R_g	4	small-signal gain-setting resistor connection
$\overline{R}_g$	5	complementary small-signal gain-setting resistor connection
C_{d1}	6	first control circuit decoupling capacitor and optional start-up capacitor connection
V_{EE}	7	ground
V_{CC}	8	DC power supply voltage
C_{d2}	9	second control circuit decoupling capacitor and optional start-up capacitor connection
CE	10	TTL-level-compatible circuit enable input
V_{RSSI}	11	received signal-strength indication output (RSSI)
V_o	12	true logarithmic output
$\overline{C}_L$	13	complementary low-frequency cut-off point setting capacitor connection
$\overline{V}_i$	14	complementary signal input

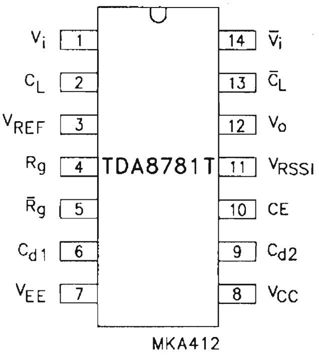


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

A true logarithmic amplifier can be realized from a cascade of similar stages each of which consists of a pair of amplifiers whose inputs and outputs are connected in parallel. One of these amplifiers can be formed by an undegenerated long-tailed pair which provides high gain but a limited linear input signal-handling capability. The other amplifier can be formed by a degenerated long-tailed pair which provides a gain of unity and a much larger linear input signal-handling capability. The overall cascade amplifies very small input signals linearly but, once these reach the level at which the undegenerated long-tailed pair in the last stage is at the limit of its linear input signal-handling capability, the output voltage becomes logarithmically dependent on the input signal level. This behavior continues until the input signal reaches the level at which the undegenerated long-tailed pair in the first stage is at the limit of its linear input signal-handling capability. The transfer characteristic beyond this point then depends on the exact configuration of the degenerated long-tailed pair in the first stage.

Three stages are used in the TDA8781T to provide a 55 dB true logarithmic dynamic range. The DC bias current in the undegenerated long-tailed pair in the first stage is made externally adjustable, by means of an off-chip resistor, to provide a small-signal gain-adjust facility. A high-level limiter is inserted between the first and second stages to provide a constant limiting output voltage which is essentially independent of the value of the gain-setting resistor. These stages can be driven by single-ended or differential inputs and the DC operating point is set by overall on-chip feedback decoupled by two off-chip capacitors which define the low-frequency cut-off point. The performance of these stages is stabilized against temperature and DC power supply voltage variations. The input to the true logarithmic amplifier is protected against damage due to excessive differential input signals by diodes.

The differential output from the true logarithmic amplifier is converted internally to a single ended output by an on-chip operational amplifier arrangement in which the DC output level is set by an externally-supplied reference voltage. The output is capable of driving loads down to 10 kΩ in parallel with 20 pF. The limiting output voltage and this output drive capability have been chosen to facilitate interfacing to a TDA8703 analog-to-digital converter. A major proportion of the DC power supply current consumption of the device is associated with provision of this output drive capability. The DC power supply consumption is significantly less when the device is driving less-highly capacitive loads.

An additional received signal-strength indication (RSSI) output is available from the true logarithmic amplifier. This output is protected against damage due to excessive current being drawn by means of a series resistor. A power-down-facility allows the circuit to be disabled from a TTL-level-compatible control input.

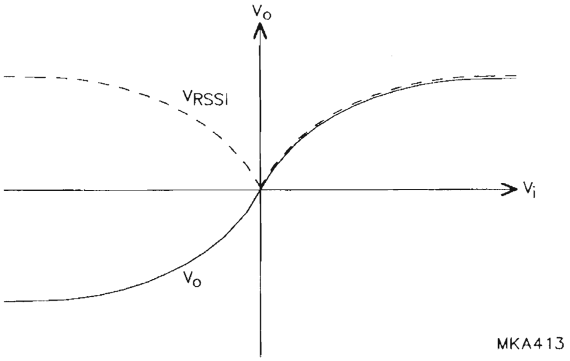


Fig.3 Transfer function.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	DC power supply voltage	−0.3	+5.5	V
V_I	DC voltage at all other pins with respect to ground	−0.3	V_{CC} + 0.3	V
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−20	+75	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

V_{CC} = 5.0 V; V_{REF} = 2.5 V; V_i at f_i = 10.7 MHz; T_{amb} = 25 °C; nominal small-signal gain setting resistor in use; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 8)						
V_{CC}	operating DC power supply voltage		4.5	5.0	5.5	V
I_{CC}	DC power supply current	V_{CC} = 5.5 V; V_i = 1 V (peak)	–	8	10	mA
I_{OFF}	DC power supply current in power-down mode	10 µs after V_{CE} changes from $V_{CE(ON)}$ to $V_{CE(OFF)}$	–	250	400	µA
Control: CE, R_g, $\overline{R}_g$, C_{d1}, C_{d2} (pins 10, 4, 5, 6 and 9)						
$V_{CE(ON)}$	circuit enable input voltage		2.0	–	V_{CC}	V
$V_{CE(OFF)}$	circuit enable input voltage in power-down mode		0	–	0.8	V
R_g	small-signal gain-setting resistor	nominal small-signal gain setting	–	3.3	–	kΩ
		total adjustment range	0	–	–	kΩ
C_{d1}, C_{d2}	control circuit decoupling capacitors		–	560	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs: V_I, V_{REF}, C_L, $\overline{C}_L$ (pins 1, 3, 2 and 13)						
f_i	operating input frequency		0.1	10.7	15	MHz
R_i	small-signal input resistance	differential input at f_i = 10.7 MHz; V_i = 10 mV (peak)	–	10	–	kΩ
C_i	input capacitance	differential input at f_i = 10.7 MHz	–	3	–	pF
$V_{i(min)}$	peak input voltage at start of true logarithmic characteristic		–	800	–	µV
$V_{i(max)}$	peak input at end of true logarithmic characteristic		–	450	–	mV
$V_{i(limit)}$	maximum peak input signal	input protection diodes not conducting	–	1	–	V
ΔV_i	spread in true logarithmic output amplitude transfer characteristic across true logarithmic range over whole temperature and DC power supply voltage range	input spread for fixed output	–	±2.5	–	dB
ΔG_v	small-signal gain-adjustment range		±6	–	–	dB
C_L, $\overline{C}_L$	low-frequency cut-off point setting capacitors	f = 100 kHz at 3 dB	–	560	–	pF
R_{REF}	external reference input resistance		–	40	–	kΩ
V_{REF}	external reference voltage		2.0	2.5	V_{CC} – 2.0	V
Outputs: V_o, V_{RSSI} (pins 12 and 13)						
$V_{o(min)}$	peak true logarithmic output voltage relative to V_{REF} at start of true logarithmic characteristic	V_i = 800 µV (peak)	–	90	–	mV
$V_{o(max)}$	peak true logarithmic output voltage relative to V_{REF} at end of true logarithmic characteristic	V_i = 450 mV (peak)	–	900	–	mV
V_o	true logarithmic peak output voltage across true logarithmic range	V_i = 1 mV (peak)	55	100	145	mV
		V_i = 10 mV (peak)	340	410	480	mV
		V_i = 100 mV (peak)	630	730	830	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{o(limit)}$	limiting peak output voltage	$V_i = 1$ V (peak)	800	950	1100	mV
$V_o - V_{REF}$	DC offset voltage	$V_i = 0$ V	−100	+35	+100	mV
ΔG_{vo}	change in small-signal true logarithmic gain referred to V_o at $V_i = 10$ mV (peak); $R_g = 3.3$ kΩ	$V_i = 5$ mV (peak); $R_g = 0$	0	–	+2	dB
		$V_i = 20$ mV (peak); $R_g = \infty$	−2	–	0	dB
ΔV_o	change in small-signal true logarithmic output voltage with frequency	$V_i = 10$ mV (peak); $f_i = 100$ kHz and 15 MHz referenced to 1 MHz	–	0.4	1.5	dB
$\Delta\phi$	spread in true logarithmic output phase transfer characteristic across true logarithmic range		–	15	–	deg
V_{RSSI}	RSSI output across true logarithmic range	$V_i = 1$ mV (peak)	1.85	2.0	2.15	V
		$V_i = 10$ mV (peak)	2.05	2.2	2.35	V
		$V_i = 100$ mV (peak)	2.25	2.4	2.55	V

APPLICATION INFORMATION

The circuit is connected as shown in the typical application circuit diagram (Fig.4). The single-ended 10.7 MHz input IF signal is applied (arbitrarily) to one of the two input pins via a ceramic filter. These inputs should not be DC coupled as this will disable the on-chip feedback which sets the DC operating point of the true logarithmic amplifier. The relatively high input impedance of these inputs facilitates correct termination of the ceramic filter by means of an off-chip resistor.

The low-frequency cut-off point is determined by the value of the capacitors which decouple the overall DC feedback as well as the value of the input coupling capacitors. The output is AC coupled to a TDA8703 analog-to-digital converter in order that the value of the voltage fed to the reference voltage input is not critical. It could be useful in other applications, where the output might be DC coupled to an alternative analog-to-digital converter, to derive this reference voltage from the centre of the input resistor chain of the analog-to-digital converter.

The additional RSSI output is required only in applications where this is not derived in subsequent digital signal processing stages. The capacitor connected to this output provides a simple peak-hold and averaging function. Excessively large values of capacitance may lead to distortion of the true logarithmic output.

It may be found advantageous to add two small capacitors to speed up the re-enabling of the circuit after it has been in power-down mode. These should be connected between the circuit enable input and the control circuit decoupling capacitors. The size of these capacitors will be related to the size of the control circuit decoupling capacitors which are required both for stability and to prevent degradation of the noise figure.

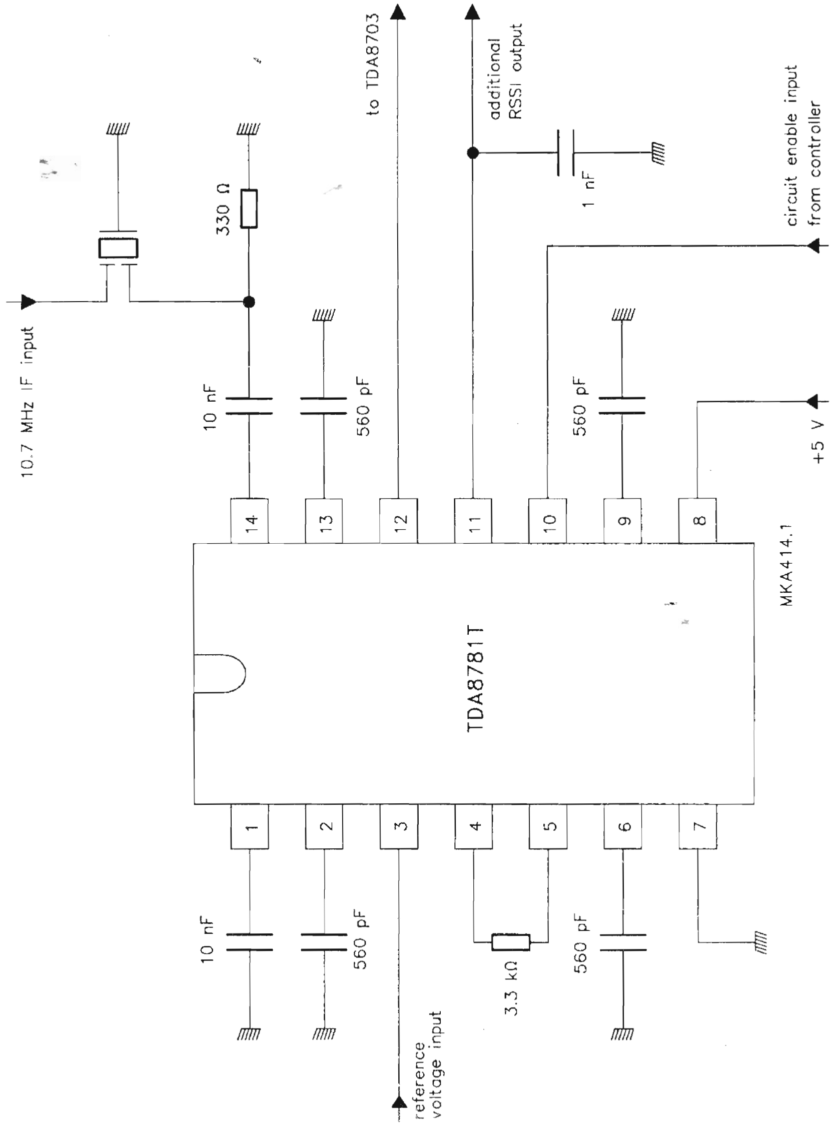


Fig.4 Typical application diagram.

Section 4
IF Systems

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The Philips Family of High Performance IF Systems

	V_{CC}	I_{CC}	Pins	Package	Input Freq	IF Freq	f_{RF} = 45MHz			RSSI Range	Fast RSSI	Freq Check Pin	IF Filter Match	Output Op Amps	Feature Highlights
							Input Sensitivity	Mixer Gain	Input IP_3						
FM IF															
NE/SA604A	4.5-8V	3.3mA @ 6V	16	D,N	25MHz	25MHz	0.22µV[1]	–	–	90dB	–	–	455kHz	–	– High Sensitivity
NE/SA614A	4.5-8V	3.3mA @ 6V	16	D,N	25MHz	25MHz	0.22µV[1]	–	–	80dB	–	–	455kHz	–	– Wide IF BW
NE/SA624	4.5-8V	3.4mA @ 6V	16	D,N	25MHz	25MHz	0.22µV[1]	–	–	90dB	✓	–	455kHz	–	
Mixer/FM IF															
NE/SA605	4.5-8V	5.7mA @ 6V	20	D,DK,N	500MHz	25MHz	0.22µV	13dB	-10dBm	90dB	–	–	455kHz	–	– High Sensitivity
NE/SA615	4.5-8V	5.7mA @ 6V	20	D,DK,N	500MHz	25MHz	0.22µV	13dB	-10dBm	80dB	–	–	455kHz	–	– High Input Frequency
NE/SA625	4.5-8V	5.8mA @ 6V	20	D,DK,N	500MHz	25MHz	0.22µV	13dB	-10dBm	90dB	✓	–	455kHz	–	
NE/SA627	4.5-8V	5.8mA @ 6V	20	D,DK,N	500MHz	25MHz	0.22µV	13dB	-10dBm	90dB	✓	✓	455kHz	–	– Wide IF BW
Low Voltage Mixer/FM IF															
SA606	2.7-7V	3.5mA @ 3V	20	D,DK,N	150MHz	2MHz	0.31µV	17dB	-9dBm	90dB	–	–	455kHz	Audio Op Amp RSSI Op Amp	– High Sensitivity
SA616	2.7-7V	3.5mA @ 3V	20	D,DK,N	150MHz	2MHz	0.31µV	17dB	-9dBm	80dB	–	–	455kHz	Audio Op Amp RSSI Op Amp	– Low Power
SA607	2.7-7V	3.5mA @ 3V	20	D,DK,N	150MHz	2MHz	0.31µV	17dB	-9dBm	90dB	–	✓	455kHz	Audio Op Amp RSSI Buffered	– Audio/RSSI Output Op Amps
SA617	2.7-7V	3.5mA @ 3V	20	D,DK,N	150MHz	2MHz	0.31µV	17dB	-9dBm	80dB	–	✓	455kHz	Audio Op Amp RSSI Buffered	
SA608	2.7-7V	3.5mA @ 3V	20	D,DK,N	150MHz	2MHz	0.31µV	17dB	-9dBm	90dB	–	✓	455kHz	Audio Buffered RSSI Op Amp	– Power-Down Mode (SA626/636)
SA626	2.7-5.5V	6.5mA @ 3V	20	D,DK	500MHz	25MHz	0.54µV[2]	11dB[2]	-16dBm[2]	90dB	✓	–	10.7MHz	Audio Buffered RSSI Op Amp	
SA636	2.7-5.5V	6.5mA @ 3V	20	D,DK	500MHz	25MHz	0.54µV[2]	11dB[2]	-16dBm[2]	90dB	✓	–	10.7MHz	RSSI Op Amp	
SA676	2.7-5.5V	3.5mA @ 3V	20	D,DK	100MHz	2MHz	0.45µV	17dB	-10dBm	70dB	–	–	455kHz	Audio Op Amp RSSI Op Amp	
Low Voltage Mixer/Digital IF															
SA637	2.7-5.5V	3.5mA @ 3V	20	D,DK	200MHz	2MHz	-117dBm[3] 0.31µV	15dB	-10dBm	90dB	✓	–	455kHz	RSSI Op Amp	

Temperature Ranges	Package Descriptions	IF Filter Match
NE: 0 to + 70°C SA: -40 to + 85°C	D: Small Outline - 16 Small Outline - 20 DK: Shrink Small Outline Package (SSOP) - 20 N: Dual In-Line Plastic - 16, 20	455kHz = 1.5kΩ 10.7MHz = 330Ω

NOTES:
1. Measured with a Philips NE/SA602A mixer prior to the IF input.
2. Measured at f_{RF} = 240MHz
3. Represents the -3dB Input Limiting point (dBm). Also shown in µV units into a 50Ω matching network.

DESCRIPTION

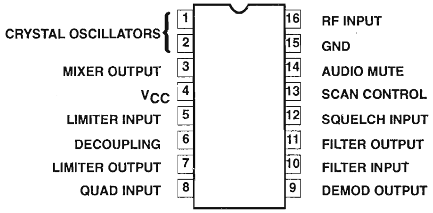
The MC3361 is a monolithic low-power FM IF signal processing system consisting of an oscillator, mixer, limiting amplifier, quadrature detector, filter amplifier, squelch, scan control and mute switch. It is intended for use in narrow band FM dual conversion communications equipment. The MC3361 is available in a 16-lead, dual-in-line plastic package and 16-lead SOL (surface-mounted miniature package).

FEATURES

- 2.0V to 8.0V operation
- Low current: 4.2mA typ at $V_{CC} = 4.0V_{DC}$
- Excellent sensitivity: 2.0µV for –3dB limiting typ
- Low external parts count
- Operation to 60MHz

PIN CONFIGURATION

D^1 and N Package



NOTE:
1. Available in 16-pin SOL package.

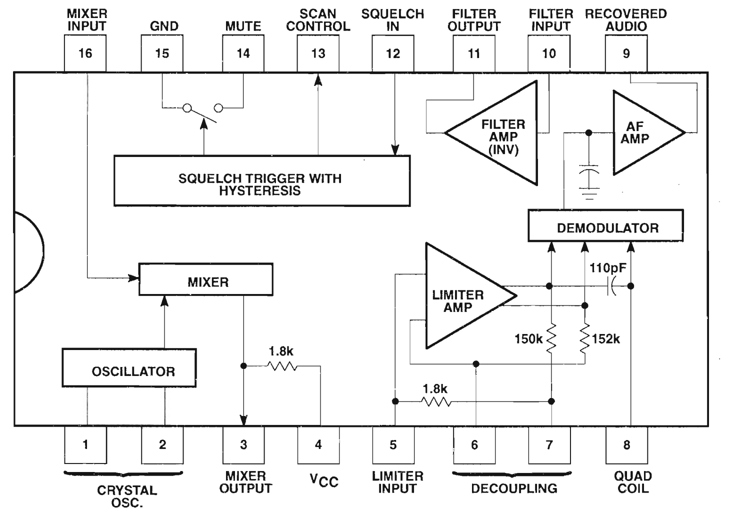
APPLICATIONS

- Cordless telephone
- Narrow band receivers
- Remote control

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	MC3361N	0406C
16-Pin Plastic Small Outline Large (SOL)	–40 to +85°C	MC3361D	0171B

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

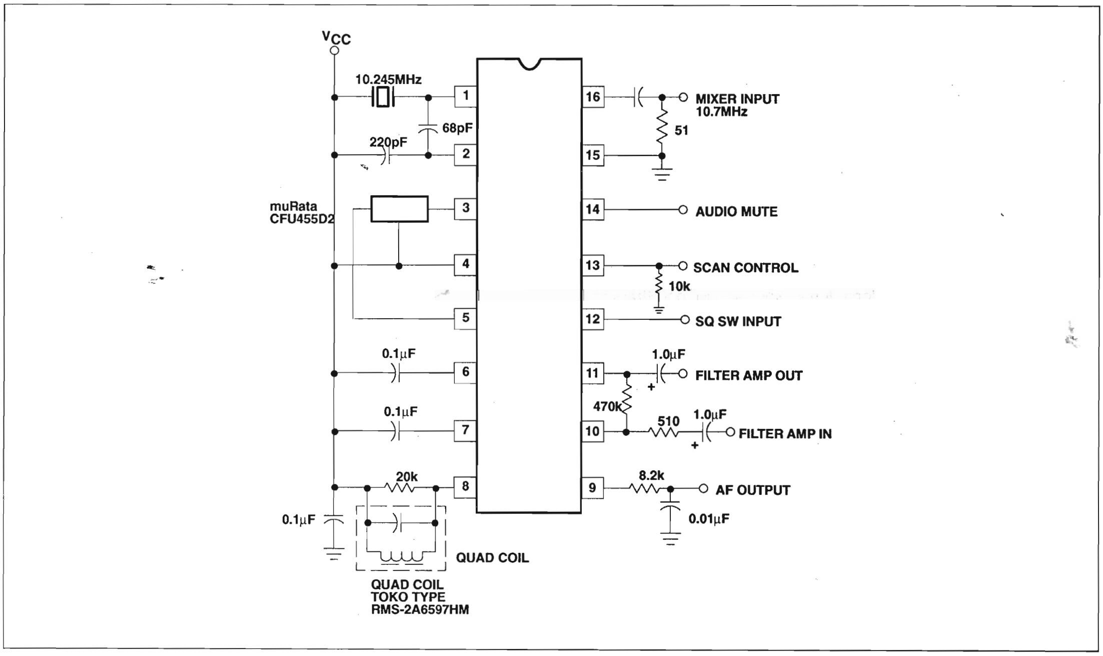
SYMBOL	PARAMETER	PIN	RATING	UNIT
V_{CC} (Max)	Power supply voltage	4	10	V_{DC}
V_{CC}	Generating supply voltage range	4	2.0 to 8.0	V_{DC}
	Detector input voltage	8	1.0	$V_{P\text{-}P}$
V_{16}	Input voltage ($V_{CC} \geq 4.0V$)	16	1.0	V_{RMS}
V_{14}	Mute function	14	–0.5 to 5.0	V_{PK}
T_J	Junction temperature		150	°C
T_A			–40 to +85	°C
T_{STG}	Storage temperature range		–65 to +150	°C

AC AND DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 4.0V_{DC}$, $f_O = 10.7MHz$, $\Delta f = +3.0kHz$, $f_{MOD} = 1.0kHz$, $T_A = 25°C$ unless otherwise noted.

PARAMETER	PIN	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Drain current (no signal) squelch off	4			4.2	7.0	mA
squelch on				5.4		
Input limiting voltage	16	–3.0dB limiting		2.0	6.0	µV
Detector output voltage	9			2.0		V_{DC}
Detector output impedance				450		Ω
Recovered audio output voltage	9	100	150	270		mV_{RMS}
Filter gain (10kHz)		$V_{IN}=1.0mV_{RMS}$	40	46		dB
Filter output voltage	11			1.7		V_{DC}
Trigger hysteresis				50		mV
Mute function low	14			10		Ω
Mute function high	14			10		MΩ
Scan function low (mute off)	13			0.5		V_{DC}
Scan function high (mute on)	13	V_{12}=GND				V_{DC}
Mixer conversion gain	3			27		dB
Mixer input resistance	16			3.6		kΩ
Mixer input capacitance	16			2.2		pF

TEST CIRCUIT



High performance low power FM IF system

NE/SA604A

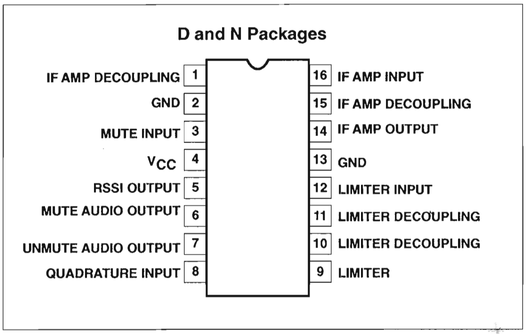
DESCRIPTION

The NE/SA604A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA604A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA604A is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature) package.

FEATURES

- Low power consumption: 3.3mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA604A meets cellular radio specifications

PIN CONFIGURATION



APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

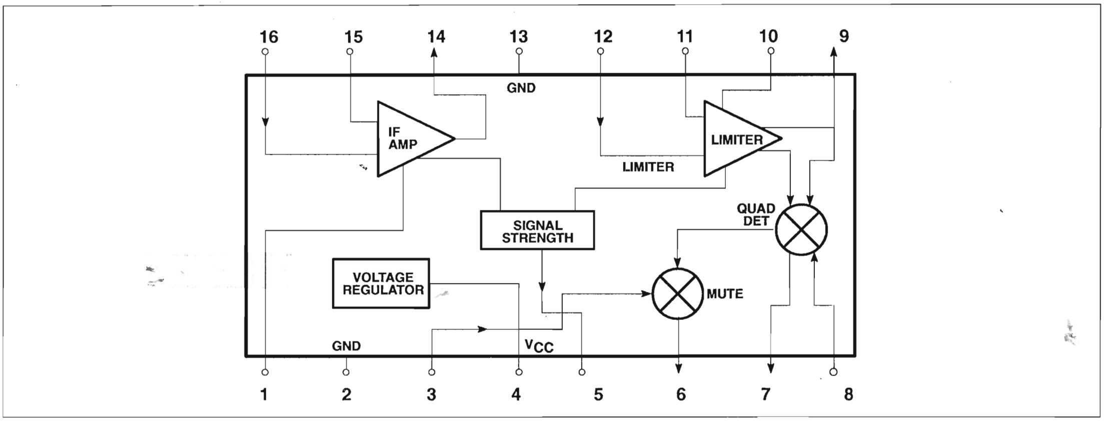
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE604AN	0406C
16-Pin Plastic Small Outline (SO) package (Surface-mount)	0 to +70°C	NE604AD	0005D
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA604AN	0406C
16-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA604AD	0005D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE604A SA604A	0 to +70 -40 to +85	°C °C
θ_{JA}	Thermal impedance D package N package	90 75	°C/W °C/W

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE604A			SA604A			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		2.5	3.3	4.0	2.5	3.3	4.0	mA
	Mute switch input threshold (ON) (OFF)		1.7		 1.0	1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

Typical reading at T_A = 25°C; V_{CC} = ±6V, unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE604A			SA604A			
			MIN	TYP	MAX	MIN	TYP	MAX	
	Input limiting -3dB	Test at Pin 16		-92			-92		dBm/50Ω
	AM rejection	80% AM 1kHz	30	34		30	34		dB
	Recovered audio level	15nF de-emphasis	110	175	250	80	175	260	mV_{RMS}
	Recovered audio level	150pF de-emphasis		530			530		mV_{RMS}
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	RSSI output[1]	RF level = -118dBm	0	160	550	0	160	650	mV
		RF level = -68dBm	2.0	2.65	3.0	1.9	2.65	3.1	V
		RF level = -18dBm	4.1	4.85	5.5	4.0	4.85	5.6	V
	RSSI range	R_4 = 100k (Pin 5)		90			90		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±1.5			±1.5		dB
	IF input impedance		1.4	1.6		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		1.4	1.6		kΩ
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ

NOTE:

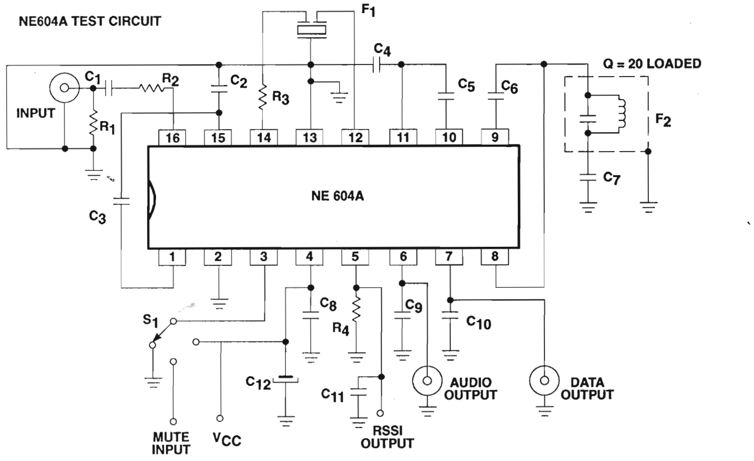
1. NE604 data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

NE604 (50)	NE604A (1.5k)/NE605 (1.5k
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm

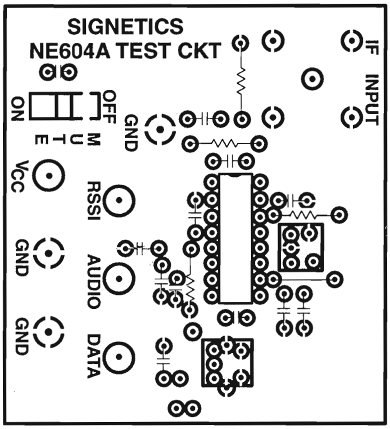
The NE605 and NE604A are both derived from the same basic die. The NE605 performance plots are directly applicable to the NE604A.

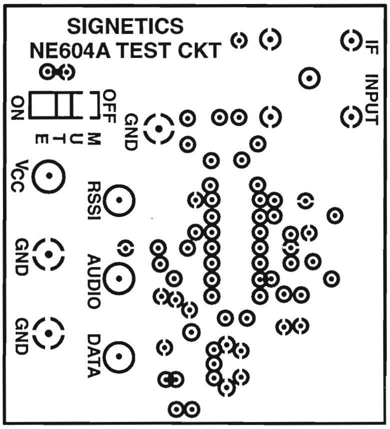
High performance low power FM IF system

NE/SA604A



C1	100nF + 80 – 20% 63V K10000–25V Ceramic
C2	100nF +10% 50V
C3	100nF ±10% 50V
C4	100nF +10% 50V
C5	100nF ±10% 50V
C6	10pF ±2% 100V NPO Ceramic
C7	100nF ±10% 50V
C8	100nF ±10% 50V
C9	15nF ±10% 50V
C10	150pF ±2% 100V N1500 Ceramic
C11	1nF ±10% 100V K2000-Y5P Ceramic
C12	6.8μF ±20% 25V Tantalum
F1	455kHz Ceramic Filter Murata SFG455A3
F2	455kHz (Ce = 180pF) TOKO RMC 2A6597H
R1	51Ω ±1% 1/4W Metal Film
R2	1500Ω ±1% 1/4W Metal Film
R3	1500Ω ±5% 1/8W Carbon Composition
R4	100kΩ ±1% 1/4W Metal Film





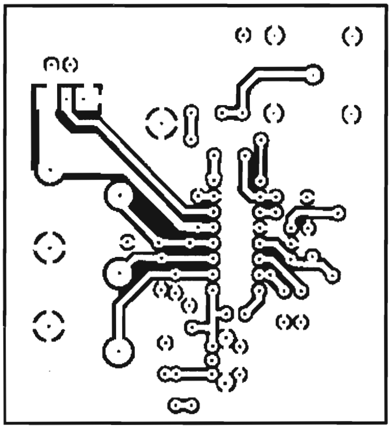


Figure 1. NE/SA604A Test Circuit

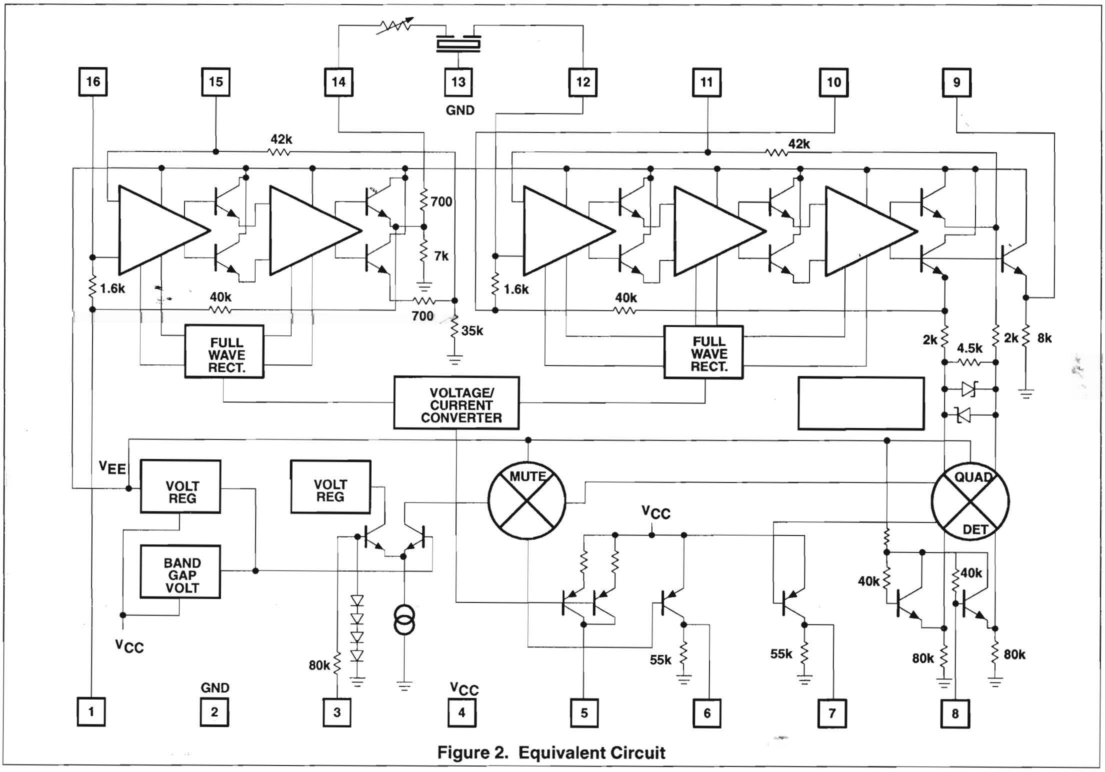


Figure 2. Equivalent Circuit

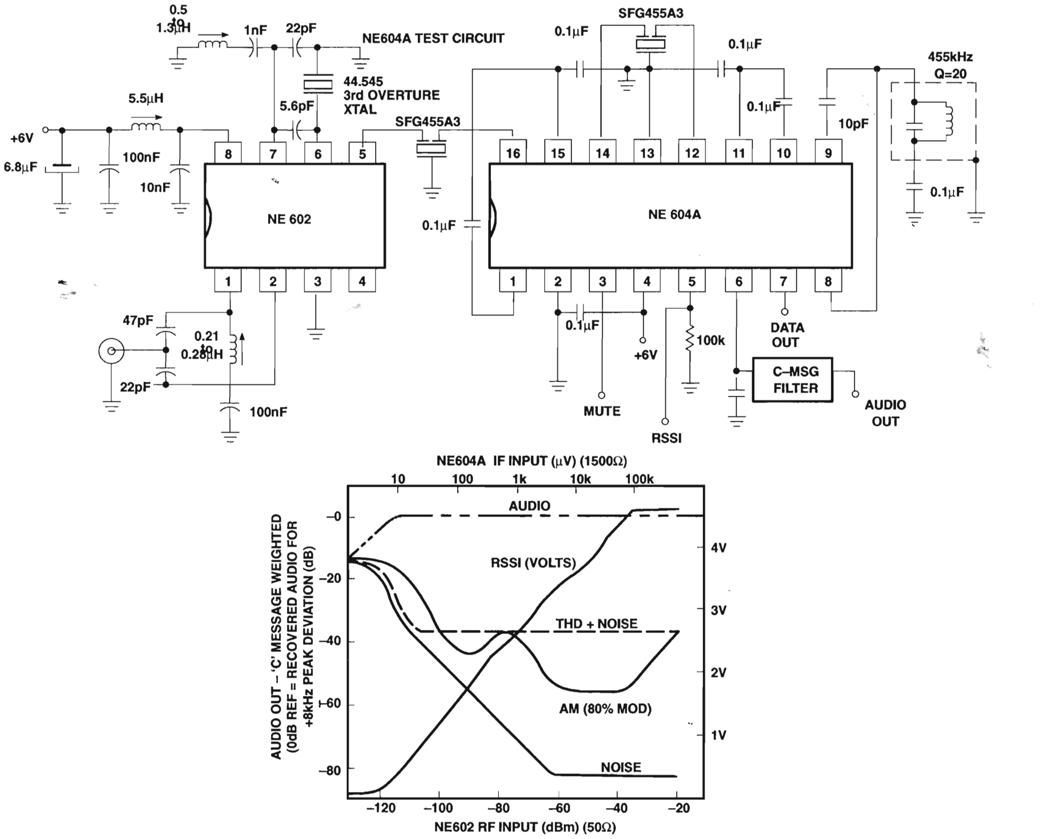


Figure 3. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The NE/SA604A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA604A cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 1. This configuration can be used as the basis for production layout.

The NE/SA604A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with output characteristic). The sub-systems are shown in Figure 2. A typical application with 45MHz input and 455kHz IF is shown in Figure 3.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 2, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 6. Distributed feedback (capacitance, inductance and radiated fields)

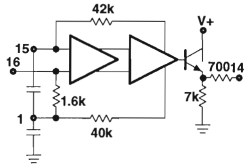


Figure 4. First Limiter Bias

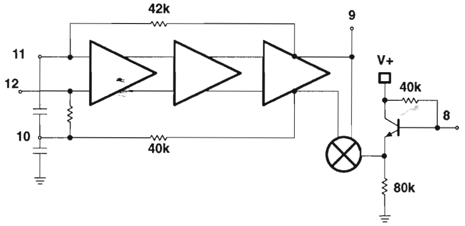


Figure 5. Second Limiter and Quadrature Detector

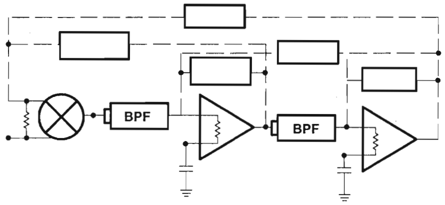
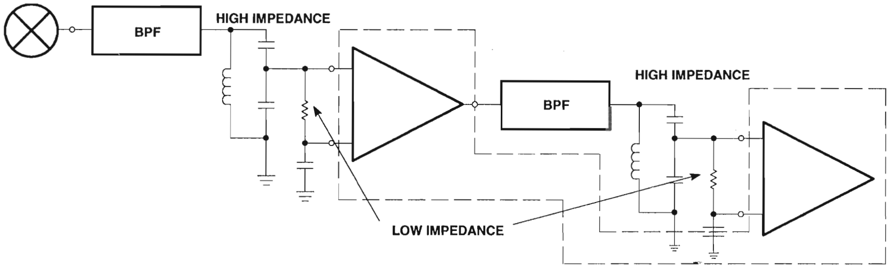
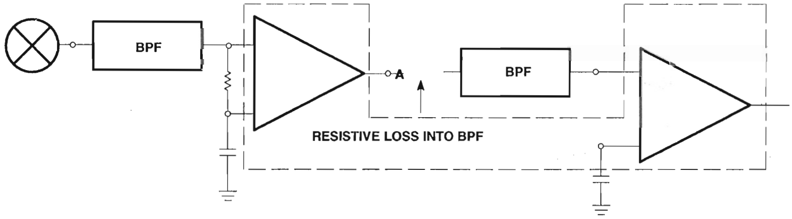


Figure 6. Feedback Paths



7a. Terminating High Impedance Filters with Transformation to Low Impedance



7b. Low Impedance Termination and Gain Reduction

Figure 7. Practical Termination

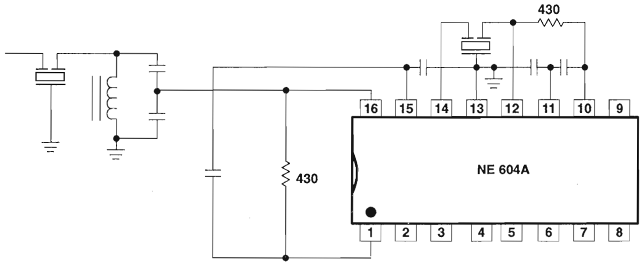


Figure 8. Crystal Input Filter with Ceramic Interstage Filter

forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in Figure 7. Reduced gain will result in reduced limiting sensitivity.

A feature of the NE604A IF amplifiers, which is not specified, is low phase shift. The NE604A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes.

Stability Considerations

The high gain and bandwidth of the NE604A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 1, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1μF monolithic right at the V_{CC} pin, and a 6.8μF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1μF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 1 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 7 demonstrates a practical means.

As illustrated in Figure 8, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 5 shows an equivalent circuit of the NE604A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 10. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

Frequency Discriminator Design Equations for NE604A

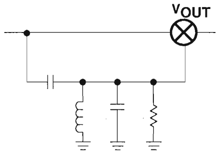


Figure 9.

$$V_O = \frac{C_S}{C_P + C_S} \bullet \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \bullet V_{IN} \qquad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \qquad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \qquad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = t_g^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1-\left(\frac{\omega_1}{\omega}\right)^2}\right] \qquad (2)$$

Figure 10 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right]$ with respect to the V_{IN}.

If $V_{IN} = A \operatorname{Sin} \omega t \Rightarrow V_O = A$ (3)

$$\operatorname{Sin}\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right]$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$V_{IN} \bullet V_O = A^2 \operatorname{Sin} \omega t$ (4)

$$\operatorname{Sin}\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right]$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2} A^2 \operatorname{Cos}\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right] \qquad (5)$$

$$= \frac{1}{2} A^2 \operatorname{Sin}\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1 \frac{\omega}{\omega_1} = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \qquad (6)$$

$$\text{For } \frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5\text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 10) and draw a vertical straight line at

$$\frac{\omega}{\omega_1} = 1.01.$$

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) ⇒ Choose a Q = 20

The internal R of the 604A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174\text{pF}$ and L = 0.7mH.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a C_S = 10pF and C_P = 164pF (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of C_S = 1pF is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Singe the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE604A demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 3) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25µV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22µV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE604A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

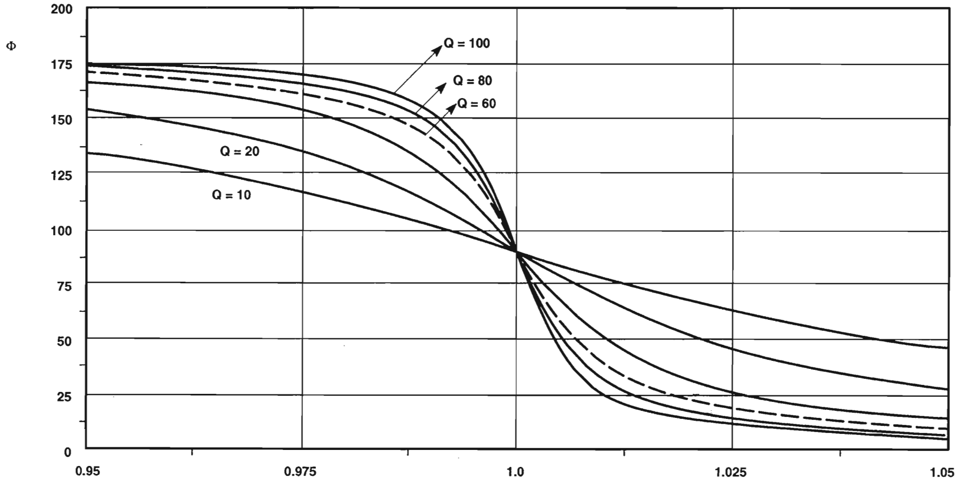


Figure 10. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

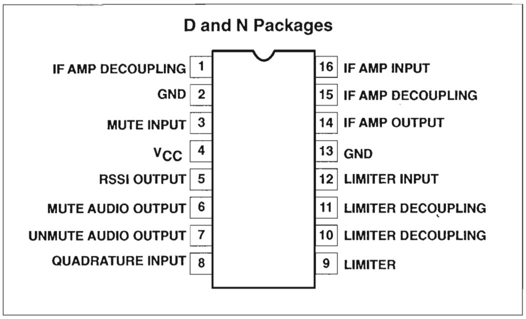
DESCRIPTION

The NE/SA614A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA614A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA614A is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature) package.

FEATURES

- Low power consumption: 3.3mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5µV across input pins (0.22µV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA614A meets cellular radio specifications

PIN CONFIGURATION



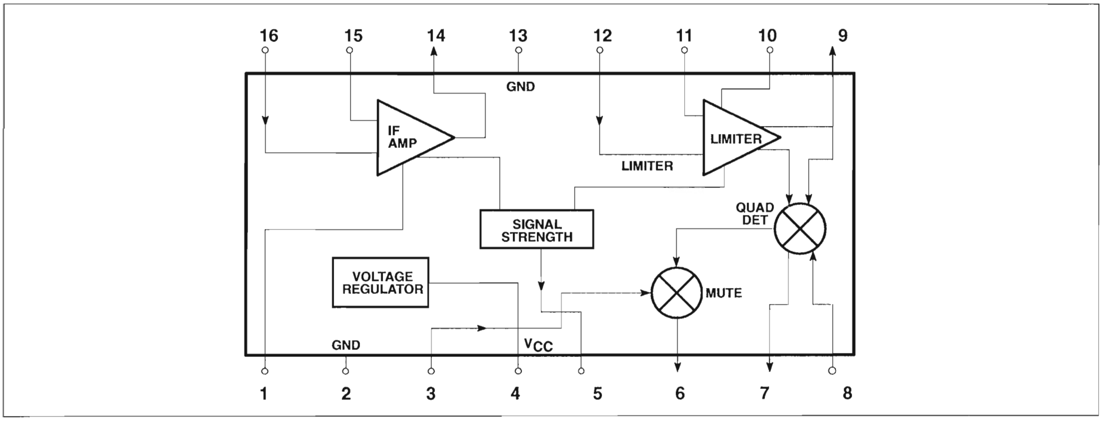
APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE614AN	0406C
16-Pin Plastic Small Outline (SO) package (Surface-mount)	0 to +70°C	NE614AD	0005D
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA614AN	0406C
16-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA614AD	0005D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE614A SA614A	0 to +70 -40 to +85	°C °C
θ_{JA}	Thermal impedance D package N package	90 75	°C/W °C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE614A			SA614A			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		2.5	3.3	4.0	2.5	3.3	4.0	mA
	Mute switch input threshold (ON) (OFF)		1.7		 1.0	1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

Typical reading at $T_A = 25°C$; $V_{CC} = \pm6V$, unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

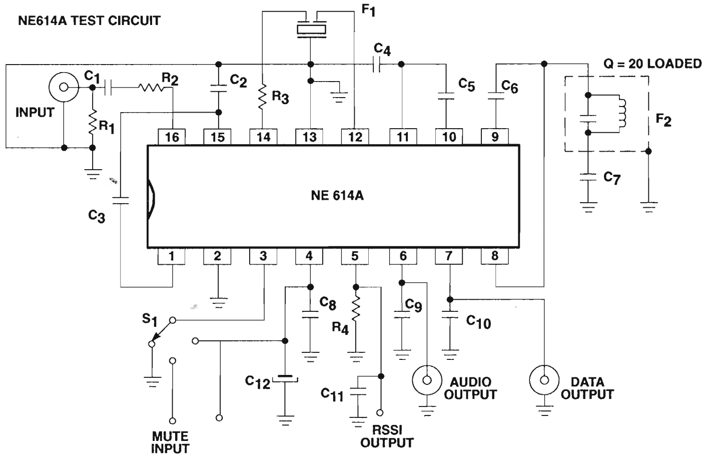
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA614A			
			MIN	TYP	MAX	
	Input limiting -3dB	Test at Pin 16		-92		dBm/50Ω
	AM rejection	80% AM 1kHz	25	33		dB
	Recovered audio level	15nF de-emphasis	60	175	260	mV_{RMS}
	Recovered audio level	150pF de-emphasis		530		mV_{RMS}
THD	Total harmonic distortion		-30	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		68		dB
	RSSI output[1]	RF level = -118dBm	0	160	800	mV
		RF level = -68dBm	1.7	2.50	3.3	V
		RF level = -18dBm	3.6	4.80	5.8	V
	RSSI range	R_4 = 100k (Pin 5)		80		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±2.0		dB
	IF input impedance		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		kΩ
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ

NOTE:

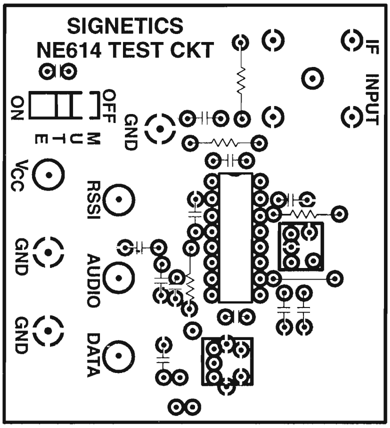
1. NE614A data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

NE614A (50)	NE614A (1.5k)/NE615 (1.5k
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm

The NE615 and NE614A are both derived from the same basic die. The NE615 performance plots are directly applicable to the NE614A.



C1	100nF + 80 – 20% 63V K10000–25V Ceramic
C2	100nF +10% 50V
C3	100nF ±10% 50V
C4	100nF +10% 50V
C5	100nF ±10% 50V
C6	10pF ±2% 100V NPO Ceramic
C7	100nF ±10% 50V
C8	100nF ±10% 50V
C9	15nF ±10% 50V
C10	150pF ±2% 100V N1500 Ceramic
C11	1nF ±10% 100V K2000-Y5P Ceramic
C12	6.8µF ±20% 25V Tantalum
F1	455kHz Ceramic Filter Murata SFG455A3
F2	455kHz (Ce = 180pF) TOKO RMC 2A6597H
R1	51Ω ±1% 1/4W Metal Film
R2	1500Ω ±1% 1/4W Metal Film
R3	1500Ω ±5% 1/8W Carbon Composition
R4	100kΩ ±1% 1/4W Metal Film



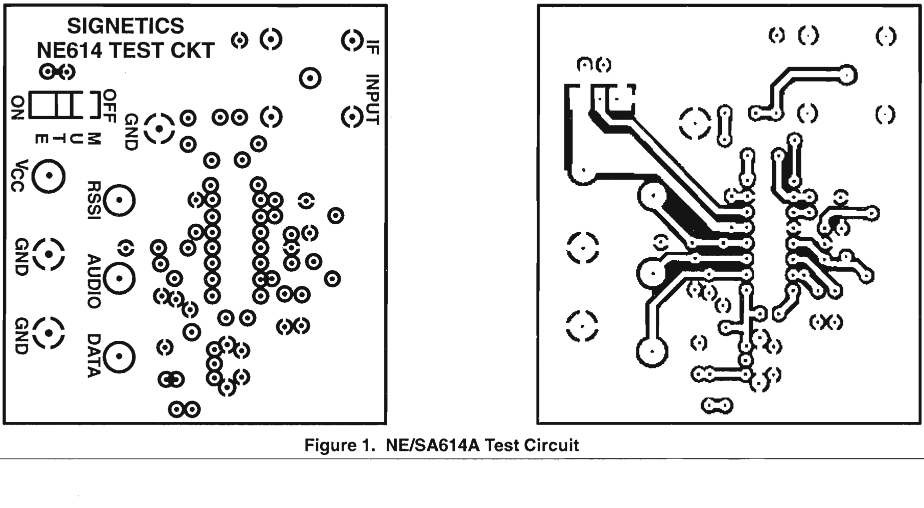


Figure 1. NE/SA614A Test Circuit

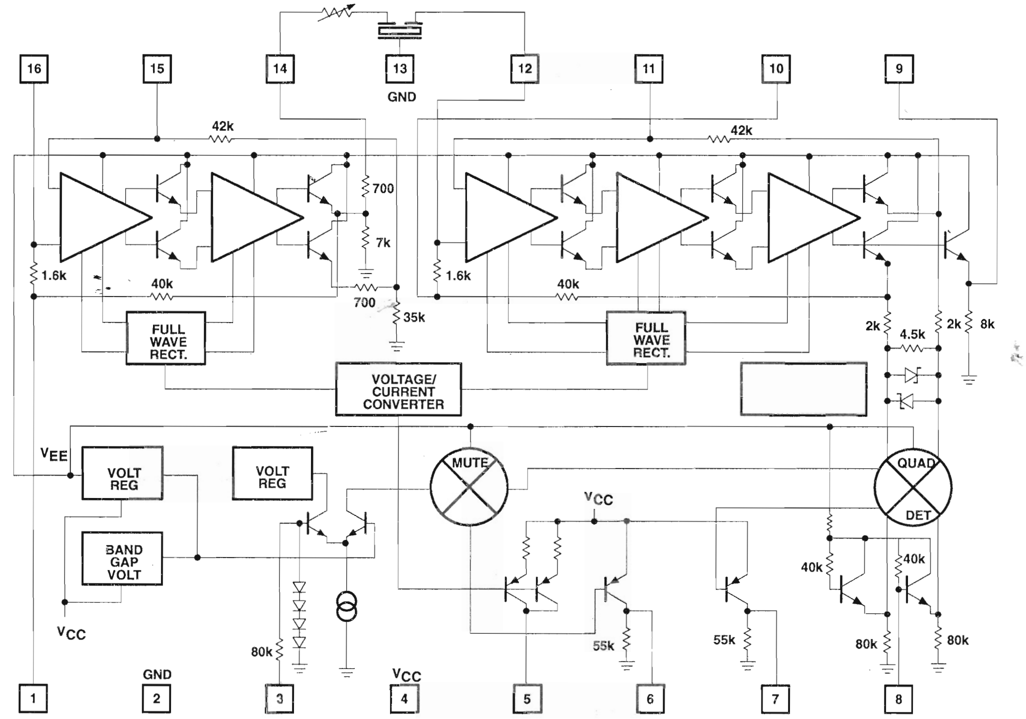


Figure 2. Equivalent Circuit

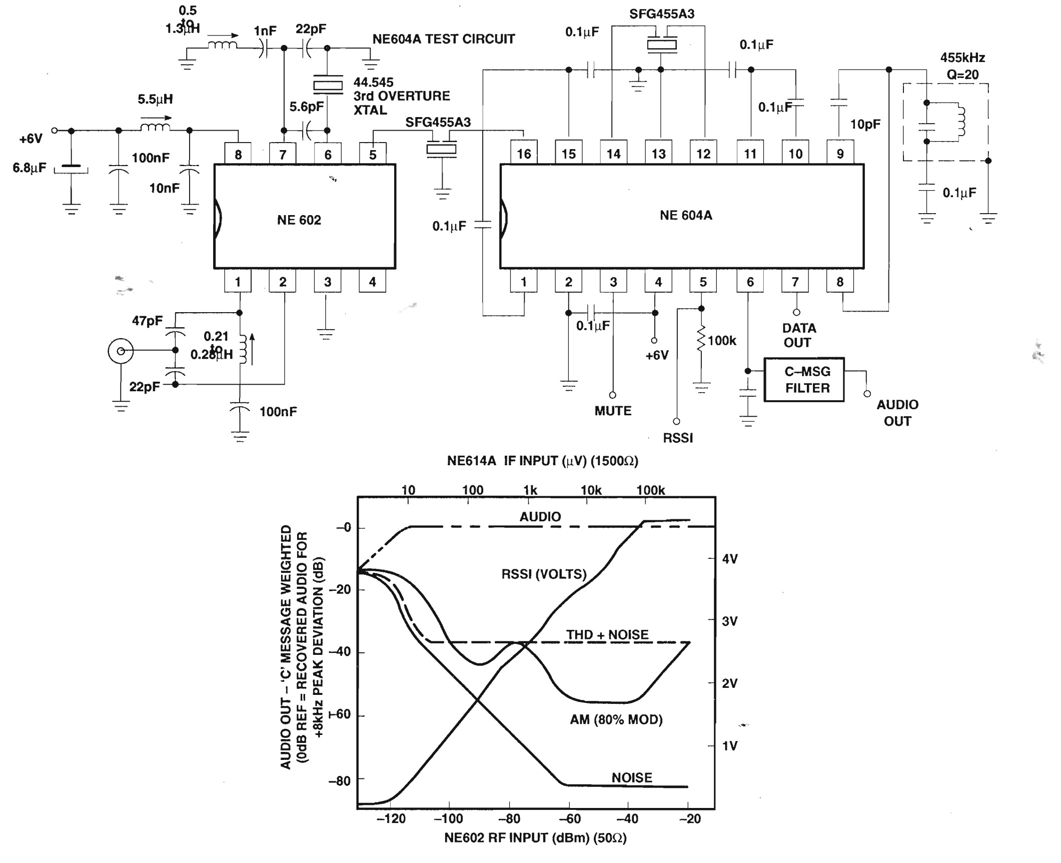


Figure 3. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The NE/SA614A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA614A cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 1. This configuration can be used as the basis for production layout.

The NE/SA614A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with log output characteristic). The sub-systems are shown in Figure 2. A typical application with 45MHz input and 455kHz IF is shown in Figure 3.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 2, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

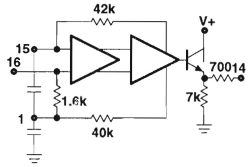


Figure 4. First Limiter Bias

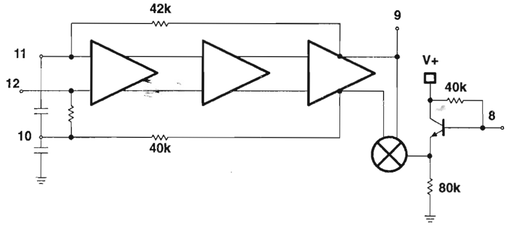


Figure 5. Second Limiter and Quadrature Detector

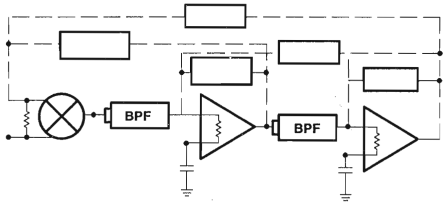
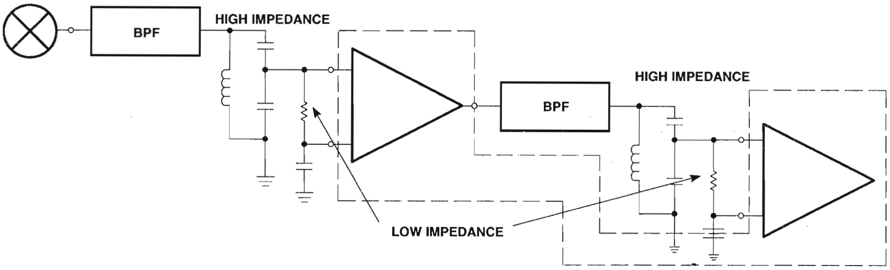
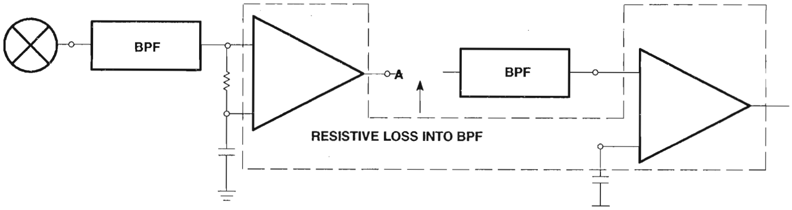


Figure 6. Feedback Paths



7a. Terminating High Impedance Filters with Transformation to Low Impedance



7b. Low Impedance Termination and Gain Reduction

Figure 7. Practical Termination

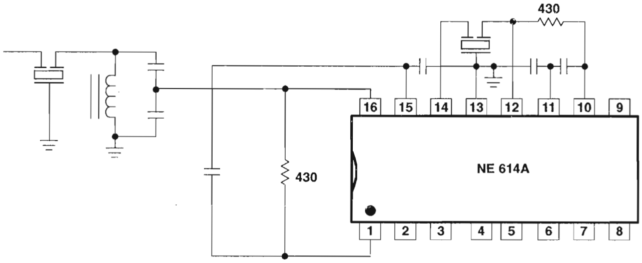


Figure 8. Crystal Input Filter with Ceramic Interstage Filter

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 6. Distributed feedback (capacitance, inductance and radiated fields) forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in Figure 7. Reduced gain will result in reduced limiting sensitivity.

A feature of the NE614A IF amplifiers, which is not specified, is low phase shift. The NE614A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes.

Stability Considerations

The high gain and bandwidth of the NE614A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 1, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1μF monolithic right at the V_{CC} pin, and a 6.8μF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1μF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 1 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 7 demonstrates a practical means.

As illustrated in Figure 8, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 5 shows an equivalent circuit of the NE614A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 10. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

Frequency Discriminator Design Equations for NE614A

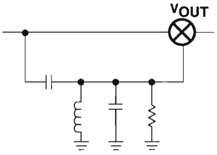


Figure 9.

$$V_O = \frac{C_S}{C_P + C_S} \bullet \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \bullet V_{IN} \qquad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \qquad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \qquad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = tg^{-1}\left[\frac{\frac{\omega_1}{Q_1 \omega}}{1 - \left(\frac{\omega_1}{\omega}\right)^2}\right] \qquad (2)$$

Figure 10 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right]$ with respect to the V_{IN}.

$$\text{If } V_{IN} = A \sin \omega t \Rightarrow V_O = A \sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right] \qquad (3)$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$$V_{IN} \bullet V_O = A^2 \sin \omega t \sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right] \qquad (4)$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2} A^2 \cos\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right] = \frac{1}{2} A^2 \sin\left(\frac{2Q_1}{\omega_1}\right)\omega \qquad (5)$$

$$V_{OUT} \propto 2Q_1 \frac{\omega}{\omega_1} = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \qquad (6)$$

$$\text{For } \frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5\text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 10) and draw a vertical straight line at

$$\frac{\omega}{\omega_1} = 1.01.$$

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) ⇒ Choose a Q = 20

The internal R of the 614A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S$ = 174pF and L = 0.7mH.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a C_S = 10pF and C_P = 164pF (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of C_S = 1pF is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Singe the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE614A demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 3) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE614A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

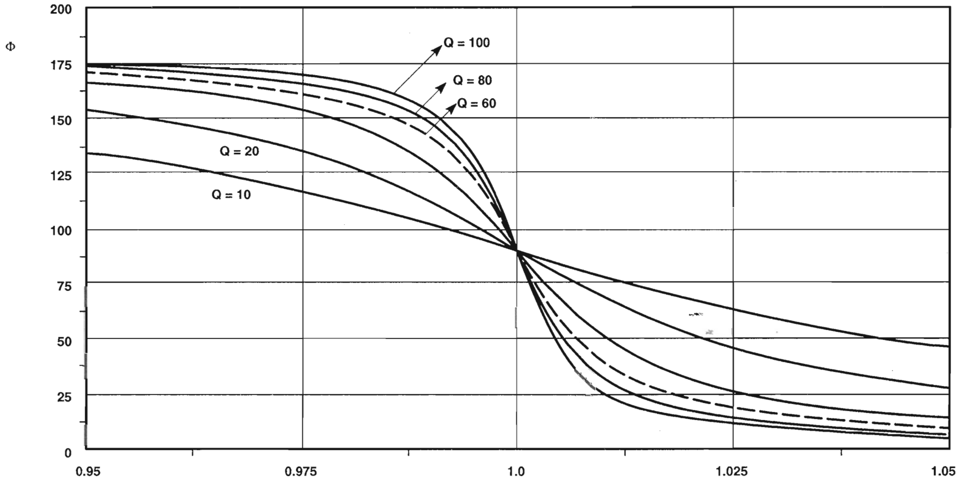


Figure 10. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_I} = 1 + \frac{\Delta\omega}{\omega_I}$

Audio decibel level detector with meter driver

AN1991

Author: Robert J. Zavrel Jr.

DESCRIPTION

Although the NE604 was designed as an RF device intended for the cellular radio market, it has features which permit other design configurations. One of these features is the Received Signal Strength Indicator (RSSI). In a cellular radio, this function is necessary for continuous monitoring of the received signal strength by the radio's microcomputer. This circuit provides a logarithmic response proportional to the input signal level. The NE604 can provide this logarithmic response over an 80dB range up to a 15MHz operating frequency. This paper describes a technique which optimizes this useful function within the audio band.

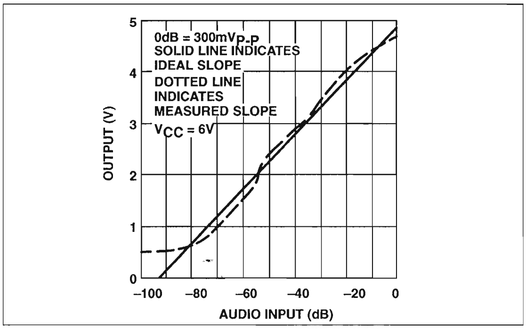
A sensitive audio level indicator circuit can be constructed using two integrated circuits: the NE604 and NE532. This circuit draws very little power (less than 5mA with a single 6V power supply) making it ideal for portable battery operated equipment. The small size and low-power consumption belie the 80dB dynamic range and 10.5µV sensitivity.

The RSSI function requires a DC output voltage which is proportional to the $\log_{10}$ of the input signal level. Thus a standard 0-5 voltmeter can be linearly calibrated in decibels over a single 80dB range. The entire circuit is composed of 9 capacitors and two resistors along with the two ICs. No tuning or calibration is required in a manufacturing setting.

The Audio Input vs Output Graph shows that the circuit is within 1.5dB tolerance over the 80dB range for audio frequencies from 100Hz to 10kHz. Higher audio levels can be measured by placing an attenuator ahead of the input capacitor. The input impedance is high (about 50k), so lower impedance terminations (50 or 600Ω) will not be affected by the input impedance. If very accurate tracking is required (<0.5dB accuracy), a 40 or 50dB segment can be "selected". A range switch can then be added with appropriate attenuators if more than 40 or 50dB dynamic range is required.

There are two amplifier sections in the 604 with 2 and 3 stages in the first and second sections respectively. Each stage outputs a sample current to a summing circuit. The summing circuit has a current mirror which appears at Pin 5. This current is proportional to the $\log_{10}$ of the input audio signal. A voltage is dropped across the 100k resistor by the current, and a 0.1µF capacitor is used to bypass and filter the output signal. The 532 op amp is used as a buffer and meter driver, although a digital voltmeter could replace both the op amp and the meter shown. The rest of the capacitors are used for power supply and amplifier input bypassing.

The RC circuit between Pins 14 and 12 forms a low-pass filter which can be adjusted by changing the value of C1. Raising the capacitance will lower the cut-off frequency and also lower the zero signal output resting voltage (about 0.6V). Lowering the capacitance value will have the opposite effect with some reduction in dynamic range, but will raise the frequency response. The 2kΩ resistor value provides the near-ideal inter-stage loss for maximum RSSI linearity. C2 can also be changed. The trade-off here is between output damping and ripple. Most analog and digital metering methods will tend to cancel the effects of small or moderate ripple voltages through integration, but high ripple voltages should be avoided.



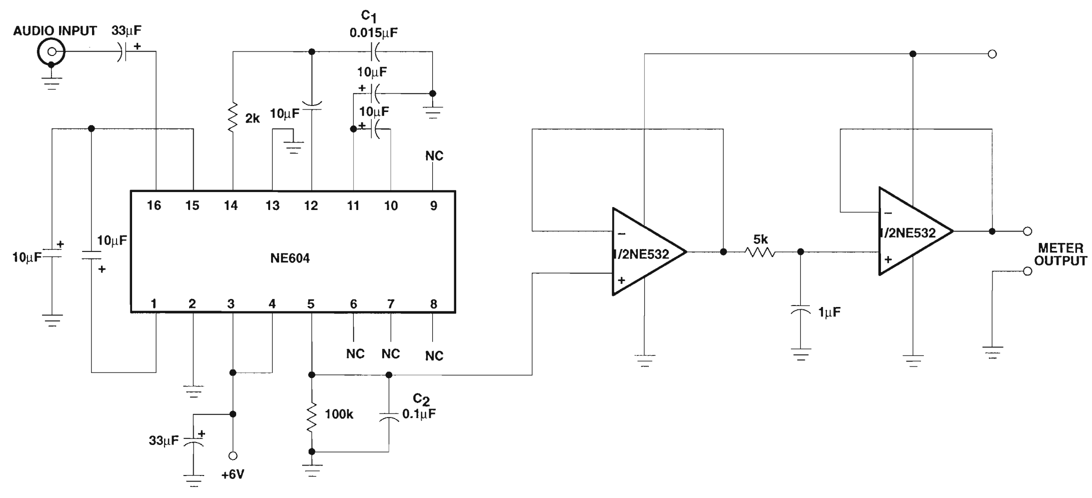


Figure 1.

A second op amp is used with an optional second filter. This filter has the advantage of a low impedance signal source by virtue of the first op amp. Again, a trade-off exists between meter damping and ripple attenuation. If very low ripple and low damping are both required, a more complex active low-pass filter should be constructed.

Some applications of this circuit might include:

1. Portable acoustic analyzer
2. Microphone tester
3. Audio spectrum analyzer
4. VU meters
5. S-meter for direct conversion radio receiver
6. Audio dynamic range testers
7. Audio analyzers (THD, noise, separation, response, etc.)

High sensitivity applications of low-power RF/IF integrated circuits

AN1993

ABSTRACT

This paper discusses four high sensitivity receivers and IF (Intermediate Frequency) strips which utilize intermediate frequencies of 10.7MHz or greater. Each circuit utilizes a low-power VHF mixer and high-performance low-power IF strip. The circuit configurations are

1. 45 or 49MHz to 10.7MHz narrowband,
2. 90MHz to 21.4MHz narrowband,
3. 100MHz to 10.7MHz wideband, and
4. 152.2MHz to 10.7MHz narrowband.

Each circuit is presented with an explanation of component selection criteria, (to permit adaptation to other frequencies and bandwidths). Optional configurations for local oscillators and data demodulators are summarized.

INTRODUCTION

Traditionally, the use of 10.7MHz as an intermediate frequency has been an attractive means to accomplish reasonable image rejection in VHF/UHF receivers. However, applying significant gain at a high IF has required extensive gain stage isolation to avoid instability and very high current consumption to get adequate amplifier gain bandwidth. By enlightened application of two relatively new low power ICs, Signetics NE602 and NE604A, it is possible to build highly producible IF strips and receivers with input frequencies to several hundred megahertz, IF frequencies of 10.7 or 21.4MHz, and sensitivity less than 2µV (in many cases less than 1µV). The Signetics new NE605 combines the function of the NE602 and the NE604A. All of the circuits described in this paper can also be implemented with the NE605. The NE602 andNE604A were utilized for this paper to permit optimum gain stage isolation and filter location.

THE BASICS

First let's look at why it is relevant to use a 10.7 or 21.4MHz intermediate frequency. 455kHz ceramic filters offer good selectivity and small size at a low price. Why use a higher IF? The fundamental premise for the answer to this question is that the receiver architecture is a hetrodyne type as shown in Figure 1.

A pre-selector (bandpass in this case) precedes a mixer and local oscillator. An IF filter follows the mixer. The IF filter is only supposed to pass the difference (or sum) of the local oscillator (LO) frequency and the preselector frequency.

The reality is that there are always two frequencies which can combine with the LO: The pre-selector frequency and the "image" frequency. Figure 2 shows two hypothetical pre-selection curves. Both have 3dB bandwidths of 2MHz. This type of pre-selection is typical of consumer products such as cordless telephone and FM radio. Figure 2A shows the attenuation of a low side image with 10.7MHz. Figure 2B shows the very limited attenuation of the low side 455kHz image.

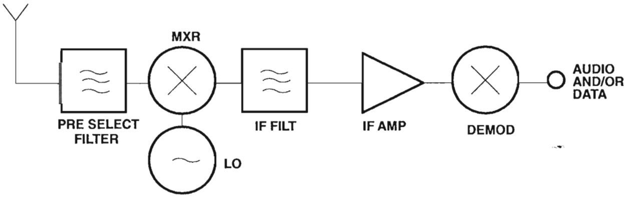


Figure 1. Basic Hetrodyne Receiver

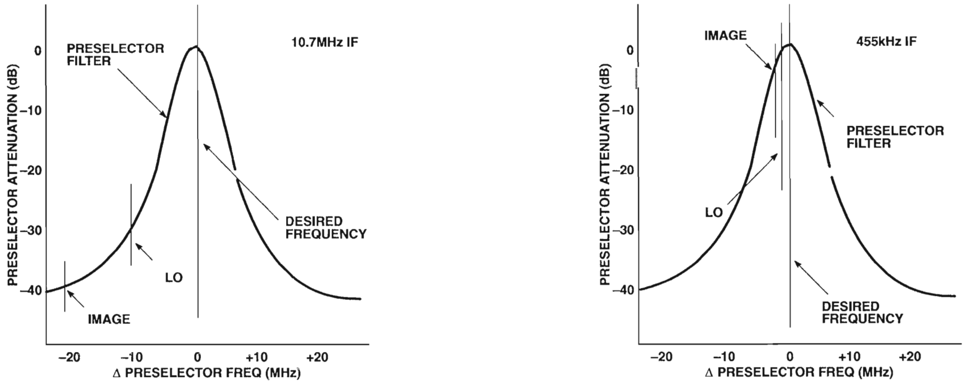


Figure 2. Effects of Preselection on Images

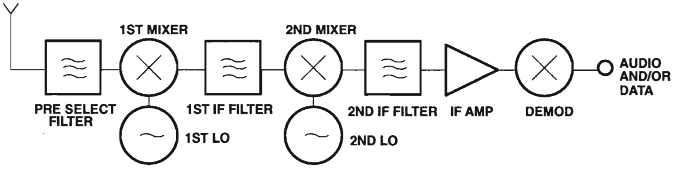


Figure 3. Dual Conversion

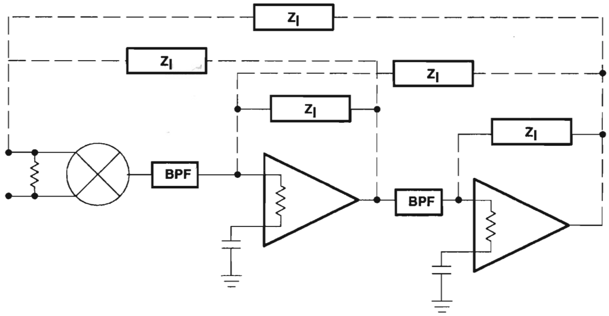


Figure 4. Feedback Paths

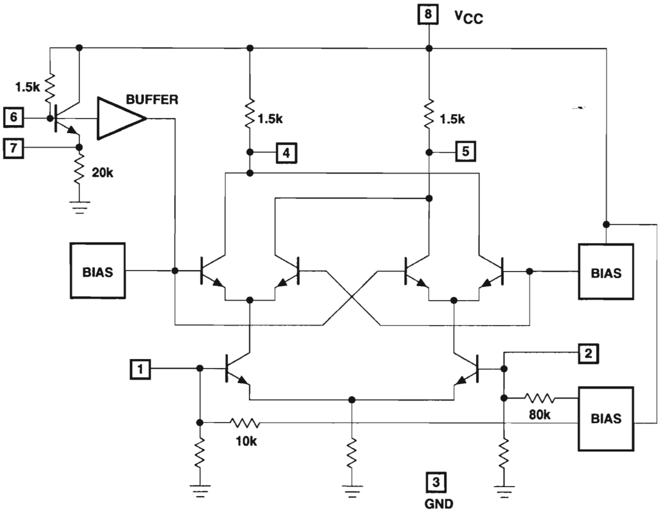


Figure 5. NE602 Equivalent Circuit

If the single conversion architecture of Figure 1 were implemented with a 455kHz IF, any interfering image would be received almost as well as the desired frequency. For this reason, dual conversion, as shown in Figure 3, has been popular.

In the application of Figure 3, the first IF must be high enough to permit the pre-selector to reject the images of the first mixer and must have a narrow enough bandwidth that the second mixer images and the intermod products due to the first mixer can be attenuated. There's more to it than that, but those are the basics. The multiple conversion hetrodyne works well, but, as Figure 3 suggests, compared to Figure 2 it is more complicated. Why, then, don't we use the approach of Figure 2?

THE PROBLEM

Historically there has been a problem: Stability! Commercially available integrated IF amplifiers have been limited to about 60dB of gain. Higher discrete gain was possible if each stage was carefully shielded and bypassed, but this can become a nightmare on a production line. With so little IF gain available, in order to receive signals of less than 10μV it was necessary to add RF gain and this, in turn, meant that the mixer must have good large signal handling capability. The RF gain added expense, the high level mixer added expense, both added to the potential for instabilities, so the multiple conversion started looking good again.

But why is instability such a problem in a high gain high IF strip? There are three basic mechanisms. First, ground and the supply line are potentially feedback mechanisms from stage-to-stage in any amplifier. Second, output pins and external components create fields which radiate back to inputs. Third, layout capacitances become feedback mechanisms. Figure 4 shows the fields and capacitances symbolically.

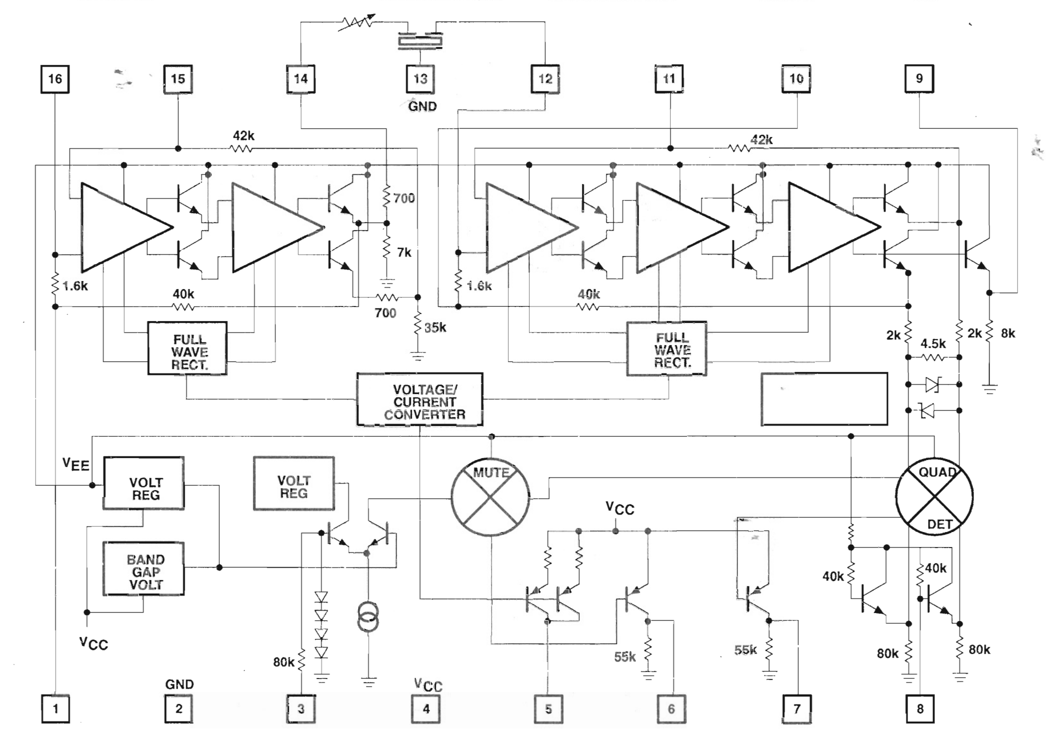


Figure 6. NE604A Equivalent Circuit

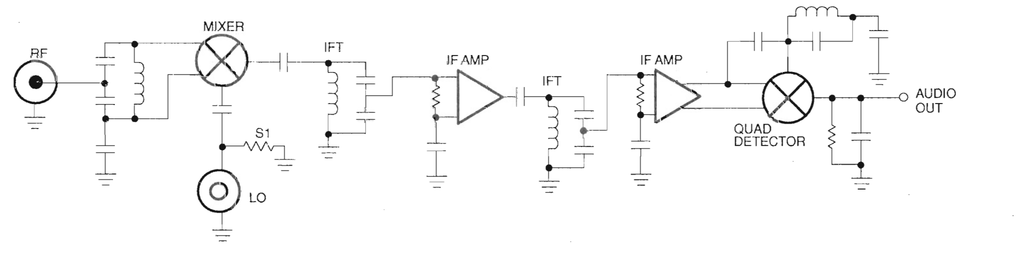


Figure 7. Symbolic Circuit

If Z_F represents the impedance associated with the circuit feedback mechanisms (stray capacitances, inductances and radiated fields), and Z_{IN} is the equivalent input impedance, a divider is created. This divider must have an attenuation factor greater than the gain of the amplifier if the amplifier is to remain stable.

- If gain is increased, the input-to-output isolation factor must be increased.
- As the frequency of the signal or amplifier bandwidth increases, the impedance of the layout capacitance decreases thereby reducing the attenuation factor.

The layout capacitance is only part of the issue. In order for traditional 10.7MHz IF amplifiers to operate with reasonable gain bandwidth, the amount of current in the amplifiers needed to be quite high. The CA3089 operates with 25mA of typical quiescent current. Any currents which are not perfectly differential must be carefully bypassed to ground. The higher the current, the more difficult the challenge. And limiter outputs and quadrature components make excellent field generators which add to the feedback scenario. The higher the current, the larger the field.

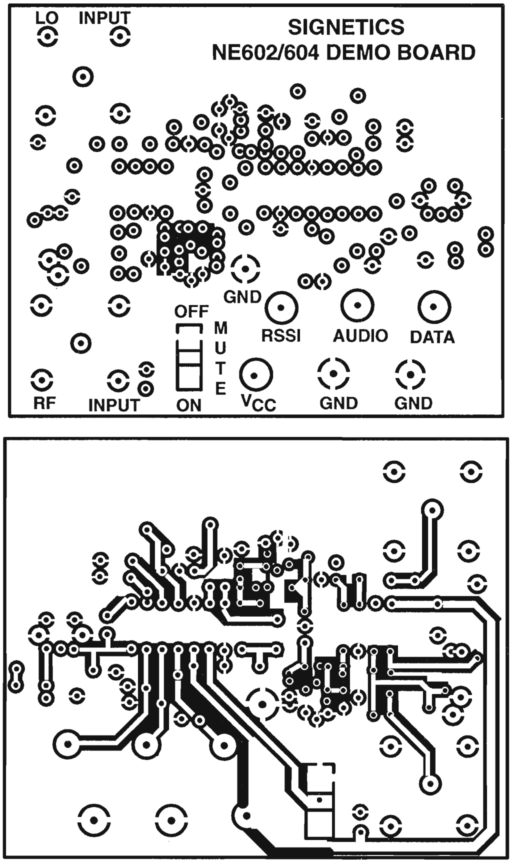


Figure 8. Circuit Board Layout

THE SOLUTION

The NE602 is a double balanced mixer suitable for input frequencies in excess of 500MHz. It draws 2.5mA of current. The NE604A is an IF strip with over 100dB of gain and a 25MHz small signal bandwidth. It draws 3.5mA of current. The circuits in this paper will demonstrate ways to take advantage of this low current and 75dB or more of the NE604A gain in receivers and IF strips that would not be possible with traditional integrated circuits. No special tricks are used, only good layout, impedance planning and gain distribution.

THE MIXER

The NE602 is a low power VHF mixer with built-in oscillator. The equivalent circuit is shown in Figure 5. The basic attributes of this mixer include conversion gain to frequencies greater than 500MHz, a noise figure of 4.6dB @ 45MHz, and a built-in oscillator which can be used up to 200MHz. LO can be injected.

For best performance with any mixer, the interface must be correct. The input impedance of the NE602 is high, typically 3kΩ in parallel with 3pF. This is not an easy match from 50Ω. In each of the examples which follow, an equivalent 50:1.5k match was used. This compromise of noise, loss, and match yielded good results. It can be improved upon. Match to crystal filters will require special attention, but will not be given focus in this paper.

This oscillator is a single transistor with an internal emitter follower driving the mixer. For best mixer performance, the LO level needs to be approximately 220mV$_{RMS}$ at the base of the oscillator transistor (Pin 6). A number of oscillator configurations are presented at the end of this paper. In each of the prototypes for this paper, the LO source was a signal generator. Thus, a 51Ω resistor was used to terminate the signal generator. The LO is then coupled to the mixer through a DC blocking capacitor. The signal generator is set for 0dBm. The impedance at the LO input (Pin 6) is approximately 20kΩ. Thus, required power is very low, but 0dBm across 51Ω does provide the necessary 220mV$_{RMS}$.

The outputs of the NE602 are loaded with 1.5kΩ internal resistors. This makes interface to 455kHz ceramic filters very easy. Other filter types will be addressed in the examples.

THE IF STRIP

The basic functions of the NE604A are ordinary at first glance: Limiting IF, quadrature detector, signal strength meter, and mute switch. **However, the performance of each of these blocks is superb.** The IF has 100dB of gain and 25MHz bandwidth. This feature will be exploited in the examples. The signal strength indicator has a 90dB log output characteristic with very good linearity. There are two audio outputs with greater than 300kHz bandwidth (one can be muted greater than 70dB). The total supply current is typically 3.5mA. This is the other factor which permits high gain and high IF.

Figure 6 shows an equivalent circuit of the NE604A. Each of the IF amplifiers has a 1.6kΩ input impedance. The input impedance is achieved by splitting a DC feedback bias resistor. The input impedance will be manipulated in each of the examples to aid stability.

BASIC CONSIDERATIONS

In each of the circuits presented, a common layout and system methodology is used. The basic circuit is shown symbolically in Figure 7.

At the input, a frequency selective transformation from 50Ω to 1.5kΩ permits analysis of the circuit with an RF signal generator. A second generator provides LO. This generator second generator provides

LO. This generator is terminated with a 51Ω resistor. The output of the mixer and the input of the first limiter are both high impedance (1.5Ω nominal). As indicated previously, the input impedance of the limiter must be low enough to attenuate feedback signals. So, the input impedance of the first limiter is modified with an external resistor. In most of the examples, a 430Ω external resistor was used to create a 330Ω input impedance (430//1.5kΩ). The first IF filter is thus designed to present 1.5kΩ to the mixer and 330Ω to the first limiter.

The same basic treatment was used between the first and second limiters. However, in each of the 10.7MHz examples, this interstage filter is not an L/C tank; it is a ceramic filter. This will be explained in the first example.

After the second limiter, a conventional quadrature detector demodulates the FM or FSK information from the carrier and a simple low pass filter completes the demodulation process at the audio outputs.

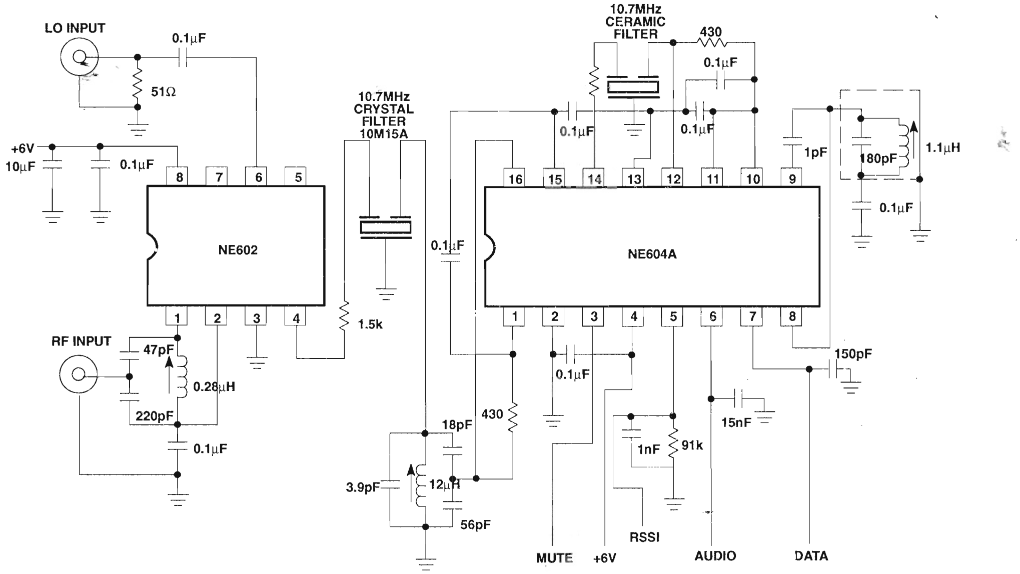


Figure 9. NE602/604A Demonstration Circuit with RF Input of 45MHz and IF of 10.7MHz ±7.5kHz

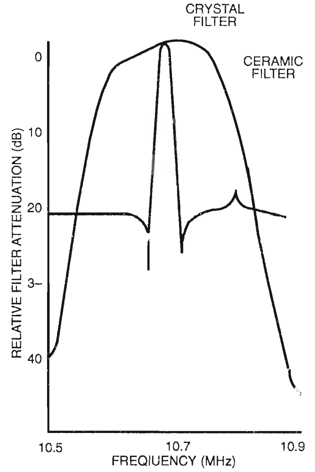
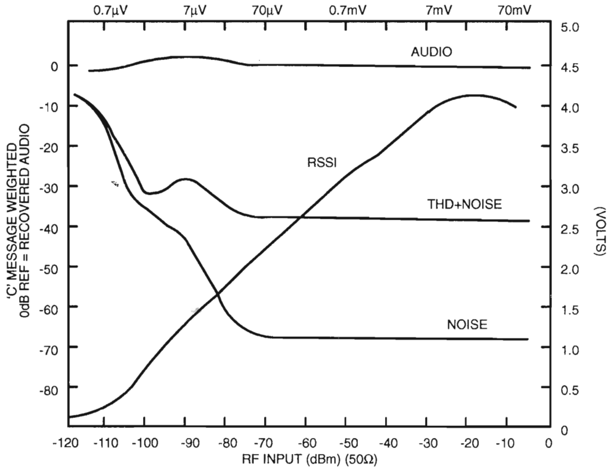


Figure 10. Passband Relationship



- **45MHz RF input**
- **55.7MHz LO (odBm)**
- **10.7MHz IF**
- **15kHz IF BW**
- **7kHz deviation**

Figure 11. VHF or UHF 2nd Conversion (Narrow Band)

As mentioned, a single layout was used for each of the examples. The board artwork is shown in Figure 8. Special attention was given to: (1) Creating a maximum amount of ground plane with connection of the component side and solder side ground at locations all over the board; (2) careful attention was given to keeping a ground ring around each of the gain stages. The objective was to provide a shunt path to ground for any stray signal which might feed back to an input; (3) leads were kept short and relatively

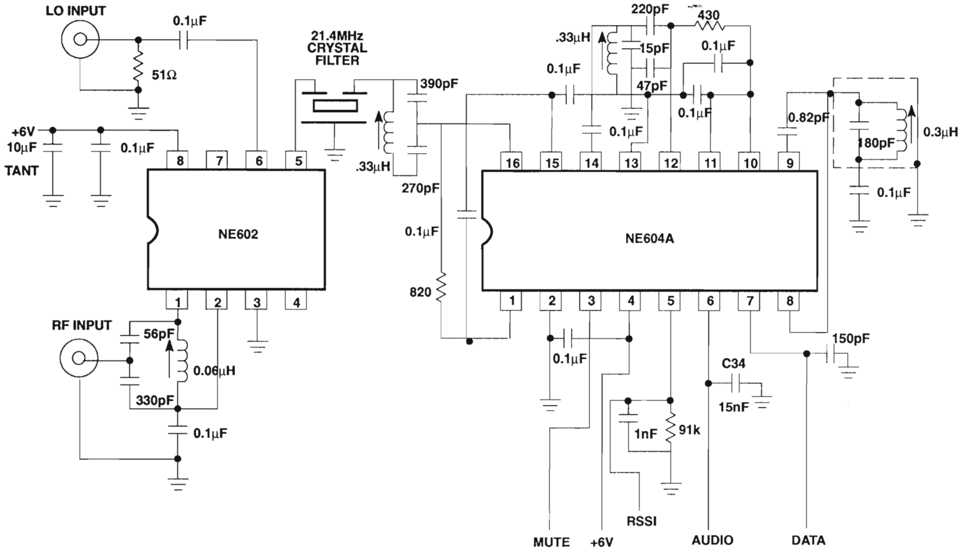
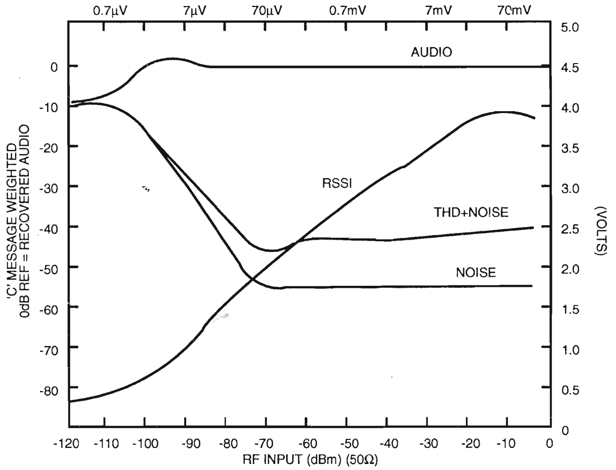


Figure 12. NE602/604A Demonstration Circuit with RF Input of 90MHz and IF of 21.4MHz ±7.5kHz



- **90MHz RF input**
- **68.6MHz LO**
  (odBm)

- **21.4MHz IF**
- **15kHz IF BW**
- **7kHz deviation**

Figure 13. UHF Second Conversion (Narrow Band) or VHF Single Conversion (Narrow Band)

wide to minimize the potential for them to radiate or pick up stray signals; finally (and very important), (4) RF bypass was done as close as possible to supply pins and inputs, with a good (10µF) tantalum capacitor completing the system bypass.

EXAMPLE: 45MHZ TO 10.7MHZ NARROWBAND

As a first example, consider conversion from 45MHz to 10.7MHz. There are commercially available filters for both frequencies so this is a realistic combination for a second IF in a UHF receiver. This circuit can also be applied to cordless telephone or short range communications at 46 or 49MHz. The circuit is shown in Figure 9.

The 10.7MHz filter chosen is a type commonly available for 25kHz channel spacing. It has a 3dB bandwidth of 15kHz and a termination requirement of 3kΩ/2pF. To present 3kΩ to the input side of the filter, a 1.5kΩ resistor was used between the NE602 output (which has a 1.5kΩ impedance) and the filter. Layout capacitance was close enough to 2pF that no adjustment was necessary. This series-resistance approach introduces an insertion loss which degrades the sensitivity, but it has the benefit of simplicity.

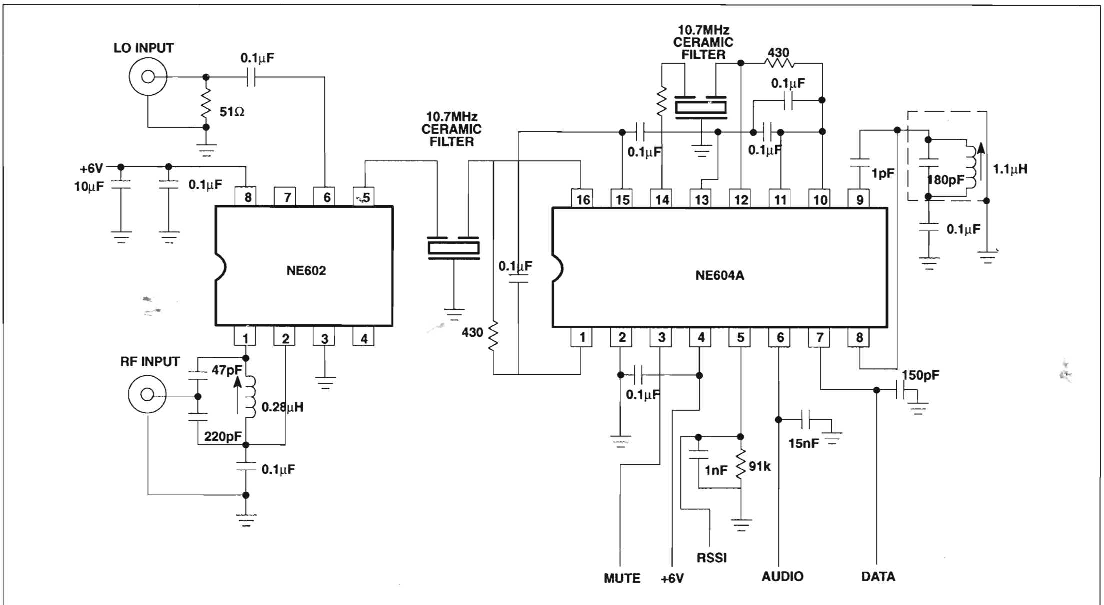


Figure 14. NE602/604A Demonstration Circuit with RF Input of ~100MHz and IF of 10.7MHz ±140kHz

The secondary side of the crystal filter is terminated with a 10.7MHz tuned tank. The capacitor of the tank is tapped to create a transformer with the ratio for 3k:330. With the addition of the 430Ω resistor in parallel with the NE604A 1.6kΩ internal input resistor, the correct component of resistive termination is presented to the crystal filter. The inductor of the tuned load is adjusted off resonance enough to provide the 2pF capacitance needed. (Actual means of adjustment was for best audio during alignment).

If appropriate or necessary for sensitivity, the same type of tuned termination used for the secondary side of the crystal filter can also be used between the NE602 and the filter. If this is desired, the capacitors should be ratioed for 1.5k:3k. Alignment is more complex with tuned termination on both sides of the filter. This approach is demonstrated in the fourth example.

A ceramic filter is used between the first and second limiters. It is directly connected between the output of the first limiter and the input of the second limiter. Ceramic filters act much like ceramic capacitors, so direct connection between two circuit nodes with different DC levels is acceptable. At the input to the second limiter, the impedance is again reduced by the addition of a 430Ω external resistor in parallel with the internal 1.6kΩ input load resistor. This presents the 330Ω termination to the ceramic filter which the manufacturers recommend.

On the input side of the ceramic filter, no attempt was made to create a match. The output impedance of the first limiter is nominally 1kΩ. Crystal filters are tremendously sensitive to correct match. Ceramic filters are relatively forgiving. A review of the manufacturers' data shows that the attenuation factor in the passband is affected with improper match, but the degree of change is small and the passband stays centered. Since the principal selectivity for this application is from the crystal filter at the input of the first limiter, the interstage ceramic filter only has to suppress wideband noise. The first filter's passband is right in the center of the ceramic filter passband. (The crystal filter passband is less than 10% of the ceramic filter passband). This passband relationship is illustrated in Figure 10.

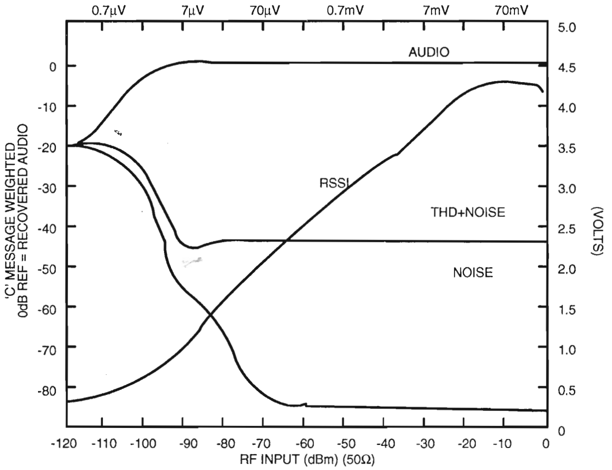
After the second limiter, demodulation is accomplished in the quadrature detector. Quadrature criteria is not the topic of this paper, but it is noteworthy that the choice of loaded Q will affect performance. The NE604A is specified at 455kHz using a quadrature capacitor of 10pF and a tuning capacitor of 180pF. (180pF gives a loaded Q of 20 at 455kHz). A careful look at the quadrature equations (Ref 3.) suggests that at 10.7MHz a value of about 1pF should be substituted for the 10pF at 455kHz.

The performance of this circuit is presented in Figure 11. The –12dB SINAD (ratio of Signal to Noise And Distortion) was achieved with a 0.6µV input.

EXAMPLE: 90MHZ TO 21.4MHZ NARROWBAND

This second example, like the first, used two frequencies which could represent the intermediate frequencies of a UHF receiver. This circuit can also be applied to VHF single conversion receivers if the sensitivity is appropriate. The circuit is shown in Figure 12.

Most of the fundamentals are the same as explained in the first example. The 21.4MHz crystal filter has a 1.5kΩ/2pF termination requirement so direct connection to the output of the NE602 is possible. With strays there is probably more than 2pF in this circuit, but the performance is good nonetheless. The output of the crystal filter is terminated with a tuned impedance-step-down transformer as in the previous example. Interstage filtering is accomplished with a 1kΩ:330 step-down ratio. (Remember, the output of the first limiter is 1kΩ and a 430Ω resistor has been added to make the second limiter input 330Ω). A DC blocking capacitor is needed from the output of the first limiter. The board was not laid out for an interstage transformer, so an "XACTO" knife was used to make some minor mods. Figure 13 shows the performance. The +12dB SINAD was with 1.6µV input.



- **94.7MHz RF input**
- **84MHz LO (odBm)**
- **10.7MHz IF**
- **280kHz IF BW**
- **75kHz deviation**

Figure 15. FM Broadcast Receiver (Wide Band)

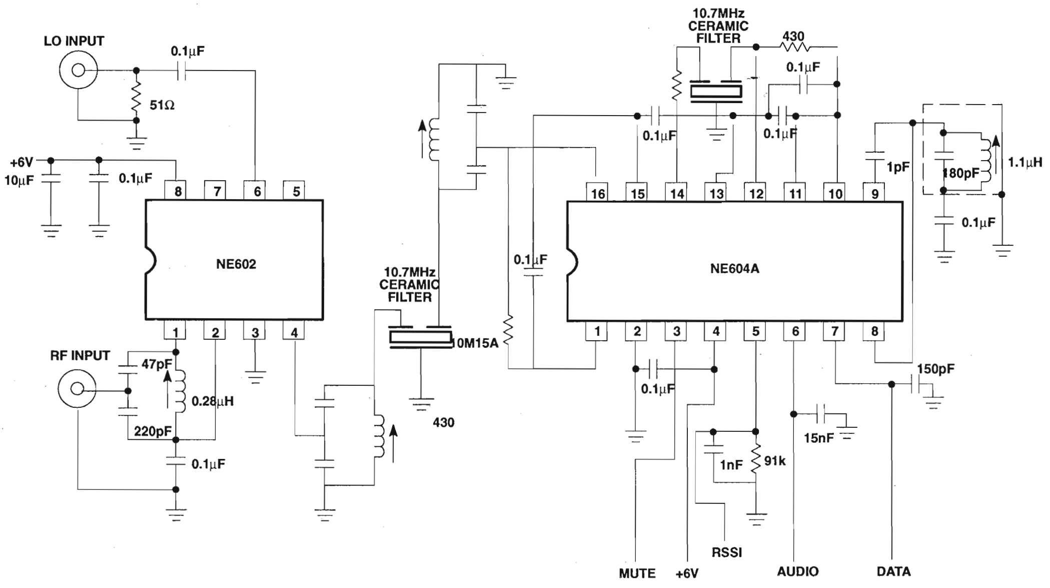
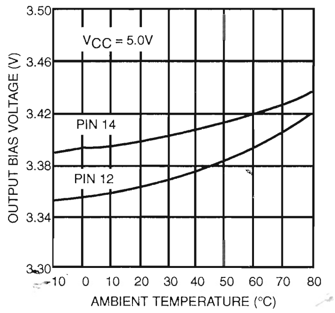


Figure 16. NE602/604A Demonstration Circuit with RF Input of 152.2MHz and IF of 10.7MHz ±7.5kHz



- 152.2MHz RF input
- 141.5MHz LO (odBm)
- 10.7MHz IF
- 15kHz IF BW
- 7kHz deviation

Figure 17. VHF Single Conversion (Narrow Band)

EXAMPLE: 100MHZ TO 10.7MHZ WIDEBAND

This example represents three possible applications: (1) low cost, sensitive FM broadcast receivers, (2) SCA (Subsidiary Communications Authorization) receivers and (3) data receivers. The circuit schematic is shown in Figure 14. While this example has the greatest diversity of application, it is also the simplest. Two 10.7MHz ceramic filters were used. The first was directly connected to the output of the NE602. The second was directly connected to the output of the first IF limiter. The secondary sides of both filters were terminated with 330Ω as in the two previous examples. While the filter bandpass skew of this simple single conversion receiver might not be tolerable in some applications, to a first order the results are excellent. (Please note that sensitivity is measured at +20dB in this wideband example.) Performance is illustrated in Figure 15. +20dB SINAD was measured with 1.8μV input.

EXAMPLE: 152.2MHZ TO 10.7MHZ NARROWBAND

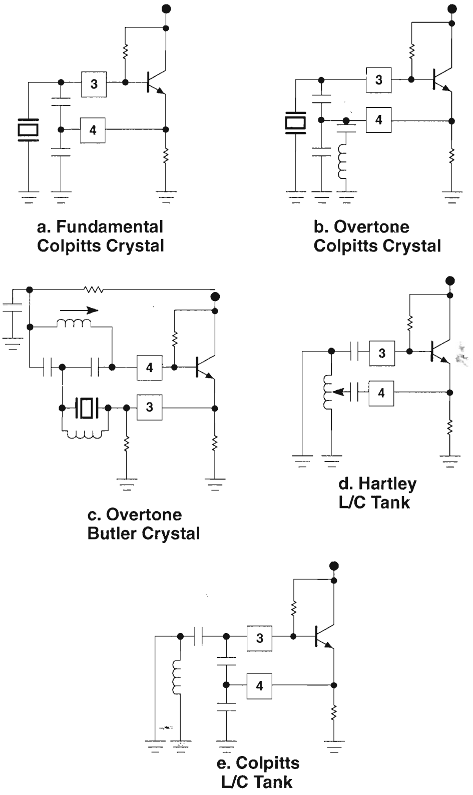
In this example (see Figure 16) a simple, effective, and relatively sensitive single conversion VHF receiver has been implemented. All of the circuit philosophy has been described in previous examples. In this circuit, tuned-transformed termination was used on the input and output sides of the crystal filter. Performance is shown in Figure 17. The +12dB SINAD sensitivity was 0.9μV.

OSCILLATORS

The NE602 contains an oscillator transistor which can be used to frequencies greater than 200MHz. Some of the possible configurations are shown in Figures 18 and 19.

L/C

When using a synthesizer, the LO must be externally buffered. Perhaps the simplest approach is an emitter follower with the base connected to Pin 7 of the NE602. The use of a dual-gate MOSFET will improve performance because it presents a fairly constant capacitance at its gate and because it has very high reverse isolation.



a. Fundamental Colpitts Crystal

b. Overtone Colpitts Crystal

c. Overtone Butler Crystal

d. Hartley L/C Tank

e. Colpitts L/C Tank

Figure 18. Oscillator Configurations

CRYSTAL

With both of the Colpitts crystal configurations, the load capacitance must be specified. In the overtone mode, this can become a sensitive issue since the capacitance from the emitter to ground is actually the equivalent capacitive reactance of the harmonic selection network. The Butler oscillator uses an overtone crystal specified for series mode operation (no parallel capacitance). It may require an extra inductor (L_0) to null out C_0 of the crystal, but otherwise is fairly easy to implement (see references).

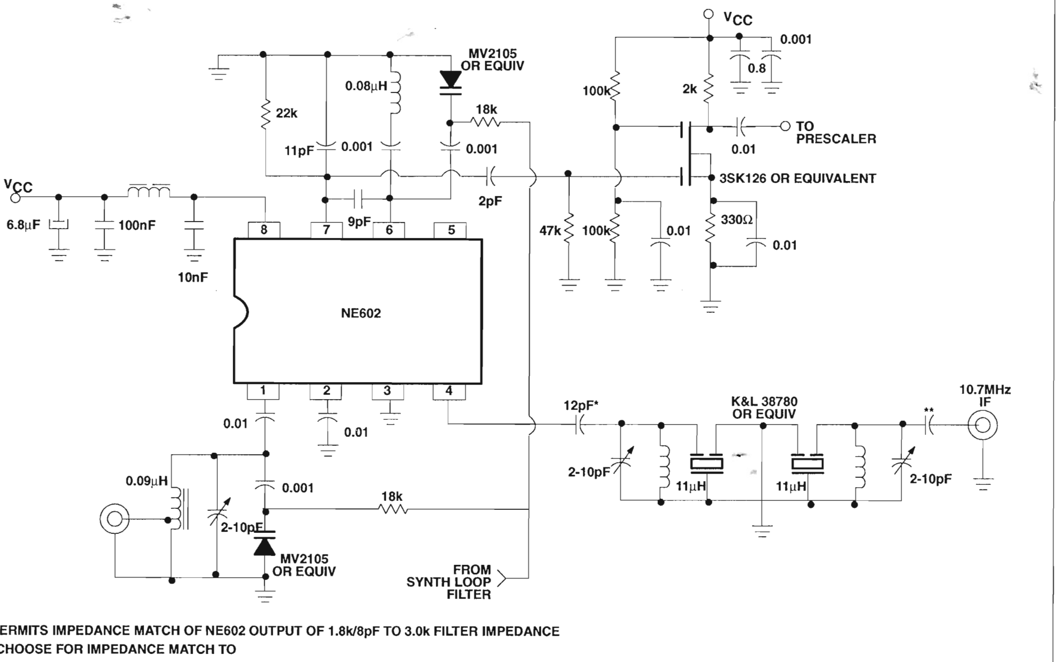
The oscillator transistor is biased with only 220μA. In order to assure oscillation in some configurations, it may be necessary to increase transconductance with an external resistor from the emitter to ground. 10kΩ to 20kΩ are acceptable values. Too small a resistance can upset DC bias (see references).

DATA DEMODULATION

It is possible to change any of the examples from an audio receiver to an amplitude shift keyed (ASK) or frequency shift keyed (FSK) receiver or both with the addition of an external op amp(s) or comparator(s). A simple example is shown in Figure 20. ASK decoding is accomplished by applying a comparator across the received signal strength indicator (RSSI). The RSSI will track IF level down to below the limits of the demodulator (–120dBm RF input in most of the examples). When an in-band signal is above the comparator threshold, the output logic level will change.

FSK demodulation takes advantage of the two audio outputs of the NE604A. Each is a PNP current source type output with 180° phase relationship. With no signal present, the quad tank tuned for the center of the IF passband, and both outputs loaded with the same value of capacitance, if a signal is received which is frequency shifted from the

IF passband, and both outputs loaded with the same value of capacitance, if a signal is received which is frequency shifted from the IF center, one output voltage will increase and the other will decrease by a corresponding absolute value. Thus, if a comparator is differentially connected across the two outputs, a frequency shift in one direction will drive the comparator output to one supply rail, and a frequency shift in the opposite direction will cause the comparator output to swing to the opposite rail. Using this technique, and L/C filtering for a wide IF bandwidth, NRZ data at rates greater than 4Mb have been processed with the new NE605.



*PERMITS IMPEDANCE MATCH OF NE602 OUTPUT OF 1.8k/8pF TO 3.0k FILTER IMPEDANCE
**CHOOSE FOR IMPEDANCE MATCH TO

Figure 19. Typical Varactor Tuned Application

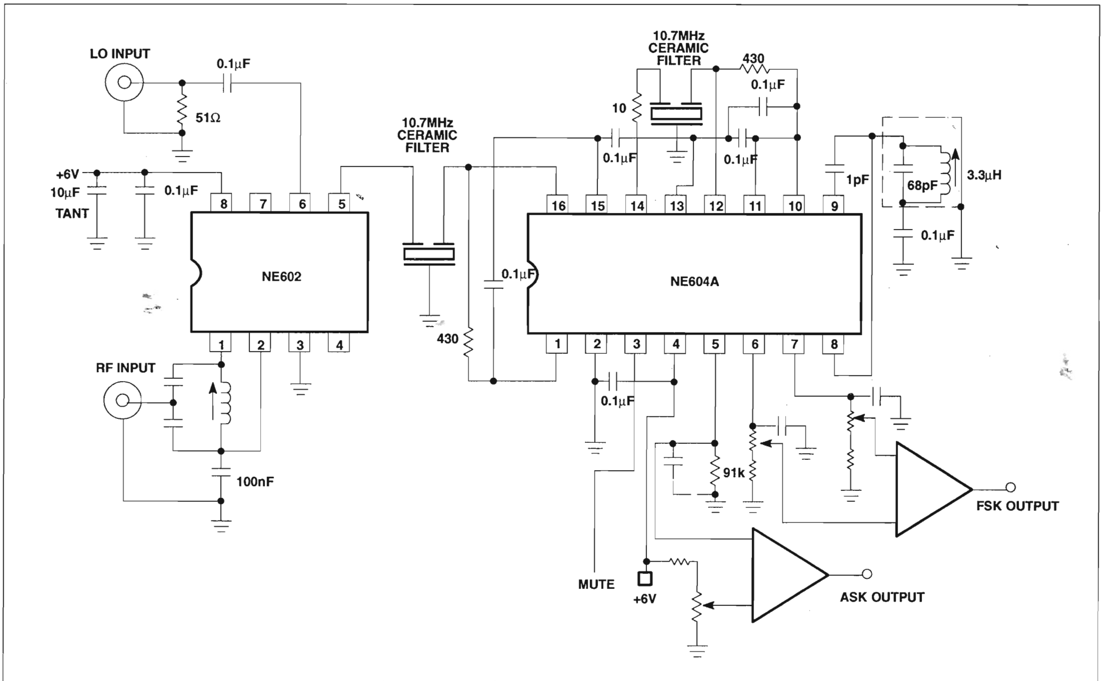


Figure 20. Basic NE602/604A Data Receiver

SUMMARY

The NE602, NE604A and NE605 provide the RF system designer with the opportunity for excellent receiver or IF system sensitivity with very simple circuitry. IFs at 455kHz, 10.7MHz and 21.4MHz with 75 to 90dB gain are possible without special shielding. The flexible configuration of the built-in oscillator of the NE602/605 add to ease of implementation. Either data or audio can be recovered from the NE604A/605 outputs.

REFERENCES

1) Anderson, D.: "Low Power ICs for RF Data Communications", Machine Design , pp 126-128, July 23, 1987.

2) Krauss, Raab, Bastian: Solid State Radio Engineering , p. 311, Wiley, 1980.

3) Matthys, R.: "Survey of VHF Crystal Oscillator Circuits," RF Technology Expo Proceedings, pp 371-382, February, 1987.

4) Signetics: "NE/SA604A High Performance Low Power FM IF System", Linear Data and Applications Manual, Signetics, 1987.

5) Signetics; "NE/SA602 Double Balanced Mixer and Oscillator", Linear Data and Applications Manual, Signetics, 1985.

6) Signetics: "AN1982–Applying the Oscillator of the NE602 in Low Power Mixer Applications", Linear Data and Applications Manual, Signetics, 1985.

High performance low power mixer FM IF system NE/SA605

DESCRIPTION

The NE/SA605 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The NE/SA605 combines the functions of Signetics' NE602 and NE604A, but features a higher mixer input intercept point, higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application. The NE/SA605 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

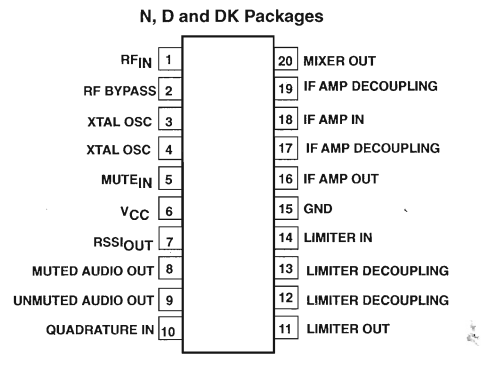
The NE/SA605 and NE/SA615 are functionally the same device types. The difference between the two devices lies in the guaranteed specifications. The NE/SA615 has a higher I_{CC}, lower input third order intercept point, lower conversion mixer gain, lower limiter gain, lower AM rejection, lower SINAD, higher THD, and higher RSSI error than the NE/SA605. Both the NE/SA605 and NE/SA615 devices will meet the EIA specifications for AMPS and TACS cellular radio applications.

For additional technical information please refer to application notes AN1994, 1995 and 1996, which include example application diagrams, a complete overview of the product, and artwork for reference.

APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

PIN CONFIGURATION



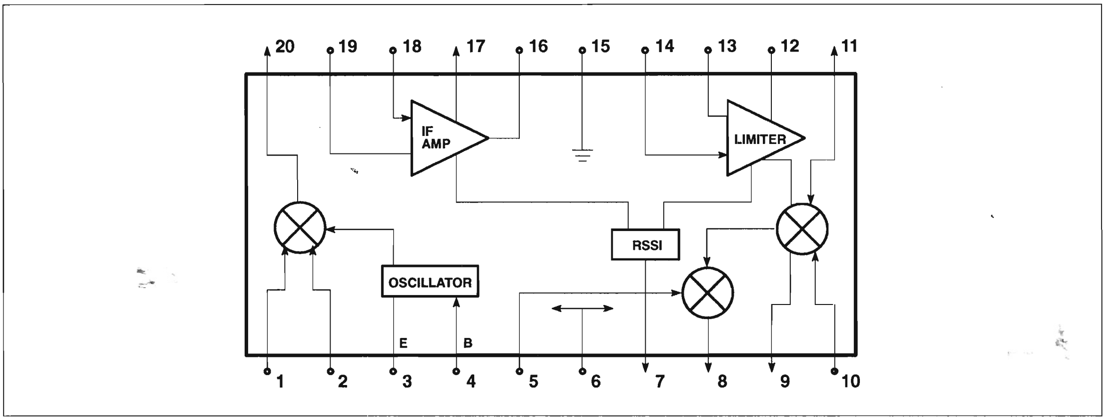
FEATURES

- Low power consumption: 5.7mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22µV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA605 meets cellular radio specifications
- ESD hardened

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE605N	0408B
20-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA605N	0408B
20-Pin Plastic Small Outline Large (SOL) package	0 to +70°C	NE605D	0172D
20-Pin Plastic Small Outline Large (SOL) package	–40 to +85°C	SA605D	0172D
20-Pin Plastic Shrink Small Outline Package (SSOP)	0 to +70°C	NE605DK	1563
20-Pin Plastic Shrink Small Outline Package (SSOP)	–40 to +85°C	SA605DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE605	0 to +70	°C
	SA605	-40 to +85	°C
θ_{JA}	Thermal impedance D package N package SSOP package	90 75 117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE605			SA605			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		5.1	5.7	6.5	4.55	5.7	6.55	mA
	Mute switch input threshold (ON)		1.7			1.7			V
	(OFF)				1.0			1.0	V

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = +6V$, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE605			SA605			
			MIN	TYP	MAX	MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)									
f_{IN}	Input signal frequency			500			500		MHz
f_{OSC}	Crystal oscillator frequency			150			150		MHz
	Noise figure at 45MHz			5.0			5.0		dB
	Third-order input intercept point	f1 = 45.0; f2 = 45.06MHz		-10			-10		dBm
	Conversion power gain	Matched 14.5dBV step-up	10.5	13	14.5	10	13	15	dB
		50Ω source		-1.7			-1.7		dB
	RF input resistance	Single-ended input	3.5	4.7		3.0	4.7		kΩ
	RF input capacitance			3.5	4.0		3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.3	1.5		1.25	1.5		kΩ
IF section									
	IF amp gain	50Ω source		39.7			39.7		dB
	Limiter gain	50Ω source		62.5			62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-113			-113		dBm
	AM rejection	80% AM 1kHz	30	34	42	29	34	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	110	150	250	80	150	260	mV_{RMS}
	Unmuted audio level, R_{11} = 100k	150pF de-emphasis		480			480		mV
	SINAD sensitivity	RF level -118dB		16			16		dB
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	550	0	160	650	mV
		IF level = -68dBm	2.0	2.5	3.0	1.9	2.5	3.1	V
		IF level = -18dBm	4.1	4.8	5.5	4.0	4.8	5.6	V
	RSSI range	R_9 = 100kΩ Pin 16		90			90		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±1.5			±1.5		dB
	IF input impedance		1.40	1.6		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.40	1.6		1.40	1.6		kΩ
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ
RF/IF section (int LO)									
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450			450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3			4.3		V

NOTE:

1. The generator source impedance is 50Ω, but the NE/SA605 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA605 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA605 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

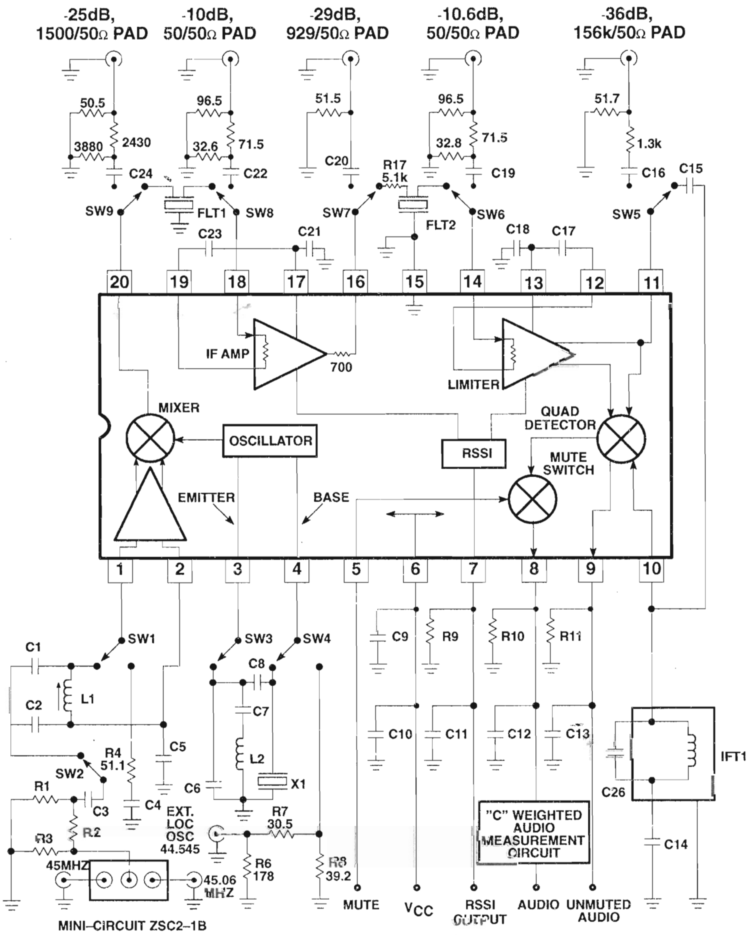
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

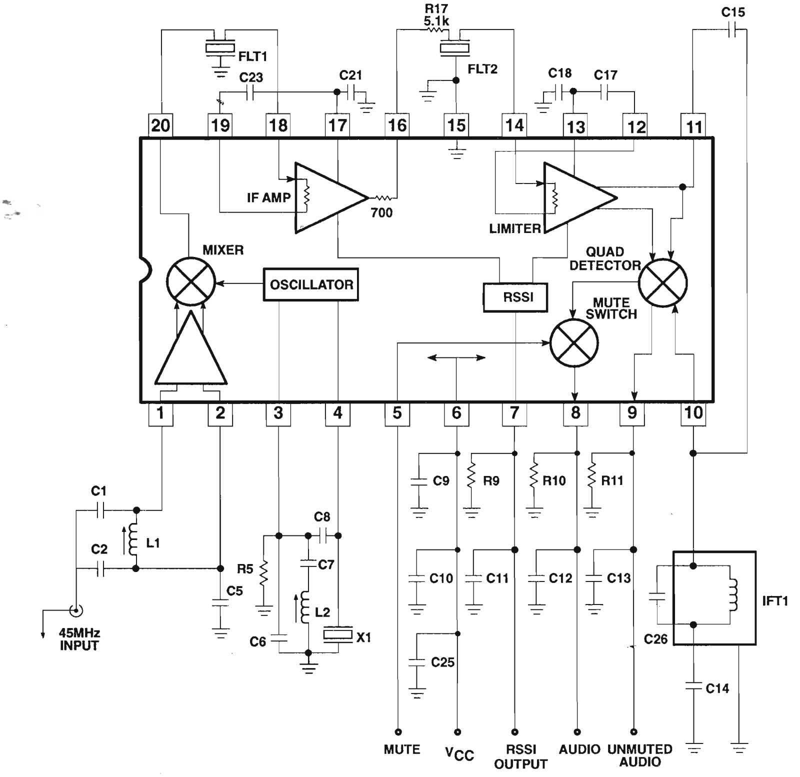


Automatic Test Circuit Component List

C1	47pF NPO Ceramic	C21	100nF ±10% Monolithic Ceramic
C2	180pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C25	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic	C26	390pF ±10% Monolithic Ceramic
C7	1nF Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C9	100nF ±10% Monolithic Ceramic	IFT 1	455kHz 270μH TOKO #303LN-1129
C10	6.8μF Tantalum (minimum) *	L1	300nH TOKO #5CB-1055Z
C11	100nF ±10% Monolithic Ceramic	L2	0.8μH TOKO 292CNS–T1038Z
C12	15nF ±10% Ceramic	X1	44.545MHz Crystal ICM4712701
C13	150pF ±2% N1500 Ceramic	R9	100k ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R17	5.1k ±5% 1/4W Carbon Composition
C15	10pF NPO Ceramic	R10	100k ±1% 1/4W Metal Film (optional)
C17	100nF ±10% Monolithic Ceramic	R11	100k ±1% 1/4W Metal Film (optional)
C18	100nF ±10% Monolithic Ceramic		

* NOTE: This value can be reduced when a battery is the power source.

Figure 1. NE/SA605 45MHz Test Circuit (Relays as shown)



Application Component List

C1	47pF NPO Ceramic
C2	180pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8μF Tantalum (minimum)
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
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L1	300nH TOKO #5CB-1055Z
L2	0.8μH TOKO 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*** NOTE: This value can be reduced when a battery is the power source.**

Figure 2. NE/SA605 45MHz Application Circuit

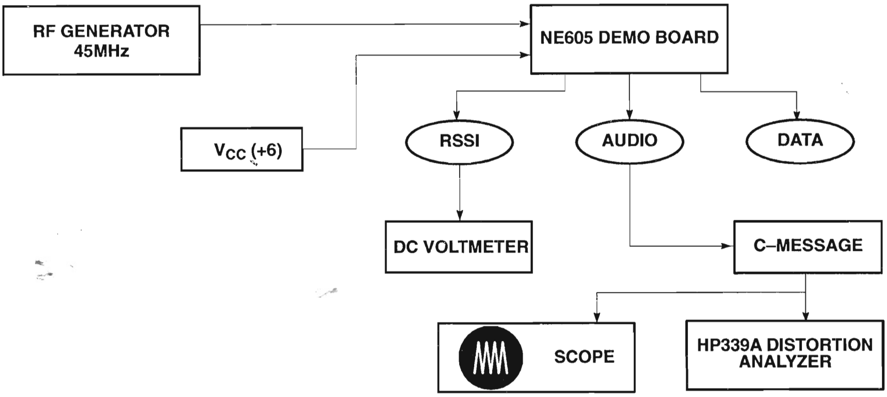


Figure 3. NE/SA605 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22μV or -120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

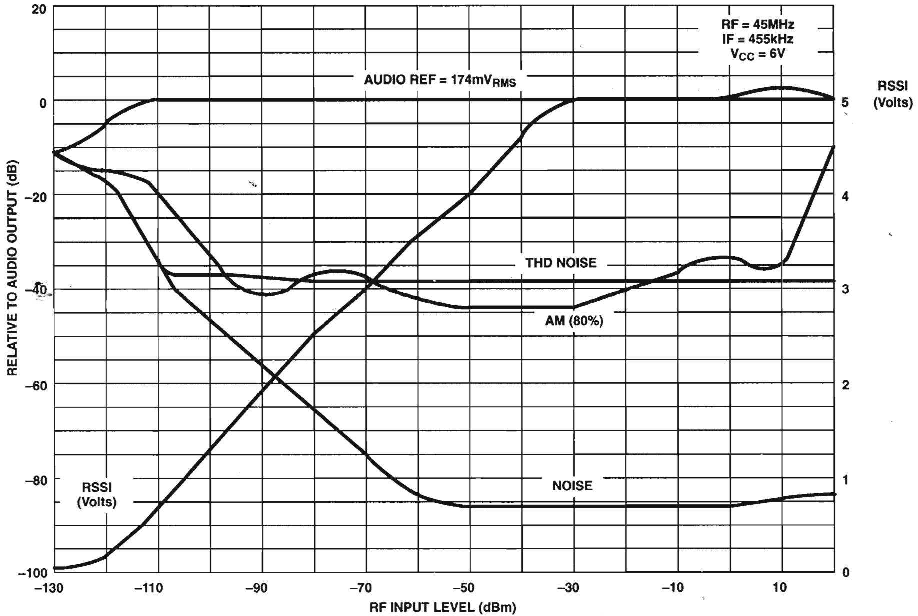


Figure 4. NE605 Application Board at 25°C

High performance low power mixer FM IF system

NE/SA615

DESCRIPTION

The NE/SA615 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The NE/SA615 combines the functions of Signetics' NE602 and NE604A, but features a higher mixer input intercept point, higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application. The NE/SA615 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

The NE/SA605 and NE/SA615 are functionally the same device types. The difference between the two devices lies in the guaranteed specifications. The NE/SA615 has a higher I_{CC}, lower input third order intercept point, lower conversion mixer gain, lower limiter gain, lower AM rejection, lower SINAD, higher THD, and higher RSSI error than the NE/SA615. Both the NE/SA605 and NE/SA615 devices will meet the EIA specifications for AMPS and TACS cellular radio applications.

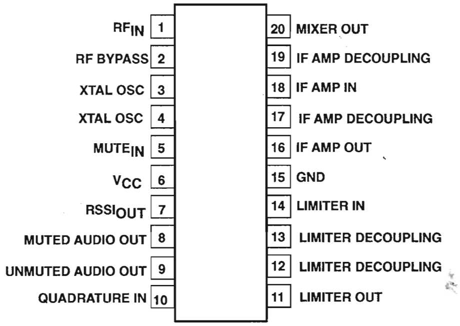
For additional technical information please refer to application notes AN1994, 1995 and 1996, which include example application diagrams, a complete overview of the product, and artwork for reference.

FEATURES

- Low power consumption: 5.7mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs – muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters

PIN CONFIGURATION

N, D and DK Packages



NOTE:
See back page for package dimensions

- Excellent sensitivity: 0.22µV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA615 meets cellular radio specifications
- ESD hardened

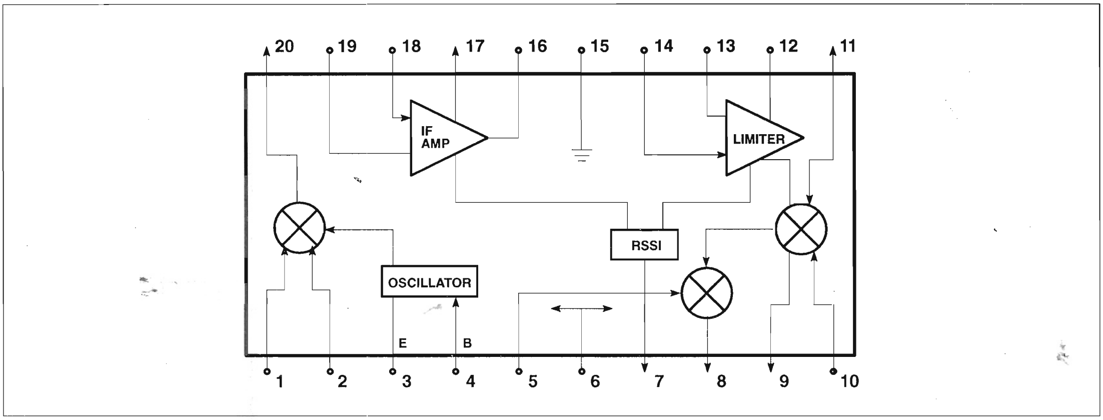
APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE615N	0408B
20-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA615N	0408B
20-Pin Plastic Small Outline Large (SOL) package	0 to +70°C	NE615D	0175D
20-Pin Plastic Small Outline Large (SOL) package	–40 to +85°C	SA615D	0175D
20-Pin Plastic Shrink Small Outline Package (SSOP)	0 to +70°C	NE615DK	1563–
20-Pin Plastic Shrink Small Outline Package (SSOP)	–40 to +85°C	SA615DK	1563–

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range NE615	0 to +70	°C
	SA615	–40 to +85	°C
θ_{JA}	Thermal impedance D package N package SSOP package	90 75 117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA615 MIN	LIMITS NE/SA615 TYP	LIMITS NE/SA615 MAX	UNITS
V_{CC}	Power supply voltage range		4.5		8.0	V
I_{CC}	DC current drain			5.7	7.4	mA
	Mute switch input threshold (ON)		1.7			V
	(OFF)				1.0	V

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = +6V$, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step–up; IF frequency = 455kHz; R17 = 5.1k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA615			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			5.0		dB
	Third-order input intercept point	f1 = 45.00; f2 = 45.06MHz		-12		dBm
	Conversion power gain	Matched 14.5dBV step-up	8.0	13		dB
		50Ω source		-1.7		dB
	RF input resistance	Single-ended input	3.0	4.7		kΩ
	RF input capacitance			3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.50		kΩ
IF section						
	IF amp gain	50Ω source		39.7		dB
	Limiter gain	50Ω source		62.5		dB
	Input limiting -3dB, $R_{17} = 5.1k$	Test at Pin 18		-109		dBm
	AM rejection	80% AM 1kHz	25	33	43	dB
	Audio level, $R_{10} = 100k$	15nF de-emphasis	60	150	260	mV_{RMS}
	Unmuted audio level, $R_{11} = 100k$	150pF de-emphasis		530		mV
	SINAD sensitivity	RF level -118dB		12		dB
THD	Total harmonic distortion		-30	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		68		dB
	IF RSSI output, $R_9 = 100kΩ$[1]	IF level = -118dBm	0	160	800	mV
		IF level = -68dBm	1.7	2.5	3.3	V
		IF level = -18dBm	3.6	4.8	5.8	V
	RSSI range	$R_9 = 100kΩ$ Pin 16		80		dB
	RSSI accuracy	$R_9 = 100kΩ$ Pin 16		±2		dB
	IF input impedance		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter intput impedance		1.40	1.6		kΩ
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ
RF/IF section (int LO)						
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3		V

NOTE:

1. The generator source impedance is 50Ω, but the NE/SA605 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA605 input (Pin 8) which is about 21dB less than the "available power" at the generator.

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The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of –10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

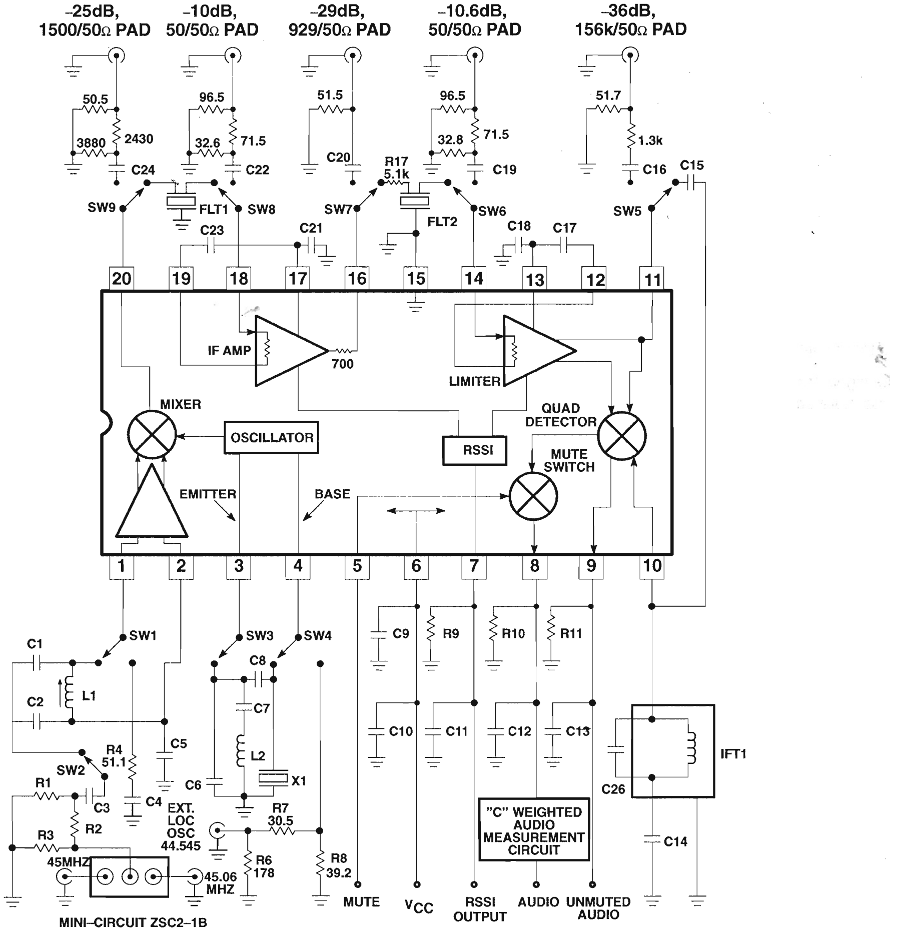
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: dB(v) = 20log V_{OUT}/V_{IN}



Automatic Test Circuit Component List

C1	47pF NPO Ceramic
C2	180pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8µF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	390pF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
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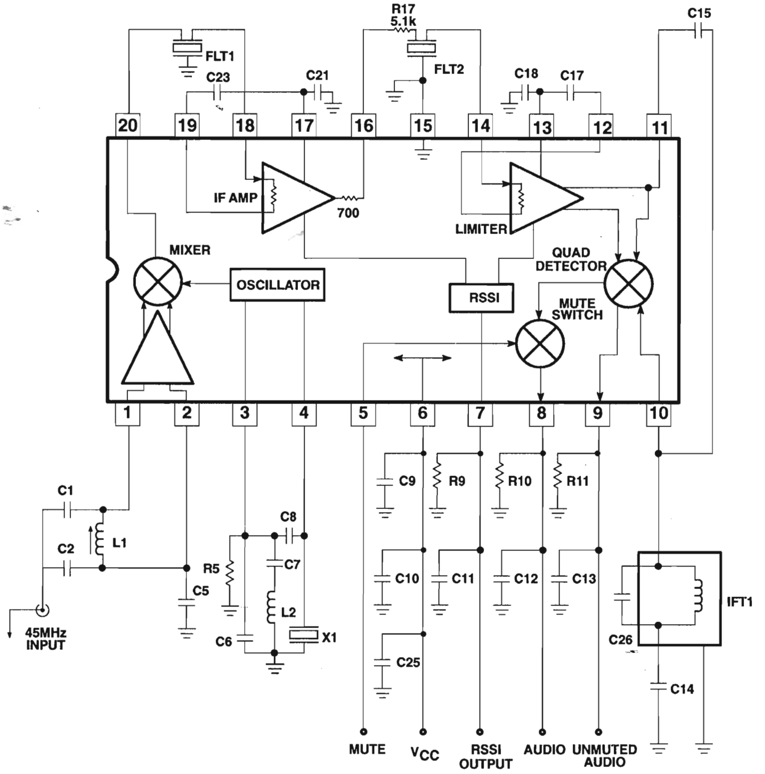
IFT 1	455kHz 270µH TOKO #303LN-1129
L1	300nH TOKO #5CB-1055Z
L2	0.8µH TOKO 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. NE/SA615 45MHz Test Circuit (Relays as shown)



NE/SA615N
Application Component List

C1	47pF NPO Ceramic	C21	100nF ±10% Monolithic Ceramic
C2	180pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C25	100nF ±10% Monolithic Ceramic
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C15	10pF NPO Ceramic	R10	100k ±1% 1/4W Metal Film (optional)
C17	100nF ±10% Monolithic Ceramic	R11	100k ±1% 1/4W Metal Film (optional)
C18	100nF ±10% Monolithic Ceramic		

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Figure 2. NE/SA615 45MHz Application Circuit

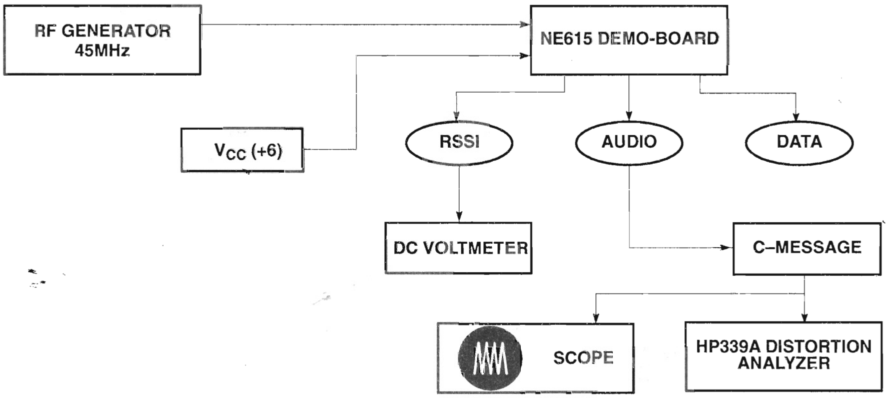

Figure 3. NE/SA615 Application Circuit Test Set Up

NOTES:
1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
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4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22µV or –120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10–15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2–3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

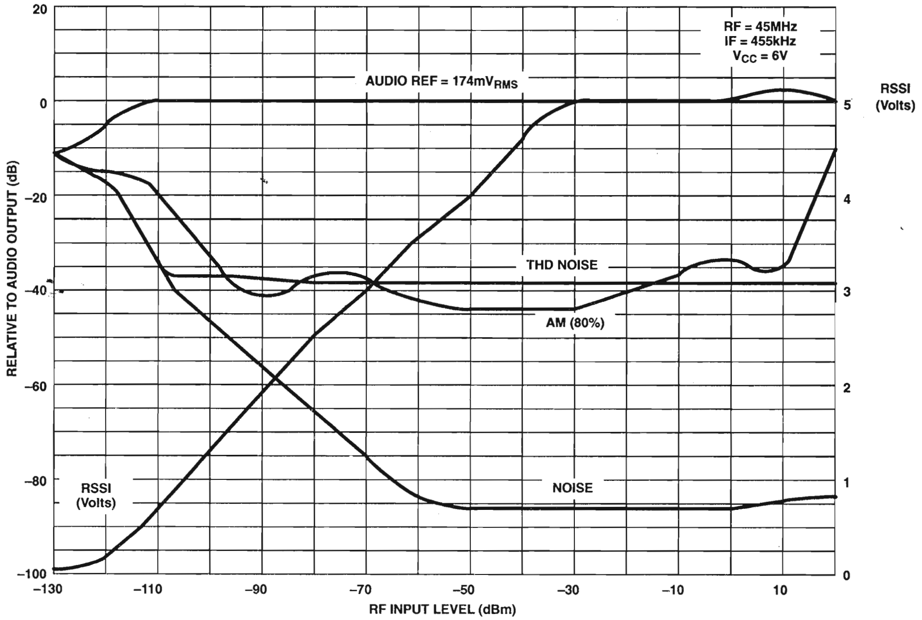


Figure 4. NE615 Application Board at 25°C

Reviewing key areas when designing with the NE605

AN1994

Author: Alvin K. Wong

INTRODUCTION

This application note addresses key information that is needed when designing with the NE605. Since the NE602 and the NE604 are closely related to the NE605, a brief overview of these chips will be helpful. Additionally, this application note will divide the NE605 into four main blocks where a brief theory of operation, important parameters, specifications, tables and graphs of performance will be given. A question & answer section is included at the end. Below is an outline of this application note:

I. BACKGROUND

- History of the NE605
- Related app. notes

II. OVERVIEW OF THE NE605

- Mixer Section
  - RF section
  - Local osc. section
  - Output of mixer
  - Choosing the IF frequency
  - Performance graphs of mixer
- IF Section
  - IF amplifier
  - IF limiter
  - Function of IF section
  - Important parameters of IF section
    - 14. Limiting
    - 15. AM rejection
    - 16. AM to PM conversion
    - 17. Interstage loss
  - IF noise figure
  - Performance graphs of IF section
- Demodulator Section
- Output Section
  - Audio and unmuted audio
  - RSSI output
  - Performance graphs of output section

III.Question & Answers

I. BACKGROUND

History of the NE605

Before the NE605 was made, the NE602 (double-balanced mixer and oscillator) and the NE604 (FM IF system) existed. The combination of these two chips make up a high performance low cost receiver. Soon after the NE605 was created to be a one chip solution, using a newer manufacturing process and design. Since the newer process and design in the NE605 proved to be better in performance and reliability, it was decided to make the NE602 and the NE604 under this new process. The NE602A and the NE604A were created. To assist the cost-conscious customer, Signetics also offered an inexpensive line of the same RF products: the NE612, NE614, and NE615.

Because the newer process and design proved to be better in performance and reliability, the older chips are going to be discontinued. Therefore, only the NE602A, NE612A, NE604A, NE614A, NE605 and NE615 will be available.

Figure 1 shows a brief summary of the RF chips mentioned above. Under the newer process, minor changes were made to improve the performance. A designer, converting from the NE602 to the NE602A, should have no problem with a direct switch. However, switching from the NE604 to the NE604A, might require more attention. This will depend on how good the original design was in the system. In the "Questions & Answers" section, the NE604 and NE604A are discussed in greater detail. This will help the designer, who used the NE604 in their original design, to switch to the "A" version. In general, a direct switch to the NE604A is simple.

Related Application Notes

There have been many application notes written on the NE602 and NE604A. Since the combination of those parts is very similar to the NE605, many of the ideas and applications still apply. In addition, many of the topics discussed here will also apply to the NE602A and NE604A.

Table 1 (see back of app note) shows the application notes available to the designer. They can be found in either the Signetics Linear Data Manual, Volume 1, or the Signetics RF Communications Handbook. Your local PhilipsComponents-Signetics sales representative can provide you with copies of these publications, or you can contact Signetics Publication Services.

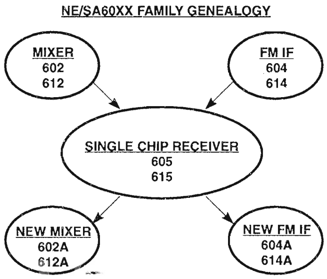


Figure 1. Overview of Selected RF Chips

II. OVERVIEW OF THE NE605

In Figure 2, the NE605 is broken up into four main areas; the mixer section, the IF section, the demodulator section and the output section. The information contained in each of the four areas focuses on important data to assist you with the use of the NE605 in any receiver application.

Mixer Section

There are three areas of interest that should be addressed when working with the mixer section. The RF signal, LO signal and the output. The function of the mixer is to give the sum/difference of the RF and LO frequencies to get an IF frequency out. This mixing of frequencies is done by a Gilbert Cell four quadrant multiplier. The Gilbert Cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell.

The RF input impedance of the mixer plays a vital role in determining the values of the matching network. Figure 3 shows the RF input impedance over a range of frequency. From this information, it can be determined that matching 50Ω at 45MHz requires matching to a 4.5kΩ resistor in parallel with a 2.5pF capacitor. An equivalent model can be seen in Figure 4 with its component values given for selected frequencies. Since there are many questions from the designer on how to match the RF input, an example is given below.

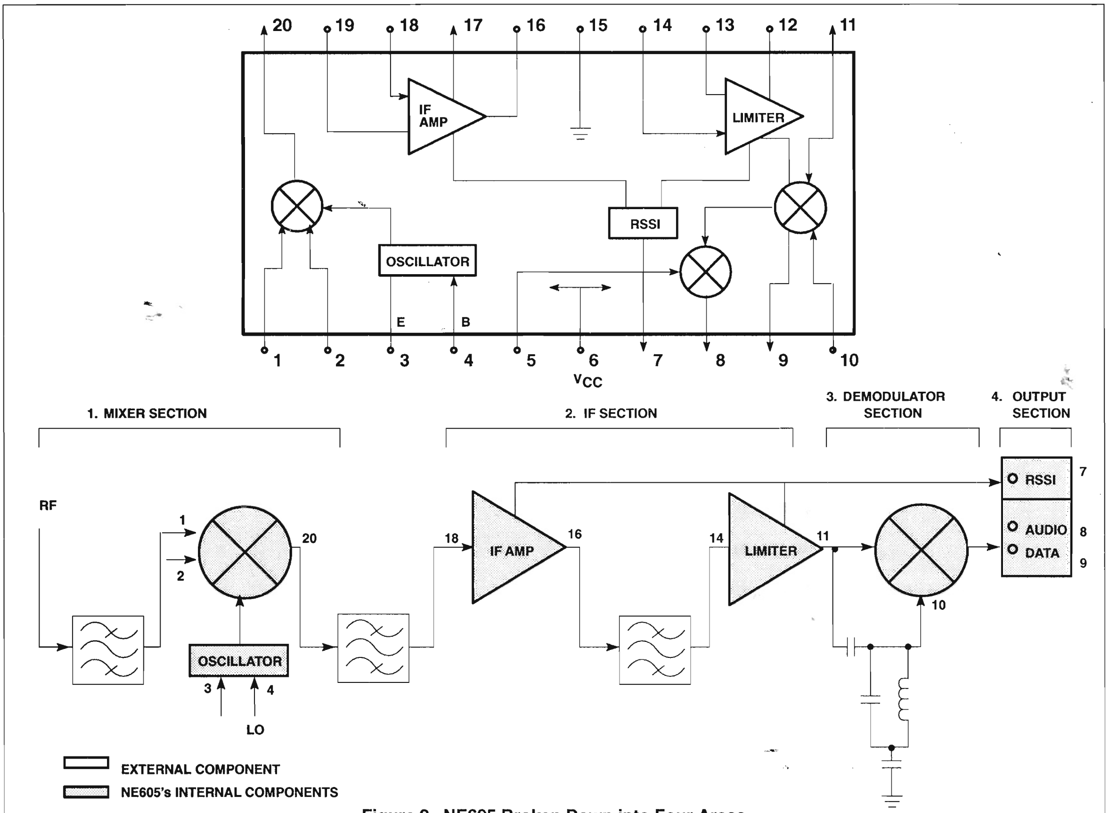


Figure 2. NE605 Broken Down into Four Areas

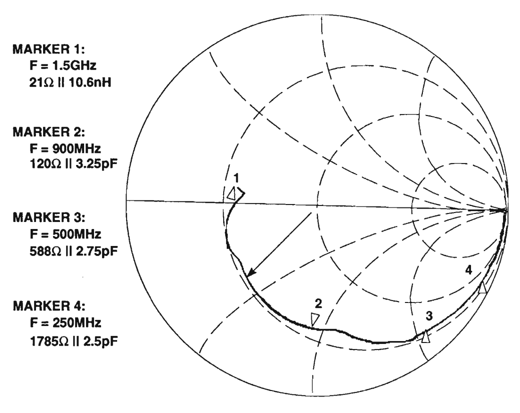
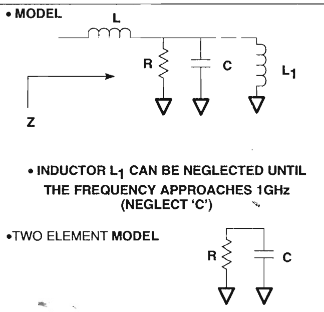


Figure 3. Smith Chart of NE605's RF Input Impedance (Pin 1 or 2)

RF Section of Mixer

The mixer has two RF input pins (Pin 1 and 2), allowing the user to choose between a balanced or unbalanced RF matching network. Table 2 (see back of app note) shows the advantages and disadvantages for either type of matching. Obviously, the better the matching network, the better the sensitivity of the receiver.


• MODEL
L
R
C
L1
Z
• INDUCTOR L1 CAN BE NEGLECTED UNTIL THE FREQUENCY APPROACHES 1GHz (NEGLECT 'C')
•TWO ELEMENT MODEL
R
C

FREQ	R II C
10MHz	5kΩ II 2.5pF
50MHz	4651Ω II 2.5pF
100MHz	3100Ω II 2.5pF
250MHz	1785kΩ II 2.5pF
500MHz	588Ω II 2.75pF
750MHz	1751Ω II 3.12pF
900MHz	120Ω II 3.2pF
1.1GHz	48Ω II 3.4pF
1.56GHz	21Ω II 10.6nH

Figure 4. Equivalent Model of RF Input Impedance

Example: Using a tapped-C network, match a 50Ω source to the RF input of the NE605 at 45MHz. (refer to Figure 5)

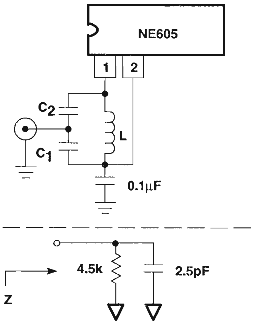


Figure 5. Tapped-C Network

Step 1. Choose an inductor value and its "Q" $L = 0.22\mu H$ $Q_P = 50$ (specified by manufacturer)

Step 2. Find the reactance of the inductor

$X_P = 2\pi FL$
$= 2\pi\,(45MHz)\,(0.22\mu H)$
$\therefore\ X_P = 62.2\Omega$

Step 3. Then,

$R_P = Q_P X_P$
$= (50)(62.2)$
$\therefore\ R_P = 3.11k\Omega$ (the inductance resistance)

Step 4. $Q = R_{TOTAL}/X_P$
$= (R_S' \,//\, R_L \,//\, R_P) / X_P$
where $R_S' = R_L$
$= 4.5k \,//\, 4.5k \,//\, 3.11k / 62.2$
$= 21.39$
$\therefore\ Q \cong 21$ (the Q of the matching network)

where:
R_S = source resistance;
R_L = load resistance;
R_S' = what the source resistance should look like to match R_L;
R_P = inductance resistance

Step 5.
$$\frac{C1}{C2} = \sqrt{\frac{R_S'}{R_S}} - 1 = 8.6$$

Step 6.
$$C_T = \frac{1}{X_P\,\omega} = \frac{1}{(62.2)\ 2\pi\ 45MHz}$$
$$= 56.86pF$$

Step 7.
$$\text{using } C_T = \frac{C1C2}{C1 + C2}$$
$$\text{where } C_T = 56.86pF,\ \frac{C1}{C2} = 8.6$$
$$C_T = \frac{C1}{\frac{C1}{C2} + 1}$$
$$\therefore\ C_1 = C_T\left(\frac{C1}{C2} + 1\right)$$
$$\text{and} C_2 = \frac{C1}{8.6}$$

thus...
$C1 = 539pF$
$C2 = 64pF$
$L = 0.22\mu H$ (value started with)

Step 8. Frequency check

$$\omega = \frac{1}{\sqrt{LC}}$$
$$2\pi F = \frac{1}{\sqrt{LC}}$$
$F = 45MHz$ (...so far so good)

Step 9. Taking care of the 2.5pF capacitor that is present at the RF input at 45MHz
$$\frac{C2_A}{C1_A} = \frac{64pF}{540pF} \qquad \text{Eq. 1.}$$
$$C_{TN} = \frac{C1_A C2_A}{C1_A + C2_A} \qquad \text{Eq. 2.}$$
where $C_{TN} = C_T - 2.5pF$
(recall value of C_T from Step 6.)

Making use of Equations 1 and 2, the new values of C1 and C2 are:
$C1_A = 524pF$
$C2_A = 60.6pF$

[NOTE: At this frequency the 2.5pF capacitor could probably be ignored since its value at 45MHz has little effect on C1 and C2.]

Step 10. Checking the bandwidth
$$Q = \frac{F}{BW}$$
$$BW = F_U - F_L$$
BW = bandwidth

F_U = upper 3dB frequency
F_L = lower 3dB frequency

Using the above formulas results in
F_U = 46MHz
F_L = 44MHz
BW = 2MHz

The above shows the calculations for a single-ended match to the NE605. For a balanced matching network, a transformer can be used. The same type of calculations will still apply once the input impedance of the NE605 is converted to the primary side of the transformer (see Figure 6). But before we transform the input impedance to the primary side, we must first find the new input impedance of the NE605 for a balanced configuration. Because we have a balanced input, the 4.5kΩ transforms to 9kΩ (4.5k + 4.5k = 9k) while the capacitor changes from 2.5pF to 1.3pF (2.5pF in series with 2.5pF is 1.3pF). Notice that the resistor values double while the capacitor values are halved. Now the 9kΩ resistor in parallel with the 1.3pF capacitor must be transformed to the primary side of the transformer (see Figure 6).

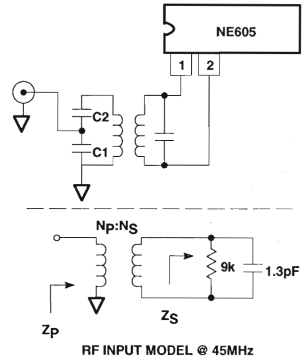


Figure 6. Using a Transformer to Achieve a Balanced Match

Procedure:

Step 1. $\frac{Z_P}{Z_S} = \left(\frac{N_P}{N_S}\right)^2$

where:
Z_P = impedance of primary side
Z_S = impedance of secondary side
N_P = number of turns on primary side
N_S = number of turns on secondary side

Step 2. Recall,
$Z_S = R \,||\, X_C$
$Z_S = 9k \,||\, j2.7k$
where
R = 9k $X_C = \frac{1}{2\pi FC} = 2.7k$ at F = 45MHz

Step 3. Assume 1:N turns ratio for the transformer

$$Z_P = \frac{Z_S}{N^2} = 2.25k \parallel j\ 680$$

(assuming N = 2)

Step 4. $\therefore C = \frac{1}{2\pi\ FX_C} = 5.2pF$

R = 2.25k
(these are the new values to match using the formulas in tapped-C)

Step 5. Because the transformer has a magnetization inductance L_M, (inductance presented by the transformer), we can eliminate the inductor used in the previous example and tune the tapped-C network with the inductance presented by the transformer.
Lets assume L_M = 0.22μH (Q=50) Therefore
C1 = 381pF
C2 = 66.8pF
F_U = 46.7MHz
F_L = 43.3MHz
BW = 3.4MHz
taking the input capacitor into consideration
C1 = 347pF
C2 = 61pF
L = 0.22μH (Q=50)

Because of leakage inductance, the transformer is far from ideal. All of these leakages affect the secondary voltage under load which will seem like the indicated turns ratio is wrong. The above calculations show one method of impedance matching. The values calculated for C1 and C2 do not take into account board parasitic capacitance, and are, therefore, only theoretical values. There are many ways to configure and calculate matching networks. One alternative is a tapped-L configuration. But the ratio of the tapped-C network is easier to implement than ordering a special inductor. The calculations of these networks can be done on the Smith Chart. Furthermore, there are many computer programs available which will help match the circuit for the designer.

Local Oscillator Section of Mixer

The NE605 provides an NPN transistor for the local oscillator where only external components like capacitors, inductors, or resistors need to be added to achieve the LO frequency. The oscillator's transistor base and emitter (Pins 4 and 3 respectively) are available to be configured in Colpitts, Butler or varactor controlled LC forms. Referring to Figure 7, the collector is internally connected directly to V_{CC}, while the emitter is connected through a 25kΩ resistor to ground. Base bias is also internally supplied through an 18kΩ resistor. A buffer/divider reduces the oscillator level by a factor of three before it is applied across the upper tree of the Gilbert Cell. The divider de-sensitizes the mixer to oscillator level variations with temperature and voltage. A typical value for the LO input impedance is approximately 10kΩ.

The highest LO frequency that can be achieved is approximately 300MHz with a 200mV_{RMS} signal on the base (Pin 4). Although it is possible to exceed the 300MHz LO frequency for the on-board oscillator, it is not really practical because the signal level drops too low for the Gilbert Cell. If an application requires a higher LO frequency, an external oscillator can be used with its $200mV_{RMS}$ signal injected at Pin 4 through a DC blocking capacitor. Table 3 (see back of app note) can be used as a guideline to determine which configuration is best for the required LO frequency.

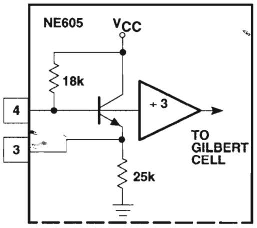


Figure 7. On-board NPN Transistor for Local Oscillator

Because the Colpitts configuration is for parallel resonance mode, it is important to know, when ordering crystals, that the load capacitance of the NE605 is 10pF. However, for the Butler configuration, the load capacitance is unimportant since the crystal will be in the series mode. Figure 8 shows the different types of LO configurations used with NE605.

If a person decides to use the Colpitts configuration in their design, they will probably find that most crystal manufacturers have their own set of standards of load capacitance. And in most cases, they are unwilling to build a special test jig for an individual's needs. If this occurs, the designer should tell them to go ahead with the design. But, the designer should also be ready to accept the crystal's frequency to be off by 200–300Hz from the specified frequency. Then a test jig provided by the designer and a 2nd iteration will solve the problem.

Output of Mixer

Once the RF and LO inputs have been properly connected, the output of the mixer supplies the IF frequency. Knowing that the mixer's output has an impedance of 1.5kΩ, matching to an IF filter should be trivial.

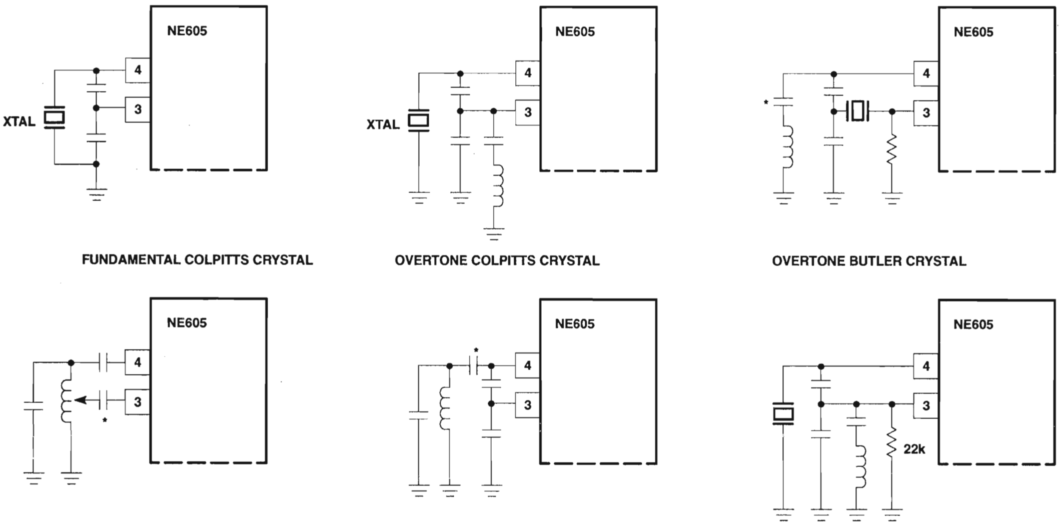
Choosing the Appropriate IF Frequency

Some of the standard IF frequencies used in industry are 455kHz, 10.7MHz and 21.4MHz. Selection of other IF frequencies is possible. However, this approach could be expensive because the filter manufacturer will probably have to build the odd IF filter from scratch.

There are several advantages and disadvantages in choosing a low or high IF frequency. Choosing a low IF frequency like 455kHz can provide good stability, high sensitivity and gain. Unfortunately, it can also present a problem with the image frequency (assuming single conversion). To improve the image rejection problem, a higher IF frequency can be used. However, sensitivity is decreased and the gain of the IF section must be reduced to prevent oscillations.

If the design requires a low IF frequency and good image rejection, it is best to use the double conversion method. This method allows the best of both worlds. Additionally, it is much easier to work with a lower IF frequency because the layout will not be as critical and will be more forgiving in production. The only drawback to this method is that it will require another mixer and LO. But, a transistor can be used for the first mixer stage (which is an inexpensive approach) and the NE605 can be used for the second mixer stage. The NE602A can also be used for the first conversion stage if the transistor approach does not meet the design requirements.

If the design requires a high IF frequency, good layout and RF techniques must be exercised. If the layout is sound and instability still occurs, refer to the "RSSI output" section which suggests solutions to these types of problems.



FUNDAMENTAL COLPITTS CRYSTAL

OVERTONE COLPITTS CRYSTAL

OVERTONE BUTLER CRYSTAL

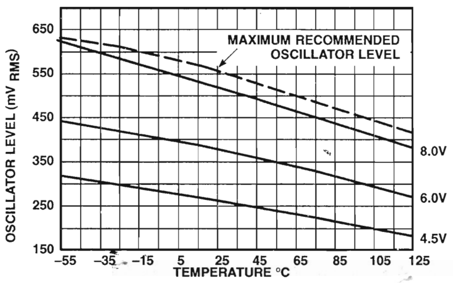
HARTLEY L/C TANK

COLPITTS L/C TANK

3–5th OVERTONE COLPITTS CRYSTAL

* DC BLOCKING CAPACITORS

Figure 8. Oscillator Configurations



C_{BE} = 5.6pF

Figure 9. NE605 Application Oscillator Level

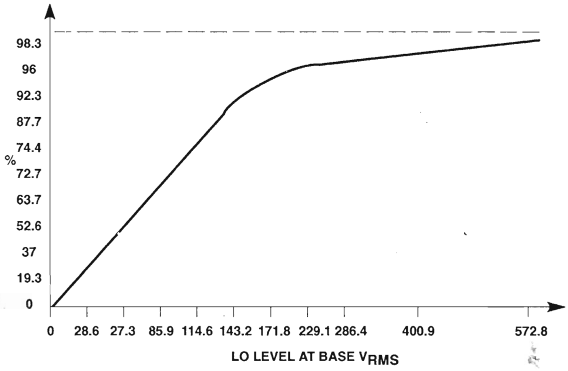


Figure 10. Mixer Efficiency vs Normalized LO Level

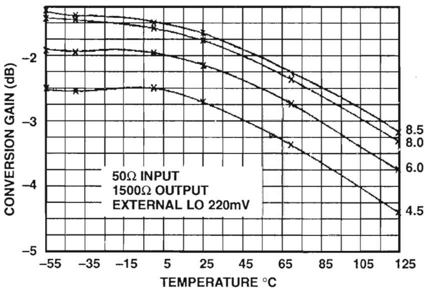


Figure 11. 50Ω Conversion Gain

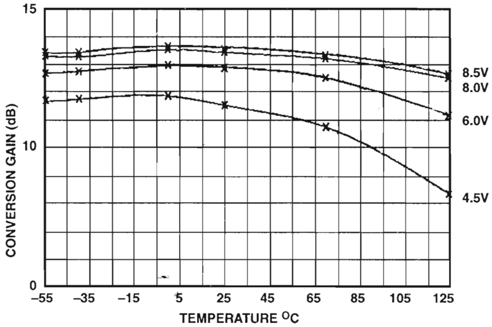


Figure 12. Single-Ended Matched Input Conversion Gain (50Ω to 1.5kΩ, 14.5dB Matching Step-up Network)

Performance Graphs of Mixer

Fig.	Description
9	Oscillator Levels vs. Temperature with Different Supply Voltages for the 44.545MHz Crystal Colpitts Applications
10	LO Efficiency vs. Normalized Peak Level at the Base of the Oscillator Transistor
11	50Ω Conversion Gain vs. Temperature with Different Supply Voltages Using an External LO
12	Mixer Matched Input Conversion Gain vs. Temperature with Different Supply Voltages
13	IF Output Power vs. RF Input Level (3rd-order Intercept Point) 1st mixer = diode mxr, 2nd mixer = 605 mxr
14	NE605 and Diode Mixer Test Set Up
15	NE605 LO Power Requirements vs. Diode Mixer
16	NE605 Conversion Gain vs. Diode Mixer
17	Comparing Intercept Points with Different Types of Mixers

Another issue to consider when determining an IF frequency is the modulation. For example, a narrowband FM signal (30kHz IF bandwidth) can be done with an IF of 455kHz. But for a wideband FM signal (200kHz IF bandwidth), a higher IF is required, such as 10.7MHz or 21.4MHz.

IF Section

The IF section consists of an IF amplifier and IF limiter. With the amplifier and limiter working together, 100dB of gain with a 25MHz bandwidth can be achieved (see Figure 18). The linearity of the RSSI output is directly affected by the IF section and will be discussed in more detail later in this application note.

IF Amplifier

The IF amplifier is made up of two differential amplifiers with 40dB of gain and a small signal bandwidth of 41MHz (when driven by a 50Ω source). The output is a low impedance emitter follower with an output resistance of about 230Ω, and an internal series build out of 700Ω to give a total of 930Ω. One can expect a 6dB loss in each amplifier's input since both of the differential amplifiers are single-ended.

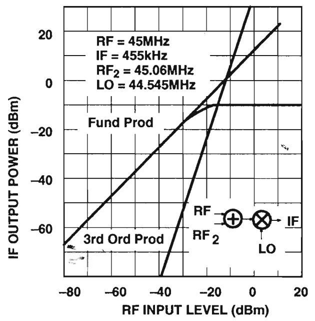


Figure 13. Third-Order Intercept and Compression

The basic function of the IF amp is to boost the IF signal and to help handle impulse noise. The IF amp will not provide good limiting over a wide range of input signals, which is why the IF limiter is needed.

IF Limiter

The IF limiter is made up of three differential amplifiers with a gain of 63dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. The IF limiter's output resistance is about 260Ω with no internal build-out. The limiter's output signal (Pin 9 onNE604A, Pin 11 on NE605) will vary from a good approximation of a square wave at lower IF frequencies like 455kHz, to a distorted sinusoid at higher IF frequencies, like 21.4MHz.

The basic function of the IF limiter is to apply a tremendous amount of gain to the IF frequency such that the top and bottom of the waveform are clipped. This helps in reducing AM and noise presented upon reception.

Function of IF Section

The main function of the IF section is to clean up the IF frequency from noise and amplitude modulation (AM) that might occur upon reception of the RF signal. If the IF section has too much gain, then one could run into instability problems. This is where crucial layout and insertion loss can help (also addressed later in this paper).

Important Parameters for the IF Section

Limiting: The audio output level of an FM receiver normally does not change with the RF level due to the limiting action. But as the RF signal level continues to decrease, the limiter will eventually run out of gain and the audio level will finally start to drop. The point where the IF section runs out of gain and the audio level decreases by 3dB with the RF input is referred to as the –3dB limiting point.

In the application test circuit, with a 5.1kΩ interstage resistor, audio suppression is dominated by noise capture down to about the –120dBm RF level at which point the phase detector efficiency begins to drop (see Interstage Loss section below).

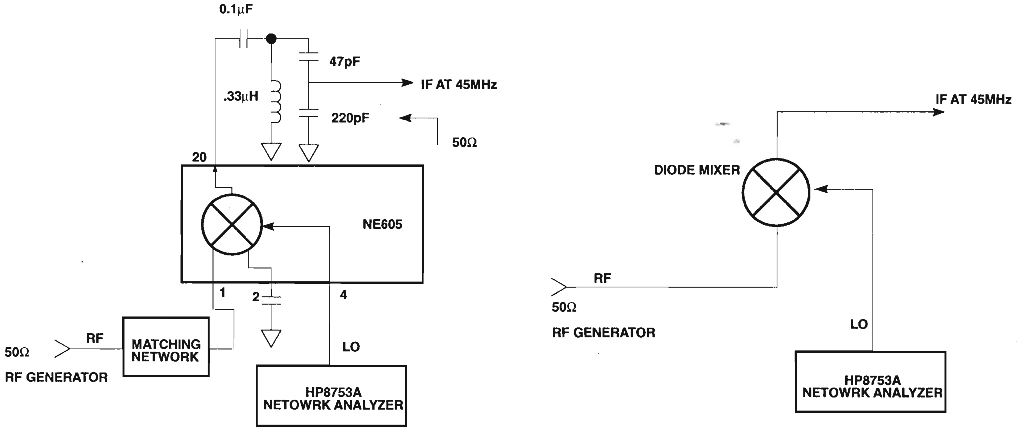


Figure 14. Test Circuits for NE605 Mixer vs Diode Mixer

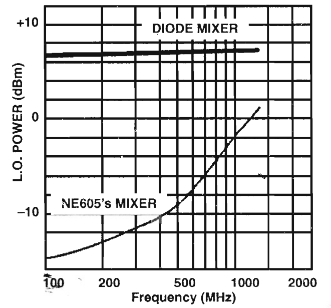


Figure 15. LO Power Requirements (Matched Input)

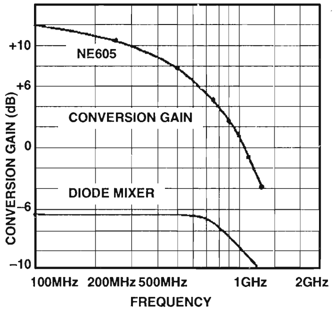


Figure 16. NE605 Conversion Gain vs. Diode Mixer

The audio drop that occurs is a function of two types of limiting. The first type is as follows: As the input signal drops below a level which is sufficient to keep the phase detector compressed, the efficiency of the detector drops, resulting in premature audio attenuation. We will call this "gain limiting". The second type of limiting occurs when there is sufficient amount of gain without de-stabilizing regeneration (i.e. keeping the phase detector fully limited), the audio level will eventually become suppressed as the noise captures the receiver. We will call this "limiting due to noise capture".

Figure 19 shows the 3dB drop in audio at about $0.26\mu V_{RMS}$, with a $-118.7dBm/50\Omega$ RF level for the NE605. Note that the level has not improved by the 11dB gain supplied by the mixer/filter since noise capture is expected to slightly dominate here.

AM rejection: The AM rejection provided by the NE605/604A is extremely good even for 80% modulation indices as depicted in Figures 20a through 20d. This performance results from the 370mV peak signal levels set at the input of each IF amplifier and limiter stage. For this level of compression at the inputs, even better performance could be expected except that finite AM to PM conversion coefficients limit ultimate performance for high level inputs as indicated in Figure 20b.

Low level AM rejection performance degrades as each stage comes out of limiting. In particular as the quadrature phase detector input drops below 100mV peak, all limiting will be lost and AM modulation will be present at the input of the quad detector (See Figure 20d).

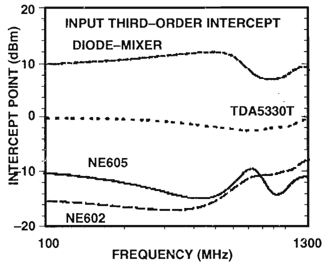


Figure 17. Comparing Different Types of Mixers

AM to PM conversion: Although AM rejection should continue to improve above –95dBm IF inputs, higher order effects, lumped under the term AM to PM conversion, limit the application rejection to about 40dB. In fact this value is proportional to the maximum frequency deviation. That is lower deviations producing lower audio outputs result directly in lower AM rejection. This is consistent with the fact that the interfering audio signal produced by the AM/PM conversion process is independent of deviation within the IF bandwidth and depends to a first estimate on the level of AM modulation present. As an example reducing the maximum frequency deviation to 4kHz from 8kHz, will result in 34dB AM rejection. If the AM modulation is reduced from 80% to 40%, the AM rejection for higher level IFs will go back to 40dB as expected. AM to PM conversion is also not a function of the quad tank Q, since an increase in Q increases both the audio and spurious AM to PM converted signal equally.

As seen above, these relationships and the measured results on the application board (Figure 36) can be used to estimate high level IF AM rejection. For higher frequency IFs (such as 21.4MHz), the limiter's output will start to deviate from a true square wave due to lack of bandwidth. This causes additional AM rejection degradation.

Interstage Loss: Figure 21 plots the simulated IF RSSI magnitude response for various interstage attenuation. The optimum interstage loss is 12dB. This has been chosen to allow the use of various types of filters, without upsetting the RSSI's linearity. In most cases, the filter insertion loss is less than 12dB from point A to point B. Therefore, some additional loss must be introduced externally. The easiest and simplest way is to use an external resistor in series with the internal build out resistor (Pin 14 in the NE604A, Pin 16 in the NE605). Unfortunately, this method mismatches the filter which might be important depending on the design. To achieve the 12dB insertion loss and good matching to the filter, an L-pad configuration can be used. Figure 22 shows the different set-ups.

Below is an example on how to calculate the resistors values for both Figures 22a and 22b.

Step 1.

$$X_{dB} = 20\log\frac{\sqrt{(960 + R_{EXT})\,R_{FLT}}}{960 + R_{EXT} + R_{FLT}} - \text{FIL [dB]}$$

(just solve for R_{EXT})

where
X = the insertions loss wanted in dB
R_{EXT} = the external resistor
R_{FLT} = the filter's input impedance
FIL = insertion loss of filter in dB

2. For our application board
X=12dB
R_{FLT} = 1.5k
FIL = 3dB
Therefore, using the above eq. gives
R_{EXT} = 5.1K

$$R_{EXT} = \left| 960 - \frac{R_{FLT}}{2 \times 10^{\left(\frac{-X_{dB}}{20}\right)}} \right|$$

Step 2.
$$R_{SHUNT} = \frac{R_{FLT}}{1 - 2 \times 10^{\left(\frac{-X_{dB}}{20}\right)}}$$

3. In this case, lets assume: FIL = –2dB therefore, X_{dB} = +10, R_{FLT} = 1.5k. The results are: R_{EXT} = 1.41k, R_{SHUNT} = 4.08k

IF noise figure

The IF noise figure of the receiver may be expected to provide at best a 7.7dB noise figure in a 1.5kΩ environment from about 25kHz to 100MHz. From a 25Ω source the noise figure can be expected to degrade to about 15.4db.

Performance Graphs of IF Section

Fig.	Description
24	IF Amp Gain vs. Temperature with Various Supply Voltages
25	IF Limiter Gain vs. Temperature with Various Supply Voltages
26	IF Amp 20MHz Response vs. Temperature
27	IF Limiter 20MHz Response vs. Temperature

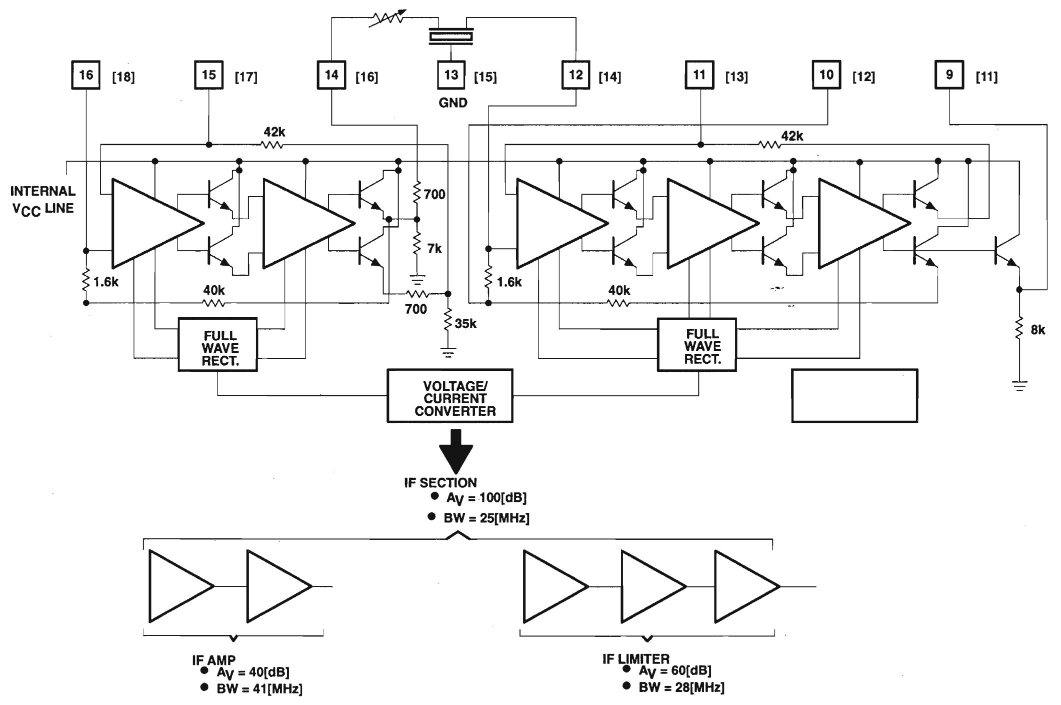


Figure 18. IF Section of NE604A [NE605]

Demodulator Section

Once the signal leaves the IF limiter, it must be demodulated so that the baseband signal can be separated from the IF signal. This is accomplished by the quadrature detector. The detector is made up of a phase comparator (internal to theNE605) and a quadrature tank (external to theNE605).

The phase comparator is a multiplier cell, similar to that of a mixer stage. Instead of mixing two different frequencies, it compares the phases of two signals of the same frequency. Because the phase comparator needs two input signals to extract the information, the IF limiter has a balanced output. One of the outputs is directly connected to the input of the phase comparator. The other signal from the limiter's output (Pin 11) is phase shifted 90 degrees (through external components) and frequency selected by the quadrature tank. This signal is then connected to the other input of the phase comparator (Pin 10 of the NE605). The signal coming out of the quadrature detector (phase detector) is then low-passed filtered to get the baseband signal. A mathematical derivation of this can be seen in the NE604A data sheet.

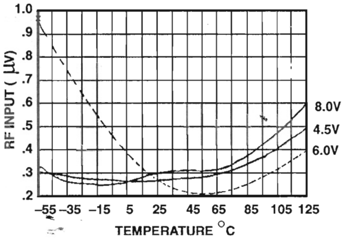


Figure 19. NE605 Application Board, –3dB Limiting (Drop in Audio)

The quadrature tank plays an important role in the quality of the baseband signal. It determines the distortion and the audio output amplitude. If the "Q" is high for the quadrature tank, the audio level will be high, but the distortion will also be high. If the "Q" is low, the distortion will be low, but the audio level will become low. One can conclude that there is a trade-off.

Output Section

The output section contains an RSSI, audio, and data (unmuted audio) outputs which can be found on Pins 7, 8, and 9, respectively, on the NE605. However, amplitude shift keying (ASK), frequency shift keying (FSK), and a squelch control can be implemented from these pins. Information on ASK and FSK can be found in Philips Components-Signetics application note AN1993.

Although the squelch control can be implemented by using the RSSI output, it is not a good practice. A better way of implementing squelch control is by comparing the bandpassed audio signal to high frequency colored FM noise signal from the unmuted audio. When no baseband signal is present, the noise coming out of the unmuted audio output will be stronger, due to the nature of FM noise. Therefore, the output of the external comparator will go high (connected to Pin 5 of the NE605) which will mute the audio output. When a baseband signal is present, the bandpassed audio level will dominate and the audio output will now unmute the audio.

Audio and Unmuted Audio (Data)

The audio and unmuted audio outputs (Pin 8 and 9, respectively, on the NE605) will be discussed in this section because they are basically the same. The only difference between them is that the unmuted audio output is always "on" while the audio output can either be turned "on" or "off". The unmuted audio output (data out) is for signaling tones in systems such as cellular radio. This allows the tones to be processed by the system but remain silent to the user. Since these tones contain information for cellular operation, the unmuted audio output can also be referred to as the "data" output. Grounding Pin 5 on the NE605 mutes the audio on Pin 8 (connecting Pin 5 to V_{CC} unmutes it).

Both of these outputs are PNP current-to-voltage converters with a 55kΩ nominal internal load. The nominal frequency response of the audio and data outputs are 300kHz. However, this response can be increased with the addition of an external resistor (<58kΩ) from the output pins to ground. This will affect the time constant and lower the audio's output amplitude. This technique can be applied to SCA receivers and data transceivers (as mentioned in the NE604A data sheet).

RSSI Output

RSSI (Received Signal Strength Indicator) determines how well the received signal is being captured by providing a voltage level on its output. The higher the voltage, the stronger the signal.

The RSSI output is a current-to-voltage converter, similar to the audio outputs. However, a 91kΩ external resistor is needed to get an output characteristic of 0.5V for every 20dB change in the input amplitude.

As mentioned earlier, the linearity of the RSSI curve depends on the 12dB insertion loss between the IF amplifier and IF limiter. The reason the RSSI output is dependent on the IF section is because of the V/I converters. The amount of current in this section is monitored to produce the RSSI output signal. Thus, the IF amplifier's rectifier is internally calibrated under the assumption that the loss is 12dB.

Because unfiltered signals at the limiter inputs, spurious products, or regenerated signals will affect the RSSI curve, the RSSI is a good indicator in determining the stability of the board's layout. With no signal applied to the front end of the NE605, the RSSI voltage level should read $250mV_{RMS}$ or less to be a good layout. If the voltage output is higher, then this could indicate oscillations or regeneration in the design.

Performance Graphs of Output Section

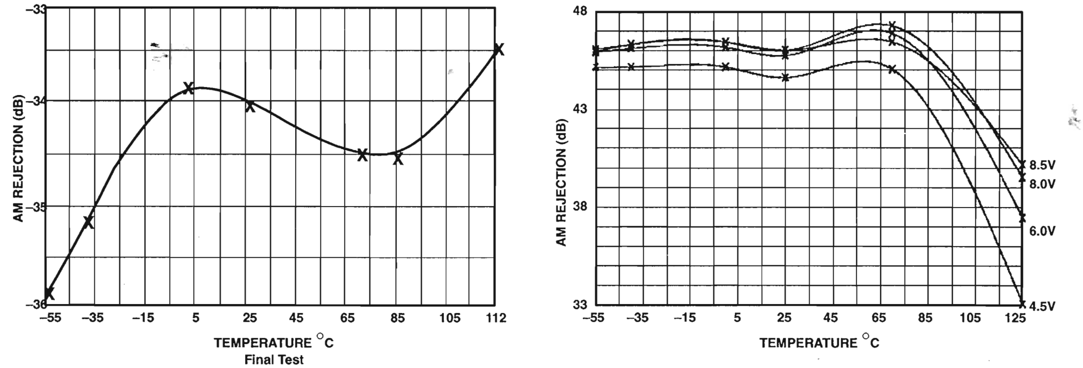
Fig.	Description
28	51kΩ Thermistor in Series with 100kΩ Resistor Across Quad Tank (Thermistor Quad Q Compensation)
29a	NE605 Application Board at –55°C
29b	NE605 Application Board at –40°C
29c	NE605 Application Board at +25°C
29d	NE605 Application Board at +85°C
29e	NE605 Application Board at +125°C
30a	NE604A for –68dBm RSSI Output vs. Temperature at Different Supply Voltages
30b	NE604A for –18dBm RSSI Output vs. Temperature at Different Supply Voltages
30c	NE605 for –120dBm RSSI Output vs. Temperature at Different Supply Voltages
30d	NE605 for –76dBm RSSI Output vs. Temperature at Different Supply Voltages
30e	NE605 for –28dBm RSSI Output vs. Temperature at different Supply Voltages
31	NE605 Audio level vs. Temperature and Supply Voltage
32	NE605 Data Output at –76dBm vs. Temperature

Referring to the NE/SA604A data sheet, there are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can be accomplished by adding attenuation between stages. More details on regeneration and stability considerations can be found in the NE/SA604A data sheet.

III. QUESTIONS & ANSWERS:

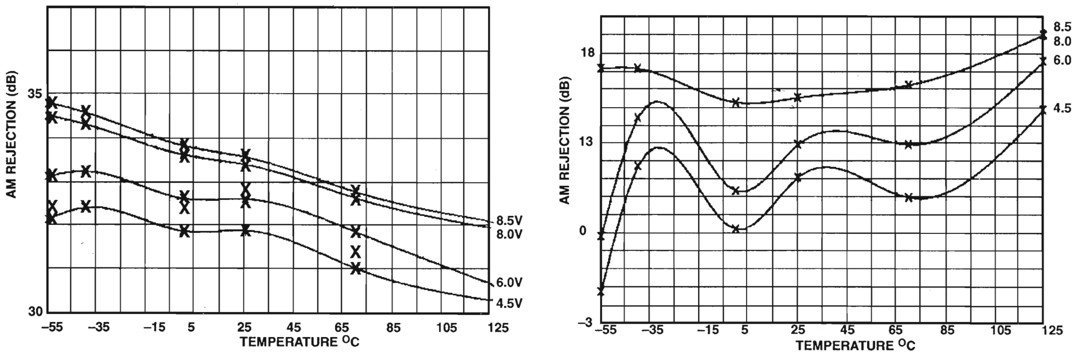
Q.–Bypass. How important is the effect of the power supply bypass on the receiver performance?

A. While careful layout is extremely critical, one of the single most neglected components is the power supply bypass in applications of NE604A or NE605. Although increasing the value of the tantalum capacitor can solve the problem, more careful testing shows that it is actually the capacitor's ESR (Equivalent Series Resistance) that needs to be checked. The simplest way of screening the bypass capacitor is to test the capacitor's dissipation factor at a low frequency (a very easy test, because most of the low frequency capacitance meters display both C, and Dissipation factor).



20a. NE604A Final Test AM Rejection at –68dBm

20b. NE605 AM Rejection at –27dBm



20c. NE605 AM Rejecection at –76dBm

20d. NE605 AM Rejection at –118dBm

Figure 20. AM Rejection Results at Different Input Levels

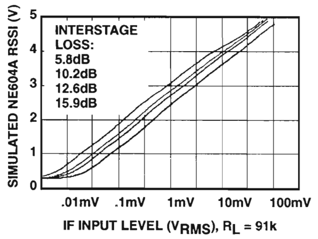


Figure 21. NE604A's RSSI Curve at Different Interstage Losses

Q.–On-chip oscillator. We cannot get the NE605 on-chip oscillator to work. What is the problem?

A. The on board oscillator is just one transistor with a collector that is connected to the supply, an emitter that goes to ground through a 25k resistor, and a base that goes to the supply through an 18k resistor. The rest of the circuit is a buffer that follows the oscillator from the transistor base (this buffer does not affect the performance of the oscillator).

Fundamental mode Colpitts crystal oscillators are good up to 30MHz and can be made by a crystal and two external capacitors. At higher frequencies, up to about 90MHz, overtone crystal oscillators (Colpitts) can be made like the one in the cellular application circuit. At higher frequencies, up to about 170MHz, Butler type oscillators (the crystal is in series mode) have been successfully demonstrated. Because of the 8GHz peak f_T of the transistors, LC Colpitts oscillators have been shown to work up to 900MHz. The problem encountered above 400MHz is that the on-chip oscillator level is not sufficient for optimum conversion gain of the mixer. As a result, an external oscillator should be used at those frequencies.

Generally, about 220mV$_{RMS}$ is the oscillator level needed on Pin 4 for maximum conversion gain of the mixer. An external oscillator driving Pin 4 can be used throughout the band. Finally, since the NE605's oscillator is similar to the NE602, all of the available application notes on NE602 apply to this case (assuming the pin out differences are taken into account by the user).

Below are a couple of points to help in the oscillator design. The oscillator transistor is biased around 250µA which makes it very hard to probe the base and emitter without disturbing the oscillator (a high impedance, low capacitance active FET probe is desirable). To solve these problems, an external 22k resistor (as low as 10k) can be used from Pin 3 to ground to double the bias current of the oscillator transistor. This external resistor is put there to ensure the start up of the crystal in the 80MHz range, and to increase the f_T of the transistor for above 300–400MHz operation. Additionally, this resistor is required for operations above 80–90MHz. When a 1k resistor from Pin 1 to ground is connected on the NE605, half of the mixer will shut off. This causes the mixer to act like an amplifier. As a result, Pin 20 (the mixer, now amplifier output) can be probed to measure the oscillator frequency. Furthermore, the signal at Pin 20 relates to the true oscillator level . This second resistor is just for optimizing the oscillator of course. Without the 1k resistor, the signal at Pin 20 will be a LO feedthrough which is very small and frequency dependent.

Finally in some very early data sheets, the base and emitter pins of the oscillator were inadvertently interchanged. The base pin is Pin 4, and the emitter pin is Pin 3. Make sure that your circuit is connected correctly.

Q.–Sensitivity at higher input frequencies. We cannot get good sensitivity like the 45MHz case at input frequencies above 70MHz. Do you have any information on sensitivity vs. input frequency?

A. The noise figure and the gain of the mixer degrade by less than 0.5dB, going from 50 to 100MHz. Therefore, this does not explain the poor degradation in sensitivity. If other problems such as layout, supply bypass etc. are already accounted for, the source of the problem can be regeneration due to the 70MHz oscillator. What is probably happening is that the oscillator signal is feeding through the IF, getting mixed with the 455kHz signal, causing spurious regeneration. The solution is to reduce the overall gain to stop the regeneration.

This gain reduction can be done in a number of places. Two simple points are the attenuator network before the second filter and the LO level (see Figure 22). The second case will reduce the mixer's noise figure which is not desirable. Therefore, increasing the Interstage loss, despite minimal effect on the RSSI linearity, is the correct solution. As the Interstage loss is increased, the regeneration problem is decreased, which improves sensitivity, despite lowering of the over-all gain (the lowest RSSI level will keep decreasing as the regeneration problem is decreased). For an 81MHz circuit it was found that increasing the Interstage loss from 12dB to about 17dB produced the best results (–119dBm sensitivity). Of course, adding any more Interstage loss will start degrading sensitivity.

Conversely, dealing with the oscillator design, low LO levels could greatly reduce the mixer conversion gain and cause degradation of the sensitivity. For the 81MHz example, a 22k parallel resistor from Pin 3 to ground is required for oscillator operation where a Colpitts oscillator like the one in the cellular application circuit is used. The LO level at Pin 4 should be around 220mV$_{RMS}$ for good operation. Lowering the LO level to approximately 150mV$_{RMS}$ may be a good way of achieving stability if increasing Interstage attenuation is not acceptable. In that case the 22k resistor can be made a thermistor to adjust the LO level vs. temperature for maintaining sensitivity and ensuring crystal start-up vs. temperature. At higher IF frequencies (above 30MHz), the interstage gain reduction is not needed. The bandwidth of the IF section will lower the overall gain. So, the possibility of regeneration decreases.

Q.–Mixer noise figure. How do you measure the mixer noise figure in NE605, and NE602?

A. We use the test circuit shown in the NE602 data sheet. The noise figure tester is the HP8970A. The noise source we use is the HP346B (ENR = 15.46dB). Note that the output is tuned for 10.7MHz. From that test circuit the NF-meter measures a gain of approximately 15dB and 5.5dB noise figure.

More noise figure data is available in the paper titled "Gilbert-type Mixers vs. Diode Mixers" presented at RF Expo '89 in Santa Clara, California. (Reprints available through Signetics Publication Services.)

Q.– What is the value of the series resistor before the IF filter in the NE605 or NE604A applications?

A. A value of 5.1kΩ has been used by us in our demo board. This results in a maximally straight RSSI curve. A lower value of about 1k will match the filter better. A better solution is to use an L pad as discussed earlier in this application note.

Q.– What is the low frequency input resistance of the NE605?

A. The data sheets indicated a worst case absolute minimum of 1.5k. The typical value is 4.7k.

Q.– What are BE-BC capacitors in the NE605 oscillator transistor?

A. The oscillator is a transistor with the collector connected to the supply and the emitter connected to the ground through a 25k resistor. The base goes to the supply through an 18k resistor. The junction capacitors are roughly about 24fF (fempto Farads) for CJE (Base-emitter capacitors), and 44fF for CJC (Collector-base capacitors). There is a 72fF capacitor for CJS (Collector-substrate capacitor). This is all on the chip itself. It should be apparent that the parasitic packaging capacitors (1.5–2.5pF) are the dominant values in the oscillator design.

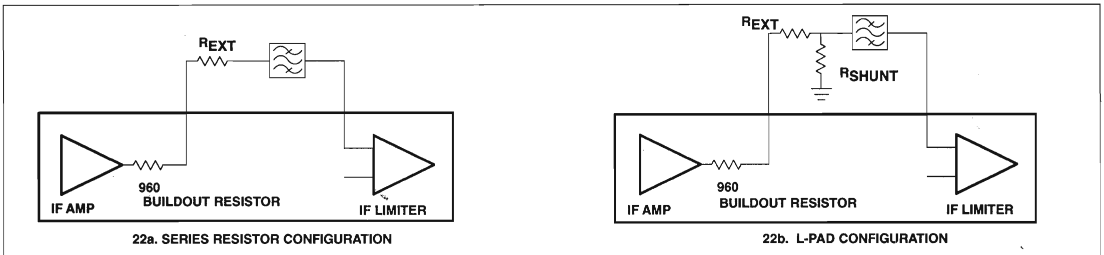


Figure 22. Implementing the 12dB Insertion Loss

Summary of Differences for NE/SA604/604A

	NE/SA604	NE/SA604A
RSSI	No temperature compensation	Internally temperature compensated
IF Bandwidth	15MHz	25MHz
IF Limiter Output	No buffer	Emitter follower buffer output with 8k in the emitter
Current Drain	2.7mA	3.7mA

Q.– What are the differences between the NE604 and NE604A? (see Table below)

A. The NE/SA604A is an improved version of the NE/SA604. Customers, who have been using the NE604 in the past, should have no trouble doing the conversion.

The main differences are that the small signal IF bandwidth is 25MHz instead of 15MHz, and the RSSI is internally temperature compensated. If external temperature compensation was used for the NE604, the designer can now cut cost with the NE604A. The designer can either get rid of these extra parts completely or replace the thermistor (if used in original temperature compensated design) with a fixed resistor.

Those using the NE604 at 455kHz should not see any change in performance. For 10.7MHz , a couple of dB improvement in performance will be observed. However, there may be a few cases where instability will occur after using NE604A. This will be the case if the PC-board design was marginal for the NE604 in the first place. This problem, however, can be cured by using a larger than 10µF tantalum bypass capacitor on the supply line, and screening the capacitors for their ESR (equivalent series resistance) as mentioned earlier. The ESR at 455kHz should be less than 0.2Ω. Since ESR is a frequency dependent value, the designer can correlate good performance with a low frequency dissipation factor, or ESR measurement, and screen the tantalum capacitors in production. There are some minor differences as well. The NE/SA604A uses about 1mA more current than the NE/SA604. An emitter follower has been added at the limiter output to present a lower and more stable output impedance at Pin 9. The DC voltage at the audio and data outputs is approximately 3V instead of 2V in the NE604, but that should not cause any problems. The recovered audio level, on the other hand, is slightly higher in the NE604A which should actually be desirable. Because of these changes, it is now possible to design 21.4MHz IFs using the NE604A, which was not possible with the NE604.

The two chips are identical, otherwise. The customers are encouraged to switch to the NE604A because it is a more advanced bipolar process than the previous generation used in theNE604. As a result we get much tighter specifications on the NE604A.

Q.– How does the NE605 mixer compare with a typical double balanced diode mixer?

A. Some data on the comparison of the conversion gain and LO power requirements are shown in this application note. These two parameters reveal the advantages in using the NE605 mixer.

The only drawback of the NE605 may seem to be its lower third-order intercept point in comparison to a diode mixer. But, this is inherent in the NE605 as a result of the low power consumption. If one compares the conversion gain of the NE605 with the conversion loss of a low cost diode mixer, it turns out that the third-order intercept point, referred to the output, is the same or better in the NE605. Another point to take into account is that a diode mixer cannot be used in the front end of a receiver without a preamp due to its poor noise figure. A third-order intercept analysis shows that the intercept point of the combination of the diode mixer and preamp will be degraded at least by the gain of the preamp. A preamp may not be needed with NE605 because of its superior noise figure.

For more detailed discussion of this topic please refer to the paper titled "Gilbert-type Mixers vs. Diode Mixers").

Q.– How can we use the NE605 for SCA FM reception?

A. The 10.7MHz application circuit described in AN1993 can be used in this case. The LO frequency should be changed and the RF front-end should be tuned to the FM broadcast range. The normal FM signal, coming out of Pin 8 of the NE605, could be expected to have about 1.5µV (into 50Ω) sensitivity for 20dB S/N. This signal should be band-pass filtered and amplified to recover the SCA sub-carrier. The output of that should then go to a PLL SCA decoder, shown on the data sheet of Signetics NE565 phase lock loop, to demodulate the base-band audio. The two outputs of the NE605 Pins 8 and 9 can be used to receive SCA data as well as voice, or features such as simultaneous reception of both normal FM, and SCA. The RSSI output, with its 90dB dynamic range, is useful for monitoring signal levels.

Q.– What is the power consumption of the NE605 or NE604A vs. temperature and V_{CC}?

A. The NE605 consumes about 5.6mA of current at 6V. This level is slightly temperature and voltage dependent as shown in Figure 33. Similar data for the NE604A is shown in Figure 34.

Q.– How can you minimize RF and LO feedthroughs

A. The RF and LO feedthroughs are due to offset voltages at the input of the mixer's differential amplifiers and the imbalance of the parasitic capacitors. A circuit, such as the one shown in Figure 35, can be used to adjust the balance of the differential amplifiers. The circuit connected to Pins 1 and 2 will minimize RF feedthrough while the circuit shown connected to Pin 6 will adjust the LO feedthrough. The only limitation is that if the RF and LO frequencies are in the 100MHz range or higher, these circuits will probably be effective for a narrow frequency range.

Q.– Distortion vs. RF input level. We get a good undistorted demodulated signal at low RF levels, but severe distortion at high RF levels. What is happening?

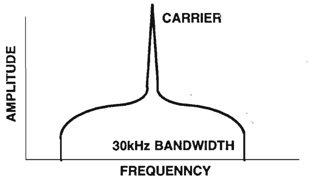
A. This problem usually occurs at 10.7MHz or at higher IF's. The IF filters have not been properly matched on both sides causing a sloping IF response. The resulting distortion can be minimized by adjusting the quad tank at the FM threshold where the IF is out of limiting. As the RF input increases, the IF stages will limit and make the IF response flat again. At this point, the effect of the bad setting of the quad tank will show itself as distortion. The solution is to always tune the quad tank for distortion at a medium RF level, to make sure that the IF is fully limited. Then, to avoid excessive distortion for low RF levels, one should make sure that the IF filters are properly matched.

Q.–The most commonly asked questions: "Why doesn't the receiver sensitivity meet the specifications?"; "Why is the RSSI dynamic range much less than expected?"; "Why does the RSSI curve dip at 0.9V and stay flat at 1V as the RF input decreases?"; "Why does the audio output suddenly burst into oscillation, or output wideband noise as the RF input goes down, instead of dying down slowly?"; "When looking at the IF output with a spectrum analyzer, why do high amplitude spurs become visible near the edge of the IF band as the RF level drops?"

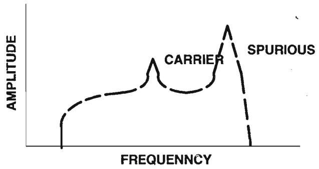
A. These are the most widely observed problems with the NE605. They are all symptoms of the same problem; instability. The instability is due to bad layout and grounding.

Regenerative instability occurs when the limiter's output signals are radiated and picked up by the high impedance inputs of the mixer and IF amp. This signal is amplified by both the IF amp and limiter. Positive feedback causes the signal to grow until the signal at the limiter's output becomes limited. Due to the nature of FM, this instability will dominate any low RF input levels and capture the receiver (see Figure 23).

Since the receiver behaves normally for high RF inputs, it misleads the designer into believing that the design is okay. Additionally the RSSI circuit cannot determine whether the signal being received is coming from the antenna or the result of regenerative instability. Therefore, RSSI will be a good instability indicator in this instance because the RSSI will stay at a high level when the received signal decreases. Looking at the IF spectrum (Pin 11 for 605, Pin 9 for 604A) with the RF carrier present (no modulation), the user will see a shape as shown below. When regenerative instability occurs, the receiver does not seem to have the ultimate sensitivity of which it is capable.



A. CARRIER AND IN BAND NOISE FOR HIGH RF LEVELS



B. FOR LOW RF LEVELS, NOISE AND SPURIOUS SIGNALS CAPTURE THE RECEIVER

Figure 23.

Make sure that a double sided layout with a good ground plane on both sides is used. This will have RF/IF loops on both sides of the board. Follow our layouts as faithfully as you can. The supply bypass should have a low ESR 10–15μF tantalum capacitor as discussed earlier. The crystal package, the inductors, and the quad tank shields should be grounded. The RSSI output should be used as a progress monitor even if is not needed as an output. The lowest RSSI level should decrease as the circuit is made more stable. The overall gain should be reduced by lowering the input impedance of the IF amplifier and IF limiter, and adding attenuation after the IF amplifier, and before the 2nd filter. A circuit that shows an RSSI of 250mV or less with no RF input should be considered close to the limit of the performance of the device. If the RSSI still remains above 250mV, the recommendations mentioned above should be revisited.

Q.– Without the de-emphasis network at the audio output, the –3dB bandwidth of the audio output is limited to only 4.5kHz. The maximum frequency deviation is 8kHz, and the IF bandwidth is 25kHz. What is the problem?

A. What is limiting the audio bandwidth in this case is not the output circuit, but the IF filters. Remember that Carson's rule for FM IF bandwidth requires the IF bandwidth to be at least:

2(Max frequency Dev. + Audio frequency)

With a 25kHz IF bandwidth and 8kHz frequency deviation, the maximum frequency that can pass without distortion is approximately 4.5kHz. 2(8kHz + 4.5kHz) is 25kHz as expected.

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"Gilbert-type Mixers vs. Diode Mixers", proceedings of R.F. Expo 1989, Fotowat, A., Murthi, E., pp. 409-413.

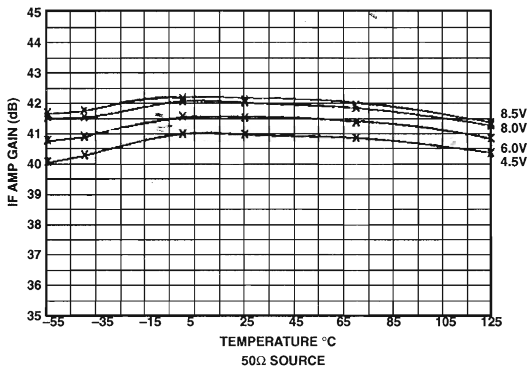


Figure 24. IF Amplifier Gain

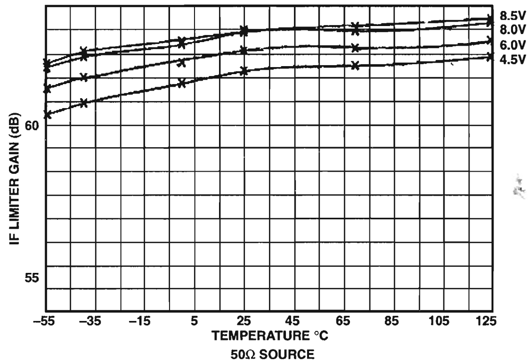


Figure 25. IF Limiter Gain

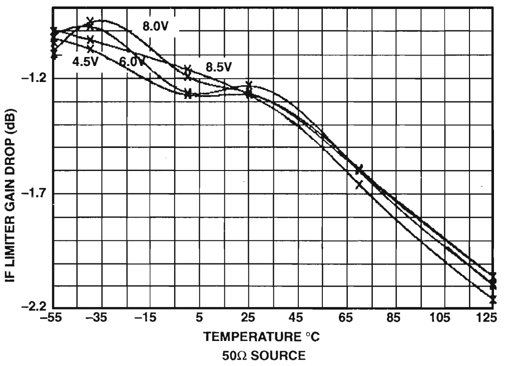


Figure 26. IF Amplifier Gain Drop, 20MHz Response

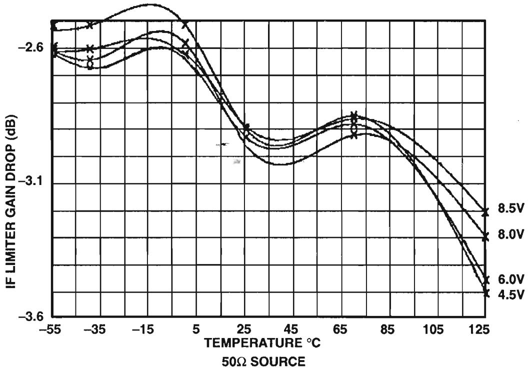


Figure 27. IF Limiter Drop, 20MHz Response

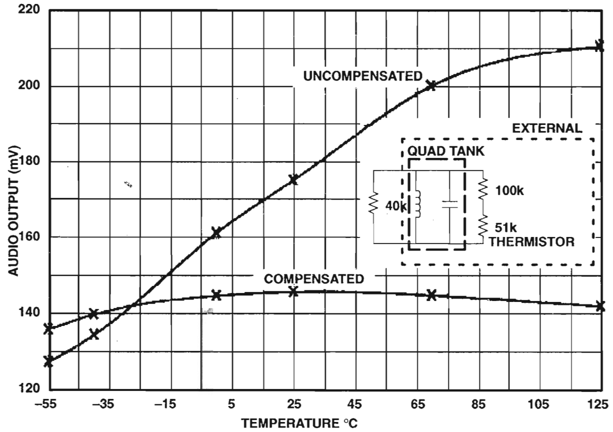
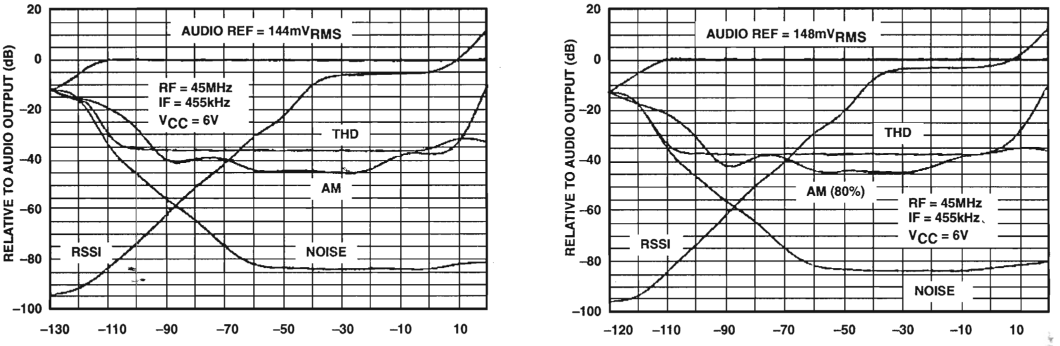
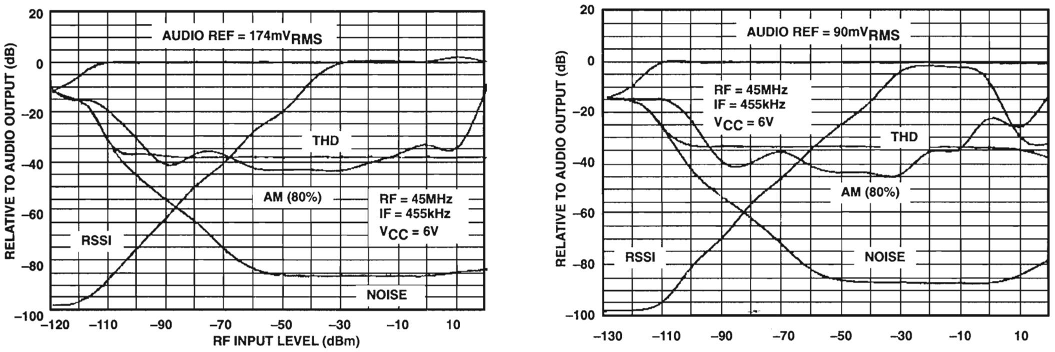


Figure 28. Audio Output: Compensated vs Uncompensated



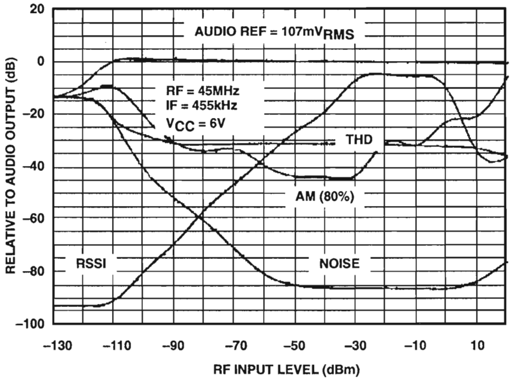
29a. NE605 Application Board at –55°C

29b. NE605 Application Board at –40°C



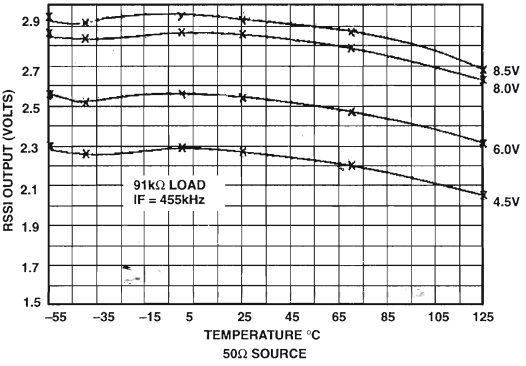
29c. NE605 Application Board at 25°C

29d. NE605 Application Board at 85°C

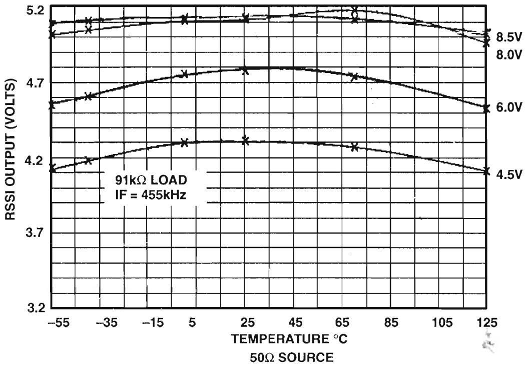


29e. NE605 Application Board at 125°C

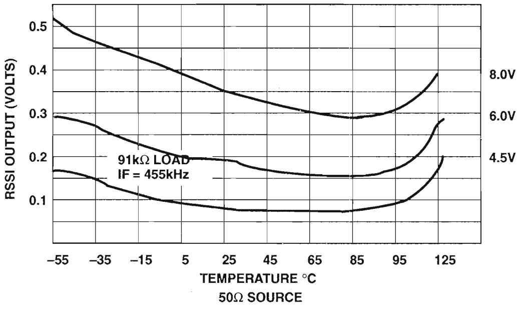
Figure 29. Performance of the NE605 Application Board at Different Temperatures



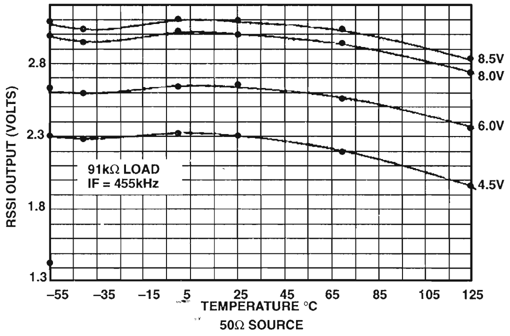
30a. NE604A for –68dBm, RSSI Output



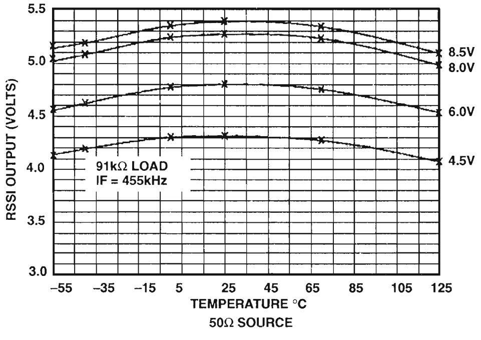
30b. NE604A for –18dBm, RSSI Output



30c. NE605 RSSI at –120dBm



30d. NE605 RSSI, –76dBm



30e. NE605 RSSI at –28dBm

Figure 30. RSSI Response for Different Inputs

Reviewing key areas when designing with the NE605 AN1994

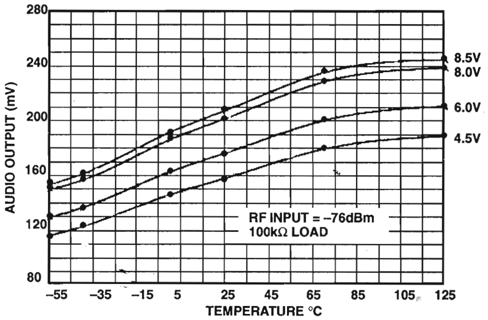


Figure 31. Audio Level vs Temperature and Supply Voltage

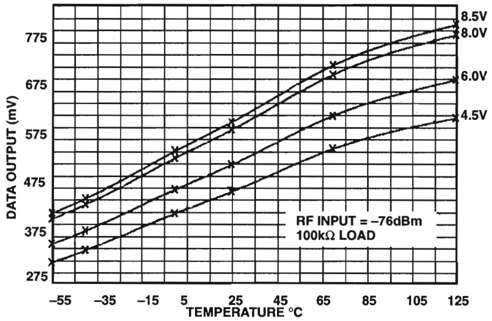


Figure 32. Data Level vs Temperature and Supply Voltage

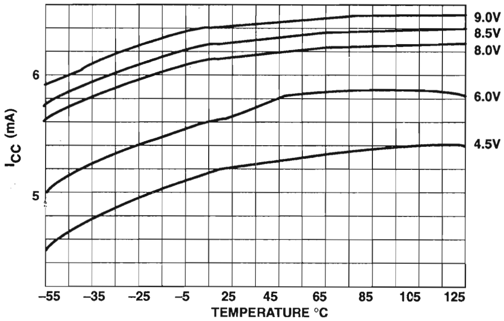


Figure 33. NE605 I_{CC} vs Temperature

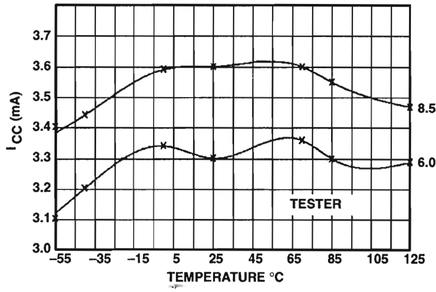


Figure 34. NE604A I_{CC} vs Temperature

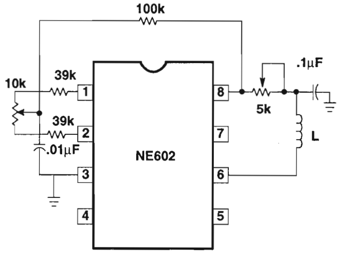
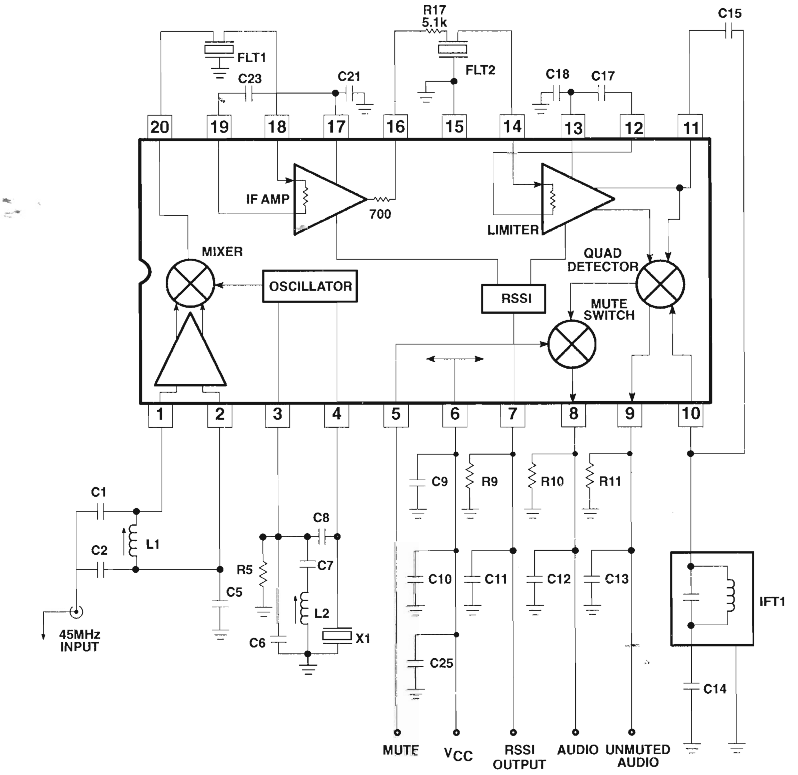


Figure 35. Minimizing RF and LO Feedthrough



Application Component List

C1	47pF NPO Ceramic
C2	180pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8µF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic

C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	3.3µH nominal Toko 292CNS–T1046Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R5	Not Used in Application Board (see Note 8)
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

* NOTE: This value can be reduced when a battery is the power source.

Figure 36. NE/SA605 45MHz Application Circuit

Reviewing key areas when designing with the NE605

AN1994

Table 1. Related Application Notes

App. Note	Date	Title	Main Topics
AN198	Feb. 1987	Designing with the NE/SA602	– Advantages/Disadvantages to single-ended or balanced matching
AN1981	Dec. 1988	New Low Power Single Sideband Circuits	– General discussion on SSB circuits – Audio processing – Phasing-filter technique
AN1982	Dec. 1988	Applying the Oscillator of the NE602 in Low Mixer Applications	– Oscillator configurations
AN199	Feb. 1987	Designing with the NE/SA604	Circuits of: – AM synchronous det. – Temp. compensated RSSI circuit – Field strength meter – Product detector
AN1991	Dec. 1988	Audio Decibel Level Detector with Meter Driver	– Uses of the 604 in application
AN1993	Dec. 1988	High Sensitivity Application Low-Power RF/IF Integrated Circuits	– An overview of the NE602 and NE604 in typical applications – Good information before getting started

Table 2. Comparing Balanced vs Unbalanced Matching

NE605 or NE602	Matching	Advantages	Disadvantages
Pins 1 and 2 (RF input)	Single-ended (unbalanced)	– Very simple circuit – No sacrifice in 3rd-order performance	– Increase in 2nd-order products
	Balanced	– Reduce 2nd-order products	– Impedance match difficult to achieve

Table 3. LO Configurations

LO (MHz)	Suggested Configuration Using On-board Oscillator
0 - 30	Fundamental mode, use Colpitts
30 - 70	3rd overtone mode, use Colpitts
70 - 90	3-5th overtone mode, use Colpitts with 22kΩ resistor connected from the emitter pin to ground
90 - 170	Use Butler, crystal in series mode, and a 22kΩ resistor connected from the emitter pin to ground
170 - 300	LC configuration

Evaluating the NE605 SO and SSOP demo-board

AN1995

Author: Alvin K. Wong

INTRODUCTION:

With the increasing demand for smaller and lighter equipment, designers are forced to reduce the physical size of their systems. There are several approaches to solving the size problem. A designer needs to look for sophisticated integrated single chip solutions, chips that are smaller in size, and chips that require minimum external components.

Philips Semiconductors offers all of these solutions in their NE605. The NE605 single-chip receiver converts the RF signal to audio and is available in three packages: DIP,SO, and SSOP. This offers total flexibility for layout considerations. The SSOP package is the smallest 20 pin package available in the market today, and allows the designer the flexibility to reduce the overall size of a layout.

When working with a smaller and tighter layout in a receiver design, it becomes important to follow good RF techniques. This application note shows the techniques used in the SO and SSOP demo-board. It does not cover the basic functionality of the NE605 but instead focuses more on the layout constraints. This application note also has a trouble-shooting chart to aid the designer in evaluating the SO and SSOP demo-board. For a complete explanation of the NE605, please refer to application note AN1994 which describes the basic block diagrams, reviews the common problems encountered with the NE605, and suggests solutions to them. Reading AN1994 is highly recommended before attempting the SO and SSOP layout.

The recommended layout demonstrates how well the chip can perform. But it should be pointed out that the combination of external parts with their tolerances plays a role in achieving maximum sensitivity.

The minimum and maximum 12dB SINAD measurement for both boards is -118dBm and -119.7dBm, respectively. A typical reading taken in the lab for both SO and SSOP demo-boards is -119dBm.

There were two different design approaches for both layouts. For the SO layout, there are inductive tuning elements (except for the LO section); for the SSOP layout there are capacitive tuning elements. This approach was taken to show the designer that both ways can be used to achieve the same 12dB SINAD measurement. However, it is worth mentioning that capacitive tuning elements are less expensive than the inductive tuning elements.

Packages Available

As mentioned above, there are three packages available for the NE605. See the "Package Outline" section of the Philips Semiconductors 1992 RF Handbook for the physical dimensions of all three packages. Notice that the DIP package is the largest of the three in physical size; the SSOP is the smallest. The recommended layout and performance graphs for the DIP package are shown in the NE605 data sheet and AN1994. But the SO and SSOP recommended layout and performance graphs are shown in this application note.

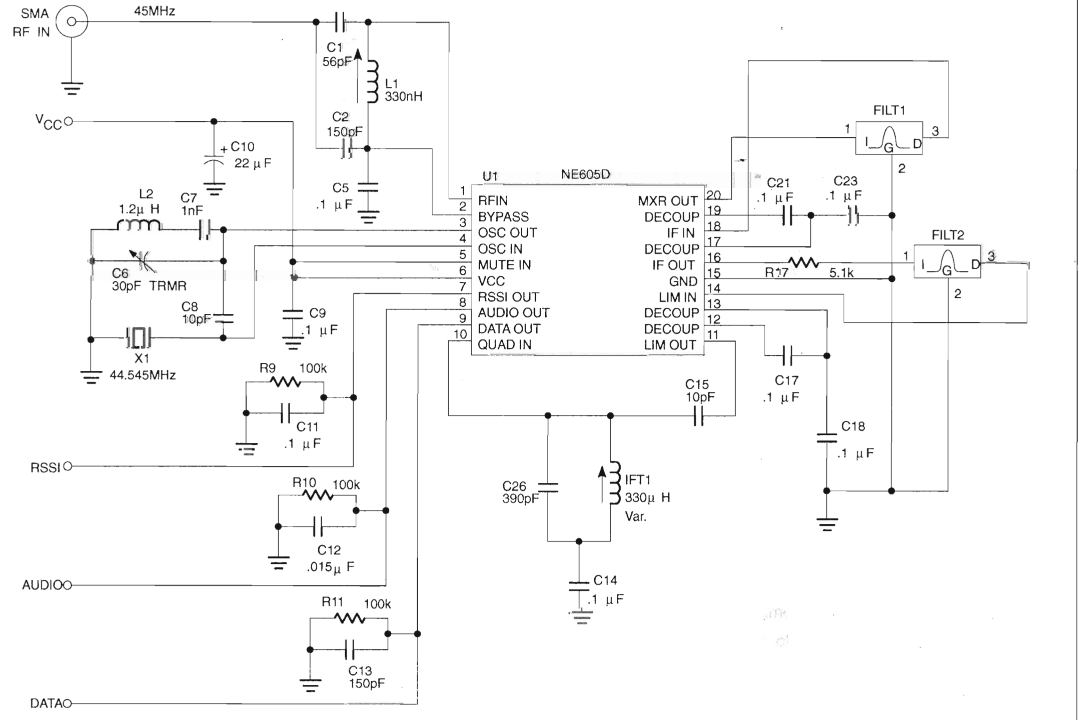


Figure 1. NE605 Schematic for the SO Layout

Evaluating the NE605 SO and SSOP demo-board

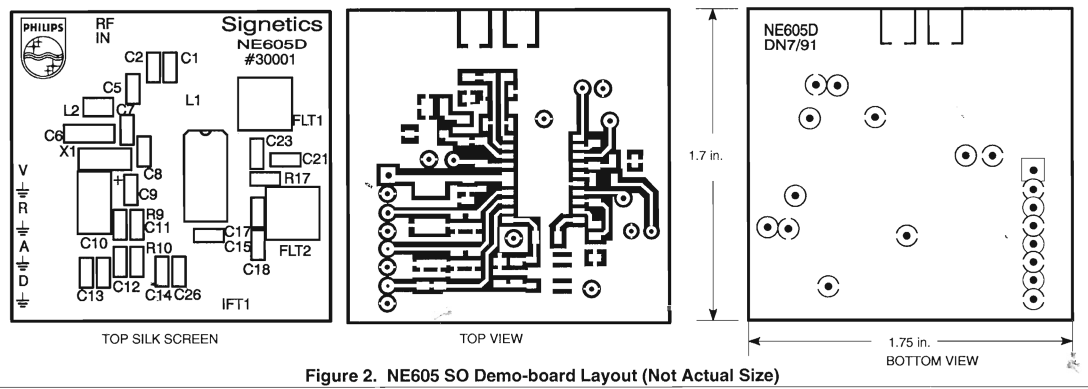


Figure 2. NE605 SO Demo-board Layout (Not Actual Size)

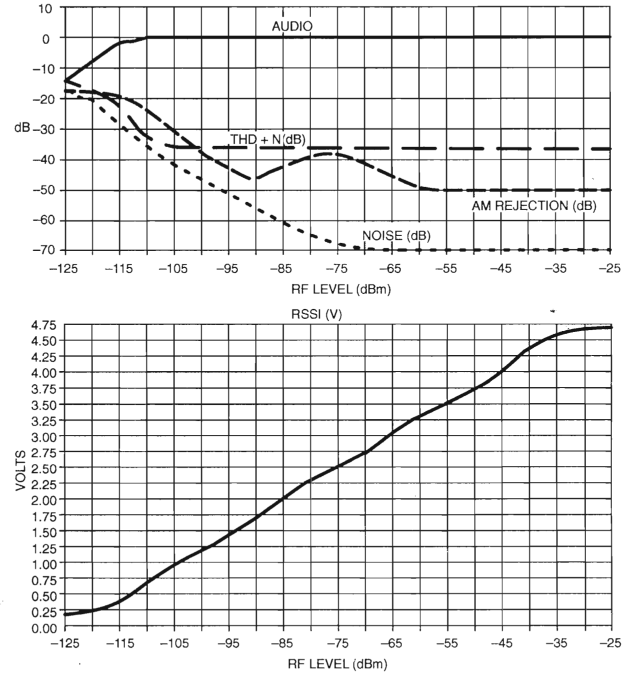


Figure 3. NE605 SO Performance Curves

SO LAYOUT:

Figure 1 shows the schematic for the SO layout. Listed below are the basic functions of each external component for Figure 1.

C1 – Part of the tapped-C network to match the front-end

C2 – Part of the tapped-C network to match the front-end

C5 – Used as an AC short to Pin 2

C6 – Used to tune the LO for the Colpitts oscillator

C7 – Used as part of the Colpitts oscillator

C8 – Used as part of the Colpitts oscillator

C9 – Supply bypassing

C10 – Supply bypassing

C11 – Used as filter

C12 – Used as filter

C13 – Used as filter

C14 – Used to AC ground the Quad tank

C15 – Used to provide the 90° phase shift to the phase detector

C17 – IF limiter decoupling cap

C18 – IF limiter decoupling cap
C21 – IF amp decoupling cap
C23 – IF amp decoupling cap
C26 – Quad tank component
L1 – Part of tapped-C network to match the front-end TOKO 5CB-1320Z
L2 – Part of the Colpitts oscillator Coilcraft 1008CS-122
R9 – Used to convert the current into the RSSI voltage
R10 – Converts the audio current to a voltage
R11 – Converts the data current to a voltage
R17 – Used to achieve the –12dB insertion loss
IFT1 – Inductor for the Quad tank TOKO 303LN-1130
FILT1 – Murata SFG455A3 455kHz bandpass filter
FILT2 – Murata SFG455A3 455kHz bandpass filter
X1 – Standard 44.545MHz crystal in QC38 package

The recommended SO layout can be found in Figure 2 and should be used as an example to help designers get started with their projects.

The SO NE605 board performance graphs can be found in Figure 3.

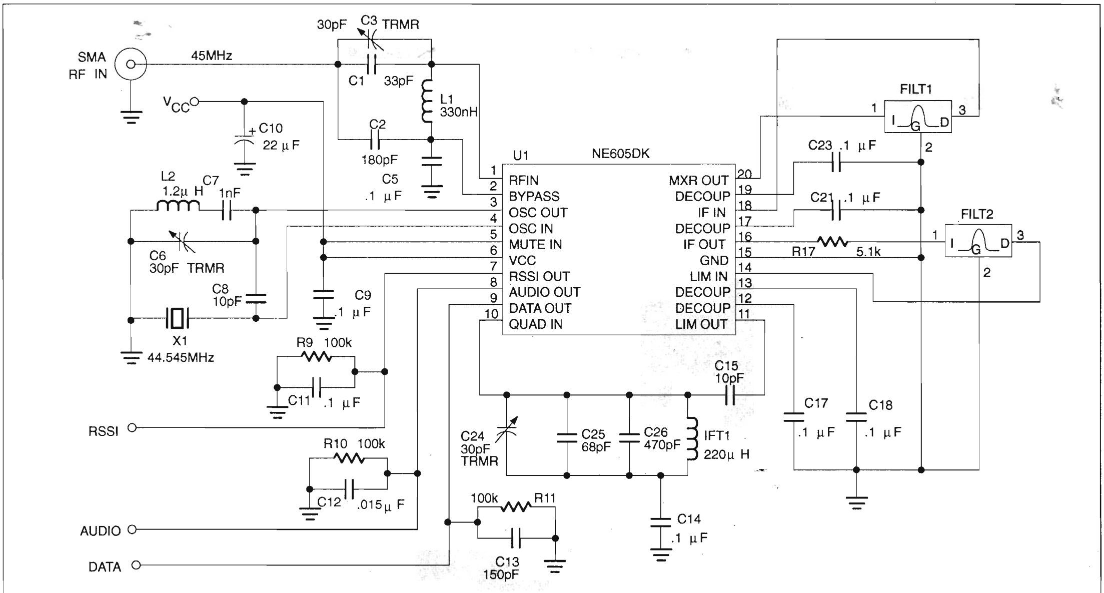


Figure 4. NE605 Schematic for the SSOP Layout

SSOP LAYOUT:

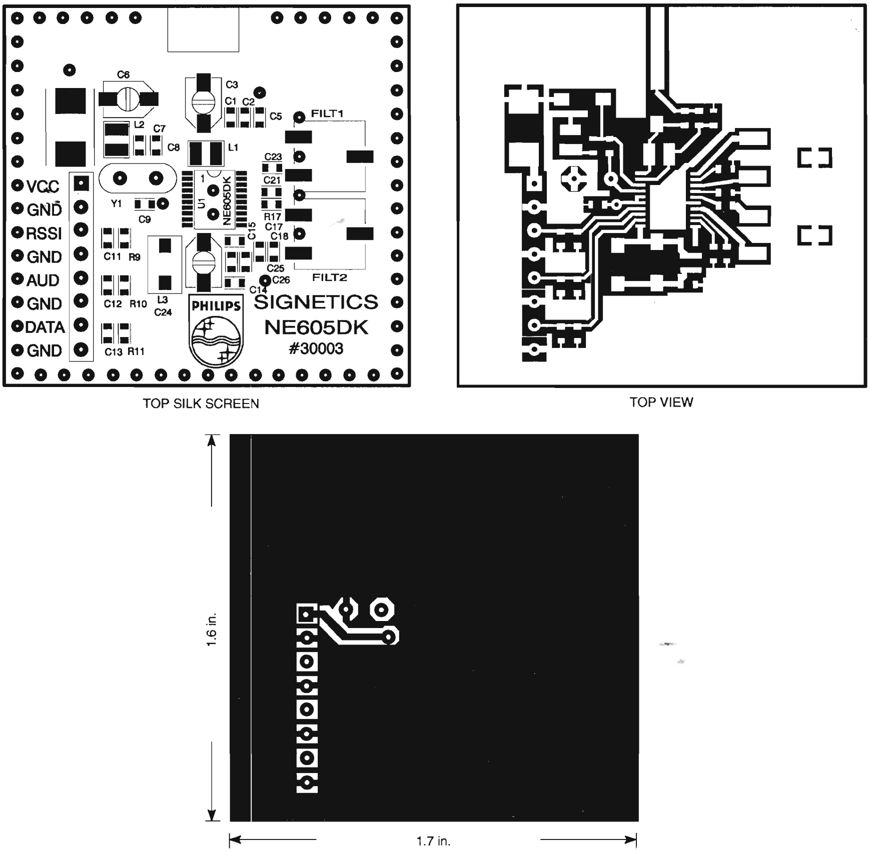
Figure 4 shows the schematic for the SSOP layout.

C1 – Part of the tapped-C network to match the front-end
C2 – Part of the tapped-C network to match the front-end
C3 – Part of the tapped-C network to match the front-end
C5 – Used as an AC short to Pin 2
C6 – Used to tune the LO for the Colpitts oscillator
C7 – Used as part of the Colpitts oscillator
C8 – Used as part of the Colpitts oscillator
C9 – Supply bypassing
C10 – Supply bypassing
C11 – Used as filter
C12 – Used as filter
C13 – Used as filter
C14 – Used to AC ground the Quad tank
C15 – Used to provide the 90° phase shift to the phase detector
C17 – IF limiter decoupling cap
C18 – IF limiter decoupling cap
C21 – IF amp decoupling cap
C23 – IF amp decoupling cap
C24 – Part of the Quad tank
C25 – Part of the Quad tank
C26 – Part of the Quad tank
L1 – Part of tapped-C network to match the front-end Coilcraft 1008CS-331
L2 – Part of the Colpitts oscillator Coilcraft 1008CS-122
R9 – Used to convert the current into the RSSI voltage
R10 – Converts the audio current to a voltage
R11 – Converts the data current to a voltage
R17 – Used to achieve the –12dB insertion loss
IFT1 – Inductor for the Quad tank Mouser ME435-2200
FILT1 – Murata SFGCC455BX 455kHz bandpass filter
FILT2 – Murata SFGCC455BX 455kHz bandpass filter
X1 – Standard 44.545MHz crystal

The SSOP layout can be found in Figure 5. The SSOP NE605 board performance graphs can be found in Figure 7.

Evaluating the NE605 SO and SSOP demo-board

The main difference between the SO and SSOP demo-boards is that the SSOP demo-board incorporates the low profile 455kHz Murata ceramic filter. It has an input and output impedance of 1.0kΩ. This presents a mismatch to our chips, but we have found that the overall performance is similar to that when we use the “blue” Murata filters that have the proper 1.5kΩ input and output impedance.



TOP SILK SCREEN

TOP VIEW

BOTTOM VIEW

Figure 5. NE605 SSOP Demo-board Layout (Not Actual Size)

Evaluating the NE605 SO and SSOP demo-board

AN1995

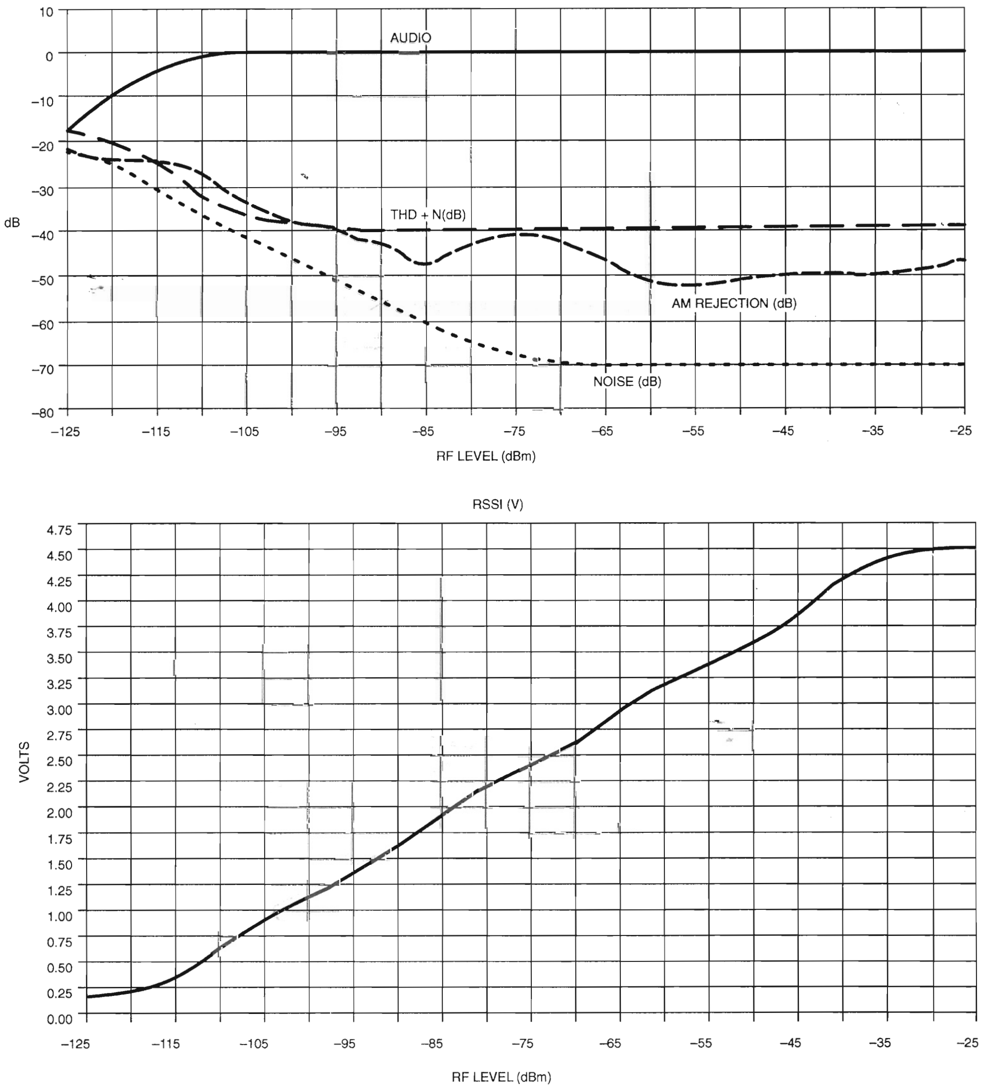
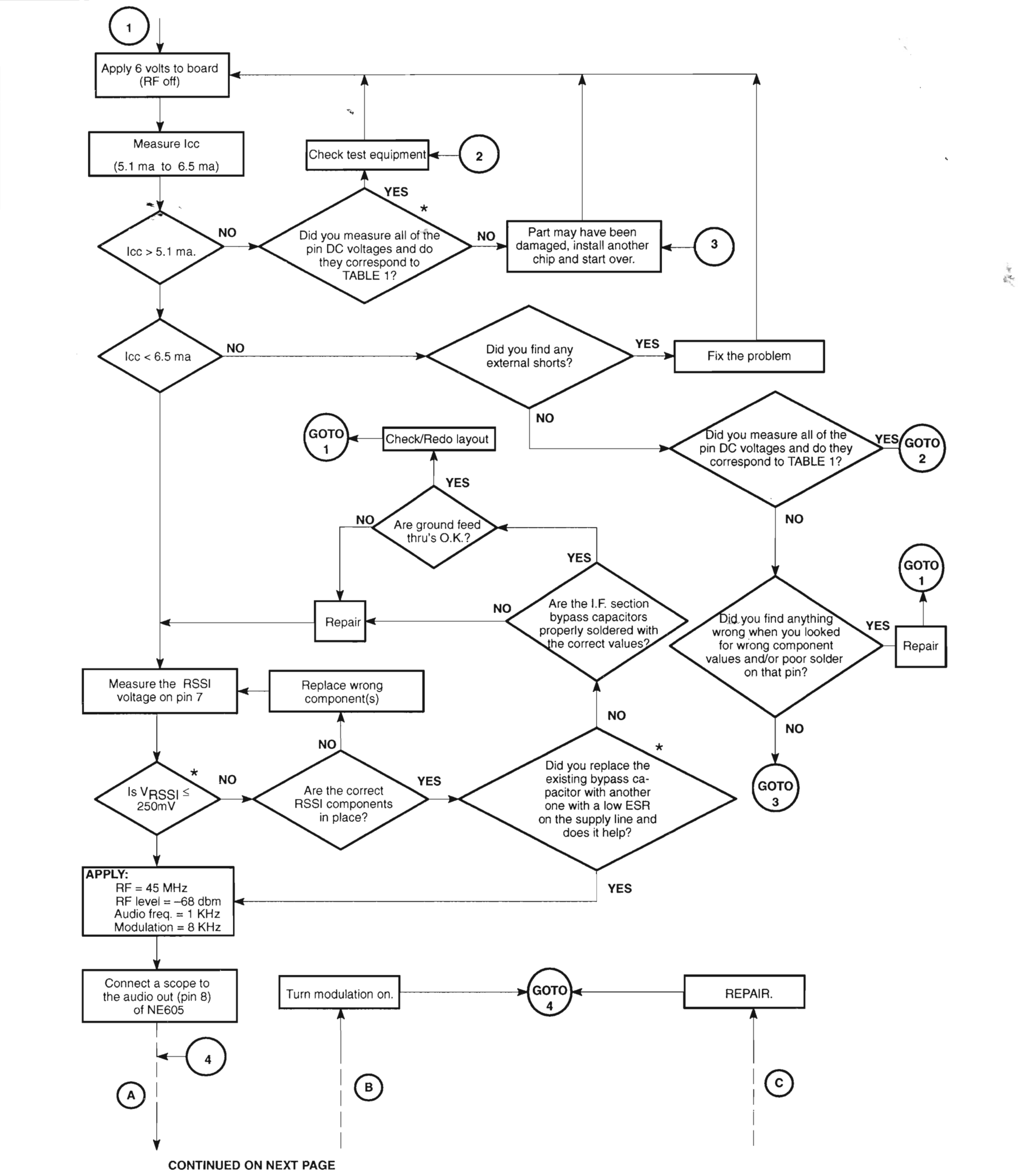


Figure 6. NE605 SSOP Performance Graphs

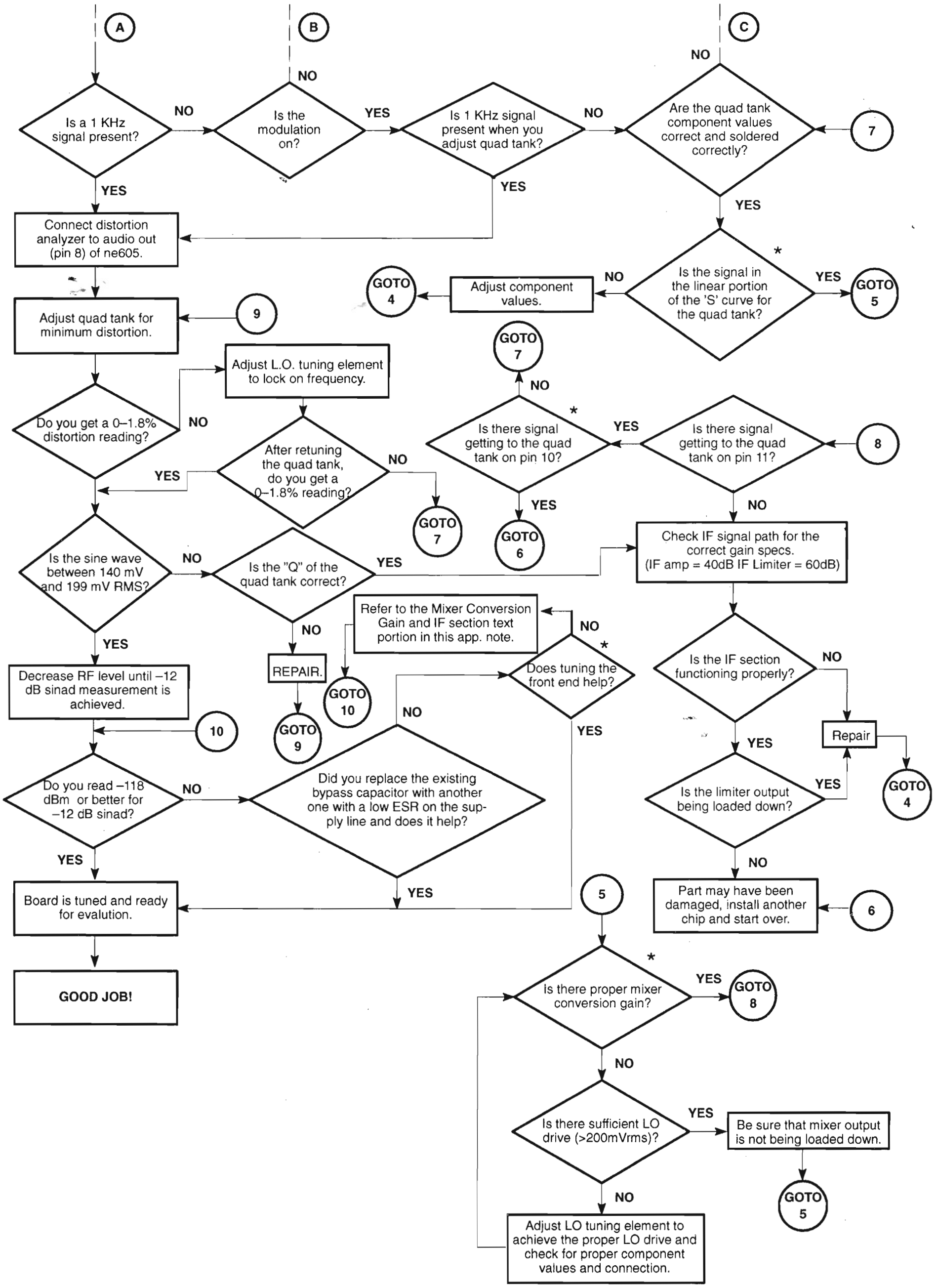
HOW TO TUNE THE NE605 DEMO-BOARD

Figure 7 shows a trouble-shooting chart for the NE605. It can be used as a general guide to tune the DIP, SO, and SSOP demo-boards. Below are some of the highlights from the trouble shooting chart that are explained in more detail.


1
Apply 6 volts to board (RF off)
Measure Icc (5.1 ma to 6.5 ma)
Check test equipment
2
YES
*
Icc > 5.1 ma.
NO
Did you measure all of the pin DC voltages and do they correspond to TABLE 1?
NO
Part may have been damaged, install another chip and start over.
3
Icc < 6.5 ma
NO
Did you find any external shorts?
YES
Fix the problem
NO
GOTO 1
Check/Redo layout
YES
Did you measure all of the pin DC voltages and do they correspond to TABLE 1?
YES
GOTO 2
NO
NO
Are ground feed thru's O.K.?
YES
GOTO 1
Repair
NO
Are the I.F. section bypass capacitors properly soldered with the correct values?
Did you find anything wrong when you looked for wrong component values and/or poor solder on that pin?
YES
Repair
Measure the RSSI voltage on pin 7
Replace wrong component(s)
NO
NO
NO
GOTO 3
*
Is $V_{RSSI} \leq$ 250mV
NO
Are the correct RSSI components in place?
YES
*
Did you replace the existing bypass capacitor with another one with a low ESR on the supply line and does it help?
YES
APPLY:
RF = 45 MHz
RF level = –68 dbm
Audio freq. = 1 KHz
Modulation = 8 KHz
Connect a scope to the audio out (pin 8) of NE605
Turn modulation on.
GOTO 4
REPAIR.
4
A
B
C

CONTINUED ON NEXT PAGE

Figure 7. Trouble-shooting Chart for the NE605 Demo-board


A
B
C
Is a 1 KHz signal present?
NO
YES
Is the modulation on?
NO
YES
Is 1 KHz signal present when you adjust quad tank?
NO
YES
Are the quad tank component values correct and soldered correctly?
7
YES
Connect distortion analyzer to audio out (pin 8) of ne605.
Is the signal in the linear portion of the 'S' curve for the quad tank?
*
NO
YES
GOTO 5
Adjust component values.
GOTO 4
Adjust quad tank for minimum distortion.
9
GOTO 7
Adjust L.O. tuning element to lock on frequency.
Do you get a 0–1.8% distortion reading?
NO
YES
After retuning the quad tank, do you get a 0–1.8% reading?
NO
GOTO 7
Is there signal getting to the quad tank on pin 10?
*
NO
YES
GOTO 6
Is there signal getting to the quad tank on pin 11?
YES
NO
8
Check IF signal path for the correct gain specs. (IF amp = 40dB IF Limiter = 60dB)
Is the sine wave between 140 mV and 199 mV RMS?
NO
YES
Is the "Q" of the quad tank correct?
YES
NO
REPAIR.
GOTO 9
Refer to the Mixer Conversion Gain and IF section text portion in this app. note.
GOTO 10
Does tuning the front end help?
*
NO
YES
Is the IF section functioning properly?
NO
YES
Repair
GOTO 4
Decrease RF level until −12 dB sinad measurement is achieved.
10
Do you read −118 dBm or better for −12 dB sinad?
NO
YES
Did you replace the existing bypass capacitor with another one with a low ESR on the supply line and does it help?
NO
YES
Is the limiter output being loaded down?
YES
NO
Board is tuned and ready for evalution.
5
Part may have been damaged, install another chip and start over.
6
GOOD JOB!
Is there proper mixer conversion gain?
*
YES
GOTO 8
NO
Is there sufficient LO drive (>200mVrms)?
YES
Be sure that mixer output is not being loaded down.
GOTO 5
NO
Adjust LO tuning element to achieve the proper LO drive and check for proper component values and connection.

*NOTE: Refer to the appropriate text section of the app. note for further details.

Evaluating the NE605 SO and SSOP demo-board

AN1995

How to tell when a part is damaged

Since most SO and SSOP sockets hinder the maximum performance of the NE605, it is advisable to solder the packages directly to the board. By this approach, one will be able to evaluate the part correctly. However, it can be a tedious chore to switch to another part using the same layout. Therefore, to be absolutely certain that the chip is damaged, one can measure the DC voltages on the NE605. Table 8 shows the DC voltages that each pin should roughly have to be a good part.

Table 8. Approximate DC Voltages for the NE605

Pin Number	DC Voltage (V)
1	1.37
2	1.37
3	5.16
4	5.94
5	N/A
6	6.00 (V_{CC})
7	N/A
8	2.00
9	2.00
10	3.49
11	1.59
12	1.59
13	1.59
14	1.65
15	0.00 (GND)
16	1.60
17	1.60
18	1.60
19	1.60
20	4.87

Note: The DC voltage on Pin 5 is not specified because it can either be V_{CC} or ground depending if the audio is muted or not (Connecting ground on Pin 5 mutes the audio on Pin 8, while V_{CC} on Pin 5 unmutes the audio).

The DC voltage on Pin 7 is not specified because its DC voltage depends on the strength of the RF signal getting to the input of the NE605. It also can be used as a stability indicator.

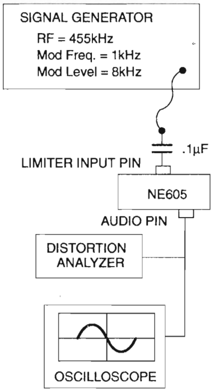
If any of the DC voltages are way off in value, and you have followed the trouble-shooting chart, the part needs to be changed.

RSSI Indicator

The next important highlight is using the RSSI pin as a stability indicator. With power connected to the part and no RF signal applied to the input, the DC voltage should read 250mV or less on Pin 7. Any reading higher than 250mV, indicates a regeneration problem. To correct for the regeneration problem, one should check for poor layout, poor bypassing, and/or poor solder joints. Bypassing the NE605 supply line with a low equivalent series resistance (ESR) capacitor to reduce the RSSI reading can improve the 12dB SINAD measurement by 8dB, as found in the lab. If the regeneration problem still exists, read AN1994.

Quad tank and S-Curve

As briefly mentioned in the chart, it is important to measure the Q of the quad tank if a distortion reading of 1.8% or less cannot be measured. Recall that if the Q of the quad tank is too high for the deviation, then premature distortion will occur. However, if the Q is too low for the deviation, the audio level will be too low. The audio level coming out of the audio pin should be 140mV$_{RMS}$ to 190mV$_{RMS}$.



FREQ. kHz	DC VOLTAGE (V)
400	1.66
430	1.24
455	2.13
480	3.08
510	2.88
⋮	⋮

Figure 8. Test Set-up to Measure S-Curve of the Quad Tank

If the distortion reading is too high and/or the audio level is too low, then it is important to measure and plot the S-curve of the quad tank. The test set-up used in the lab can be seen in Figure 8.

The following steps were taken to measure the S-curve for the SO and SSOP demo-boards.

Step 1. Remove the second IF ceramic filter from the demo-board.

Step 2. Connect a signal generator to the limiters input through a DC blocking capacitor.

Step 3. Connect a DC voltmeter and an oscilloscope to the audio output pin.

Step 4. Set the signal generator to a 455kHz signal and be sure that the modulation is on (RF=455kHz Mod Freq = 1kHz Mod Level=8kHz). Apply this 455Khz signal to the limiter input such that there is a sinewave on the oscilloscope screen. Adjust the quad tank for maximum sinewave amplitude on the oscilloscope or for lowest distortion. Additionally, adjust the supply input signal to the NE605 such that the 1kHz sinewave reaches its maximum amplitude.

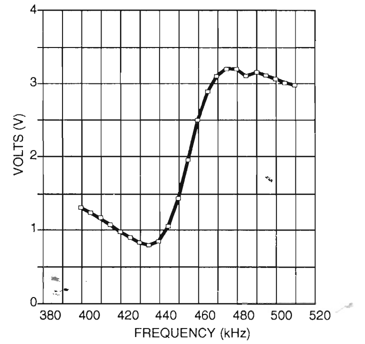


Figure 9. S-Curve for NE605 SO Demo-board

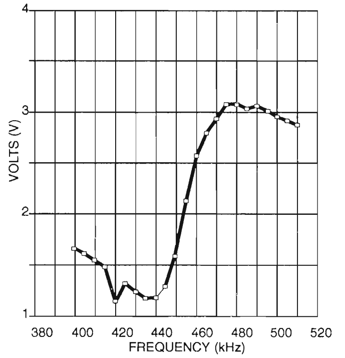


Figure 10. S-Curve for NE605 SSOP Demo-board

Step 5. Turn off the modulation and start taking data. Measure the Frequency vs DC voltage. Vary the frequency incrementally and measure the DC voltage coming out of the audio pin. Remember that once the modulation is turned off, the sine-wave will disappear from the oscilloscope screen.

Step 6. Plot the S-curve.

Figures 9 and 10 show the S-curve measurements for the SO and SSOP demo-boards. Notice that the center of the S-curve is at 455kHz. The overall linearity determines how much deviation is allowed before premature distortion. Since our application requires ±8kHz of deviation, our S-curve is good because it exceeds the linear range of 447kHz to 463kHz.

If the Q of the quad tank needs to be lowered, a designer should put a resistor in parallel with the inductor. The lower the resistor value, the more the Q will be lowered. If the Q needs to be increased, choose a higher Q component. More information on the Quad tank can be found in the NE604A data sheet.

If the linear section of the S-curve is not centered at 455kHz, the quad tank component values need to be recalculated. The way to determine the component values is by using $F = \frac{1}{2\pi\sqrt{LC}}$ where F should be the IF frequency. In the case of the demo-boards, the IF = 455kHz.

Front End Tuning

The best way to tell if the front end of the NE605 is properly matched is to use a network analyzer in a S11 setting. The lower the dip, the greater the absorption of the wanted frequency. Figures 11 and 12 show the S11 dip for the front end matching of the SO and SSOP demo-boards, respectively.

We have found in the lab that a -8dB to -10dB dip is usually sufficient to get the maximum signal transfer such that a good 12dB SINAD reading is met. The front end circuit uses a tapped-C impedance transformation circuit which matches the 50Ω source with the input impedance of the mixer.

In the process of matching the front end, we have found that the ratio of the two capacitors play an important role in transferring the signal from the source to the mixer input. There should be approximately a 4:1 or 5:1 ratio.

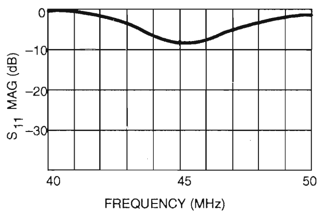


Figure 11. S11 Front-End Response for SO Demo-board

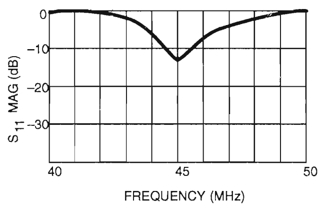


Figure 12. S11 Front-End Response for SSOP Demo-board

Checking the Conversion Gain of the Mixer

Once the front end has been properly matched, a designer should check the conversion gain if there are problems with the SINAD measurement. Be sure to turn off the modulation when making this measurement.

The method of measuring conversion gain on the bench is fairly simple. For our demo-boards, measure the strength of the 455kHz signal on the matching output network of the mixer with a FET probe. Then measure the 45MHz RF input signal on the matching input network of the mixer. Subtract the two numbers and the measured conversion gain should be around 13dB. Make sure that the input and output matching networks for the mixer have the same impedance since we are measuring voltage gain to get power gain ($P = V^2/R$). Of course this conversion gain value will change if there is a different RF input. In AN1994, Figure 16 shows how the conversion gain varies with different RF input frequencies.

Checking the gains in the IF Section

If the IF section does not give 100dB of gain, then the -118dBm SINAD measurement cannot be achieved. In fact some symptoms of low or no audio level can be due to the IF section.

One way of checking the function of the IF section is to check the gain of the IF amplifier and the IF limiter. The IF amplifier gain should be around 40dB and the IF limiter gain should be around 60dB.

To check this, connect a FET probe to the output of the amplifier. Apply a strong input signal with no modulation and then slowly lower the input signal and wait for the output of the amplifier to decrease. Measure the strength of the output signal in dB and then subtract from it the strength of the input signal in dB. This resulting number indicates the maximum gain of that section. (This method assumes matched input and output impedance.)

If a designer finds one of the sections with lower gain, then one area to check are the IF bypass capacitors. Be sure that the IF bypass capacitors have a good solid connection to the pad. It was also found in the lab that the RSSI stability reading improves when the IF bypass is properly installed.

QUESTION & ANSWER SECTION

Q: When I measure the bandpass response of the IF filters on the SSOP demo-board, it appears to have a little hump compared to the SO demo-board which has a flat filter response. Why is there a difference in the bandpass response when the SO and SSOP 605 chips are similar?

A: The answer has to do with the ceramic filters and not the package of the NE605. The reason why the SO demo-board has a flat bandpass response is because it is matched properly with the filter. The SSOP demo board uses the new Murata low profile ceramic 455kHz filter. Unfortunately, the input and output impedance is now 1kΩ instead of 1.5kΩ. This presents an impedance mismatch which creates the hump to occur in the bandpass response. But one does not have to worry too much about this response because the situation does not affect the overall performance that much. Additionally, the 12 SINAD measurement is similar whether using the "blue" (1.5kΩ) or "white" (1.0kΩ) Murata filters.

If you are worried about this, then switch to the correct "blue" Murata filters. The SSOP package will work with those filters as well. But if your design has strict height requirements, the white filters are a good solution.

Q: How much LO signal do you see at the RF port?

A: The worst LO leakage seen at the RF input on the SO and SSOP demo-board is -40dBm/441mV. This seems to vary with the LO level into the base of the on board transistor. This measurement will also vary with different LO frequencies. The NE605 SO and SSOP demo-boards have a LO frequency of 44.545MHz. Since there are so many variables, a designer needs to measure his/her own board for an accurate LO-RF isolation measurement.

There are several ways to improve the LO leakage from getting to the antenna. One can choose a higher IF frequency and tighten up the bandwidth of the front-end filter. Another solution is to add a low noise amplifier between the antenna and the mixer, and/or design a double conversion receiver and make sure the 1st mixer has a LO-RF isolation which meets the system specifications.

Q: On the SO and SSOP demo-board, the LO oscillator circuit is tunable with a variable capacitor. Is this a requirement?

A: No. The variable capacitor is used to tune the LO freq., but one can use a fixed value. The advantage of going with a fixed value capacitor is that it is a cheaper component part and there is no need for tuning. The only advantage with a tunable LO is that a designer can optimize the performance of the receiver.

Q: I know that the IF bandwidth of the NE605 allows me to build an IF of 21.4MHZ. Will the NE605 SSOP package perform just as good at 21.4MHz IF as it does at 455kHz?

A: Although we have not worked with NE605 SSOP at 21.4MHZ, we believe that it would be difficult to get a 12dB SINAD measurement at -120dBm. The wavelengths are much smaller at 21.4MHz than 455kHz. Since the wavelengths are smaller, there is a higher probability of regeneration occurring in the IF section. Therefore, a designer will probably have to reduce the gain in the IF section. Additionally, the SSOP package has pins that are physically closer together than with the normal type of packaged parts which can contribute to the unstable state with higher IF frequencies.

Demodulating at 10.7MHz IF with the NE/SA605/625

AN1996

Author: Alvin K. Wong

INTRODUCTION

The need for high speed communications is increasing in the market place. To meet these needs, high performance receivers must demodulate at higher IF frequencies to accommodate for the wider deviations in FM systems.

The standard 455kHz IF frequency, which is easier to work with, and thus more forgiving in production, no longer satisfies the high speed communication market. The next higher standard IF frequency is 10.7MHz. This frequency offers more potential bandwidth than 455kHz, allowing for faster communications.

Since the wavelength at 10.7MHz is much smaller than 455kHz, the demand for a good RF layout and good RF techniques increases. These demands aid in preventing regeneration from occuring in the IF section of the receiver. This application note will discuss some of the RF techniques used to obtain a stable receiver and reveal the excellent performance achieved in the lab.

BACKGROUND

If a designer is working with the NE/SA605 for the first time, it is highly recommended that he/she reads AN1994 and AN1995. These two application notes discuss the NE/SA605 in great detail and provide a good starting point in designing with the chip.

Before starting a design, it is also important to choose the correct part. Philips Semiconductors offers an extensive receiver line to meet the growing demands of the wireless market. Table 1 (see end of app note) displays the different types of receivers and their key features. With the aid of this chart, a designer will get a good idea for choosing a chip that best fits their design needs.

If low voltage receiver parts are required in a design, a designer can choose between a NE/SA606, SA607, SA608, or SA626. All of these low voltage receivers are designed to operate at 3V while still providing high performance to meet the specifications for cellular radio. All of these parts can operate with an IF frequency as high as 2MHz. However, the SA626 can operate with a standard IF frequency of 10.7MHz and also provide fast RSSI speed. Additionally the SA626 has a power down mode to conserve battery power.

A close look at Table 1 will also show that there are subtle differences between the 3V receivers. The main differences between the NE/SA606, SA607, and SA608 can be seen in the audio and RSSI output structure. Additionally the SA607 and SA608 provide a frequency check pin which can aid in locking in the desired received frequency over temperature.

OBJECTIVE

The objective of this application note is to show that the NE/SA605 can perform well at an IF frequency of 10.7MHz. Since most Philips Semiconductors receiver demo-boards are characterized at RF = 45MHz/IF = 455kHz, we decided to continue to characterize at this frequency. This way we could compare how much degradation (for different IFs) there was with a RF = 45MHz/IF = 455kHz vs RF = 45MHz/ IF = 10.7MHz. As we will discuss later, there was minimal degradation in performance.

We also tested at RF = 240MHz/IF = 10.7MHz. The 240MHz RF is sometimes referred to as the first IF for double conversion receivers. Testing the board at RF=83.16MHz (which is also a common first IF for analog cellular radio) and IF = 10.7MHz was not done because the conversion gain and noise figure does not change that much compared to 45MHz input. Therefore, we can probably expect the same type of performance at 83.16MHz.

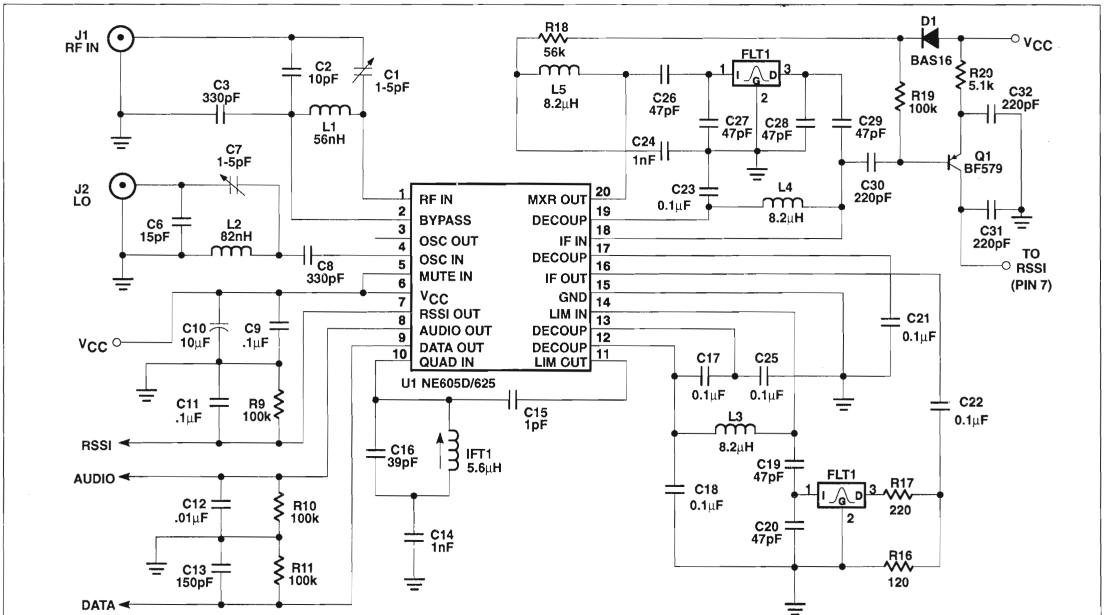


Figure 1. NE/SA605/625 Schematic: RF = 240MHz, LO = 229.3MHz, IF = 10.7MHz

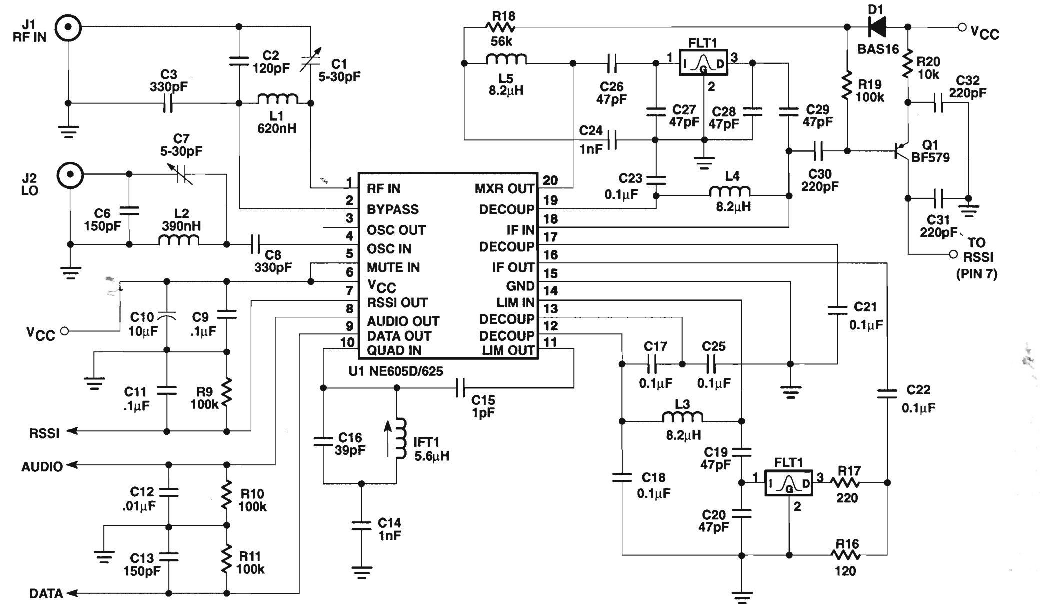


Figure 2. NE/SA605/625 Schematic: RF = 45MHz, LO = 55.7MHz, IF = 10.7MHz

The RF = 240MHz/IF = 10.7MHz demo-board is expected to perform less than the RF = 45MHz/IF = 10.7MHz demo-board because the mixer conversion gain decreases while the noise figure increases. These two parameters will decrease the performance of the receiver as the RF frequency increases.

With the new demands for fast RSSI time, Philips Semiconductors has also designed receiver chips with fast RSSI speed: The NE/SA624, NE/SA625 and SA626. The NE/SA625 can also be used in this layout because it is pin-for-pin compatible with the NE/SA605. The RSSI circuitry was the only change done for the NE/SA625, so performance will be similar to the NE/SA605. Performance graphs shown in this application note will reveal the similarities.

For systems requiring low voltage operation, IF=10.7MHz and fast RSSI speed, the SA626 will be the correct choice, however, this application note does not address the performance of the SA626 because the SA626 was not available at this writing.

Board Set-Up and Performance Graphs

Figures 1 and 2 show the NE/SA605/625 schematics for the 240MHz and 45MHz boards, respectively. Listed below are the basic functions of each external components for both Figures 1 and 2.

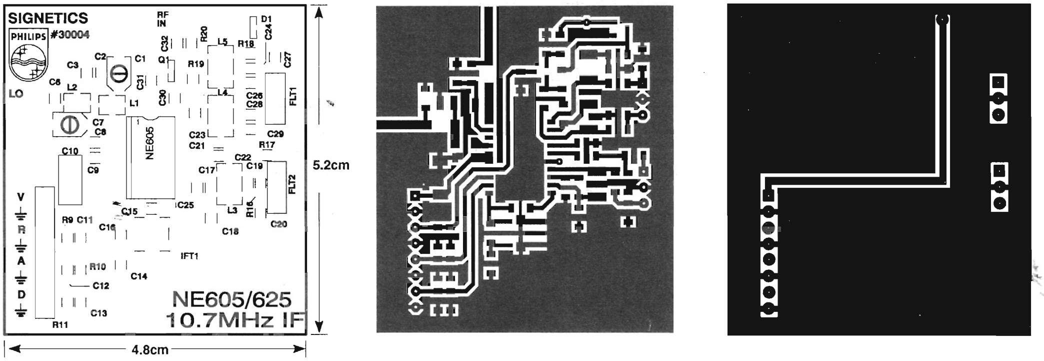
SO Layout Schematic List

U1- NE/SA605 or NE/SA625
FLT1-10.7MHz ceramic filter Murata SFE10.7MA5-A (280kHz BW)
FLT2-10.7MHz ceramic filter Murata SFE10.7MA5-A (280kHz BW)

Note: If a designer wants to use different IF bandwidth filters than the ones used in this application note, the quad tank's S-curve may need to be adjusted to accommodate the new bandwidth.

C1- Part of the tapped-C network to match the front-end mixer
C2- Part of the tapped-C network to match the front-end mixer
C3- Used as an AC short to Pin 2 and to provide a DC block for L1 which prevents the upsetting of the DC biasing on Pin 1
C6- part of the tapped-C network to match the LO input
C7- part of the tapped-C network to match the LO input
C8- DC blocking capacitor
C9- Supply Bypassing
C10-Supply bypassing (this value can be reduced if the NE/SA605/625 is used with a battery)
C11-used as a filter, cap value can be adjusted when higher RSSI speed is preferred over lower RSSI ripple
C12-used as a filter
C13-used as a filter
C14-used to AC ground the quad tank
C15-used to provide the 90° phase shift to the phase detector
C16-quad tank component to resonant at 10.7MHz with IFT1 and C15
C17-IF limiter decoupling capacitor
C18-DC block for L3 which prevents the upsetting of the DC biasing on Pin 14
C19-part of the tapped-C network for FLT2
C20-part of the tapped-C network for FLT2
C21-IF amp decoupling cap
C22-DC blocking cap
C23-IF amp decoupling cap and DC block for L3 which prevents the upsetting of the DC biasing on Pin 14
C24-provides DC block for L5 which prevents the upsetting of the DC biasing on Pin 20
C25-IF limiter decoupling capacitor
C26-part of the tapped-C network for FLT1
C27-part of the tapped-C network for FLT1
C28-part of the tapped-C network for FLT1
C29-part of the tapped-C network for FLT1

R9- used to convert the current into the RSSI voltage
R10-converts the audio current to a voltage
R11-converts the data current to a voltage
R16-used to kill some of the IF signal for stability purposes
R17-used in conjunction with R16 for a matching network for FLT2



TOP SILK SCREEN

TOP VIEW

BOTTOM VIEW

Figure 3. NE/SA605/625 SO Demo-Board Layouts (Not Actual Size)

L1 - part of the tapped-C network to match the front-end mixer
L2 - part of the tapped-C network to match the front-end mixer
L3- part of the tapped-C network to match the input of FLT2
L4- part of the tapped-C network to match the input of FLT1
L5- part of the tapped-C network to match the input of FLT1

RSSI Extender Circuit

R18-provides bias regulation, the gain will stay constant over varying V_{CC}
R19-for biasing, buffer RF DC voltage
R20-provides the DC bias, RSSI gain (when R20 increases, RSSI gain decreases
C30-DC blocking capacitor which connects the ceramic filter's output to the PNP transistor's input
C31-decoupling capacitor, and should be removed for measuring RSSI systems speed
C32-peak detector charge capacitor
D1- diode to stabilize the bias current
Q1- Philips BF579 PNP transistor
IFT1-part of the quad tank circuit

There are minor differences between Figures 1 and 2. The RF and LO tapped-C component values are changed to accommodate for the different RF and LO test frequencies (RF=240MHz and 45MHz and LO = 229.3MHz and 55.7MHz). The other difference is the value of R20. This resistor value was changed to optimize the RSSI curve's linearity (see RSSI extender section in this application note for further details).

The recommended NE/SA605/625 layout is shown in Figure 3. This layout can be integrated with other systems.

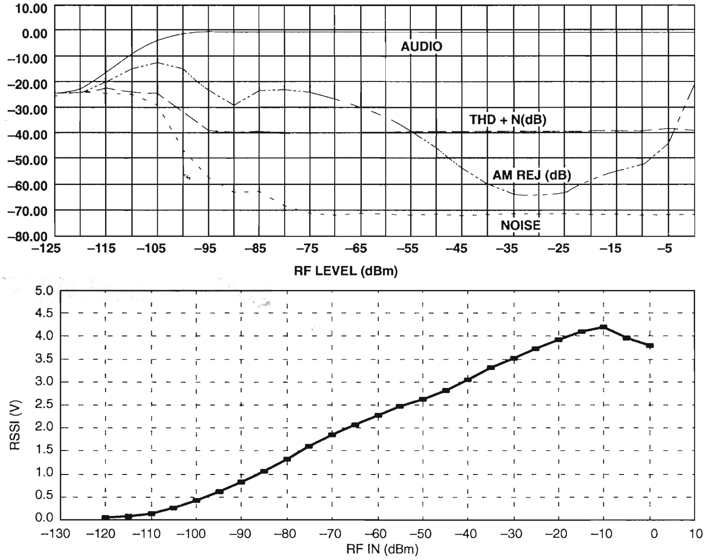


Figure 4. NE/SA625 SO Performance Graphs at 240MHz

Figures 4 through 7 show the performance graphs for the NE/SA605 & NE/SA625 at 240MHz and 45MHz RF inputs. There was no real noticeable difference in performance between a NE/SA605 or NE/SA625 except for AM rejection. The NE/SA605 appears to have a little better AM rejection, but from the end user's point of view, there is no difference between the receiver. All the other measurements were perfect, including SINAD.

RF Input

The NE/SA605/625 board is set up to receive an RF input of 240MHz (see Figure 1). This is achieved by implementing a tapped-C network. The deviation should be set to ±70kHz to achieve ***-110dBm to -112dBm for -12dB SINAD***. However, the deviation can be increased to ±100kHz, depending on the bandwidth of the IF filter and the Q of the quad tank.

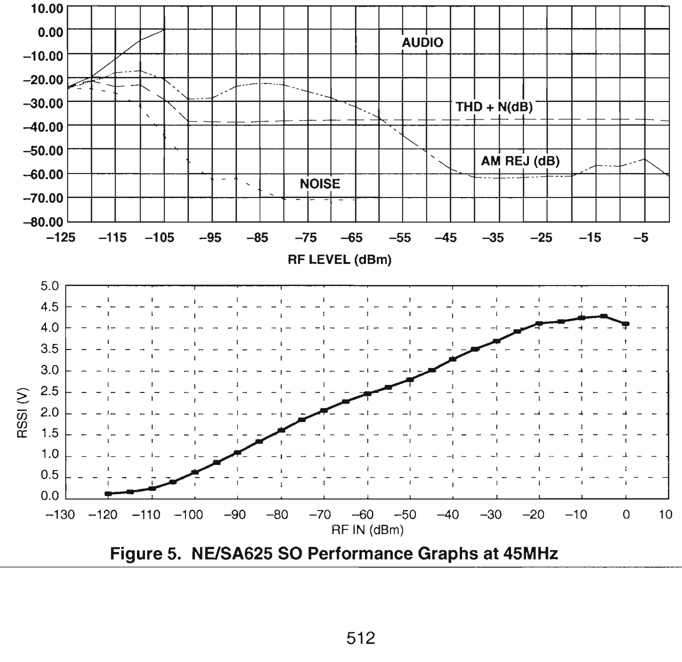


Figure 5. NE/SA625 SO Performance Graphs at 45MHz

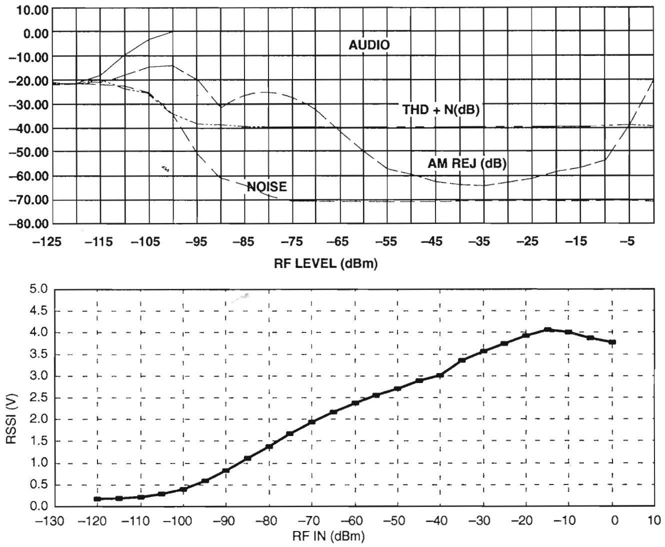


Figure 6. NE/SA605SO Performance Graphs at 240MHz

Because we wanted to test the board at 45MHz, we changed the values of the tapped-C network for the RF and LO ports (see Figure 2). We found that a ***-116dBm to -118dBm for -12dB SINAD*** could be achieved. With these results, we were pretty close to achieving performance similar to our standard 455kHz IF board.

A designer can also make similar RF and LO component changes if he/she needs to evaluate the board at a different RF frequency. *It should be noted that if a designer purchases a stuffed NE/SA605/625 demo-board from Philips Semiconductors its set up will be for an RF input frequency of 240MHz.* AN1994 will aid the designer in calculating the tapped-C values for other desired frequencies, while AN1995 will be of value for making S11 bench measurements. Just remember that the input impedance will differ for different RF frequencies.

LO Input

The LO frequency should be 229.3MHz for the RF = 240MHz demo-board and have a drive level of -10dBm to 0dBm (this also applies for the RF = 45MHz and LO = 55.7MHz). The drive level is important to achieve maximum conversion gain. The LO input also has a matched tapped-C network for efficiency purposes which makes for good RF practices.

If a designer wanted to change the matching network to inject a different LO frequency, he/she could follow the steps in AN1994 and assume that the input impedance is around 10kΩ for low frequency inputs. The main goal is to get maximum voltage transfer from the signal generator to the inductor.

An external oscillator circuit was used to provide greater flexibility in choosing different RF and LO frequencies; however, an on-board oscillator can be used with the NE/SA605/625. New high frequency fundamental crystals, now entering the market, can also be used for high LO frequency requirements. Most receiver systems, however, will use a synthesizer to drive the LO port.

10.7MHz Ceramic Filters

The input and output impedance of the 10.7MHz ceramic IF filters are 330Ω. The NE/SA605/625's input and output impedances are roughly 1.5KΩ. Therefore, a matching circuit had to be implemented to obtain maximum voltage transfer. Tapped-C networks were used to match the filters input and output impedance.

But in this case, we decided to go with non-tuning elements to reduce set-up time. Figure 8 shows the values chosen for the network.

Although our total deviation is 140kHz, we used 280kHz IF bandwidth filters to maximize for fast RSSI speed. The SINAD performance difference between using 180kHz BW filter versus 280kHz BS filter was insignificant.

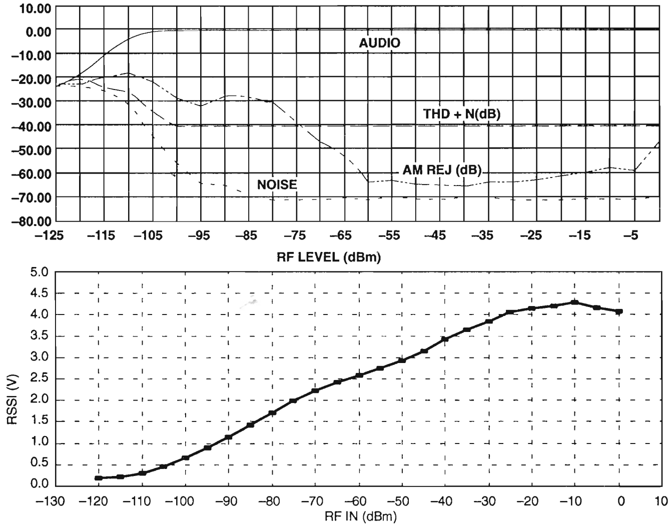


Figure 7. NE/SA605 SO Performance Graphs at 45MHz

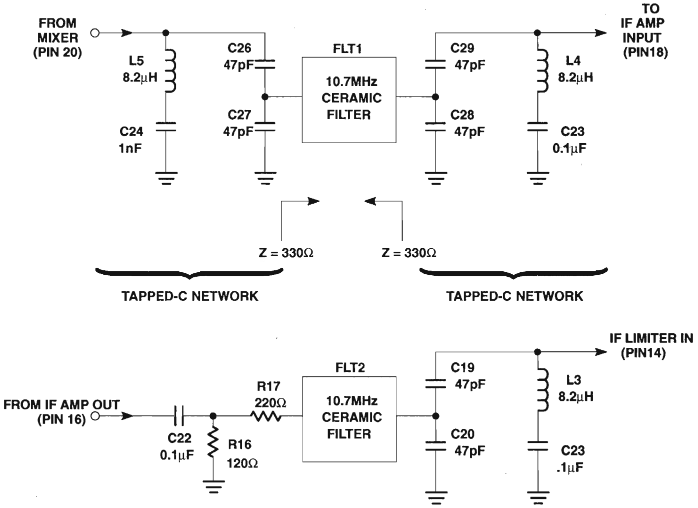


Figure 8. Matching Configuration for FLT1 and FLT2

Stabilizing the IF Section From Regeneration

Because the gain in the IF section is 100dB and the wavelength for 10.7MHz is small, the hardest design phase of this project was to stabilize the IF section.

The steps below show the methods used to obtain a stable layout.

1. The total IF section (IF amp and limiter) gain is 100dB which makes it difficult to stabilize the chip at 10.7MHz. Therefore, a 120Ω (R16 of Figure 1) resistor was used to kill some of the IF gain to obtain a stable system. (NOTE: Expect AM rejection performance to degrade as you decrease the IF gain externally.)
2. Since the tapped-C inductors for FLT1 and FLT2 are not shielded, it is important not to place them too close to one another. Magnetic coupling will occur and may increase the probability of regeneration.
3. It was also found that if the IF limiter bypass capacitors do not have the same physical ground, the stability worsens. Referring to Figure 1, the IF limiter bypass capacitors (C17, C25) are connected to assure a common ground.
4. The positioning of ground feedthroughs are vital. A designer should put feedthroughs near the IF bypass capacitors ground

points. In addition, feedthroughs are needed underneath the chip. Other strategic locations are important for feedthroughs where insufficient grounding occurs.

5. Shielding should be used after the best possible stability is achieved. The NE/SA605/625 demo-board is stable, so shielding was not used. However, if put into a bigger system, shielding should be used to keep out unwanted RF frequencies. As a special note, if a good shield is used, it can increase the R16 resistor value such that there is less IF gain to kill to achieve stability. This means the RSSI dynamic range is improved. So if a designer does not want to implement the RSSI extender circuit, but is still concerned with SINAD and RSSI range, he/she can experiment with R16 and shielding because there is a correlation between them (see RSSI extender section in this application note for more information). In addition, AM rejection performance will improve due to the greater availability of the total IF gain.

The key to stabilizing the IF section is to kill the gain. This was done with a resistor (R16 in Figure 8) to ground. All the other methods mentioned above are secondary compared to this step. Lowering the value of this resistor reduces the gain and the increasing resistor value kills less gain. For our particular layout, 120Ω was chosen to obtain a stable board, but we were careful not to kill too much gain. One of the downfalls of killing too much gain is that the SINAD reading will become worse and the RSSI dynamic range is reduced.

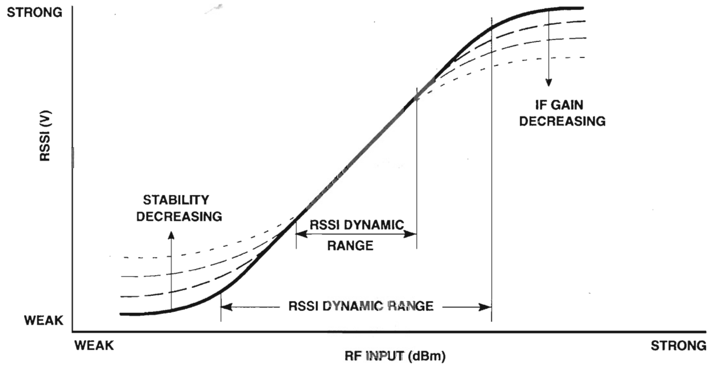
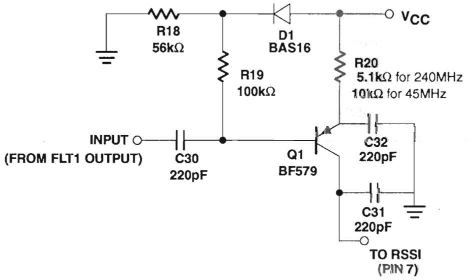


Figure 9. RSSI Dynamic Range



RSSI EXTENDER COMPONENT LIST AND EXPLANATION

R18–provides bias regulation, the gain will stay constant over varying V_{CC}
R19–for biasing, buffer RF DC voltage
R20–provides the DC bias, RSSI gain (when R20 increases, RSSI gain decreases
C30–DC blocking capacitor which connects the ceramic filter's output to the PNP transistor's input
C31–de-coupling capacitor
C32–peak detector charge capacitor
D1–diode to prevent improper current flow
Q1–Philips BF579 PNP transistor

Figure 10. External RSSI Extender Circuit

RSSI Dynamic Range

There are two main factors which determine the RSSI dynamic range. These two factors are 1.) how stable is the board, and 2.) how much gain is killed externally. If the board is unstable, a high RSSI voltage reading will occur at the bottom end of the curve. If too much gain is taken away, the upper half of the curve is flattened. Thus the dynamic range can be affected. Figure 9 shows how the linear range can be decreased under the conditions mentioned above.

It is important to choose the appropriate resistor to kill enough gain to get stability but not too much gain to affect the upper RSSI curve dynamic range. Because we had to kill some IF gain to achieve good board stability and good SINAD readings, our RSSI overall dynamic range was reduced on the upper end of the curve.

Because SINAD and the RSSI dynamic range are two important parameters for most of our customers, we decided to add an "RSSI extender" modification to the board to get the best of both worlds. Together with the RSSI external modification and the "stability resistor", we can now achieve excellent SINAD readings and maintain a wide RSSI dynamic range.

RSSI Extender Circuit

The RSSI extender circuit increases the upper dynamic range roughly about 20-30dB for the 240MHz demo-board. The NE/SA605/625 demo-board has 90-100dB of linear dynamic range when the RSSI modification is used.

Referring to Figure 10, one can see that one transistor is used with a few external components. The IF input signal to the PNP transistor is tapped after the ceramic filter to ensure a clean IF signal. The circuit then senses the strength of the signal and converts it to current, which is then summed together with the RSSI output of the chip.

The PNP transistor stage has to be biased as a class B amplifier. The circuit provides two functions. It is a DC amplifier and an RF detector. The gain of the RSSI extender can be controlled by R20 and R9 (Gain = R9/R20). Adjusting R20 is preferable because it controls the upper half of the RSSI curve, whereas adjusting R9 shifts the whole RSSI curve.

If a different RF frequency is supplied to the mixer input, it is important to set the external RSSI gain accordingly. When the RF input was changed from 240MHz to 45MHz, the conversion gain of the mixer increased. Therefore, the earlier gain settings for the RSSI extender was too much. A lower gain setting had to be implemented such that a smoother transition would occur.

Quad Tank

The quad tank is tuned for 10.7MHz ($F=1/2\pi\sqrt{LC}$). Figure 1 shows the values used (C14,C15, C16, IFT1) and Figure 11 shows the S-curve. The linear portion of the S-curve is roughly 200kHz. Therefore, it is a good circuit for a total deviation of 140kHz. It is possible to deviate at 200kHz, but this does not leave much room for part tolerances.

If more deviation is needed, a designer can lower the S-curve with a parallel resistor connected to the quadrature tank. A designer should play with different value resistors and plot the S-curve to pick the best value for the design. To key in on the resistor value with minimum effort, a designer can put a potentiometer in parallel with the quad tank and tune it for best distortion. Then the designer can use fixed value resistors that are close to the potentiometer's value.

Fixed quad tank component values can be used to eliminate tuning, but a designer must allow for part tolerances and temperature considerations. For better performance over temperature, a resonator/discriminator can be used. Thus, no tuning is required for the quad tank section, which wili save on production costs.

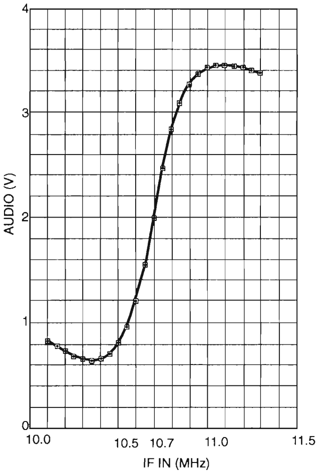


Figure 11. 10.7MHz Quad Tank S-Curve

RSSI System Speed

The RSSI rise and fall times are important in applications that use pulsed RF in their design. The way we define the speed is how fast the RSSI voltage can travel up and down the RSSI curve. Figure 12 shows a representation of this. Five different pulsed RF levels were tested to get a good representation of the RSSI speed. One can predict that the stronger the pulsed signal, the higher the RSSI voltage and the longer it will take for the fall time to occur. Generally speaking, the rise time is determined by how long it takes to charge up an internal capacitor. The fall time depends on how long it takes to discharge this capacitor.

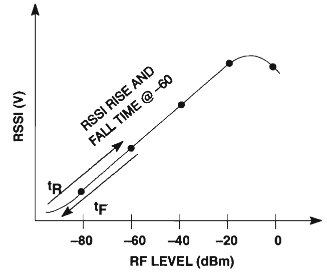


Figure 12. RSSI Cuve with Pulsed RF Levels

It is also important to understand that there are two types of RSSI speeds. The first type is the RSSI *chip* speed and the second is the RSSI *system* speed. The RSSI *chip* speed will be faster than the *system* speed. The bandwidth of the external filters and other external parts can slow down the RSSI system speed dramatically.

Figure 13 shows the bench set up for the RSSI system speed measurements. The pulsed RF was set for 10kHz and and the RSSI output was monitored with a digital oscilloscope. Figure 14 shows how the rise and fall times were measured on the oscilloscope.

The modifications done on the NE/SA625 board are shown in Figure 15. The RSSI caps C11 and C31 were eliminated, and the RSSI resistor values were changed. We wanted to see how much time was saved by using a smaller RSSI resistor value.

The RSSI system speed for the 240MHz NE/SA625 demo board is shown in Figure 16. Again, the only modification was that the RSSI caps (C11 and C31) were taken out and the RSSI resistor value (R9) was varied. For different RF levels, the speed seems to vary slightly, but this is expected. The higher the RSSI voltage, the longer it will take to come back down the RSSI curve for the fall time.

Looking more closely at Figure 16, one can note that the 0dBm input level has a faster fall time than the -20dBm level. This occurs because of the limited dynamic range of the test equipment. The equipment does not have sufficient on/off range, so at 0dBm the 'off' mode is actually still on. Therefore, you don't get a true reading.

At 0dBm the RSSI voltage is lower than –20dBm. The reason why this happens is because the RSSI linearity range stops at -10dBm. When the RF input drive is too high (e.g., 0dBm), the mixer conversion gain decreases, which causes the RSSI voltage to drop.

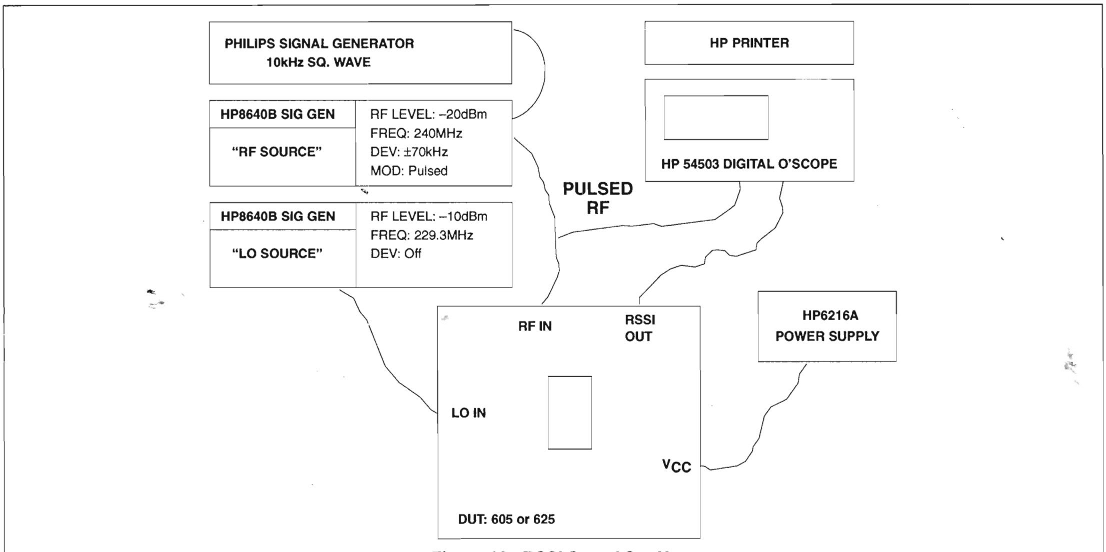


Figure 13. RSSI Speed Set-Up

QUESTION AND ANSWER SECTION

Q. What should the audio level at Pin 8 be?

A. The audio level is at $580mV_{P-P}$ looking directly at the audio output pin and does not include a C-message filter. However, the audio output level will depend on two factors: the "Q" of the quadrature tank and the deviation used. The higher the quad tanks "Q", the larger the audio level. Additionally, the more deviation applied, the larger the audio output. But the audio output will be limited to a certain point.

Q. Am I required to use the 10μF supply capacitor?

A. No, a smaller value can be used. The 10μF capacitor is a suggested value for evaluation purposes. Most of the time a power supply is used to evaluate our demo boards. If the supply is noisy, it will degrade the receiver performance. We have found that a lower value capacitor can be used when the receiver is powered by a battery. But it is probably safer to stay at a reasonable capacitor size.

Q. Can I use different IF filters for my required bandwidth specifications?

A. Yes, you can order different IF filters with different bandwidths. Some of the standard manufacturers have 180kHz, 230kHz, and 280kHz bandwidths for 10.7MHz ceramic filters. Just be sure that the quad tank "S-curve" is linear for your required bandwidth. The NE/SA605/625 demo-board has a 200kHz linearity for the quad tank. So ±70kHz deviation is perfect.

We have also found that even though the IF filter's bandwidth might be more than our requirements, it does not really degrade overall receiver performance. But to follow good engineering practices, a designer should order filters that are closest to their requirements. Going with wider bandwidth filters will give you better RSSI system speed.

Q. I want to use part of your demo board for my digital receiver project. Can you recommend a good 10.7MHz filter with accurate 10.7MHz center frequency which can provide minimum phase delay?

A. At the present time, I only know of one manufacturer that is working on a filter to meet digital receiver requirements. Murata has a surface mount 10.7MHz filter. The number is FX-6502 (SFECA 10.7). It was specifically designed for Japanese digital cordless phones. You can adapt these filters to our NE/SA605/625 demo board.

We also used these filters in our layout and got similar SINAD and RSSI system speed performance compared to the standard 10.7MHz filters (280kHz BW). I believe the difference between the filters will be apparent for digital demodulation schemes.

Q. If the system RSSI time is dependent on the external components used, like the IF filters, then what is the difference in using the NE/SA605 vs the NE/SA625?

A. The difference comes in the fall time for high IF frequencies. You are correct that for IFs like 455kHz, there is probably little delta difference because the filter's bandwidth prohibits the speed dramatically. However, for 10.7MHz IFs, there will be a difference in the fall time between the chips because the bandwidths are much wider. Therefore, the chips will play a role in the RSSI system speed. The chip difference in RSSI speed will depend on your overall system configuration.

Q. Why does the AM rejection performance look better on the NE/SA605, 455kHz IF board than the NE/SA605/625 10.7MHz IF demo-board?

A. For the 455kHz IF demo-board there is more IF gain available compared to the 10.7MHz IF board. Recall that for the 10.7MHz IF board, some of the IF gain was killed externally for stability reasons. Since the IF gain helps improve AM rejection performance, by killing IF gain, AM rejection is decreased.

Q. The NE/SA605/625 10.7MHz IF demo-board is made for the SO package. Can I use your SSOP package and expect the same level of performance?

A. We have not done a SSOP layout yet. But if the same techniques are used, I am sure the SSOP package will work. The SA626 demo-board will be done in SSOP, and probably be available in the future.

Q. I tried to duplicate your RSSI system reading measurements using your demo-board and I get slower times. What am I doing wrong?

A. The RSSI system speed measurements are very tricky. Make sure your cable lengths are not too long. I have found that when making microsecond measurements, lab set-up is of utmost importance. Also, make sure the RSSI caps (C11 and C31) are removed from the circuit.

Also be sure that the bandwidth of your IF filters is not slowing down the RSSI system speed (Cf: section on RSSI system speed).

Q. I am going to use your design in my NTT cordless digital phone. Can you recommend a 240.05MHz filter?

A. Murata SX-4896 (SAMAFC 240.05) is a filter you can use for your application.

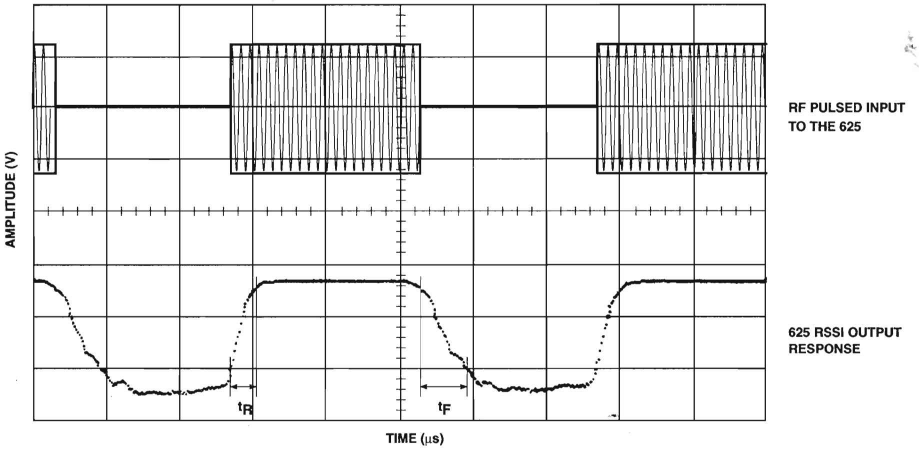


Figure 14. Oscilloscope Display of RSSI System Rise and Fall Time

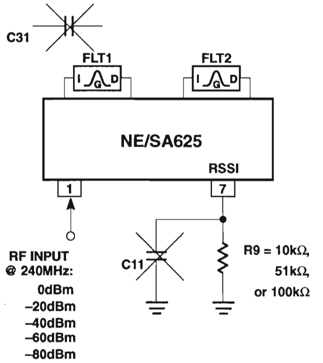


Figure 15. NE/SA625 RSSI Test Circuit Configuration

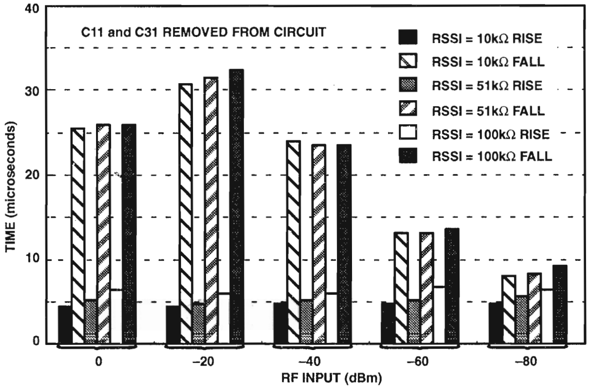


Figure 16. RSSI Systems Rise and Fall Time with Different RSSI Resistor Values

Demodulating at 10.7MHz IF with the NE/SA605/625

AN1996

Table 1. FM/IF Family Overview

		NE602A/604A		NE605	SA606	SA607	SA608	NE624	NE625	SA626	NE627
V_{CC}		4.5–8V	4.5–8V	4.5–8V	2.7–7V	2.7–7V	2.7–7V	4.5-8.0V	4.5-8.0V	2.7–5.5V	4.5-8.0V
I_{CC}		2.4mA@6V	3.3mA @ 6V	5.7mA @ 6V	3.5mA @ 3V	3.5mA @ 3V	3.5mA @ 3V	3.4mA @ 6V	5.8mA @ 6V	6.5mA @ 3V	5.8mA @ 6V
Number of Pins		8	16	20	20	20	20	16	20	20	20
Packages NE: 0 to +70°C SA: –40 to +85°C N: Plastic DIP D: Plastic SO FE: Ceramic DIP DK: SSOP		NE602AN NE602AD NE602AFE SA602AN SA602AD SA602AFE	NE604AN NE604AD SA604AN SA604AD	NE605N NE605D NE605DK SA605N SA605D SA605DK	SA606N SA606D SA606DK	SA607N SA607D SA607DK	SA608N SA608D SA608DK	NE624N NE624D SA624N SA624D	NE625N NE625D NE625DK SA625N SA625D SA625DK	SA626D SA626DK	NE627N NE627D NE627DK SA627N SA627D SA627DK
–12dB SINAD (RF = 45MHz), IF = 455kHz) 1kHz Tone, 8kHz Dev.		–120dBm / .22uV		–120dBm / .22uV	–117dBm / .31uV	–117dBm / .31uV	–117dBm / .31uV	–120dBm / .22uV	–120dBm / .22uV	–112dBm / .54uV (RF = 240MHz) (IF = 10.7MHz) 1kHz Tone, +/–70kHz Dev.	–120dBm / .22uV
Process f_t		8GHz		8GHz	8GHz	8GHz	8GHz	8GHz	8GHz	8GHz	8GHz
For lower cost version and less performance		612A & 614A		615	616	617	—	—	—	—	—
Features		– Audio & Data pins – IF BW of 25MHz – No external matching required for standard 455kHz IF filter		– Audio & Data pins – IF BW of 25MHz – No external matching required for standard 455kHz IF filter	– Low voltage – Internal RSSI and audio op amps – No external matching required for standard 455kHz IF filter – IF BW of 2MHz	– Freq check pin – Low voltage – Internal RSSI and audio op amps – Unity gain RSSI output – No external matching required for standard 455kHz IF filter – IF BW of 2MHz	– Freq check pin – Low voltage – Internal RSSI and audio op amps – Unity gain audio output – No external matching required for standard 455kHz IF filter – IF BW of 2MHz	– Fast RSSI Time – Pin-to-Pin compatible with 604A – No external matching required for standard 455kHz IF filter	– Fast RSSI Time – Pin-to-Pin compatible with 605 – No external matching required for standard 455kHz IF filter	– Power down mode – Low voltage – Fast RSSI Time – IF BW of 25MHz – Internal RSSI & audio op amps – No external matching required for standard 10.7MHz IF filter	– Fast RSSI Time – Freq check pin – IF BW of 25MHz – Internal RSSI & audio op amps – No external matching required for standard 455kHz IF filter
RSSI OUTPUT SECTION	**Dynamic Range**	90dB		90dB	90dB	90dB	90dB	90dB	90dB	90dB	90dB
	Accuracy	+/–1.5dB		+/–1.5dB	+/–1.5dB	+/–1.5dB	+/–1.5dB	+/–1.5dB	+/–1.5dB	+/–1.5dB	+/–1.5dB
455kHz IF	**Rise * Time**	—	1.4us	—	—	—	—	1.1us	1.2us	—	1us
	Fall * Time	—	21.3us	—	—	—	—	1.3us	2.1us	—	1.7us
10.7MHz IF	**Rise * Time**	—	1.5us	—	—	—	—	1.2us	1.2us	1.2us	0.9us
	Fall * Time	—	19.4us	—	—	—	—	1.6us	2us	2us	1.4us

***NOTE: No IF filters in the circuit**

Table 1. (cont.) FM/IF Family Overview

			NE602A/604A		NE605	NE606	SA607	SA608	NE624	NE625	SA626	NE627
MIXER		Max. Conversion Power Gain (RF = 45MHz; IF = 455kHz)	17dB	—	13dB	17dB	17dB	17dB	—	13dB	13dB	13dB
		3rd Order Intercept Point (Input) f1 = 45MHz f2 = 45.06MHz	–13dB	—	–10dBm	–9dBm	–9dBm	–9dBm	—	–10dBm	–11dBm f1 = 240.05 f2 = 240.35	–10dBm
		Noise Figure @45MHz	5dB	—	5dB	6.2dB	6.2dB	6.2dB	—	5dB	11dB @ 240MHz	5dB
		RF Input Resistance and Capacitance @45MHz	1.5k 3pF	—	4.7k 3.5pF	8k 3pF	8k 3pF	8k 3pF	—	4.7k 3.5pF	4.7k 3.5pF @ 240MHz	4.7k 3.5pF
		Output Resistance	1.5k	—	1.5k	1.5k	1.5k	1.5k	—	1.5k	330	1.5k
IF SECTION	IF AMP	Input Impedance	—	1.6k	1.6k	1.5k	1.5k	1.5k	1.6k	1.6k	330	1.5k
		Output Impedance	—	1.0k	1.0k	330	330	330	1.0k	1.0k	330	1.0k
		Gain	—	40dB	40dB	44dB	44dB	44dB	40dB	40dB	44dB	40dB
		BW	—	41MHz	41MHz	5.5MHz	5.5MHz	5.5MHz	41MHz	41MHz	40MHz	40MHz
	IF LIMITER	Input Impedance	—	1.6k	1.6k	1.5k	1.5k	1.5k	1.6k	1.6k	330	1.5k
		Output * Impedance	—	330	330	330	330	330	330	330	330	330
		Gain	—	60dB	60dB	58dB	58dB	58dB	40dB	60dB	58dB	60dB
		BW	—	28MHz	28MHz	4.5MHz	4.5MHz	4.5MHz	28MHz	28MHz	28MHz	28MHz
		Total IF Gain	—	100dB	100dB	100dB	100dB	100dB	100dB	100dB	96dB (includes –6dB pad)	100dB
		Total IF BW	—	25MHz	25MHz	2MHz	2MHz	2MHz	25MHz	25MHz	25MHz	25MHz

NOTE: *Not designed to drive a matched load

Low-voltage high performance mixer FM IF system SA606

DESCRIPTION

The SA606 is a low-voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA606 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink small outline package).

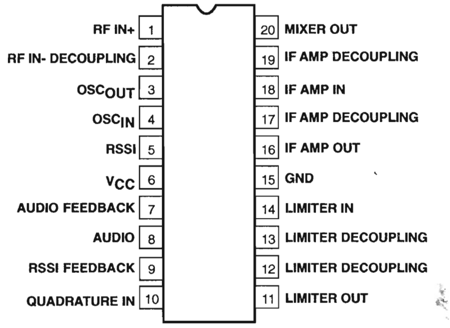
The SA606 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio and RSSI outputs have amplifiers with access to the feedback path. This enables the designer to level adjust the outputs or add filtering.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31µV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA606 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs

PIN CONFIGURATION

D, DK and N Packages



- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Wireless systems
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receiver
- Single conversion VHF receivers

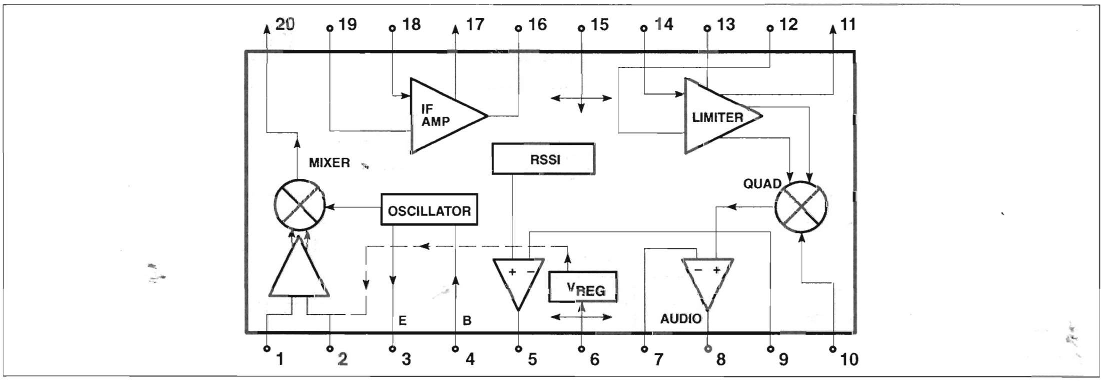
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA606N	0408B
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA606D	0172D
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA606DK	1563

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		7	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range		-40 to +85	°C
θ_{JA}	Thermal impedance	D package DK package N package	90 117 75	°C/W

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4kΩ and R18 = 3.3kΩ; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third-order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF level = -52dBm		-9		dBm
	Conversion voltage gain	Matched 14.5dBV step-up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single-ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting -3dB, R_{17a} = 2.4k, R_{17b} = 3.3k	Test at Pin 18		-109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level	Gain of two (2kΩ AC load)	70	120	160	mV
	SINAD sensitivity	IF level -110dBm		17		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
THD	Total harmonic distortion		-35	-50		dB
S/N	Signal-to-noise ratio	No modulation for noise		62		dB
	RF RSSI output, $R_9 = 2k\Omega$	RF level = -118dBm		0.3	.80	V
		RF level = -68dBm	.70	1.1	1.80	V
		RF level = -23dBm	1.20	1.8	2.50	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance	Pin 18	1.3	1.5		kΩ
	IF output impedance	Pin 16		0.3		kΩ
	Limiter input impedance	Pin 14	1.3	1.5		kΩ
	Limiter output impedance	Pin 11		0.3		kΩ
	Limiter output voltage	Pin 11		130		mV_{RMS}
RF/IF section (int LO)						
	Audio level	$3V = V_{CC}$, RF level = -27dBm		120		mV_{RMS}
	System RSSI output	$3V = V_{CC}$, RF level = -27dBm		2.2		V
	System SINAD sensitivity	RF level = -117dBm		12		dB

CIRCUIT DESCRIPTION

The SA606 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of -9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

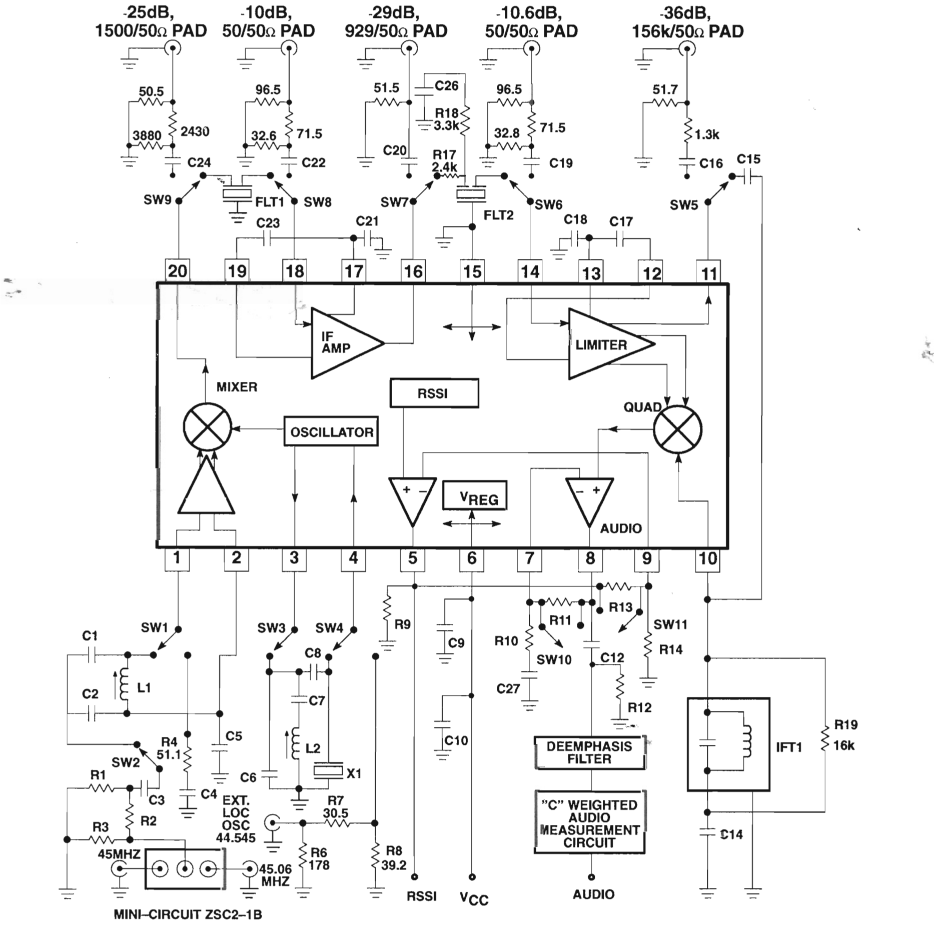
The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

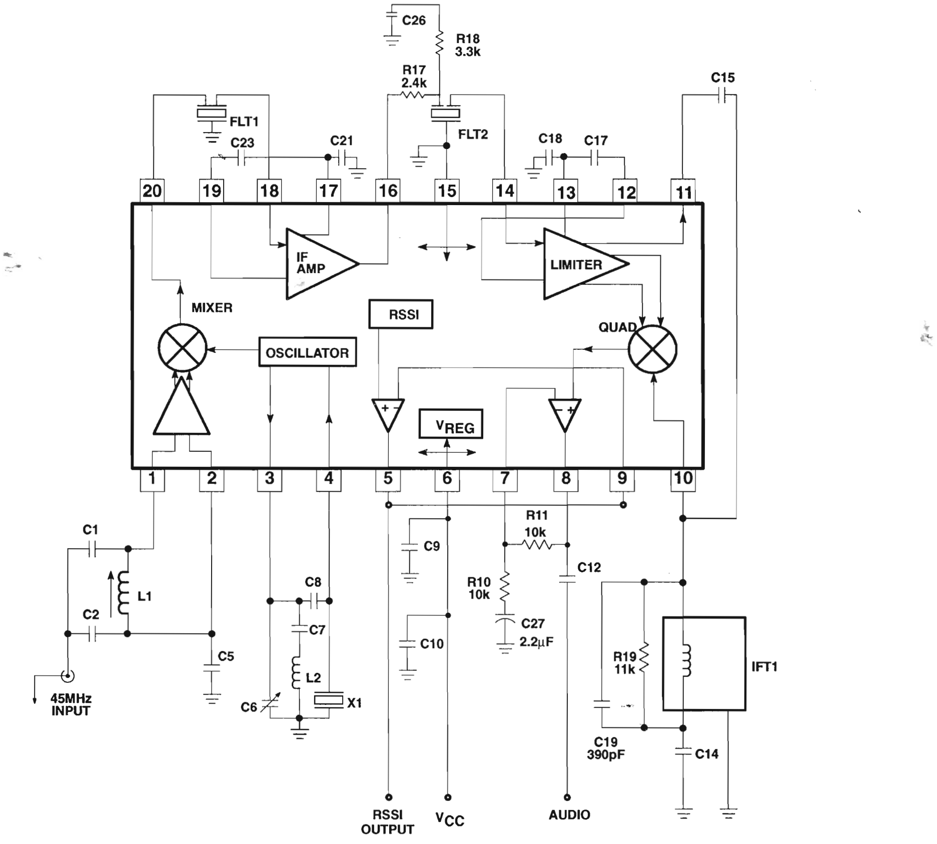


Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C27	2.2μF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C5	100nF ±10% Monolithic Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C6	22pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C7	1nF Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C8	10.0pF NPO Ceramic	L2	0.8μH nominal
C9	100nF ±10% Monolithic Ceramic		Toko 292CNS–T1038Z
C10	10μF Tantalum (minimum) *	X1	44.545MHz Crystal ICM4712701
C12	2.2μF	R9	2kΩ ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R10	10kΩ ±1%
C15	10pF NPO Ceramic	R11	10kΩ ±1%
C17	100nF ±10% Monolithic Ceramic	R12	2kΩ ±1%
C18	100nF ±10% Monolithic Ceramic	R13	20kΩ ±1%
C21	100nF ±10% Monolithic Ceramic	R14	10kΩ ±1%
C23	100nF ±10% Monolithic Ceramic	R17	2.4kΩ ±5% 1/4W Carbon Composition
C25	100nF ±10% Monolithic Ceramic	R18	3.3kΩ
C26	100nF ±10% Monolithic Ceramic	R19	16kΩ

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. SA606 45MHz Test Circuit (Relays as shown)



NE606D/DK Demo Board
Application Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	5-30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10µF Tantalum (minimum) *
C12	2.2µF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2µF Tantalum
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330µH TOKO 303LN-1130
L1	.33µH TOKO SCB-1320Z
L2	1.2µH
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

* NOTE: This value can be reduced when a battery is the power source.

Figure 2. SA606 45MHz Application Circuit

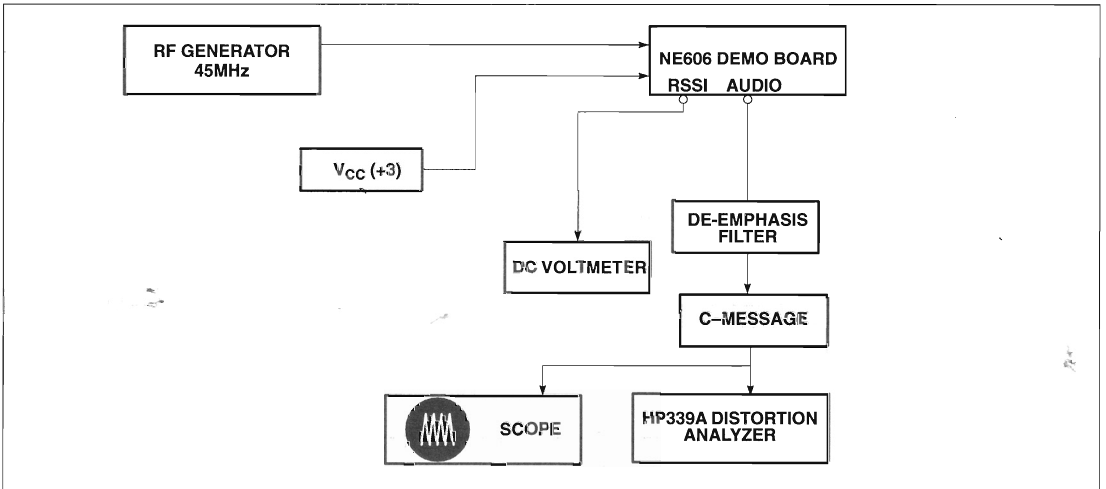


Figure 3. SA606 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35µV or -116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 10kΩ.

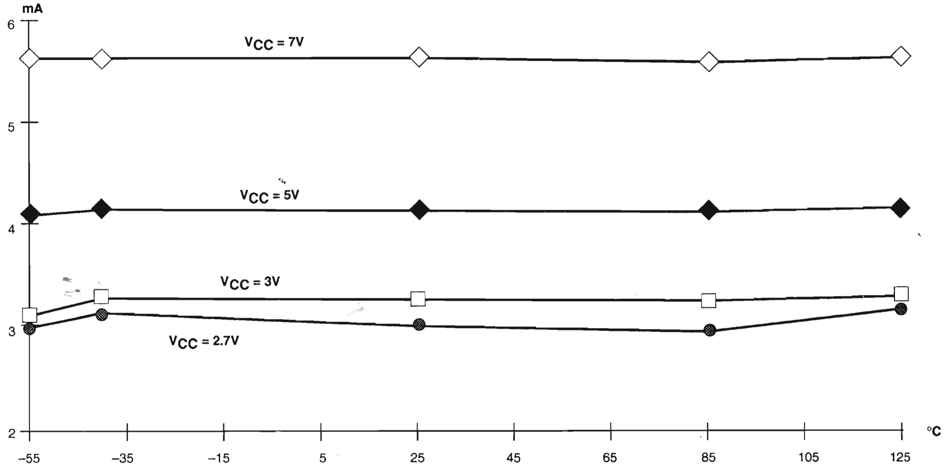


Figure 4. I_{CC} vs Temperature

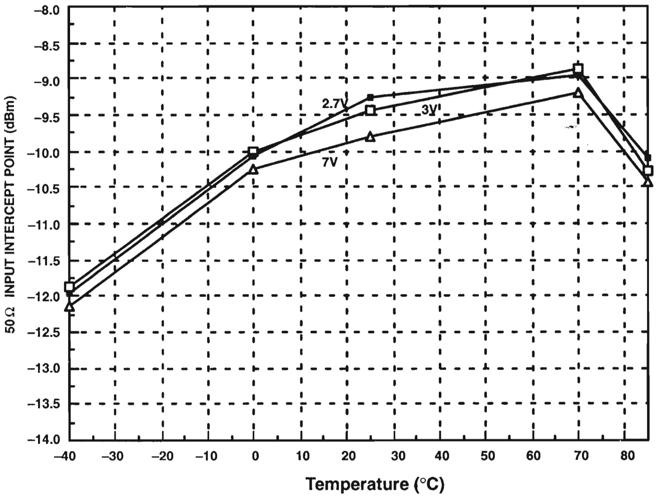


Figure 5. Third Order Intercept Point vs Supply Voltage

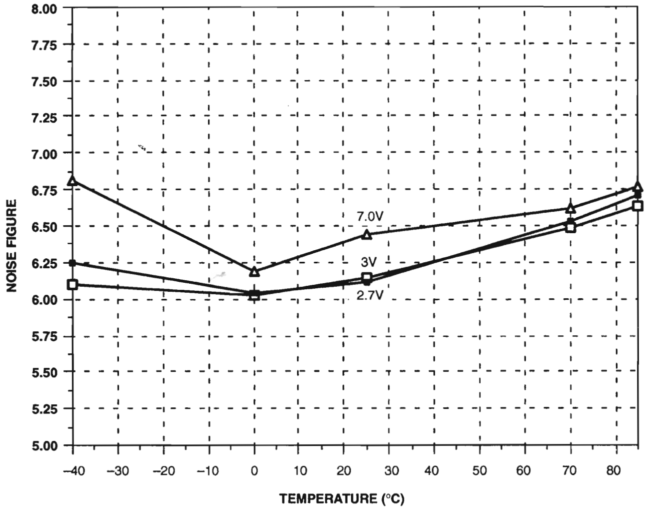


Figure 6. Mixer Noise Figure vs Supply Voltage

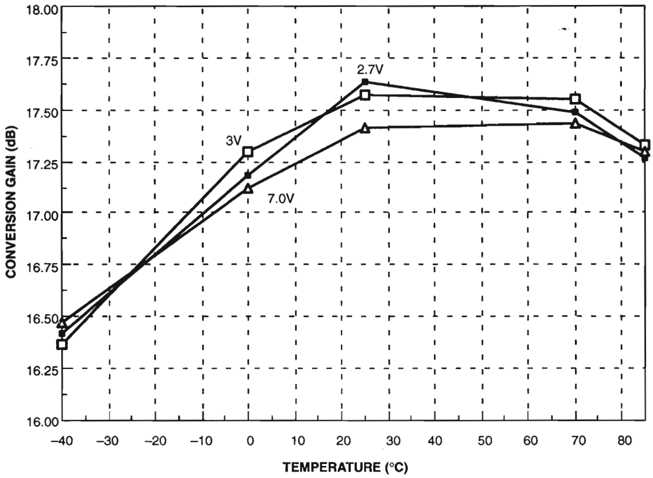
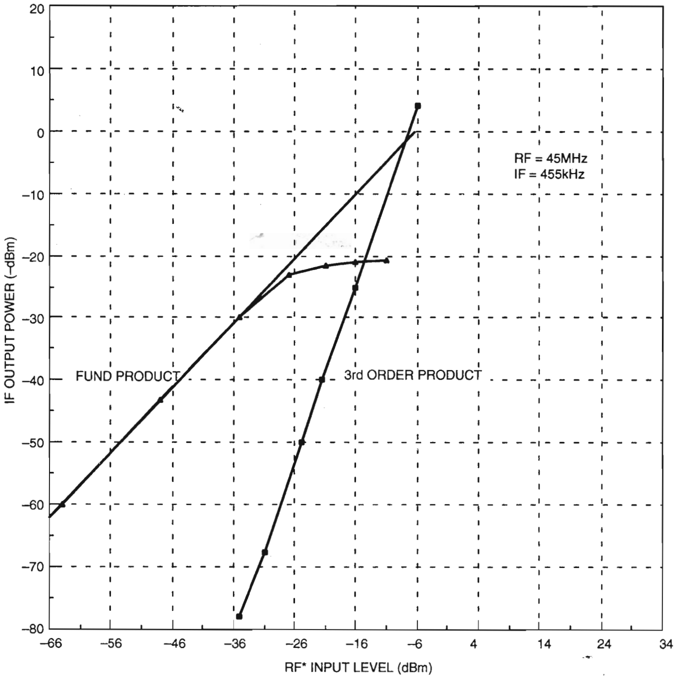


Figure 7. Conversion Gain vs Supply Voltage



*50Ω INPUT

Figure 8. Mixer Third Order Intercept and Compression

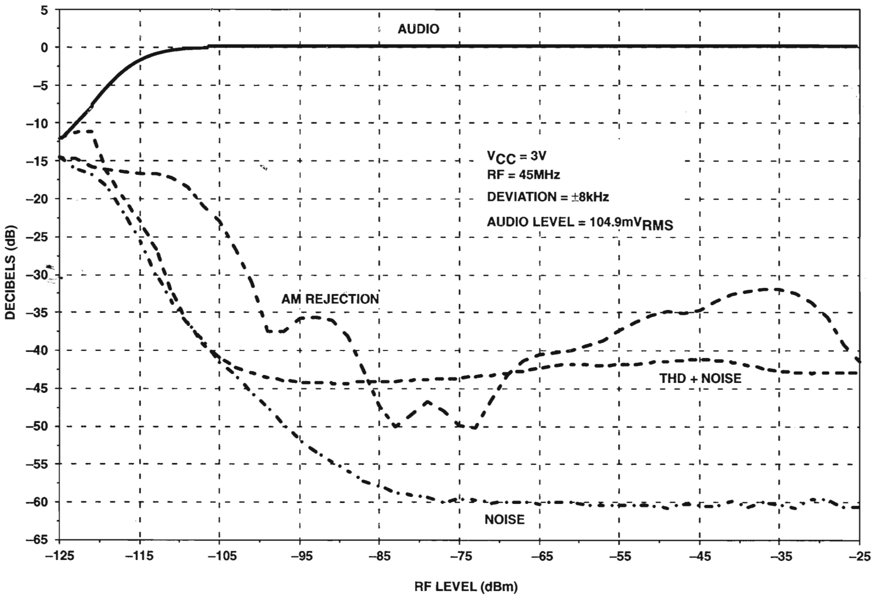


Figure 9. Sensitivity vs RF Level (-40°C)

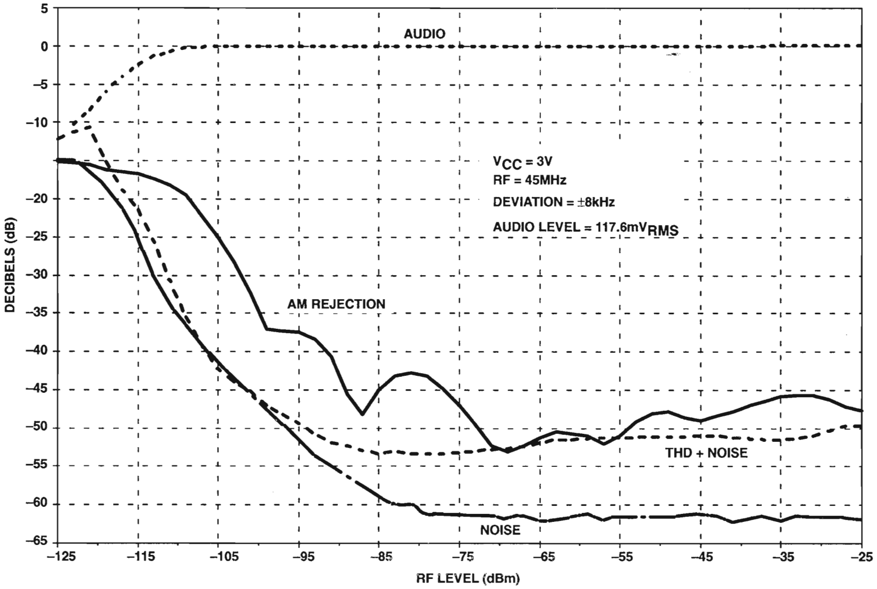


Figure 10. Sensitivity vs RF Level (+25°C)

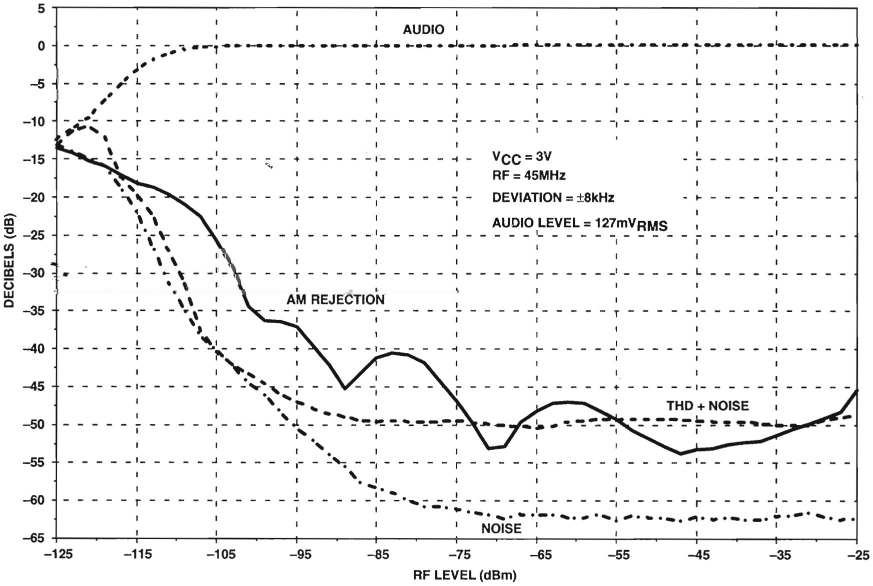


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

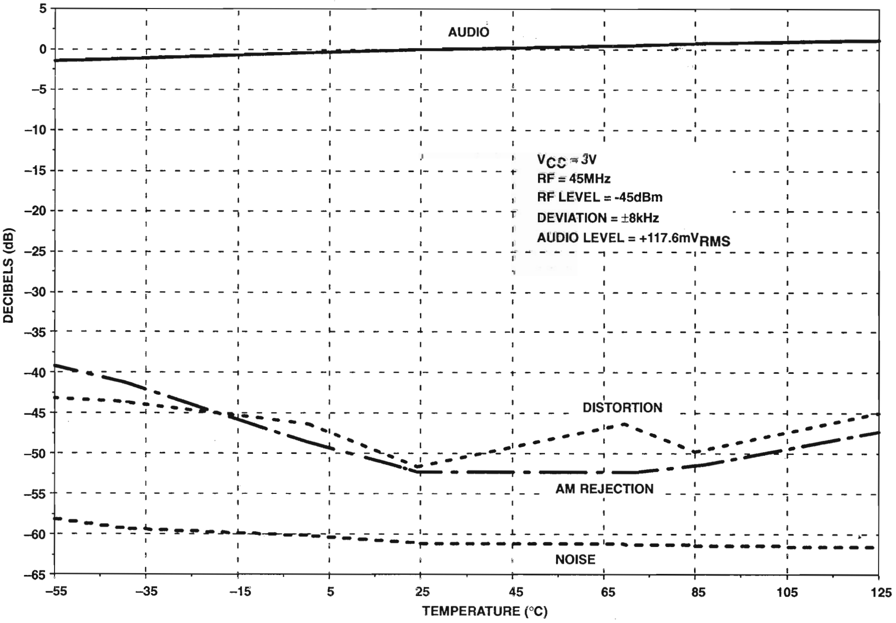


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

Low-voltage high performance mixer FM IF system

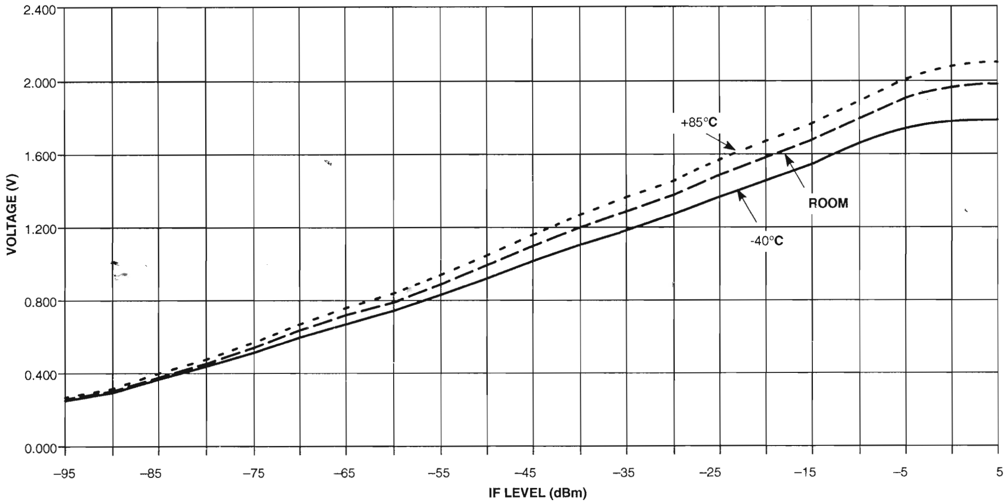


Figure 13. RSSI (455kHz IF @ 3V)

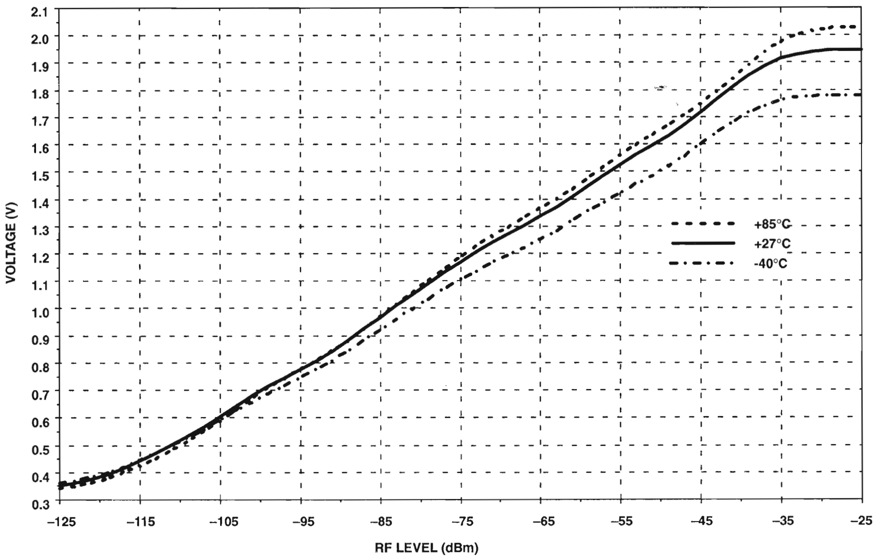


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

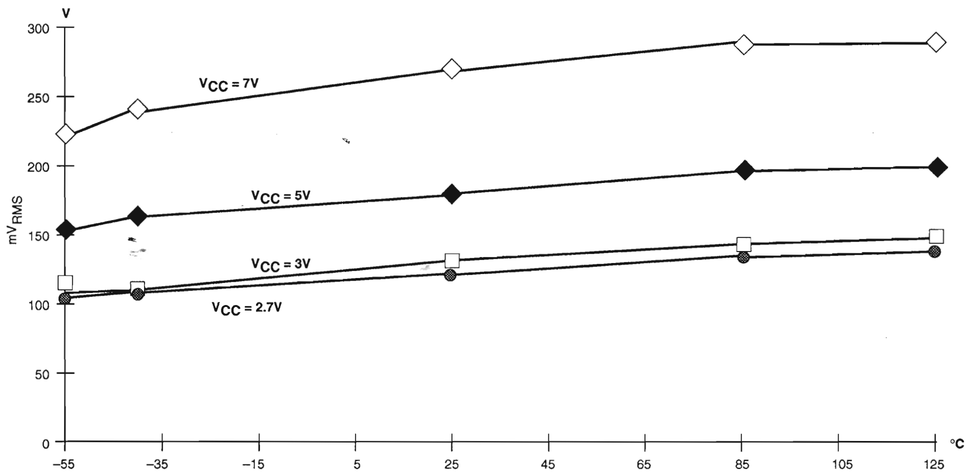


Figure 15. Audio Output vs Temperature

*Applies to Stand-Alone data sheets only.

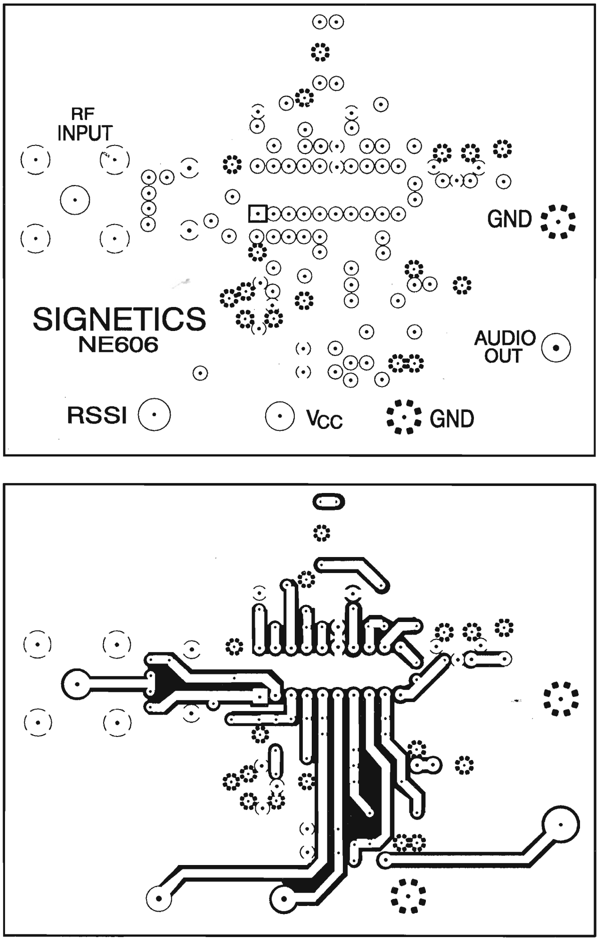


Figure 16. SA606N DIP Product Board Layout (Actual Size* — For Reference Use Only)

*Applies to Stand-Alone data sheets only.

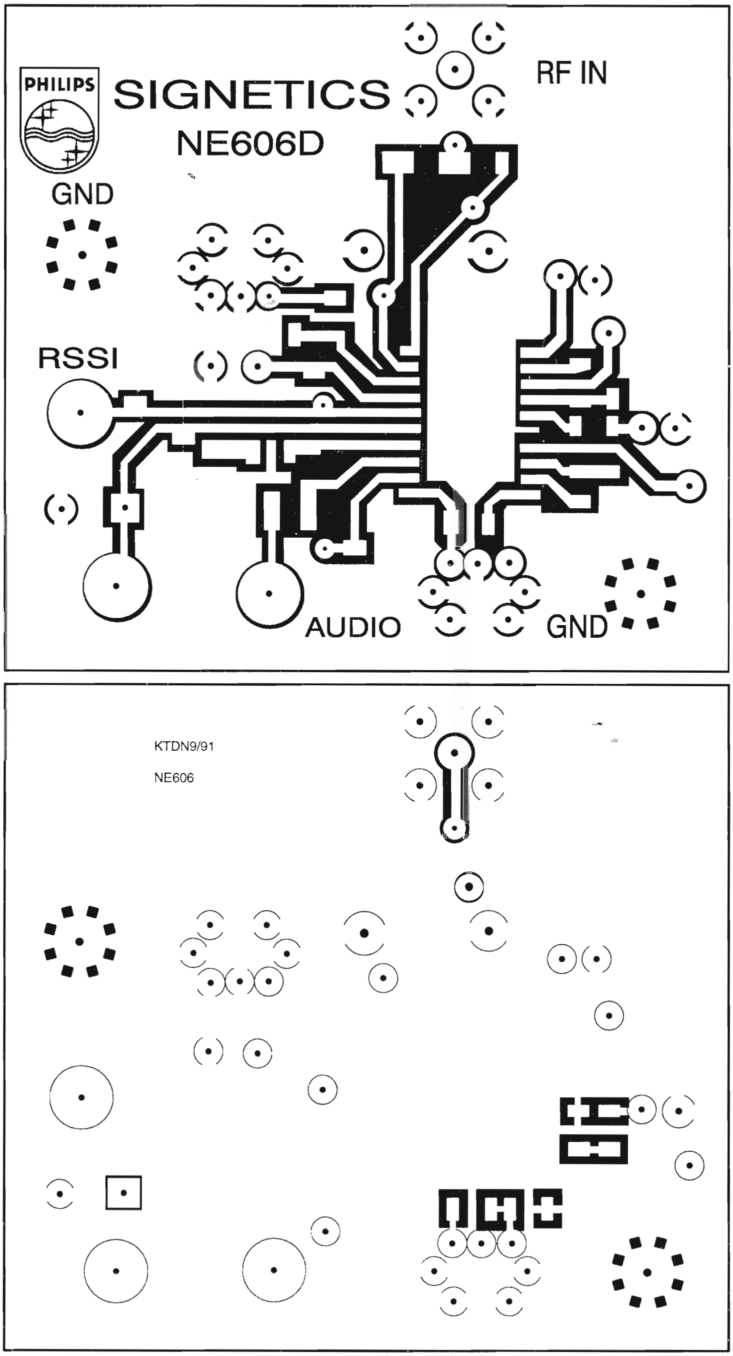
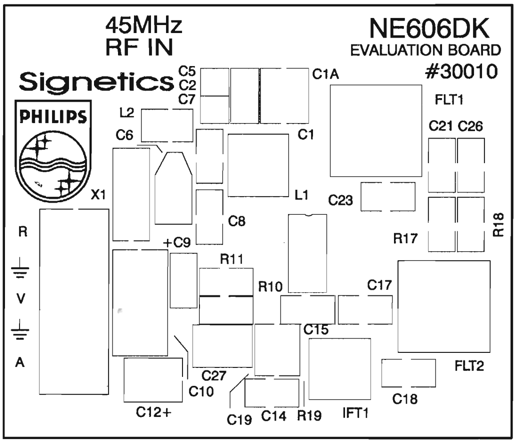
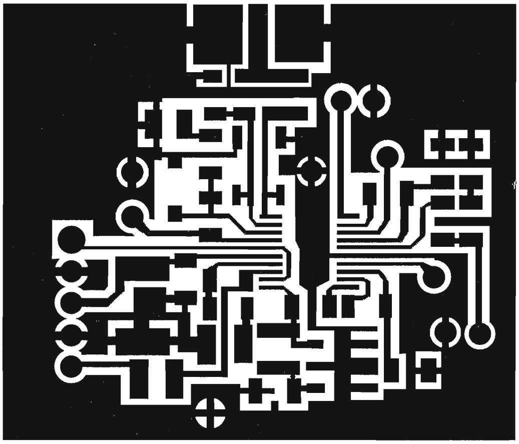


Figure 17. SA606D SOL Product Board Layout (2X Actual Size* — For Reference Use Only)

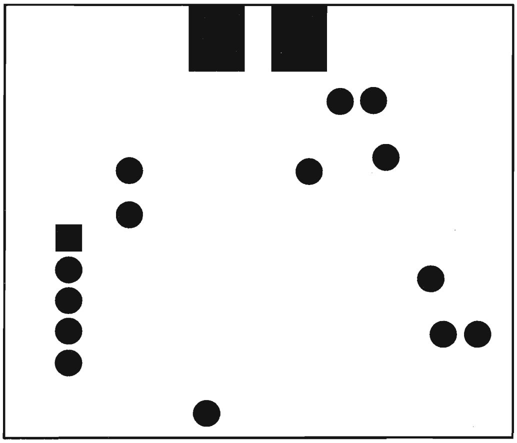
606 Silk Screen



606 TOP



606 BOTTOM



NOTE;
All views are TOP VIEW and
not actual size. For reference only.

DESCRIPTION

The SA616 is a low-voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA616 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink small outline package).

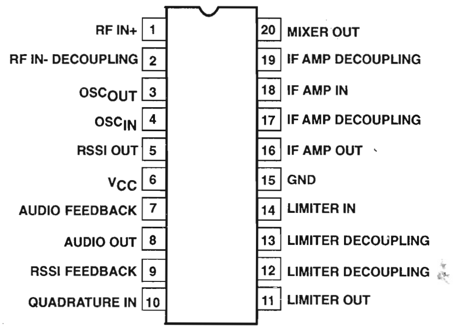
The SA616 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE615. The audio and RSSI outputs have amplifiers with access to the feedback path. This enables the designer to adjust the output levels or add filtering.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz IF amp/limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 80dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31µV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA616 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

PIN CONFIGURATION

D, DK and N Packages



APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Wireless systems
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receiver
- Single conversion VHF receivers

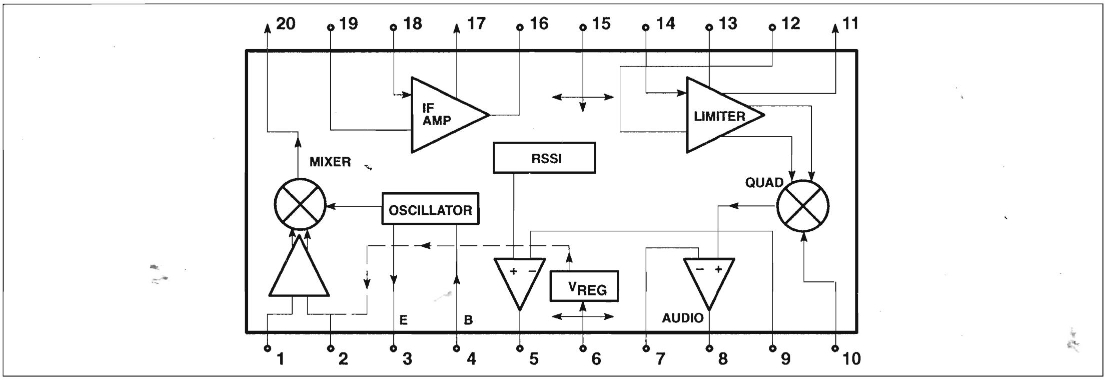
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA616N	0408B
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA616D	0172D
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA616DK	1563

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		7	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range		-40 to +85	°C
θ_{JA}	Thermal impedance	D package DK package N package	90 117 75	°C/W

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	5.0	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4kΩ and R18 = 3.3kΩ; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.8		dB
	Third-order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF level = -52dBm		-9		dBm
	Conversion power gain	Matched 14.5dBV step-up	11	17		dB
		50Ω source		+2.5		dB
	RF input resistance	Single-ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting -3dB, R_{17a} = 2.4k, R_{17b} = 3.3k	Test at Pin 18		-105		dBm
	AM rejection	80% AM 1kHz		40		dB
	Audio level	Gain of two (2kΩ AC load)	60	120		mV
	SINAD sensitivity	IF level -110dBm		17		dB
THD	Total harmonic distortion		-30	-45		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
S/N	Signal-to-noise ratio	No modulation for noise		62		dB
	RF RSSI output, R_9 = 2kΩ	RF level = -118dBm		0.3	.80	V
		RF level = -68dBm	.70	1.1	2	V
		RF level = -23dBm	1.0	1.8	2.50	V
	RSSI range			80		dB
	RSSI accuracy			±2		dB
	IF input impedance	Pin 18	1.3	1.5		kΩ
	IF output impedance	Pin 16		0.3		kΩ
	Limiter input impedance	Pin 14	1.3	1.5		kΩ
	Limiter output impedance	Pin 11		0.3		kΩ
	Limiter output voltage	Pin 11		130		mV_{RMS}
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = -27dBm		120		mV_{RMS}
	System RSSI output	3V = V_{CC}, RF level = -27dBm		2.2		V
	System SINAD sensitivity	RF level = -117dBm		12		dB

CIRCUIT DESCRIPTION

The SA616 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of -9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

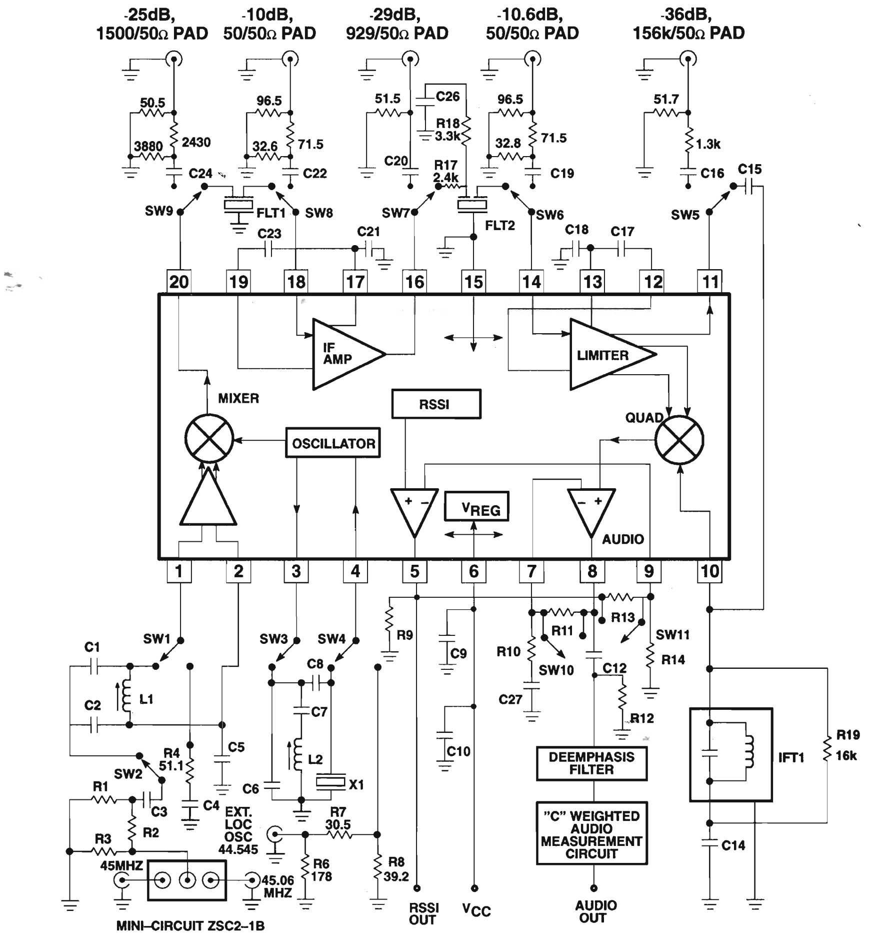
The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

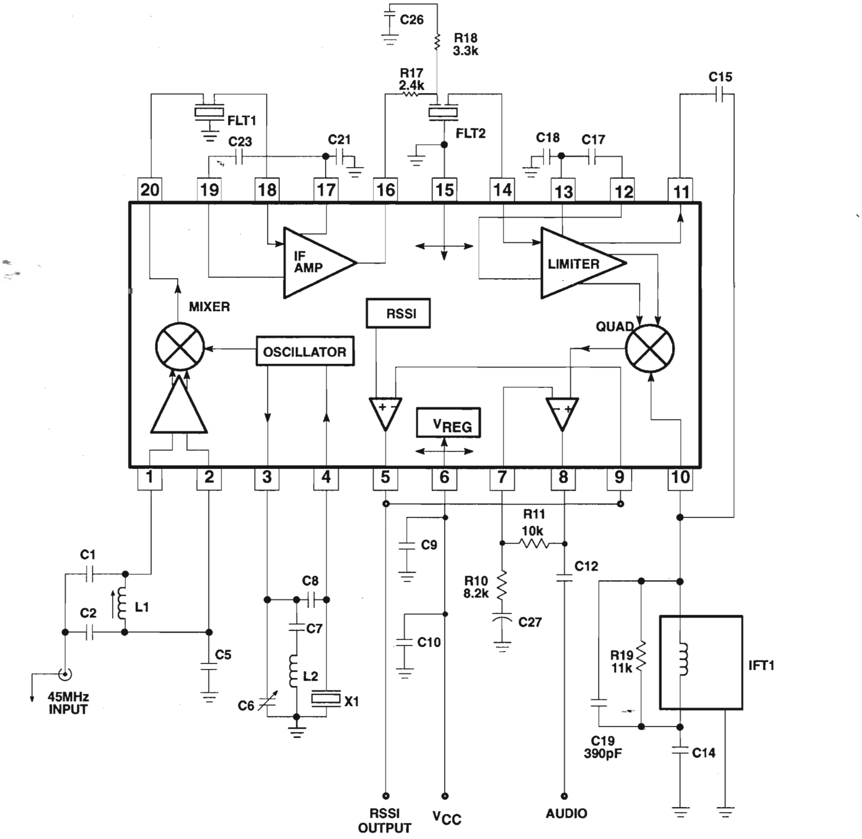
NOTE: dB(v) = 20log V_{OUT}/V_{IN}



Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C27	100nF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C5	100nF ±10% Monolithic Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C6	22pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C7	1nF Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C8	10.0pF NPO Ceramic	L2	0.8μH nominal
C9	100nF ±10% Monolithic Ceramic		Toko 292CNS–T1038Z
C10	15μF Tantalum (minimum)	X1	44.545MHz Crystal ICM4712701
C12	2.2μF	R9	2kΩ ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R10	8.2kΩ ±1%
C15	10pF NPO Ceramic	R11	10kΩ ±1%
C17	100nF ±10% Monolithic Ceramic	R12	2kΩ ±1%
C18	100nF ±10% Monolithic Ceramic	R13	20kΩ ±1%
C21	100nF ±10% Monolithic Ceramic	R14	10kΩ ±1%
C23	100nF ±10% Monolithic Ceramic	R17	2.4kΩ ±5% 1/4W Carbon Composition
C25	100nF ±10% Monolithic Ceramic	R18	3.3kΩ
C26	100nF ±10% Monolithic Ceramic	R19	16kΩ

Figure 1. SA616 45MHz Test Circuit (Relays as shown)



NE616D/DK Demoboard Application Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15µF Tantalum (minimum)
C12	2.2µF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2µF Tantalum
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330µH TOKO 303LN-1130
L1	.33µH TOKO SCB-1320Z
L2	1.2µH
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

Figure 2. SA616 45MHz Application Circuit

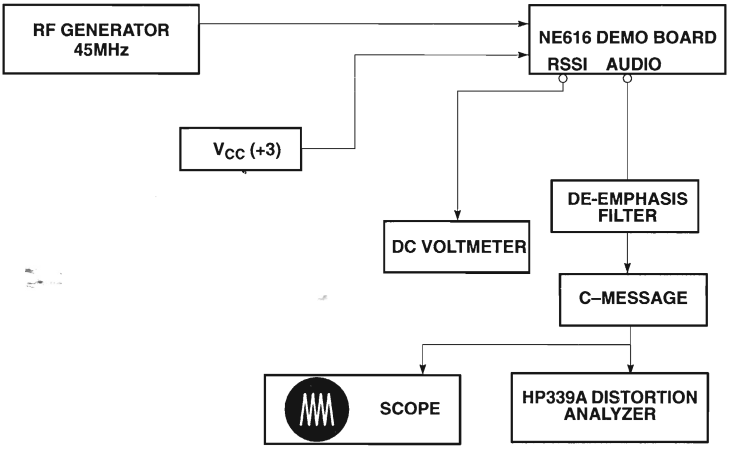


Figure 3. SA616 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35µV or -116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

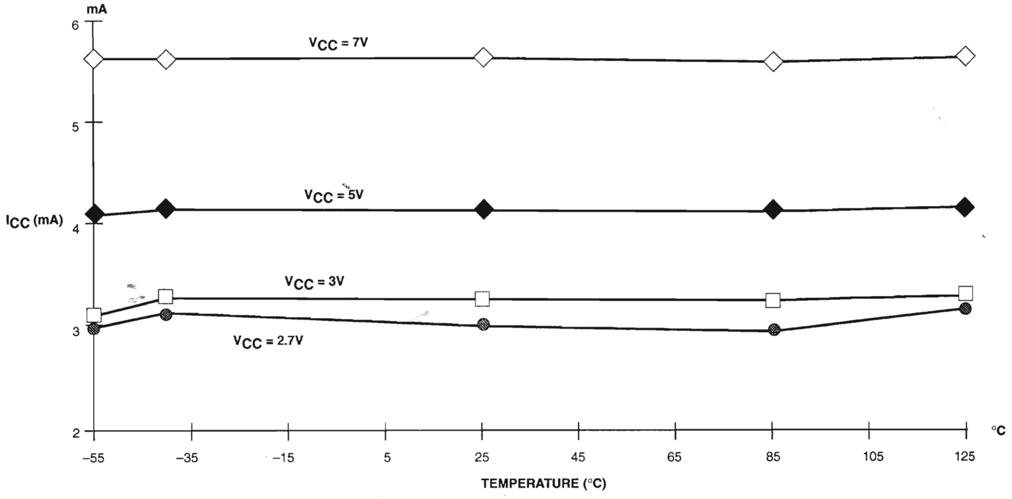


Figure 4. I_{CC} vs Temperature

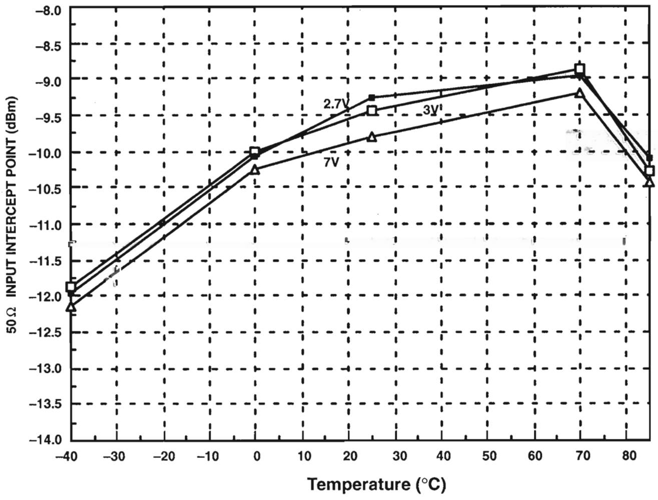


Figure 5. Third Order Intercept Point vs Supply Voltage

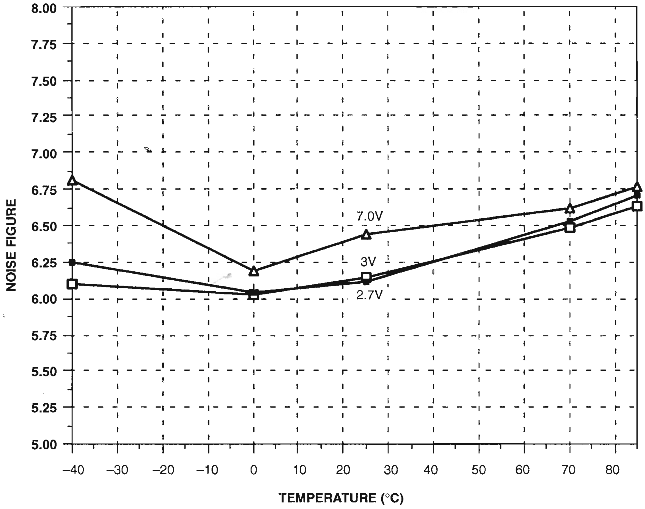


Figure 6. Mixer Noise Figure vs Supply Voltage

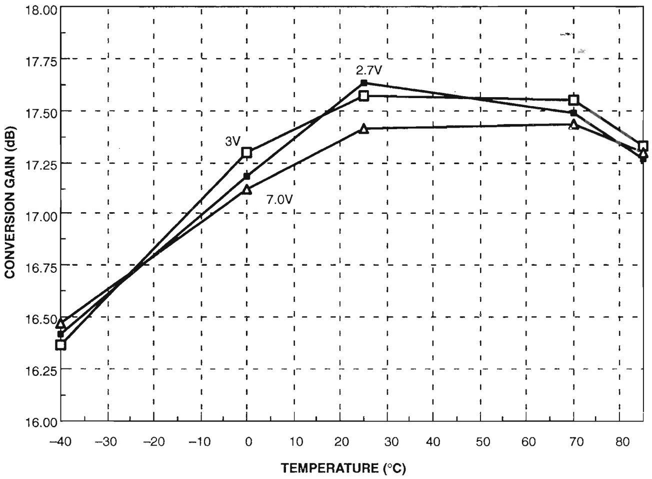


Figure 7. Conversion Gain vs Supply Voltage

Low-voltage high performance mixer FM IF system

SA616

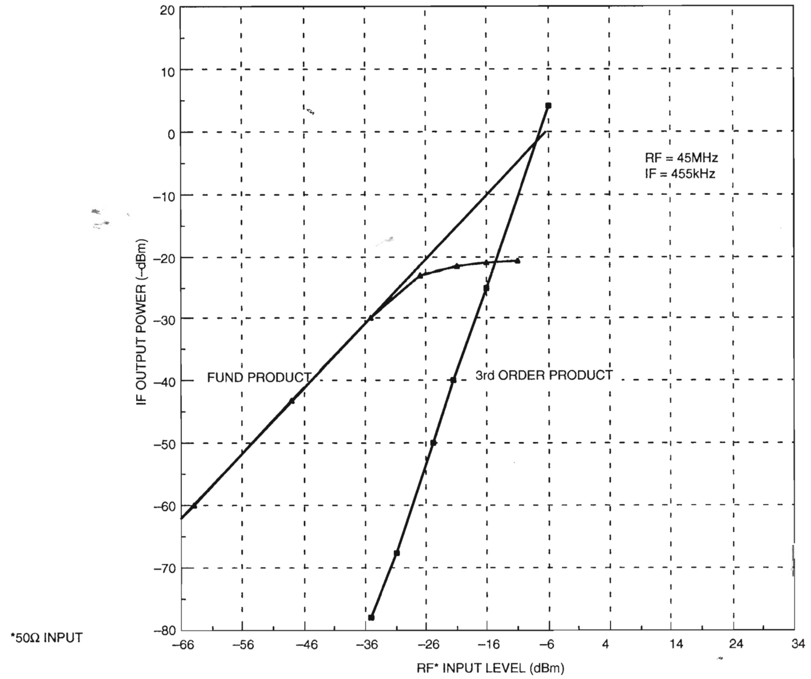


Figure 8. Mixer Third Order Intercept and Compression

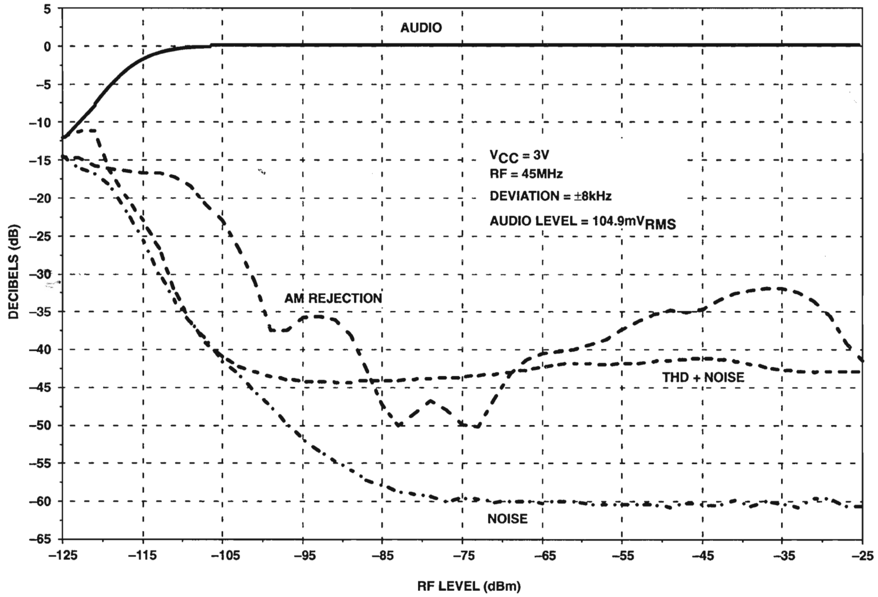


Figure 9. Sensitivity vs RF Level (-40°C)

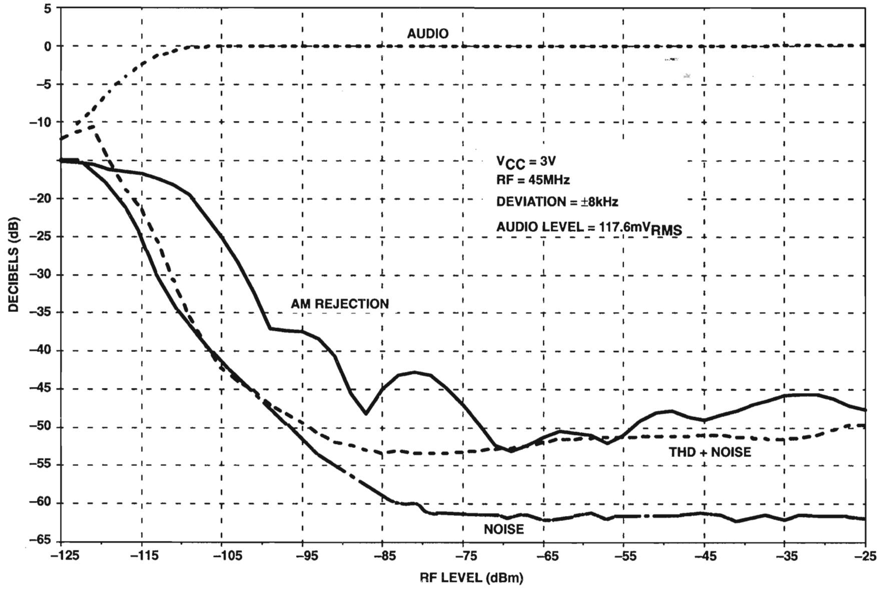


Figure 10. Sensitivity vs RF Level (+25°C)

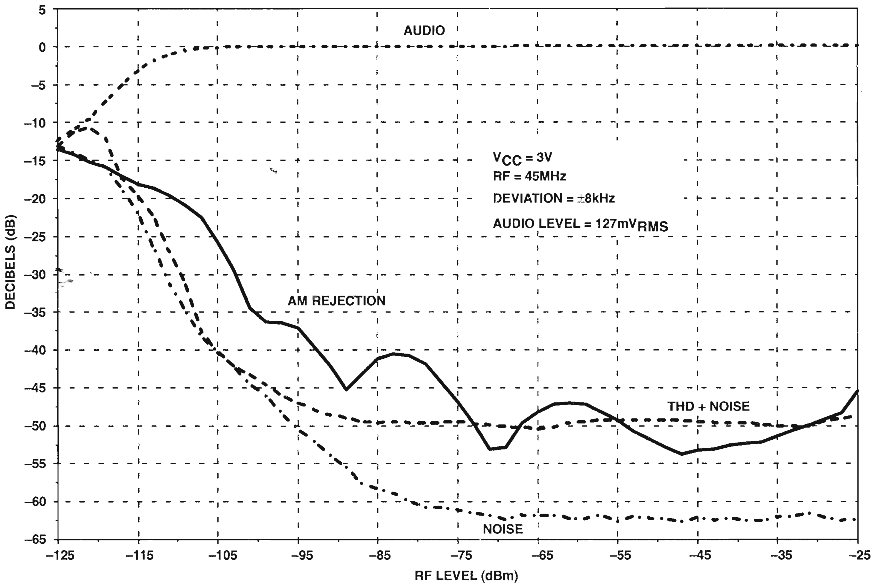


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

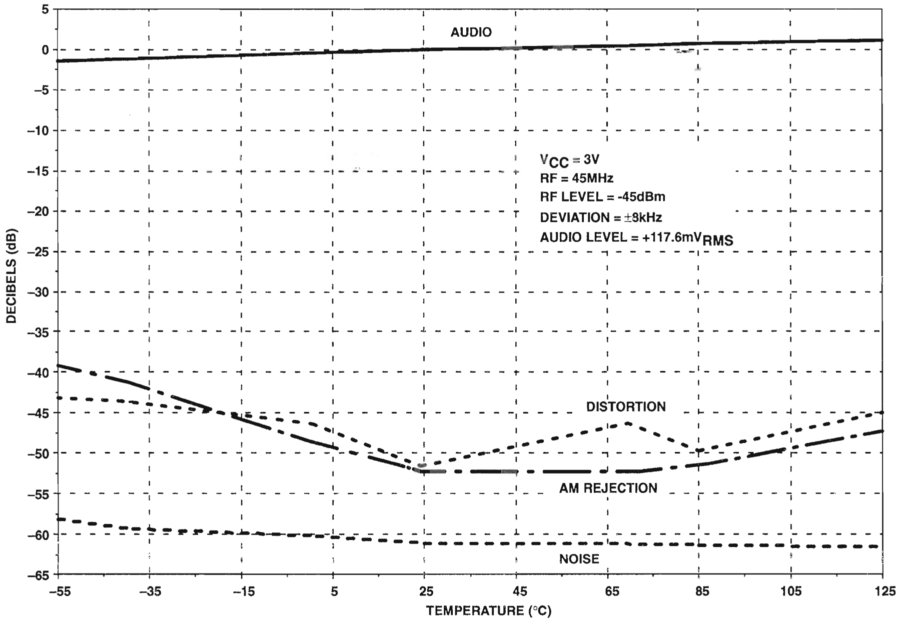


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

Low-voltage high performance mixer FM IF system SA616

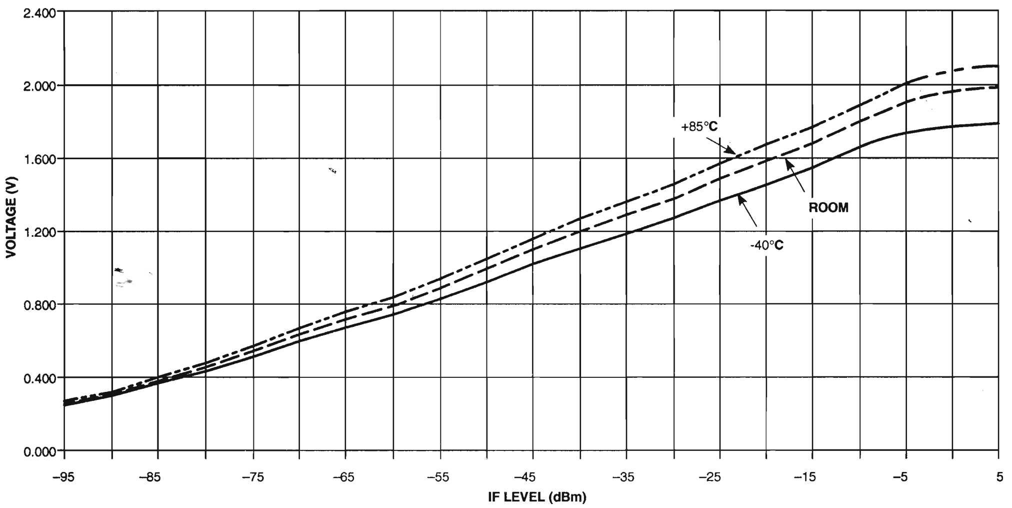


Figure 13. RSSI (455kHz IF @ 3V)

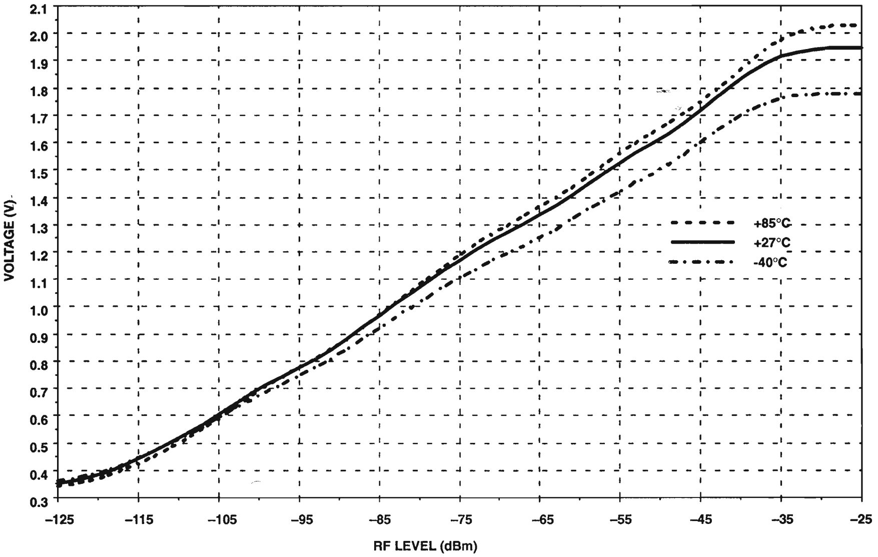


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

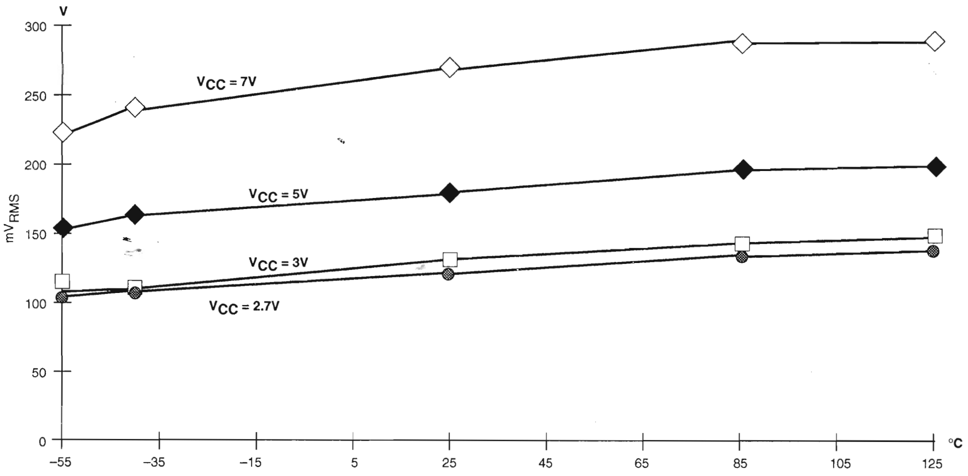
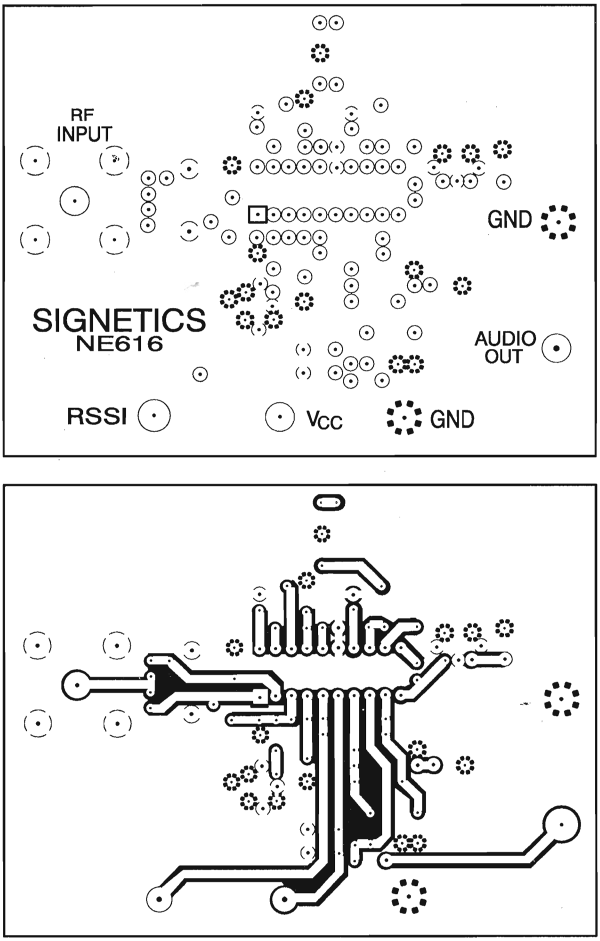


Figure 15. Audio Output vs Temperature

Low-voltage high performance mixer FM IF system SA616



***Applies to Stand-Alone data sheets only.**

Figure 16. SA616N DIP Product Board Layout (Actual Size* — For Reference Use Only)

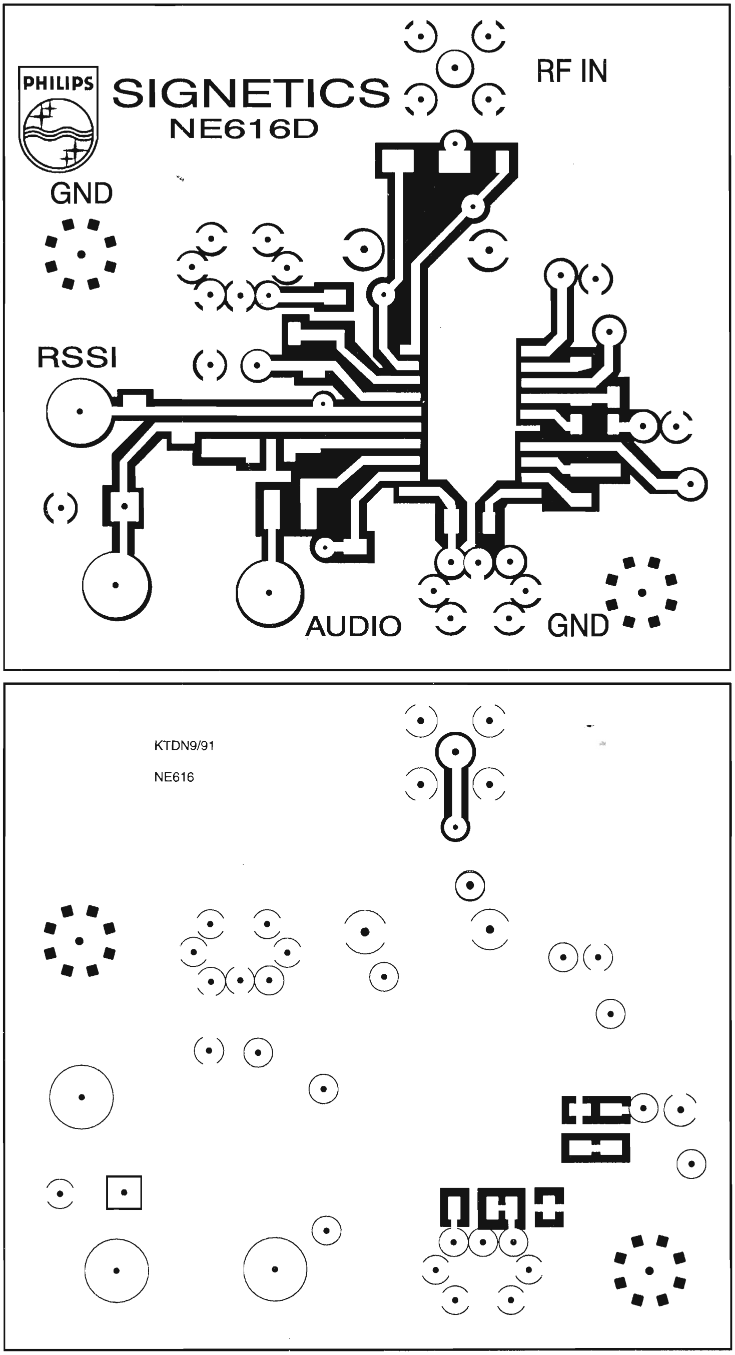
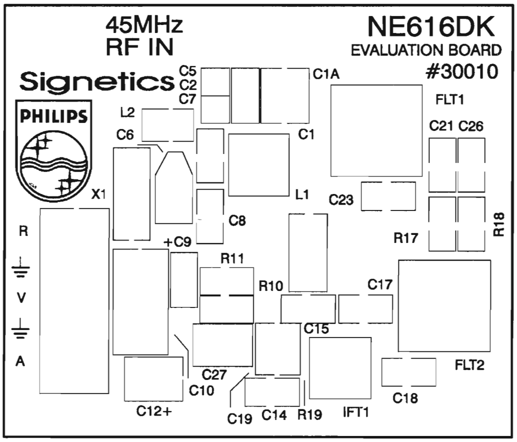
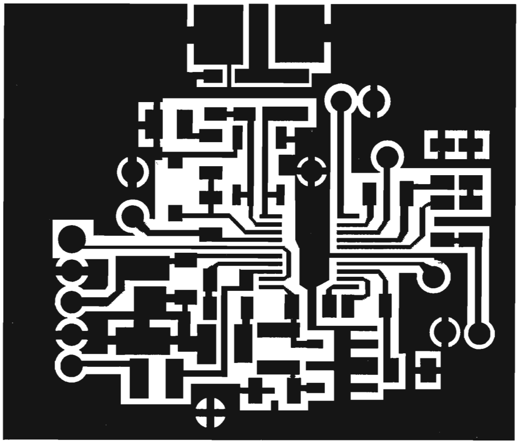


Figure 17. SA616D SOL Product Board Layout (2X Actual Size* — For Reference Use Only)

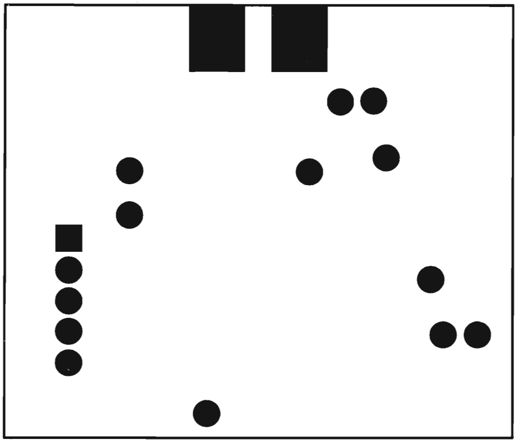
***Applies to Stand-Alone data sheets only.**



616 Silk Screen



616 TOP



616 BOTTOM

NOTE;
All views are TOP VIEW and
not actual size. For reference only.

Low voltage high performance mixer FM IF system SA607

DESCRIPTION

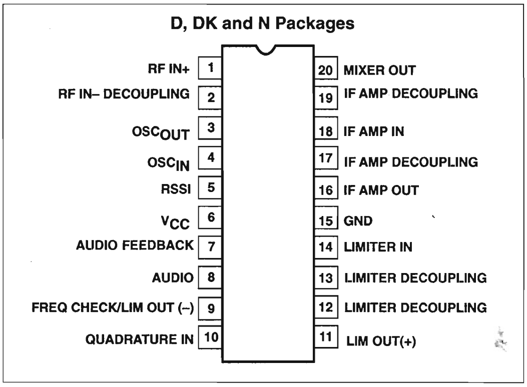
The SA607 is a low voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA607 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP package.

The SA607 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio output has an internal amplifier with the feedback pin accessible. The RSSI output is buffered. The SA607 also has an extra limiter output. This signal is buffered from the output of the limiter and can be used to perform frequency check. This is accomplished by comparing a reference frequency with the frequency check signal using a comparator to a varactor or PLL at the oscillator inputs.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31µV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA607 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Buffered frequency check output
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

PIN CONFIGURATION



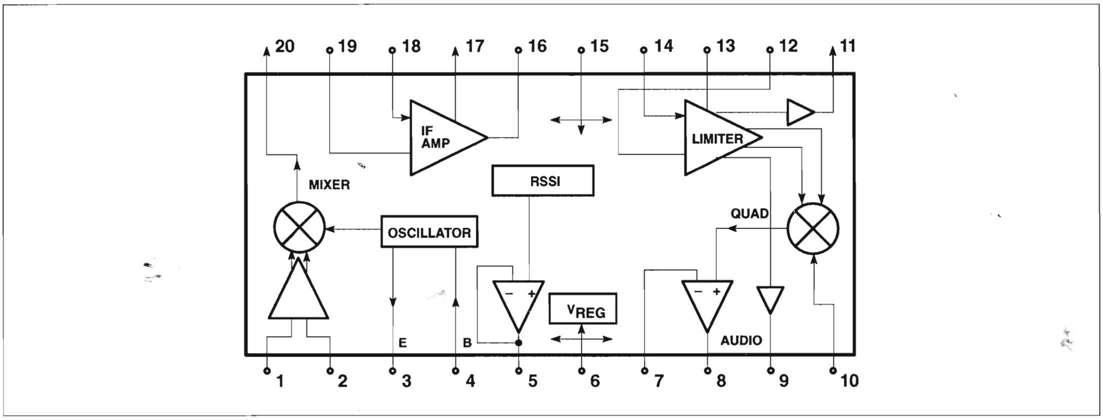
APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Narrow band cellular applications (NAMPS/NTACS)
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receivers
- Single conversion VHF receivers
- Wireless systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA607N	0408B
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA607D	0172D
20-Pin Plastic Shirnk Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA607DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range SA607	–40 to +85	°C
θ_{JA}	Thermal impedance D package DK package N package	90 117 75	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA607			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

Low voltage high performance mixer FM IF system SA607

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = +3V$, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4k; R18 = 3.3k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA607			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF Level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17} = 2.4k	Test at Pin 18		–109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level	Gain of two (2kΩ AC load)	70	120	160	mV
	SINAD sensitivity	RF level –110dB		17		dB
THD	Total harmonic distortion		–35	–50		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	0.8	V
		IF level = –68dBm	.70	1.1	1.80	V
		IF level = –23dBm	1.2	1.8	2.5	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance		1.3	1.5		kΩ
	IF output impedance			0.3		kΩ
	Limiter input impedance		1.30	1.5		kΩ
	Limiter output impedance	(Pin 11)		200		Ω
	Limiter output level	(Pin 11) No load 5kΩ load		130 115		mV$_{RMS}$
	Frequency check/limiter output impedance	(Pin 9)		200		Ω
	Frequency check/limiter output level	(Pin 9) No load 5kΩ load		130 115		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		120		mV$_{RMS}$
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:

1. The generator source impedance is 50Ω, but the SA607 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA607 input (Pin 18) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The SA607 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

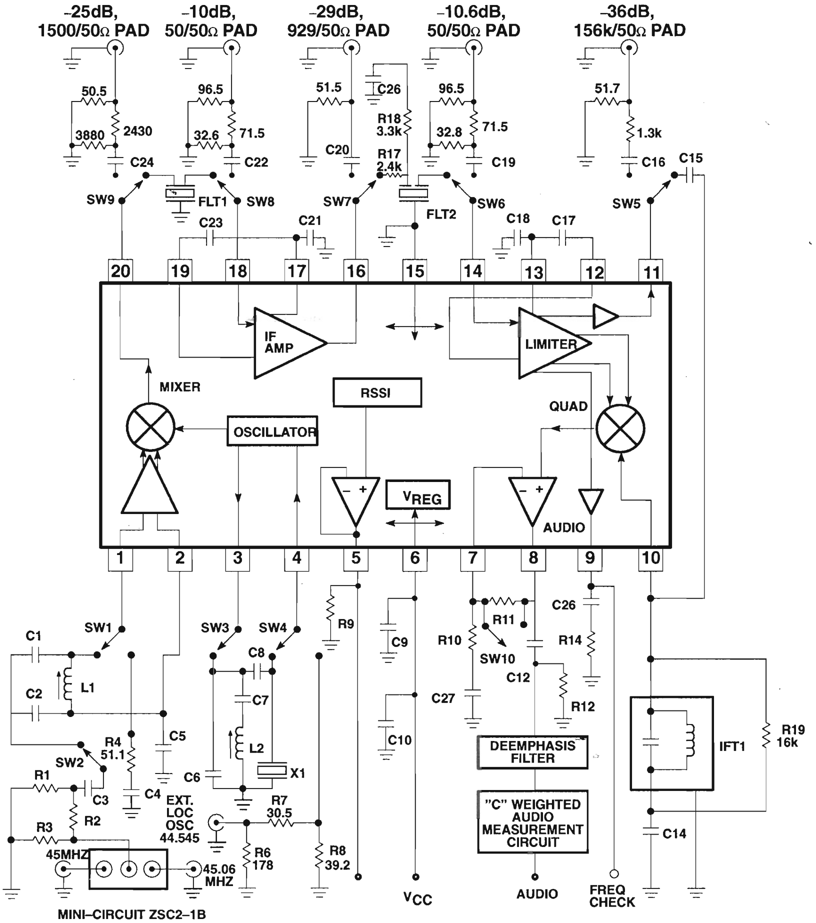
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal is buffered through an internal unity gain op amp. The frequency check pin provides a buffered limiter output. This is useful for implementing an AFC (Automatic Frequency Check) function. This same output can also be used in conjunction with limiter output (Pin 11) for demodulating FSK (Frequency Shift Keying) data. Both pins are of the same amplitude, but 180° out of phase.

NOTE: Limiter output or Frequency Check output has drive capability of a load minimum of 2kΩ or higher to obtain 115mV output level.

NOTE: dB(v) = 20log V_{OUT}/V_{IN}



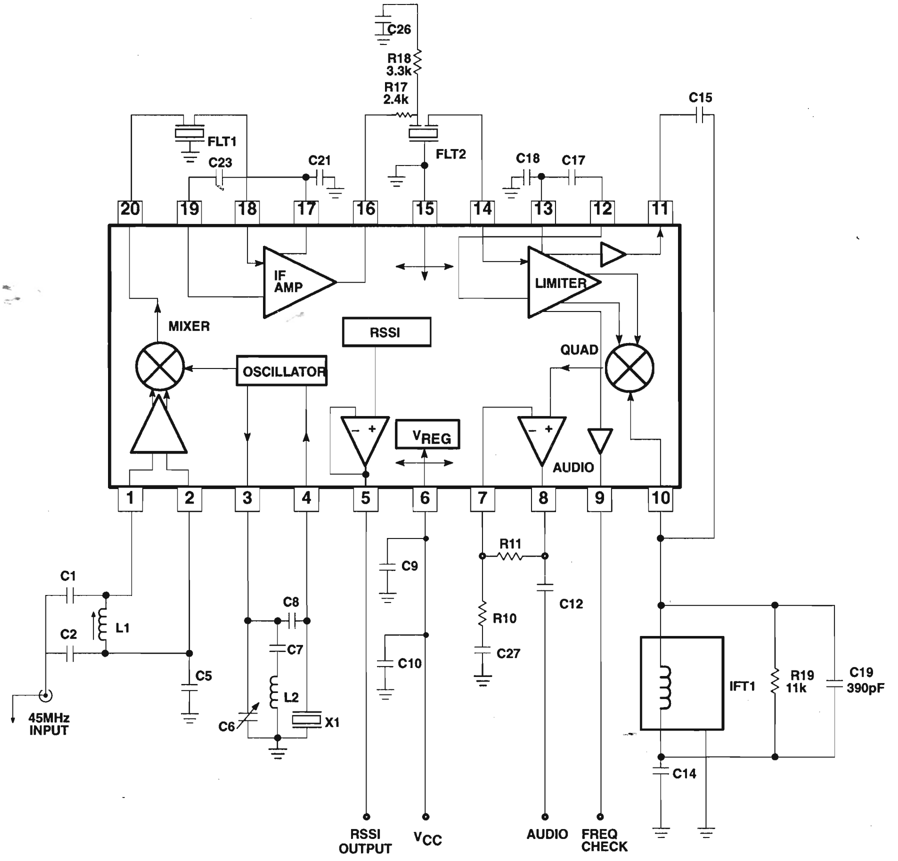
Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic

C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC-2A6597H
L1	147–160nH Coilcraft UNI-10/142-04J08S
L2	0.8μH nominal Toko 292CNS-T1038Z
X1	44.545MHz Crystal ICM4712701
R9	2kΩ ±1% 1/4W Metal Film
R10	8.2kΩ ±1%
R11	10kΩ ±1%
R12	2kΩ ±1%
R14	5kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. SA607 45MHz Test Circuit (Relays as shown)



SA607D/DK
Application Component List

C1	51pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C2	220pF NPO Ceramic	C26	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C27	2.2µF Tantalum
C6	5-30pF trim cap	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C7	1nF Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	IFT 1	330µH TOKO 303LN-1130
C9	100nF ±10% Monolithic Ceramic	L1	.33µH TOKO SCB-1320Z
C10	10µF Tantalum (minimum) *	L2	1.2µH Coilcraft 1008C S-122
C12	2.2µF ±10% Tantalum	X1	44.545MHz Crystal Hy–Q
C14	100nF ±10% Monolithic Ceramic	R5	Not Used in Application Board (see Note 8, pg 8)
C15	10pF NPO Ceramic	R10	8.2k ±5% 1/4W Carbon Composition
C17	100nF ±10% Monolithic Ceramic	R11	10k ±5% 1/4W Carbon Composition
C18	100nF ±10% Monolithic Ceramic	R17	2.4k ±5% 1/4W Carbon Composition
C19	390pF ±10% Monolithic Ceramic	R18	3.3k ±5% 1/4W Carbon Composition
C21	100nF ±10% Monolithic Ceramic	R19	11k ±5% 1/4W Carbon Composition

***NOTE: This value can be reduced when a battery is the power source.**

Figure 2. SA607 45MHz Application Circuit

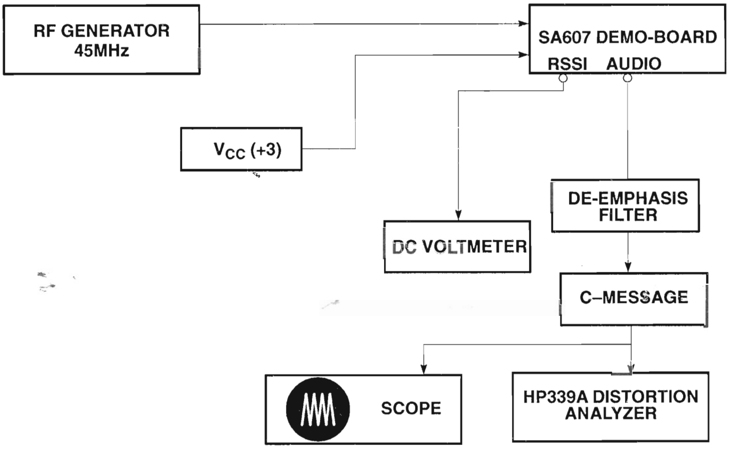


Figure 3. SA607 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35μV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

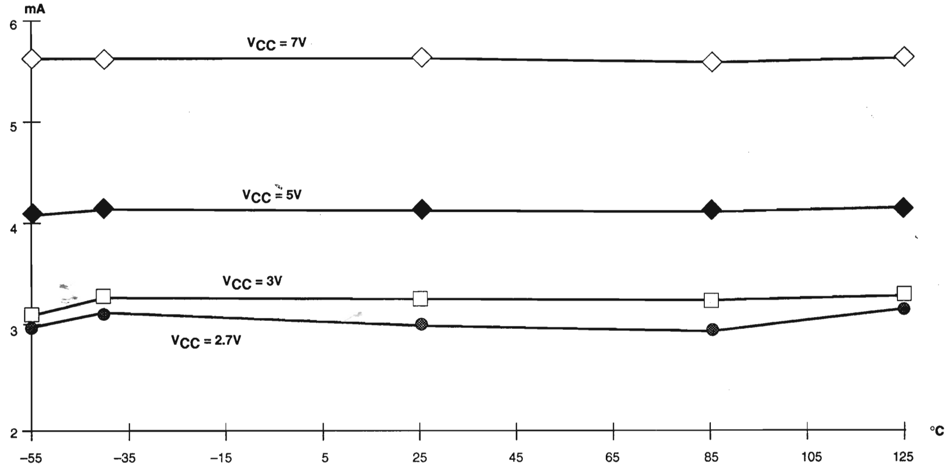


Figure 4. I_{CC} vs Temperature

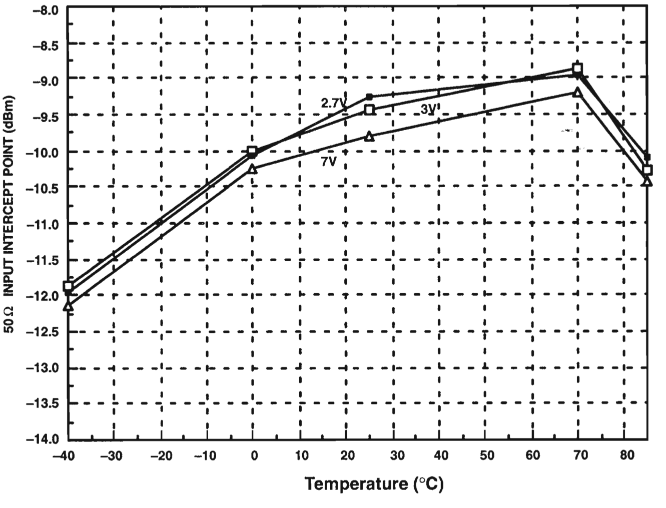


Figure 5. Third Order Intercept Point vs Supply Voltage

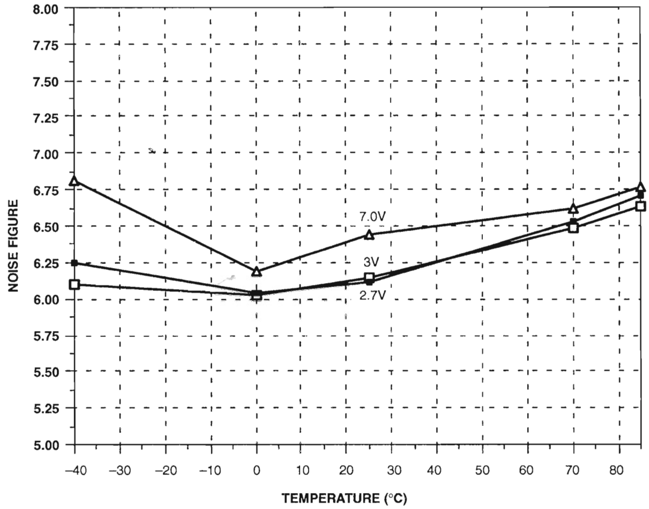


Figure 6. Mixer Noise Figure vs Supply Voltage

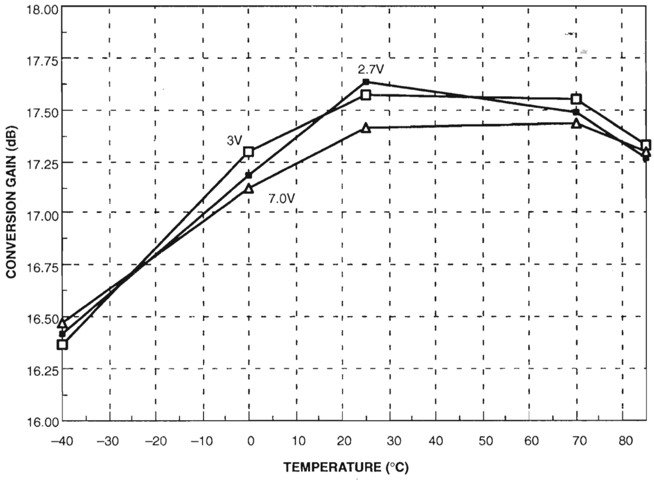


Figure 7. Conversion Gain vs Supply Voltage

Low voltage high performance mixer FM IF system SA607

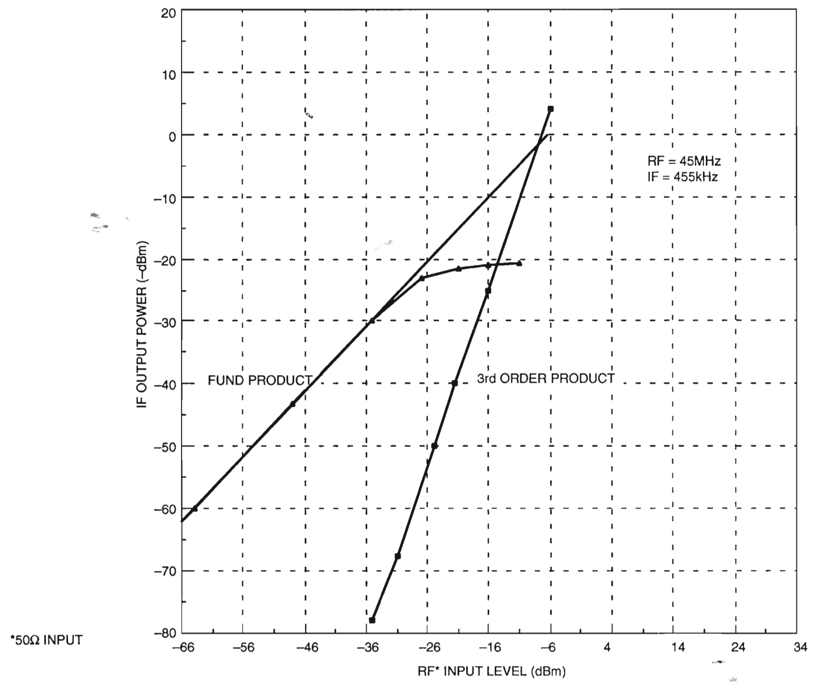


Figure 8. Mixer Third Order Intercept and Compression

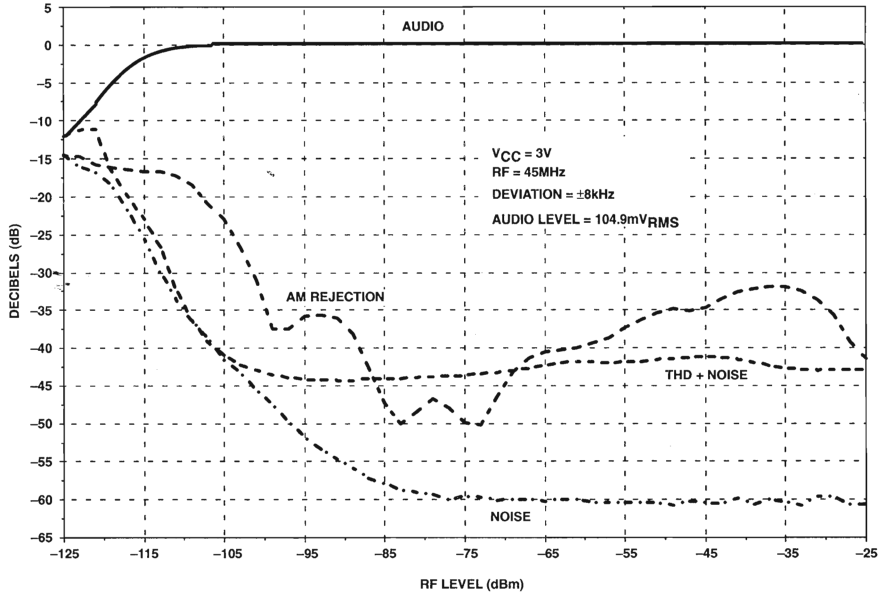


Figure 9. Sensitivity vs RF Level (–40°C)

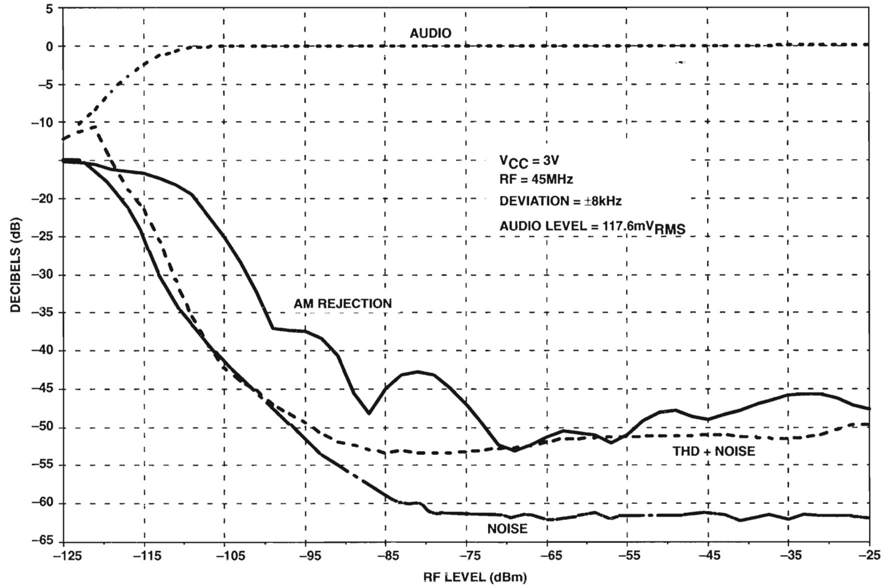


Figure 10. Sensitivity vs RF Level (+25°C)

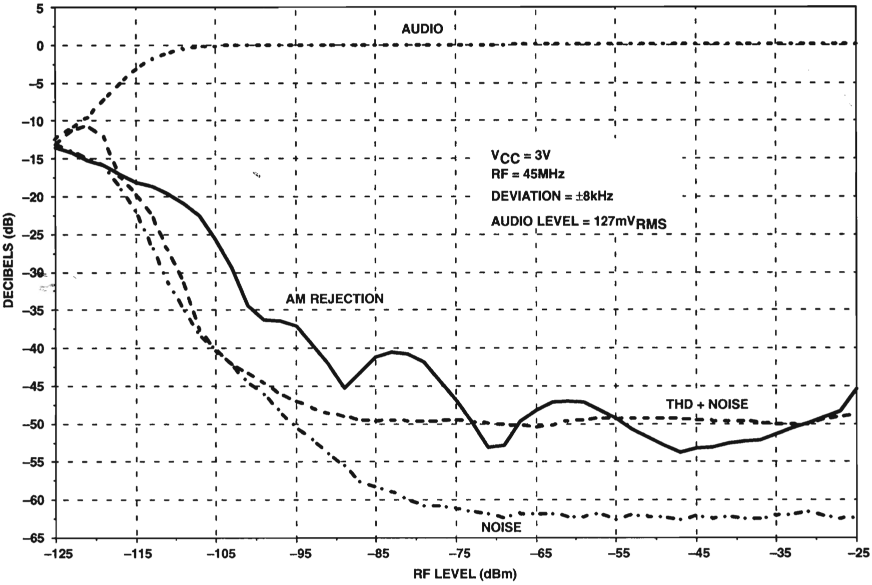


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

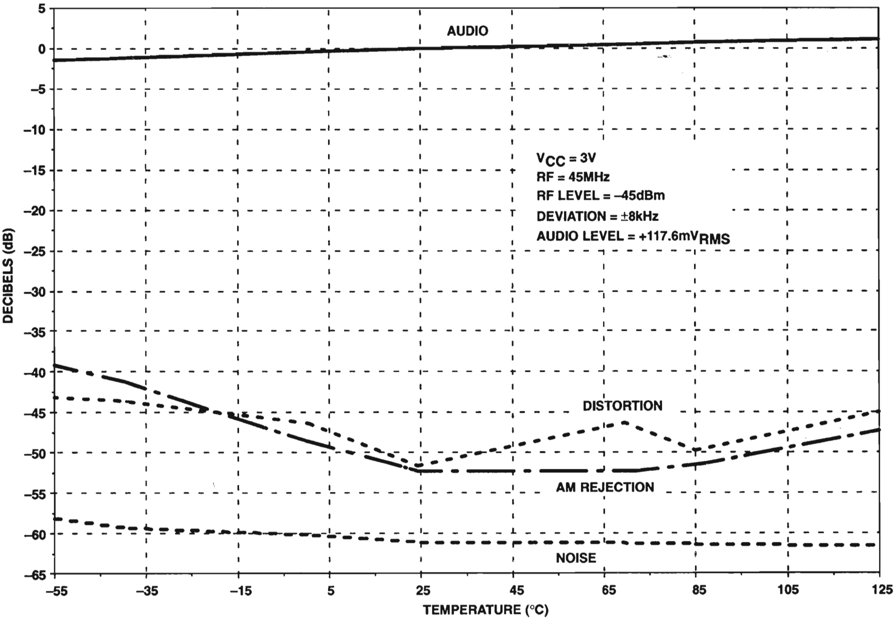


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

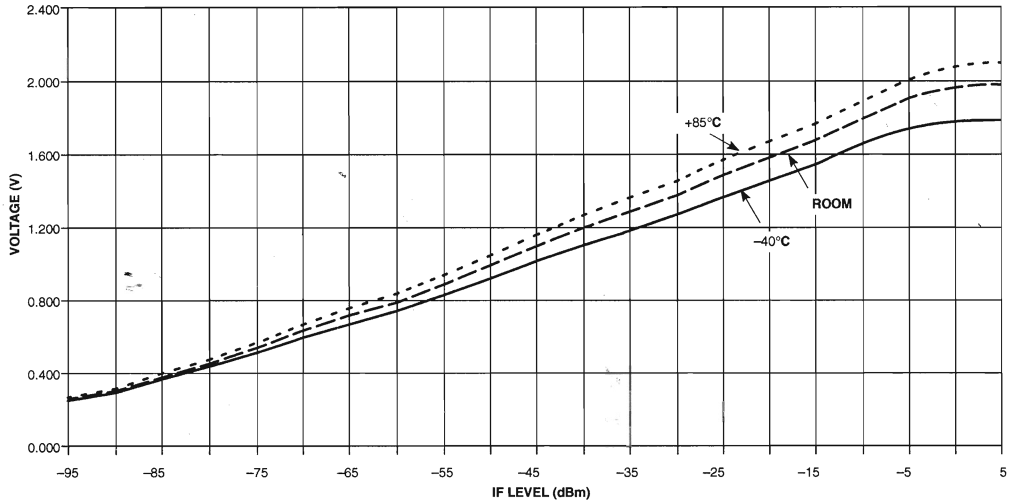


Figure 13. RSSI (455kHz IF @ 3V)

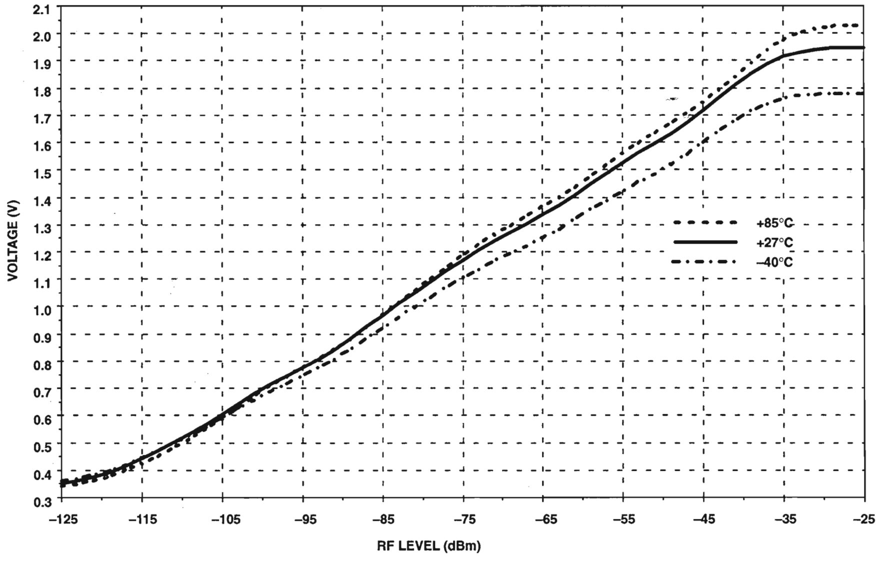


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

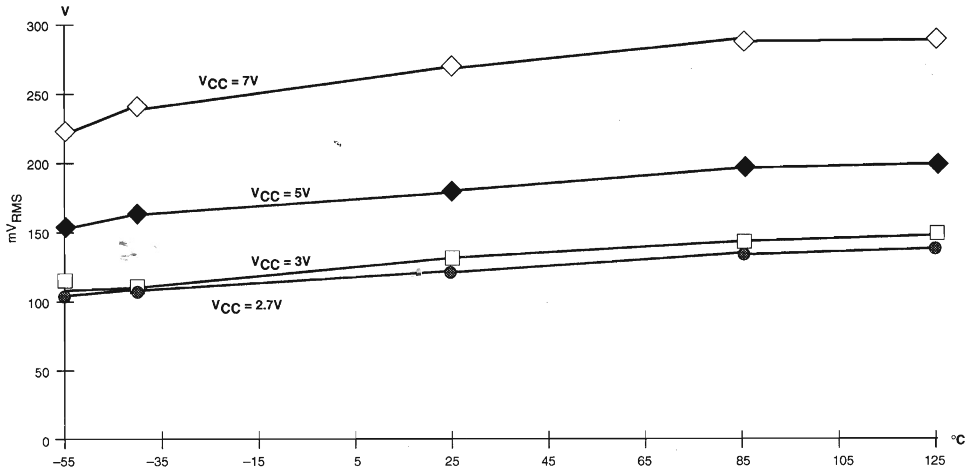
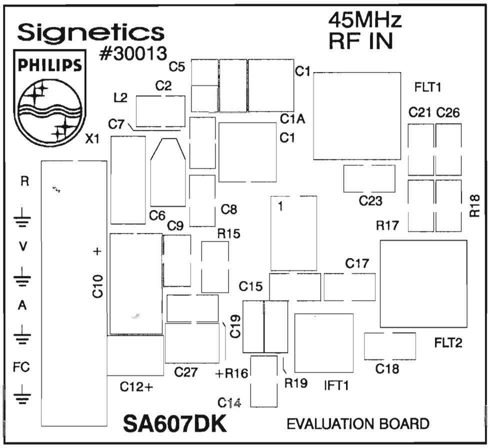
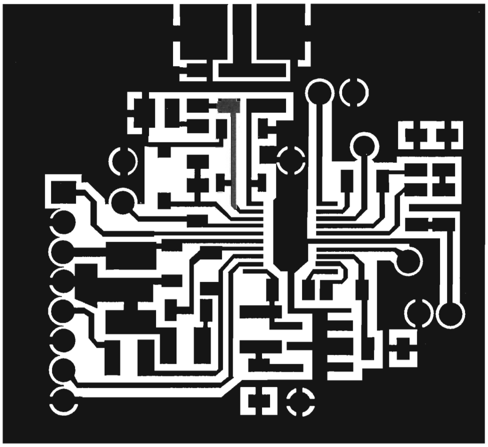


Figure 15. Audio Output vs Temperature

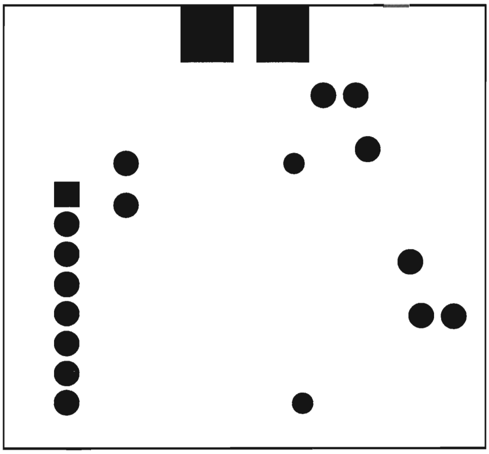
Low voltage high performance mixer FM IF system SA607



607 Silk Screen



607 TOP



607 BOTTOM

NOTE;
All views are TOP VIEW and
not actual size. For reference only.

Low-voltage high performance mixer FM IF system SA617

DESCRIPTION

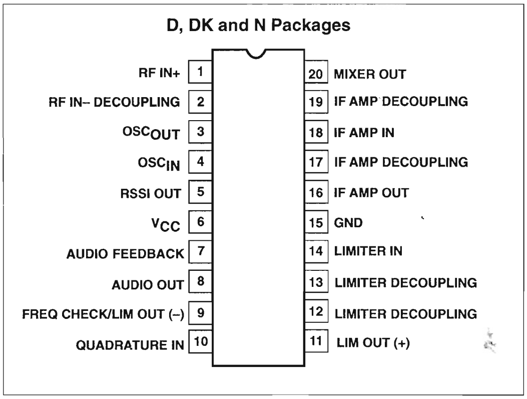
The SA617 is a low voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA617 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP package.

The SA617 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio output has an internal amplifier with the feedback pin accessible. The RSSI output is buffered. The SA617 also has an extra limiter output. This signal is buffered from the output of the limiter and can be used to perform frequency check. This is accomplished by comparing a reference frequency with the frequency check signal using a comparator to a varactor or PLL at the oscillator inputs.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz IF amp/limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 80dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA617 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Buffered frequency check output

PIN CONFIGURATION



- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

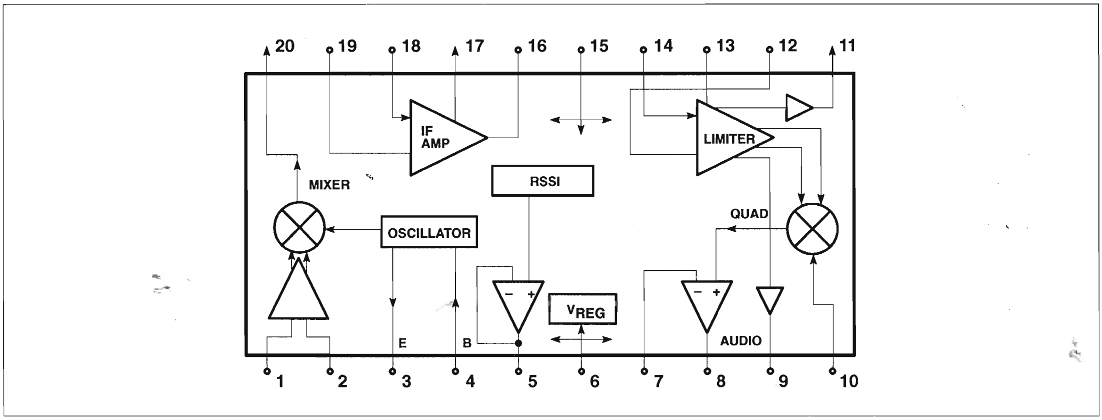
APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Narrow band cellular applications (NAMPS/NTACS)
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receivers
- Single conversion VHF receivers
- Wireless systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA617N	0408B
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA617D	0172D
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA617DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range SA617	–40 to +85	°C
θ_{JA}	Thermal impedance D package DK package N package	90 117 75	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA617			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	5.0	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4k; R18 = 3.3k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA617			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.8		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF Level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	11.0	17		dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17} = 2.4k	Test at Pin 18		–105		dBm
	AM rejection	80% AM 1kHz		40		dB
	Audio level	Gain of two (2kΩ AC load)	60	114		mV
	SINAD sensitivity	RF level –110dB		13		dB
THD	Total harmonic distortion		–30	–45		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	0.8	V
		IF level = –68dBm	.70	1.1	2.0	V
		IF level = –23dBm	1.0	1.8	2.5	V
	RSSI range			80		dB
	RSSI accuracy			±2.0		dB
	IF input impedance		1.3	1.5		kΩ
	IF output impedance			0.3		kΩ
	Limiter input impedance		1.30	1.5		kΩ
	Limiter output impedance	(Pin 11)		200		Ω
	Limiter output level	(Pin 11) No load 2.4kΩ load		130 115		mV$_{RMS}$
	Frequency Check/limiter output impedance	(Pin 9)		200		Ω
	Frequency Check/limiter output level	(Pin 9) No load 2.4kΩ load		130 115		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		240		mV$_{RMS}$
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:

1. The generator source impedance is 50Ω, but the SA617 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA617 input (Pin 18) which is about 21dB less than the “available power” at the generator.

CIRCUIT DESCRIPTION

The SA617 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of −9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

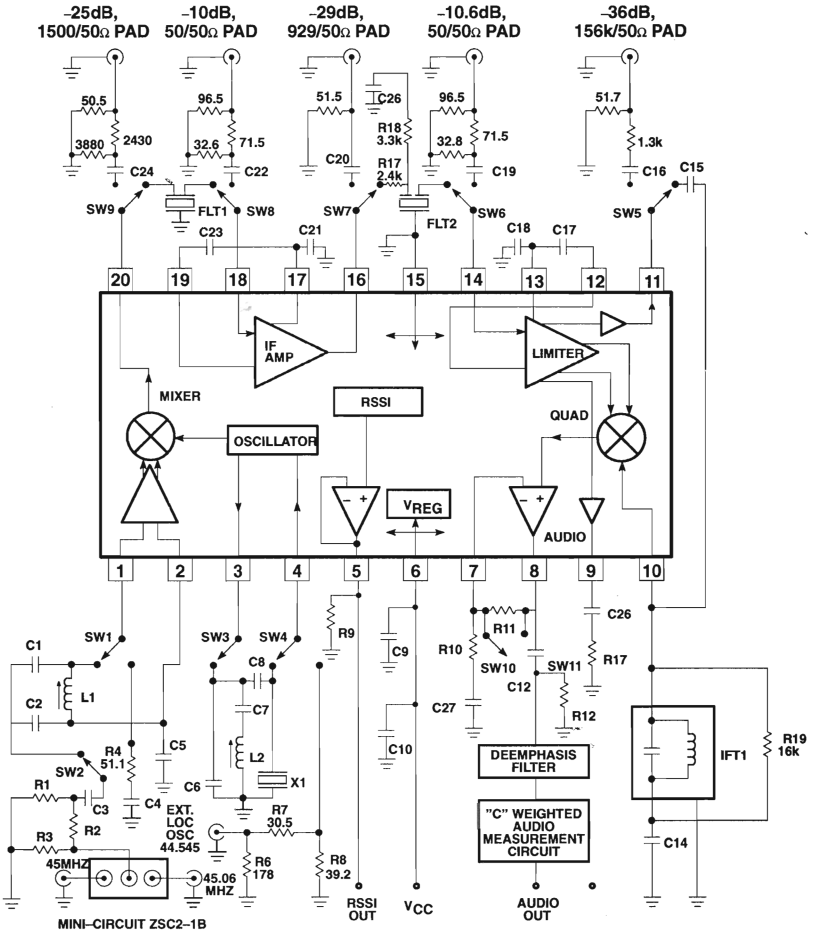
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 2kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal is buffered through an internal unity gain op amp. The frequency check pin provides a buffered limiter output. This is useful for implementing an AFC (Automatic Frequency Check) function. This same output can also be used in conjunction with limiter output (Pin 11) for demodulating FSK (Frequency Shift Keying) data. Both pins are of the same amplitude, but 180° out of phase.

NOTE: Limiter output or Frequency Check output has drive capability of a load minimum of 2kΩ or higher to obtain 115mV output level.

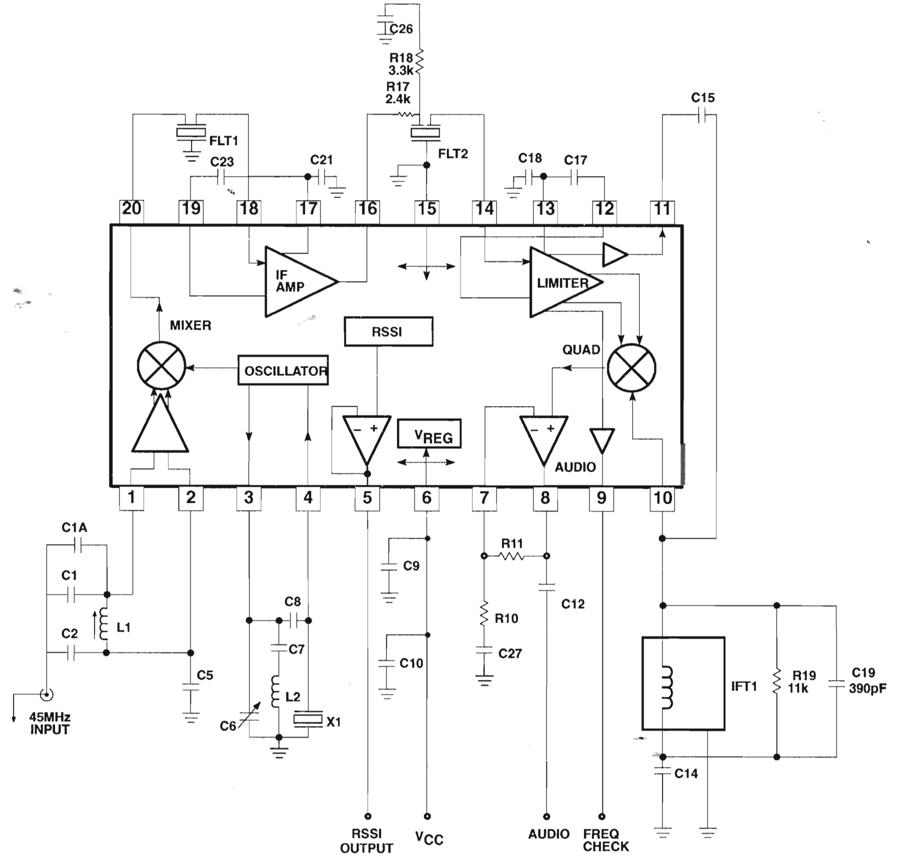
NOTE: dB(v) = 20log V_{OUT}/V_{IN}



Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15μF Tantalum (minimum)
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC-2A6597H
L1	147-160nH Coilcraft UNI-10/142-04J08S
L2	3.3μH nominal Toko 292CNS-T1046Z
X1	44.545MHz Crystal ICM4712701
R9	2kΩ ±1% 1/4W Metal Film
R10	8.2kΩ ±1%
R11	10kΩ ±1%
R12	2kΩ ±1%
R14	10kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

Figure 1. SA617 45MHz Test Circuit (Relays as shown)



SA617DK
Application Component List

C1A	18pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C1	33pF NPO Ceramic	C26	100nF ±10% Monolithic Ceramic
C2	220pF NPO Ceramic	C27	2.2µF Tantalum
C5	100nF ±10% Monolithic Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C6	30pF trim cap	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C7	1nF Ceramic	IFT 1	330µH TOKO 303LN-1130
C8	10.0pF NPO Ceramic	L1	.33µH TOKO SCB-1320Z
C9	100nF ±10% Monolithic Ceramic	L2	1.2µH
C10	15µF Tantalum (minimum)	X1	44.545MHz Crystal ICM4712701
C12	2.2µF ±10% Tantalum	R5	Not Used in Application Board (see Note 8, pg 8)
C14	100nF ±10% Monolithic Ceramic	R10	8.2k ±5% 1/4W Carbon Composition
C15	10pF NPO Ceramic	R11	10k ±5% 1/4W Carbon Composition
C17	100nF ±10% Monolithic Ceramic	R17	2.4k ±5% 1/4W Carbon Composition
C18	100nF ±10% Monolithic Ceramic	R18	3.3k ±5% 1/4W Carbon Composition
C19	390pF ±10% Monolithic Ceramic	R19	11k ±5% 1/4W Carbon Composition
C21	100nF ±10% Monolithic Ceramic		

Figure 2. SA617 45MHz Application Circuit

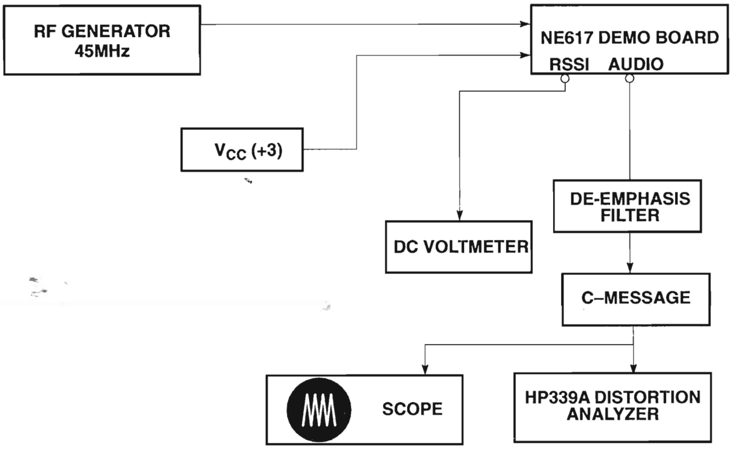


Figure 3. SA617 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35µV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

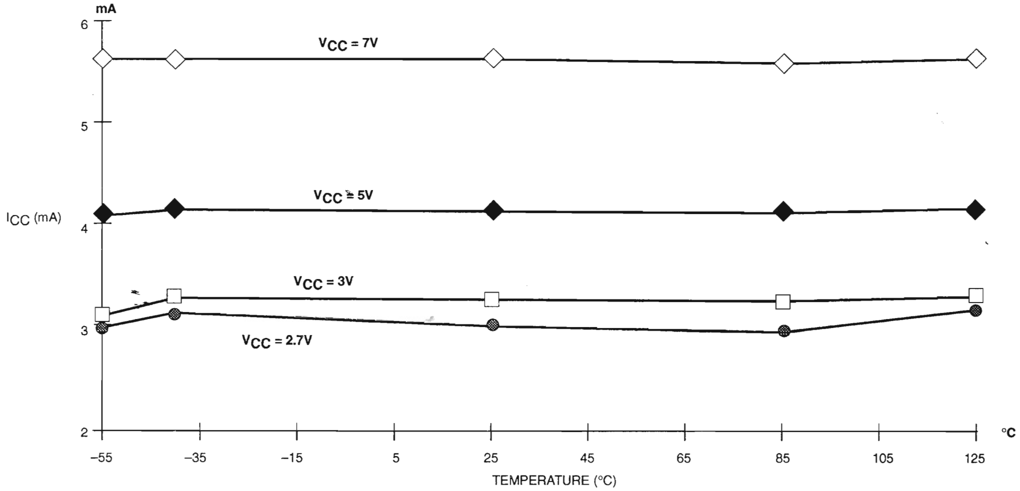


Figure 4. I_{CC} vs Temperature

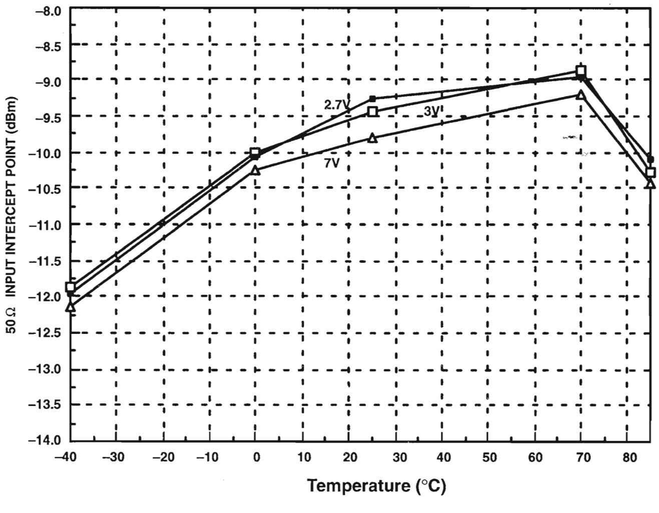


Figure 5. Third Order Intercept Point vs Supply Voltage

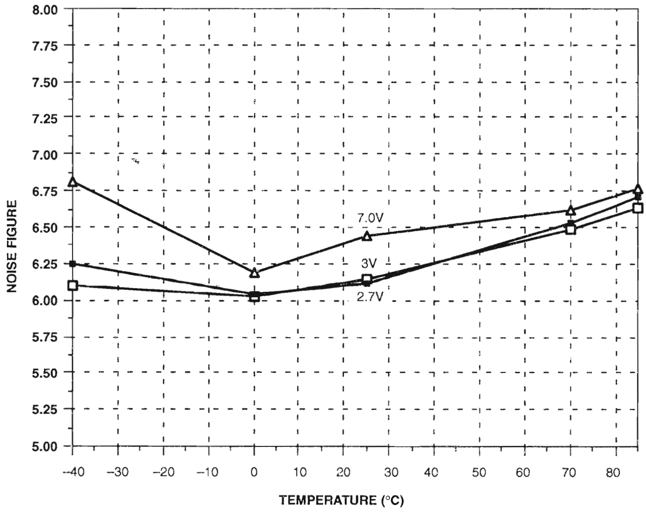


Figure 6. Mixer Noise Figure vs Supply Voltage

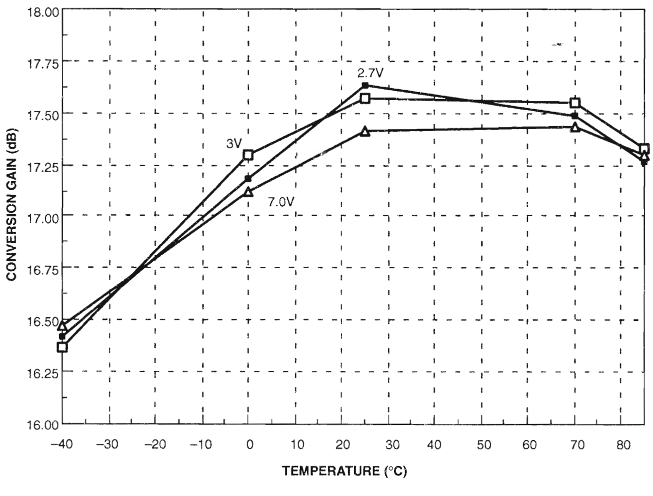


Figure 7. Conversion Gain vs Supply Voltage

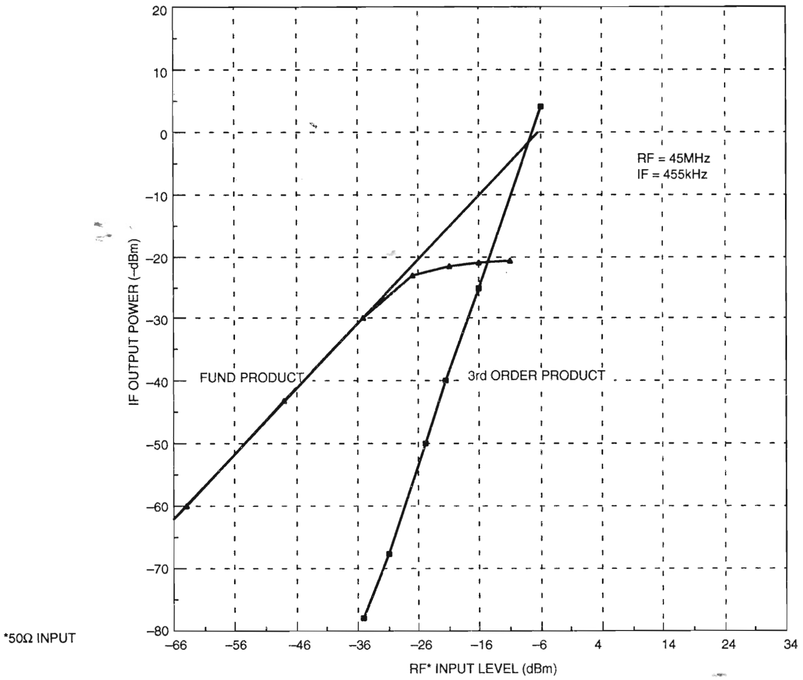


Figure 8. Mixer Third Order Intercept and Compression

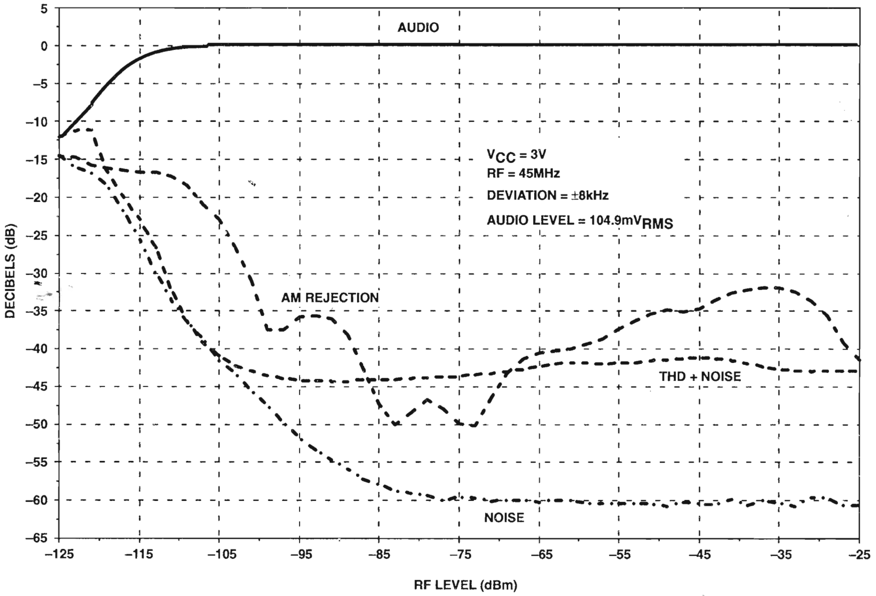


Figure 9. Sensitivity vs RF Level (–40°C)

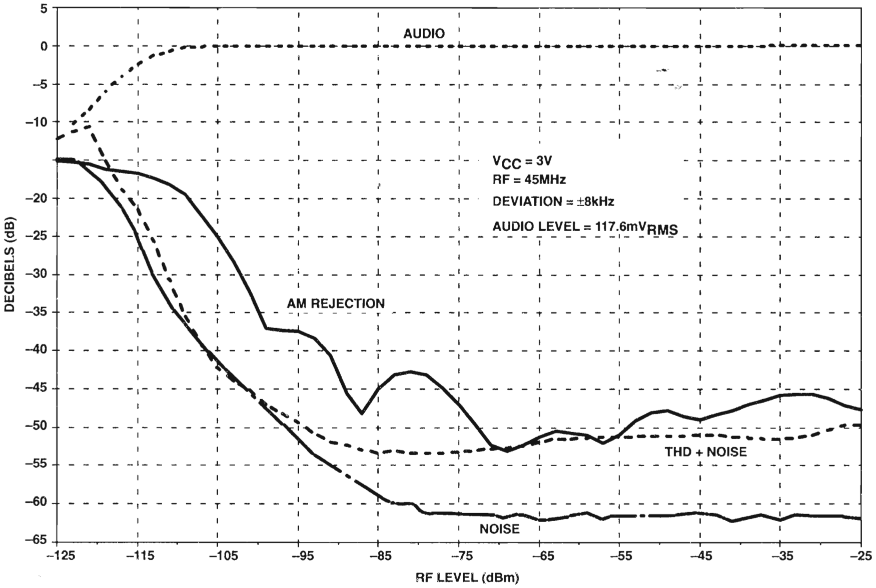


Figure 10. Sensitivity vs RF Level (+25°C)

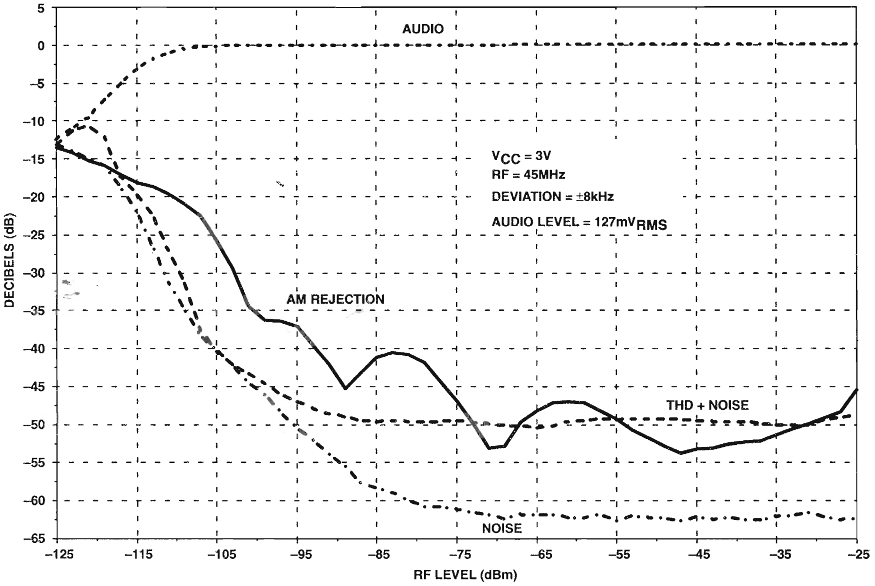


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

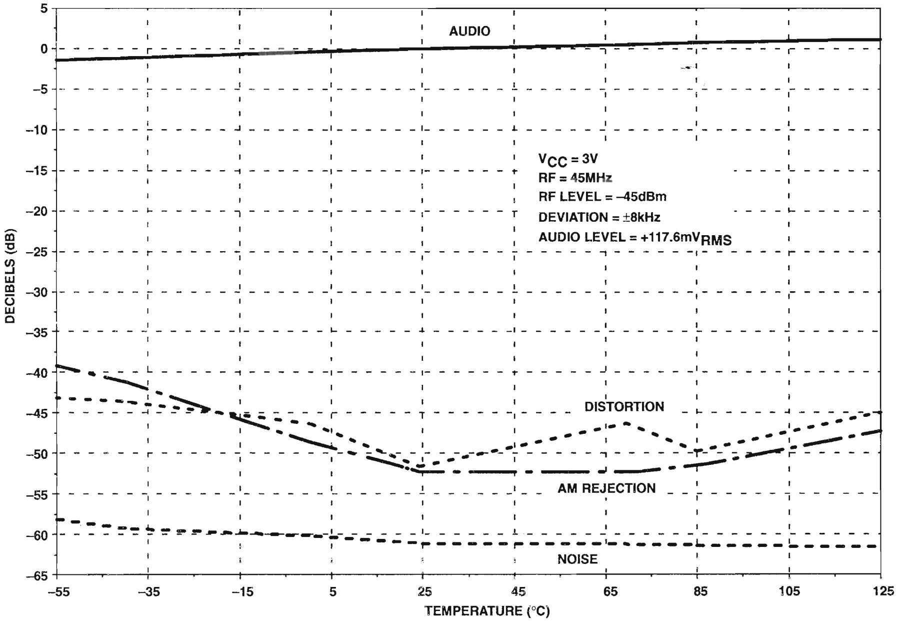


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

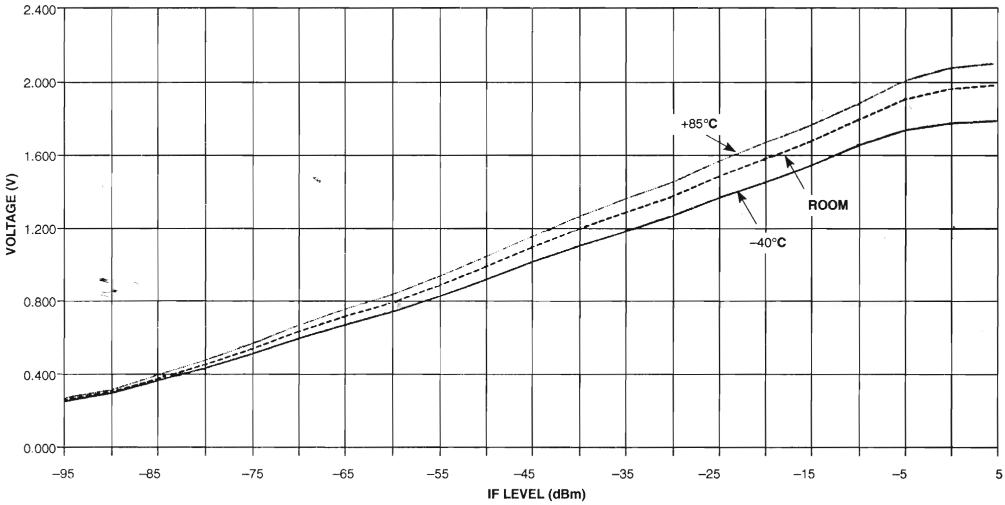


Figure 13. RSSI (455kHz IF @ 3V)

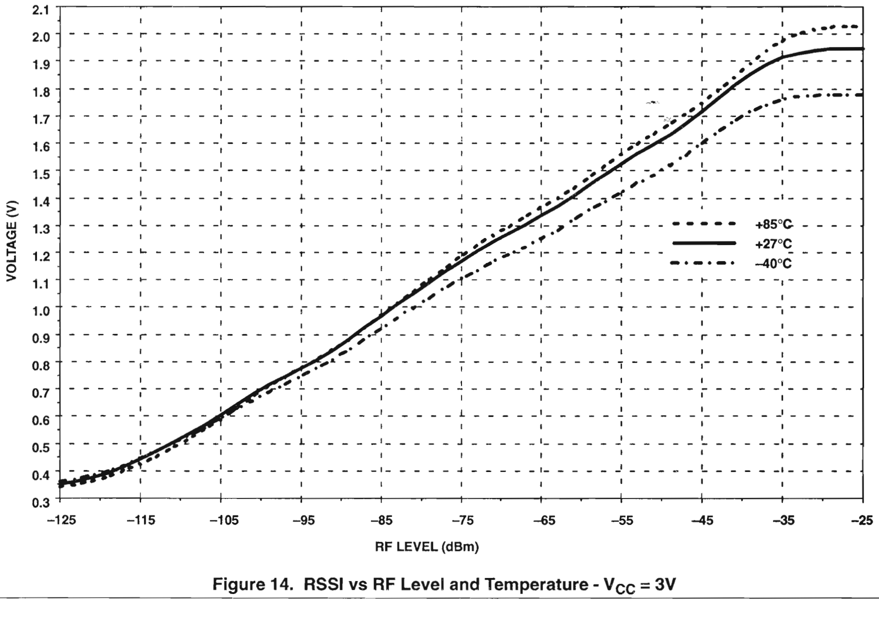


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

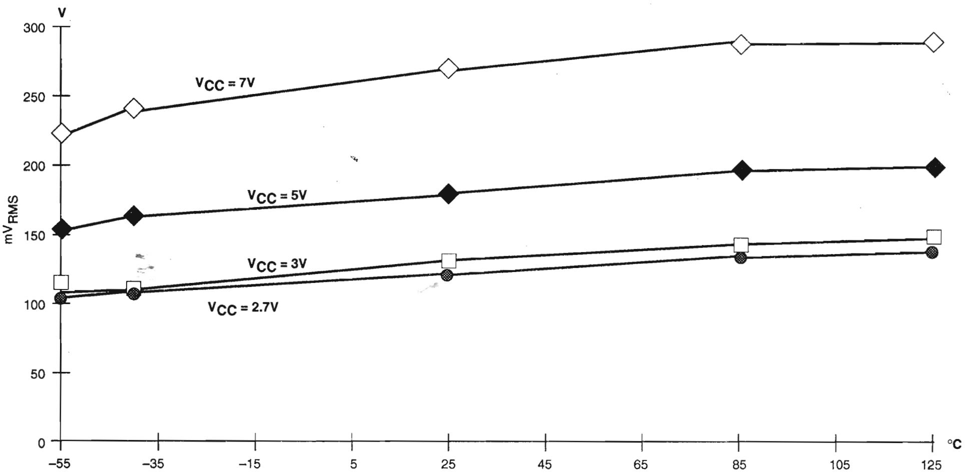


Figure 15. Audio Output vs Temperature

Low voltage high performance mixer FM IF system SA608

DESCRIPTION

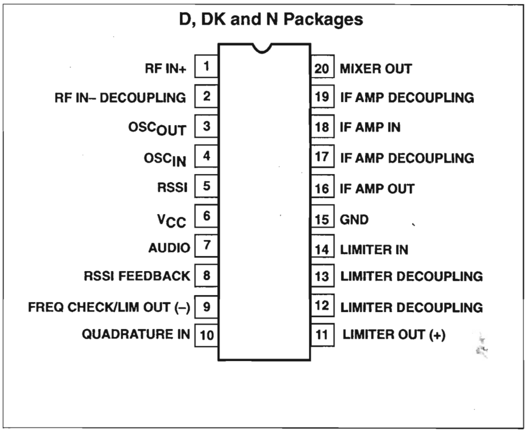
The SA608 is a low voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA608 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP package.

The SA608 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio output is buffered. The RSSI output has an internal amplifier with the feedback pin accessible. The SA608 also has an extra limiter output. This signal is buffered from the output of the limiter and can be used to perform frequency check. This is accomplished by comparing a reference frequency with the frequency check signal using a comparator to a varactor or PLL at the oscillator inputs.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA608 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Buffered frequency check output
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

PIN CONFIGURATION



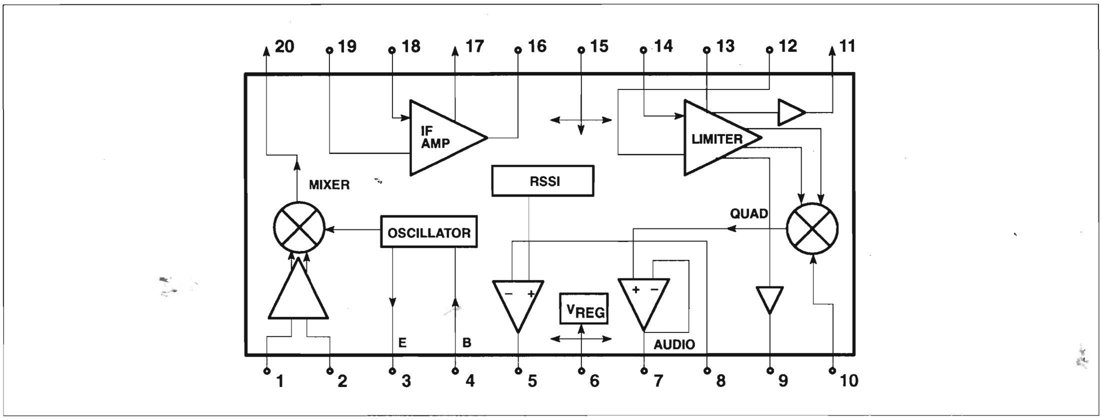
APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Narrow band cellular applications (NAMPS/NTACS)
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receivers
- Single conversion VHF receivers
- Wireless systems

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA608N	0408B
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA608D	0172D
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA608DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range SA608	–40 to +85	°C
θ_{JA}	Thermal impedance D package DK package N package	90 117 75	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA608 MIN	LIMITS SA608 TYP	LIMITS SA608 MAX	UNITS
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = +3V$, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4k; R18 = 3.3k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical charactерristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA608			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF Level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17} = 2.4k	Test at Pin 18		–109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level[2]		35	60	80	mV
	SINAD sensitivity	RF level –110dB		17		dB
THD	Total harmonic distortion		–35	–50		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	0.8	V
		IF level = –68dBm	.70	1.1	1.80	V
		IF level = –23dBm	1.2	1.8	2.5	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance		1.3	1.5		kΩ
	IF output impedance			0.3		kΩ
	Limiter input impedance		1.30	1.5		kΩ
	Limiter output impedance	(Pin 11)		200		Ω
	Limiter output level	(Pin 11) no load 5kΩ load		130 115		mV$_{RMS}$
	Frequency check/lim (–) output impedance	(Pin 9)		200		Ω
	Frequency check/lim (–) output level	(Pin 9) no load 5kΩ load		130 115		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		120		mV$_{RMS}$
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:

1. The generator source impedance is 50Ω, but the SA608 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA608 input (Pin 18) which is about 21dB less than the “available power” at the generator.
2. By using 45kΩ load across the Quad detector coil, you will have Audio output at 115mV with –42dB distortion.

CIRCUIT DESCRIPTION

The SA608 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

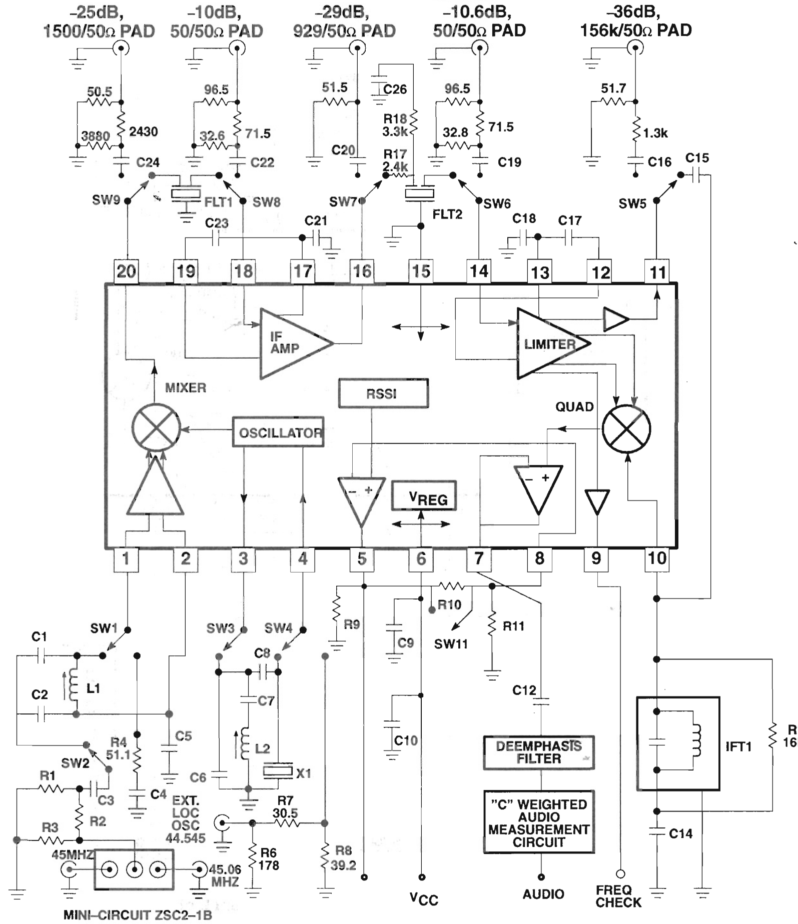
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp is configured as a unity gain buffer.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal is buffered through an internal unity gain op amp. The frequency check pin provides a buffered limiter output. This is useful for implementing an AFC (Automatic Frequency Check) function. This same output can also be used in conjunction with limiter output (Pin 11) for demodulating FSK (Frequency Shift Keying) data. Both pins are of the same amplitude, but 180° out of phase.

NOTE: Limiter or Frequency Check output has drive capability of a 5kΩ minimum or higher in order to obtain 120mV$_{RMS}$ output level.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

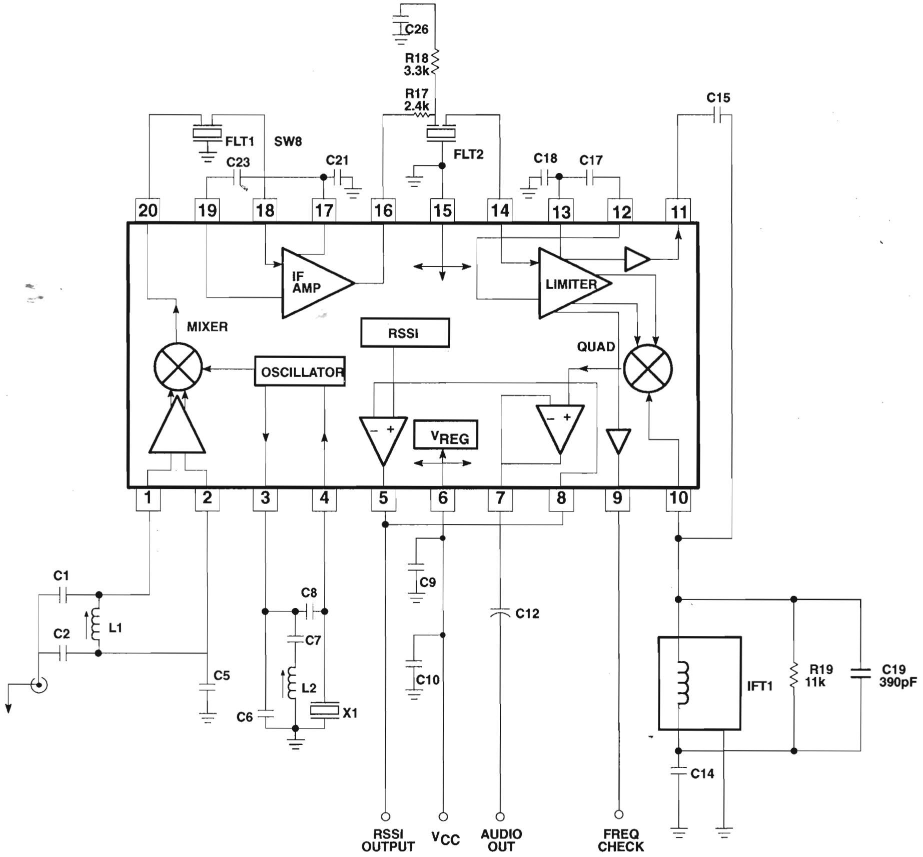


Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10µF Tantalum (minimum) *
C12	2.2µF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1µF ±10% Monolithic Ceramic
C27	2.2µF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8µH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	2kΩ ±1% 1/4W Metal Film
R10	10kΩ ±1%
R11	10kΩ ±1%
R14	5kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. SA607 45MHz Test Circuit (Relays as shown)



Product Board SA608D/DK Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	5-30pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330μH TOKO 303LN–1130
L1	0.33μH TOKO SCB–1320Z
L2	1.2μH Coilcraft 1008CS–122
X1	44.545MHz Crystal Hy-Q
R9	2kΩ ±1% 1/4W Metal Film
R10	8.2kΩ ±1%
R11	10kΩ ±1%
R14	10kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

Figure 2. SA608 45MHz Test Circuit (Relays as shown)

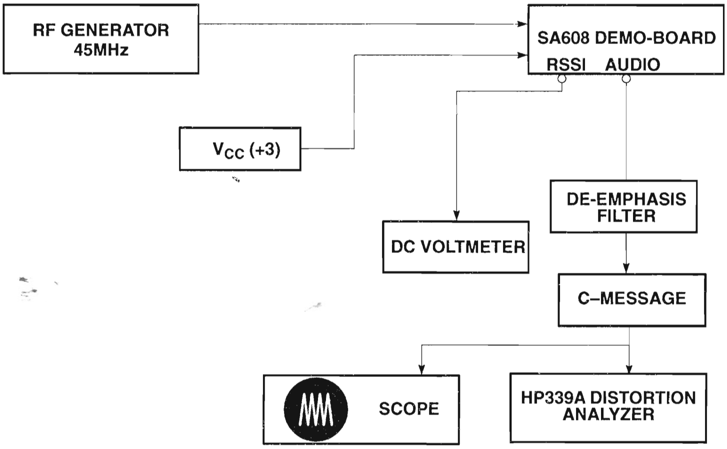


Figure 3. SA608 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35μV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

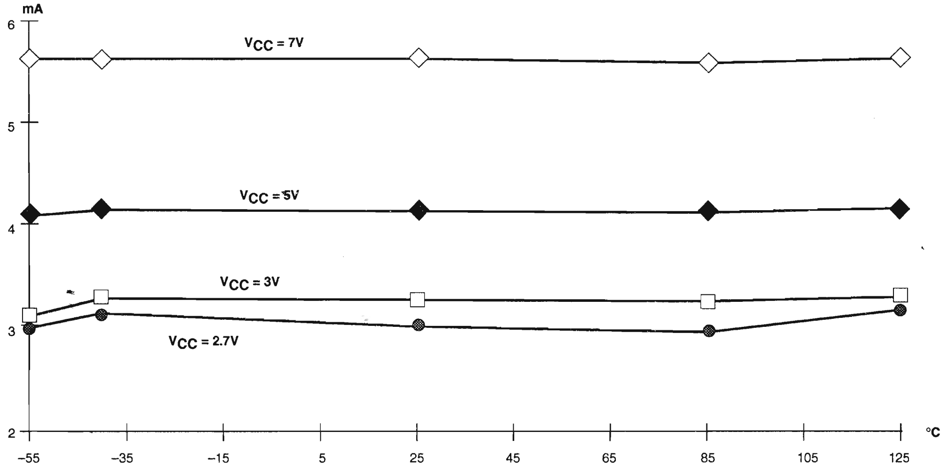


Figure 4. I_{CC} vs Temperature

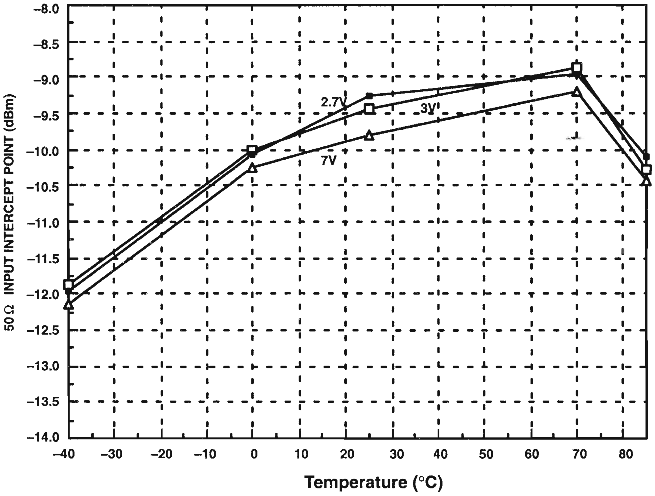


Figure 5. Third Order Intercept Point vs Supply Voltage

Low voltage high performance mixer FM IF system

SA608

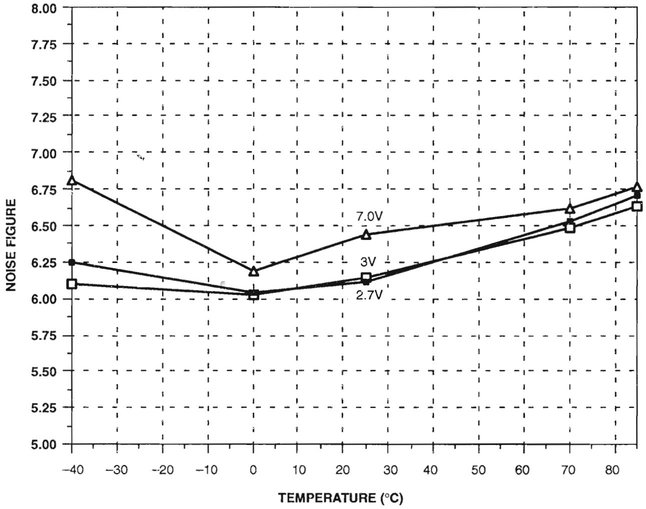


Figure 6. Mixer Noise Figure vs Supply Voltage

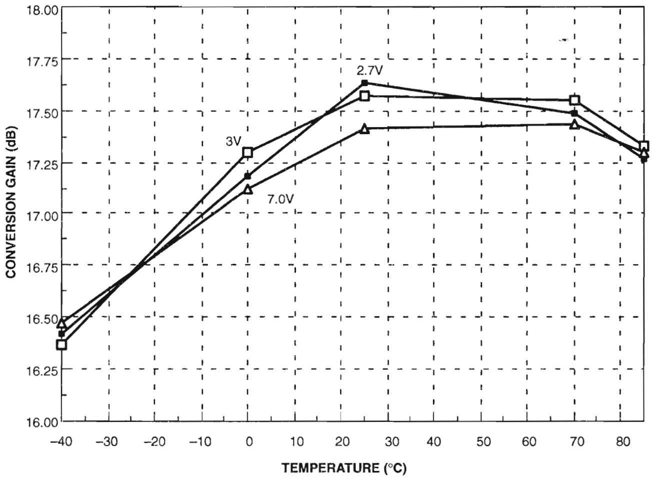


Figure 7. Conversion Gain vs Supply Voltage

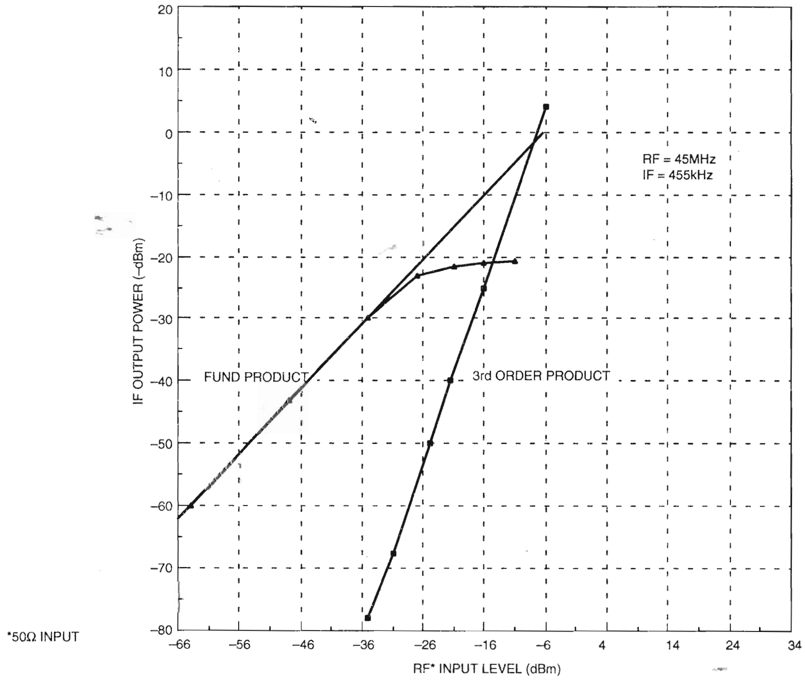


Figure 8. Mixer Third Order Intercept and Compression

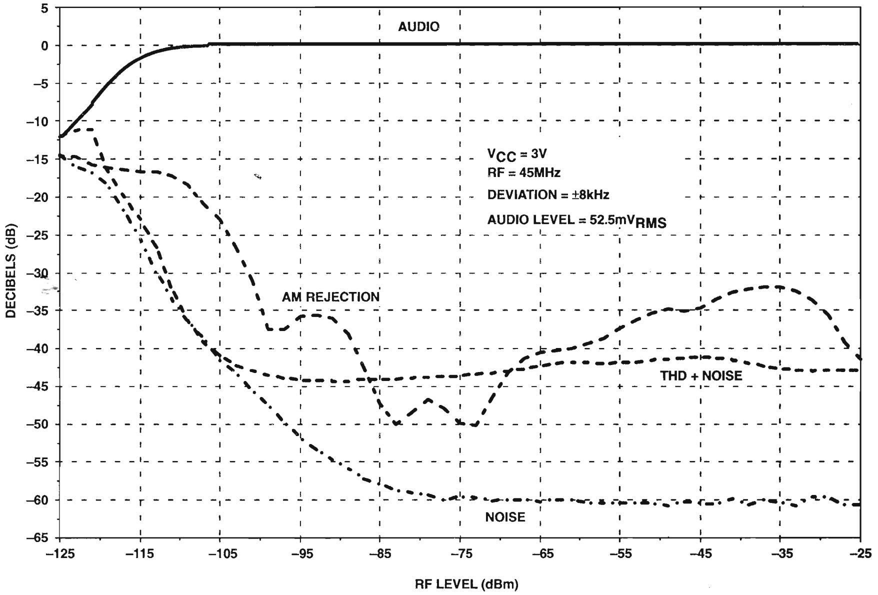


Figure 9. Sensitivity vs RF Level (–40°C)

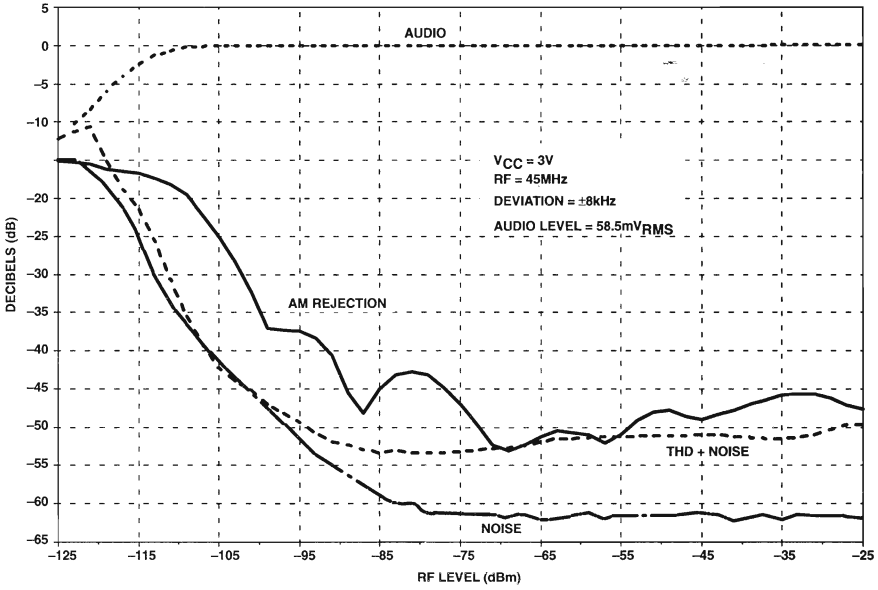


Figure 10. Sensitivity vs RF Level (+25°C)

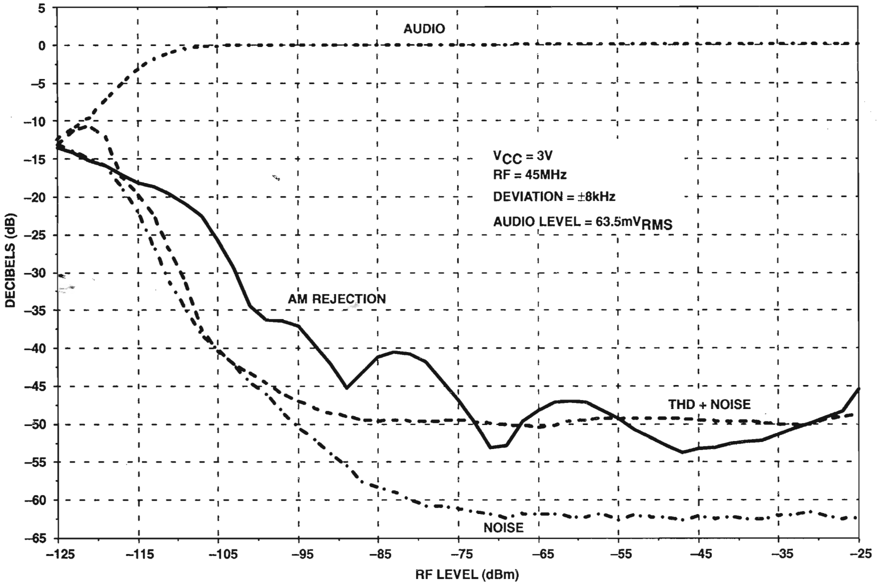


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

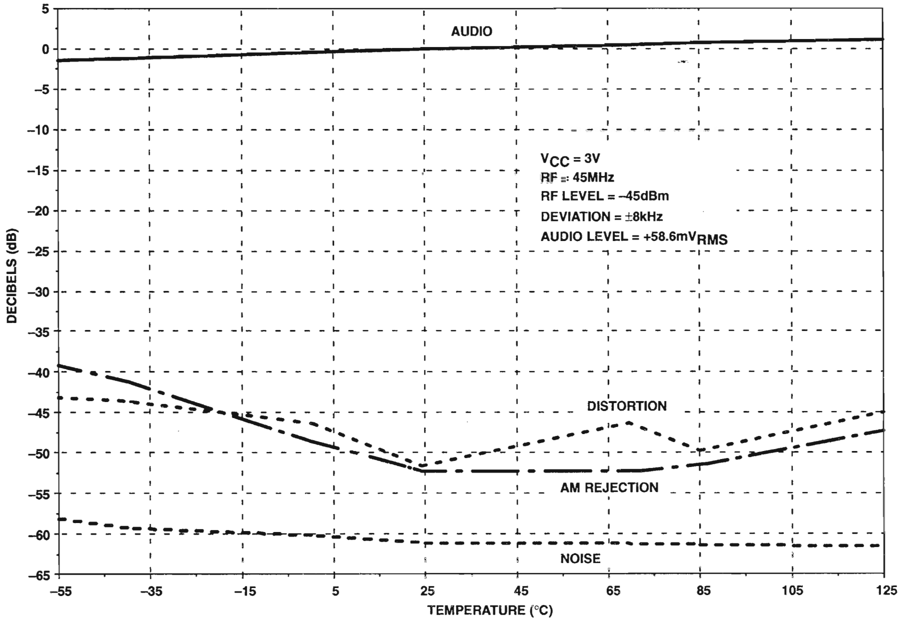


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

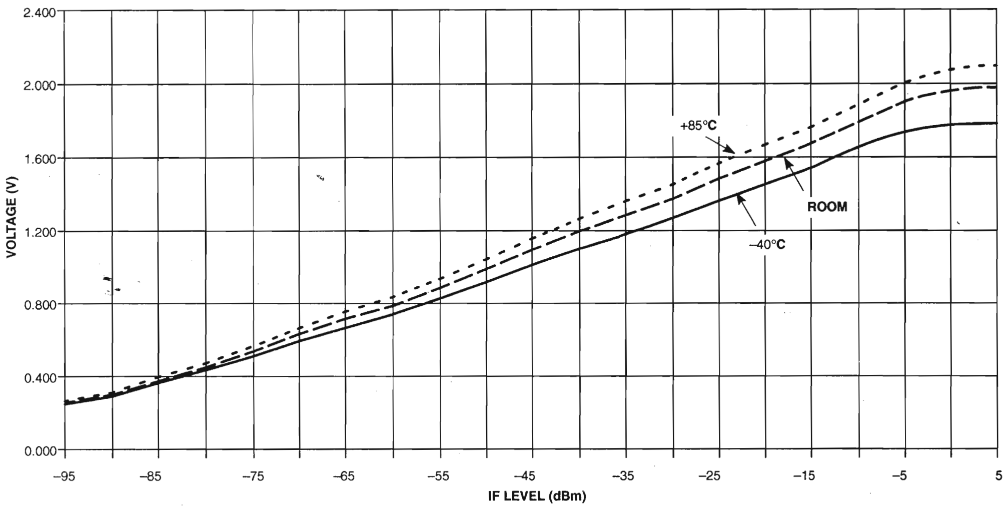


Figure 13. RSSI (455kHz IF @ 3V)

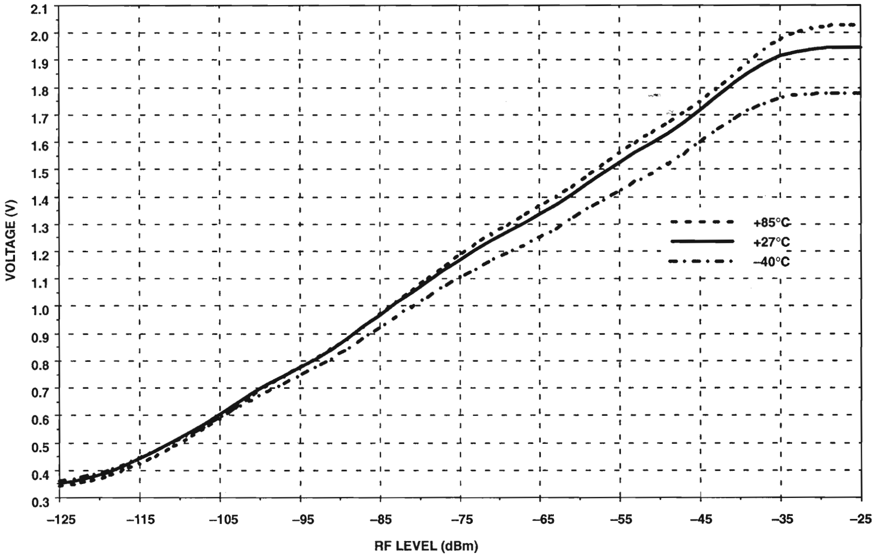


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

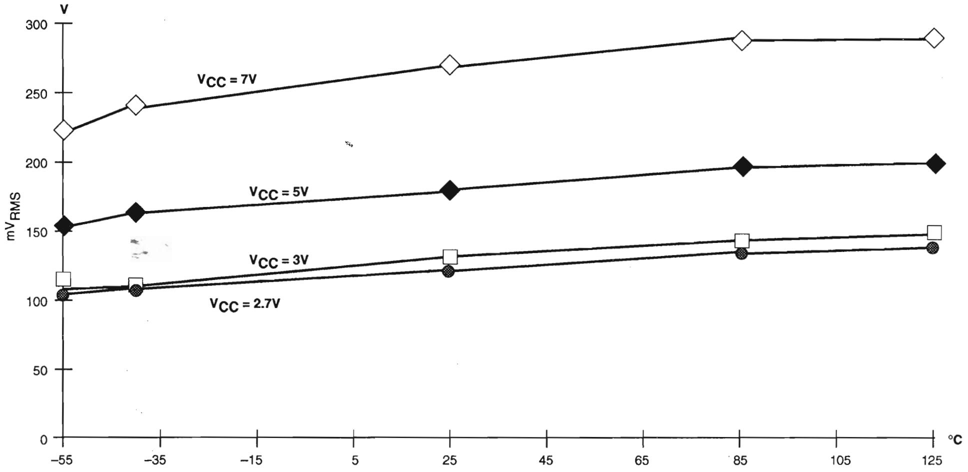


Figure 15. Audio Output vs Temperature

High performance low power FM IF system with high-speed RSSI

NE/SA624

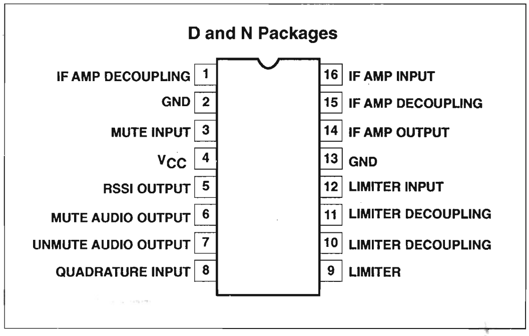
DESCRIPTION

The NE/SA624 is pin-to-pin compatible with the NE/SA604A, but has faster RSSI rise and fall time. The NE/SA624 is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA624 features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA624 is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature) package.

FEATURES

- Low power consumption: 3.4mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Fast RSSI rise and fall time
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA624 meets cellular radio specifications

PIN CONFIGURATION



APPLICATIONS

- Digital cellular base station
- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

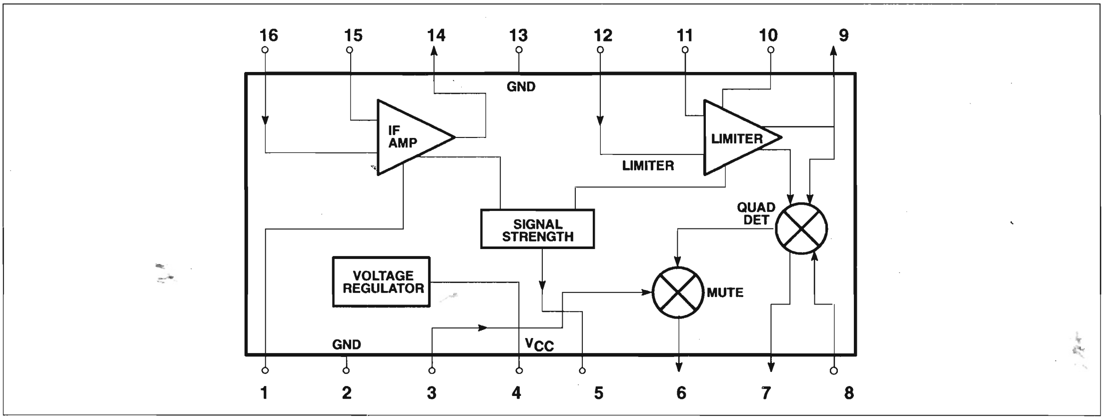
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE624N	0406C
16-Pin Plastic Small Outline (SO) package (Surface-mount)	0 to +70°C	NE624D	0005D
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA624N	0406C
16-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA624D	0005D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE624 SA624	0 to +70 -40 to +85	°C °C
θ_{JA}	Thermal impedance D package N package	90 75	°C/W °C/W

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE624			SA624			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		2.5	3.4	4.2	2.5	3.4	4.2	mA
	Mute switch input threshold (ON) (OFF)		1.7		1.0	1.7		1.0	V V

AC ELECTRICAL CHARACTERISTICS

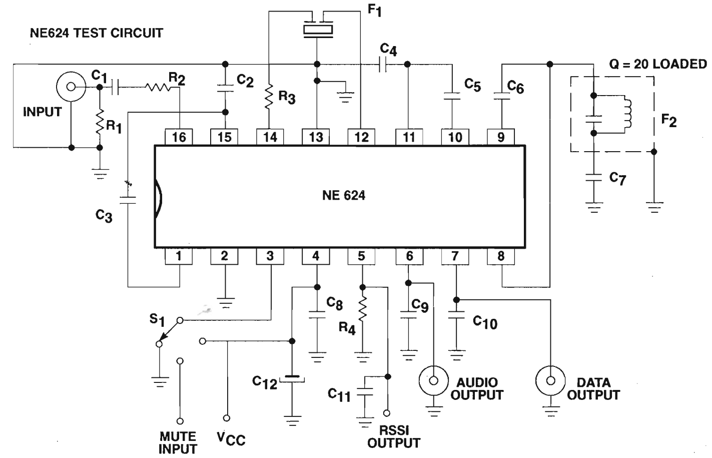
Typical reading at $T_A = 25°C$; $V_{CC} = +6V$, unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE624			SA624			
			MIN	TYP	MAX	MIN	TYP	MAX	
	Input limiting -3dB	Test at Pin 16		-92			-92		dBm/50Ω
	AM rejection	80% AM 1kHz	30	34		30	34		dB
	Recovered audio level	15nF de-emphasis	110	175	250	80	175	260	mV$_{RMS}$
	Recovered audio level	150pF de-emphasis		530			530		mV$_{RMS}$
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	RSSI output[1]	RF level = -118dBm	0	160	550	0	160	650	mV
		RF level = -68dBm	2.0	2.65	3.0	1.9	2.65	3.1	V
		RF level = -18dBm	4.1	4.85	5.5	4.0	4.85	5.6	V
	RSSI output rise time (10kHz pulse, no IF filter)	IF freq. = 455kHz							
		IF level = -44dBm		1.1			1.1		µs
		IF level = -16dBm		1.2			1.2		µs
		IF freq. = 10.7MHz							
		IF level = -44dBm		1.2			1.2		µs
		IF level = -16dBm		1.1			1.1		µs
	RSSI output fall time (10kHz pulse, no IF filter)	IF freq. = 455kHz							
		IF level = -44dBm		1.3			1.3		µs
		IF level = -16dBm		4.7			4.7		µs
		IF freq. = 10.7MHz							
		IF level = -44dBm		1.6			1.6		µs
		IF level = -16dBm		4.2			4.2		µs
	RSSI range	R_4 = 100k (Pin 5)		90			90		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±1.5			±1.5		dB
	IF input impedance		1.4	1.6		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		1.4	1.6		kΩ
	Limiter output impedance			300			300		Ω
	Limiter output level no load			280			280		mV$_{RMS}$
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ

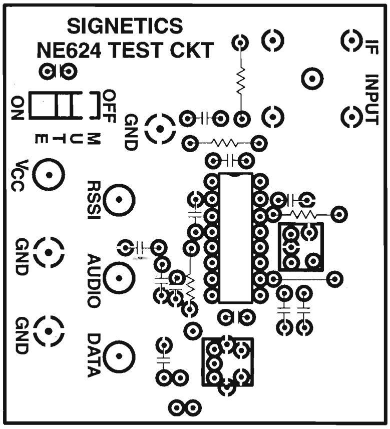
NOTE:

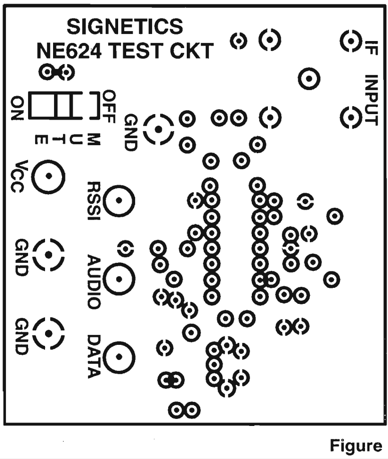
1. NE604 data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

NE604 (50)	NE624 (1.5k)/NE605 (1.5k
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm



C1	100nF + 80 – 20% 63V K10000–25V Ceramic
C2	100nF +10% 50V
C3	100nF ±10% 50V
C4	100nF +10% 50V
C5	100nF ±10% 50V
C6	10pF ±2% 100V NPO Ceramic
C7	100nF ±10% 50V
C8	100nF ±10% 50V
C9	15nF ±10% 50V
C10	150pF ±2% 100V N1500 Ceramic
C11	1nF ±10% 100V K2000-Y5P Ceramic
C12	6.8μF ±20% 25V Tantalum
F1	455kHz Ceramic Filter Murata SFG455A3
F2	455kHz (Ce = 180pF) TOKO RMC 2A6597H
R1	51Ω ±1% 1/4W Metal Film
R2	1500Ω ±1% 1/4W Metal Film
R3	1500Ω ±5% 1/8W Carbon Composition
R4	100kΩ ±1% 1/4W Metal Film





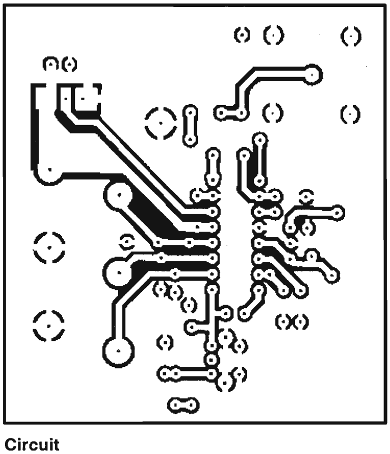


Figure 1. NE/SA624 Test Circuit

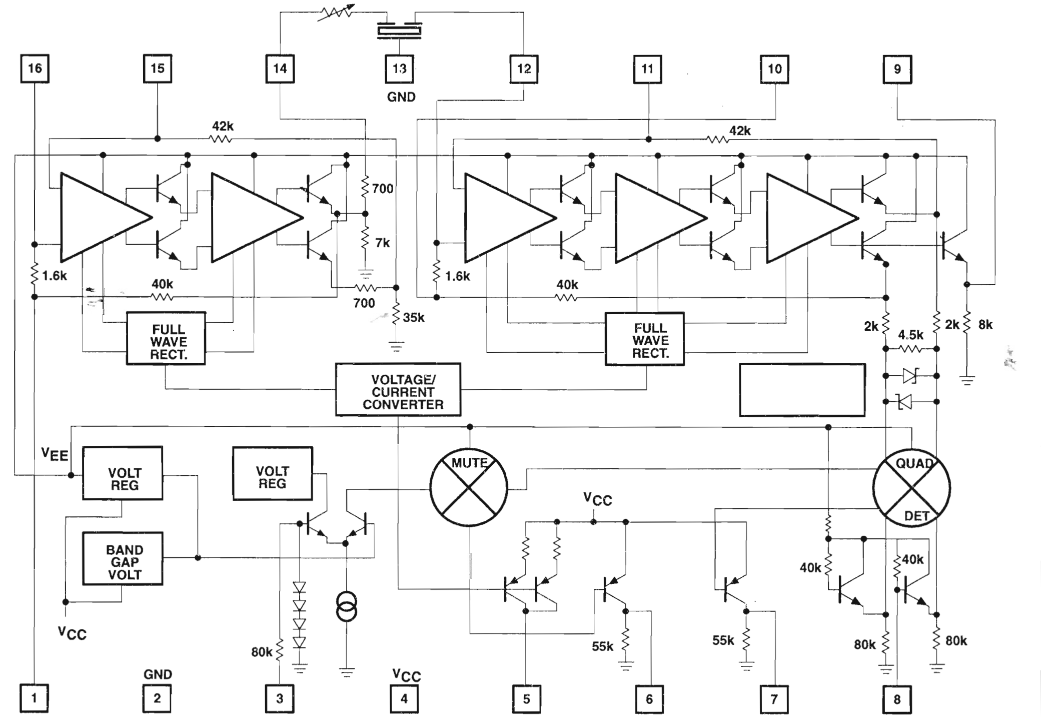


Figure 2. Equivalent Circuit

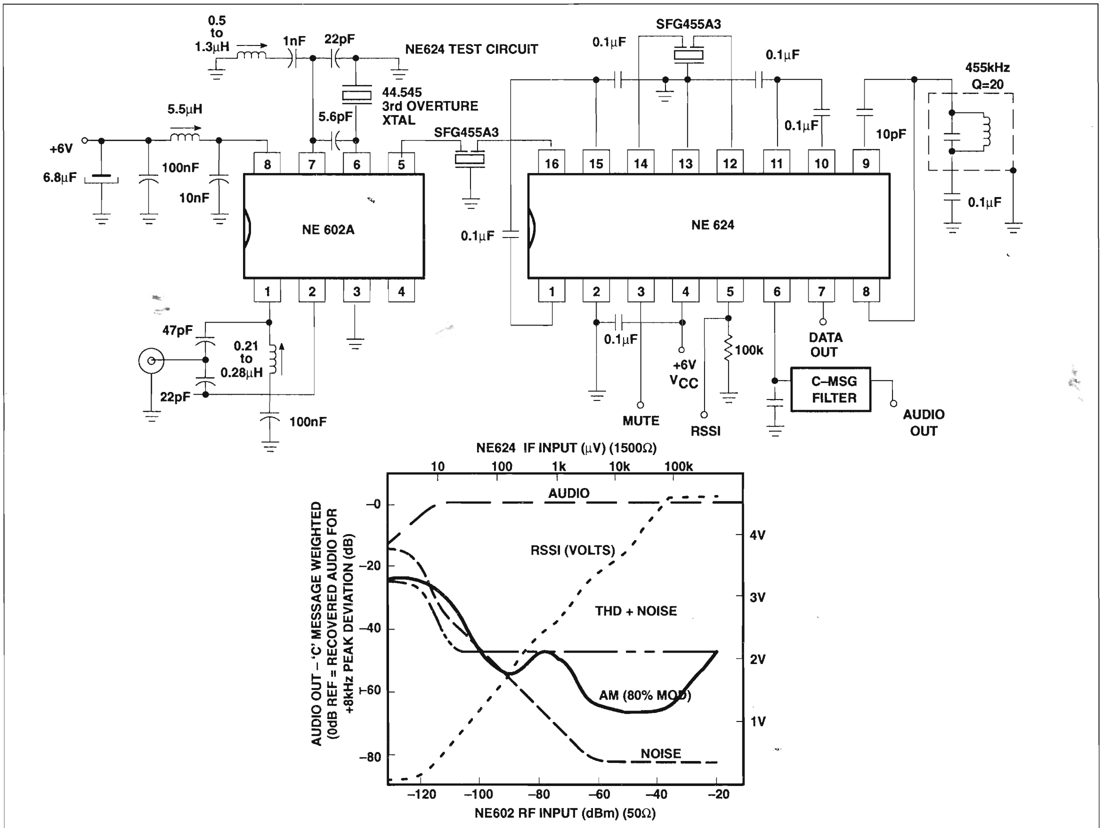


Figure 3. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The NE/SA624 is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA624 cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 1. This configuration can be used as the basis for production layout.

The NE/SA624 is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with output characteristic). The sub-systems are shown in Figure 2. A typical application with 45MHz input and 455kHz IF is shown in Figure 3.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 2, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

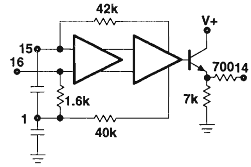


Figure 4. First Limiter Bias

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 6. Distributed feedback (capacitance, inductance and radiated fields)

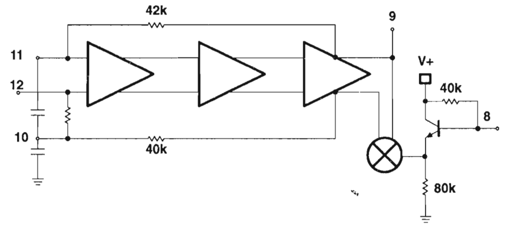


Figure 5. Second Limiter and Quadrature Detector

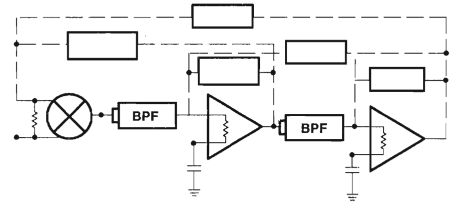
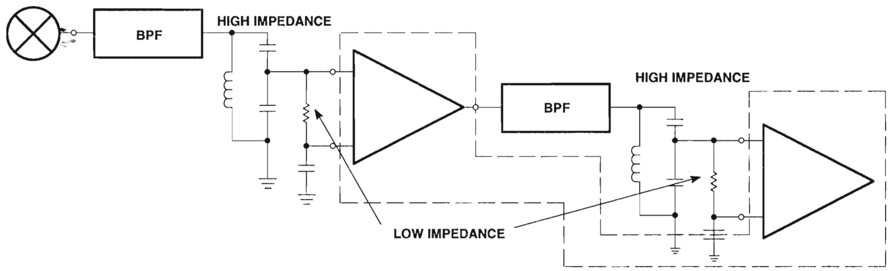
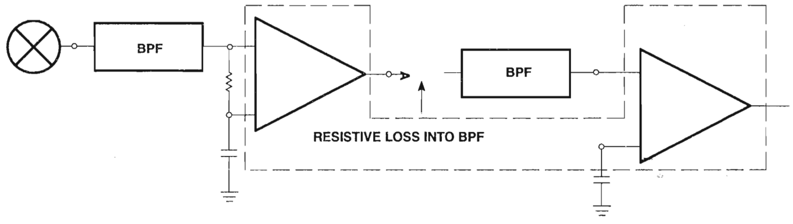


Figure 6. Feedback Paths



a. Terminating High Impedance Filters with Transformation to Low Impedance



b. Low Impedance Termination and Gain Reduction

Figure 7. Practical Termination

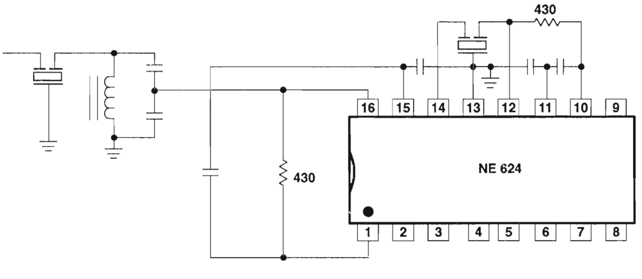


Figure 8. Crystal Input Filter with Ceramic Interstage Filter

forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a “normal” manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in Figure 7. Reduced gain will result in reduced limiting sensitivity.

A feature of the NE624 IF amplifiers, which is not specified, is low phase shift. The NE624 is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes. Additional information will be provided in the upcoming product specification (this is a preliminary specification) when characterization is complete.

Stability Considerations

The high gain and bandwidth of the NE624 in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 1, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1μF monolithic right at the V_{CC} pin, and a 6.8μF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1μF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 1 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 7 demonstrates a practical means.

As illustrated in Figure 8, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 5 shows an equivalent circuit of the NE624 quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 10. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

Frequency Discriminator Design Equations for NE624

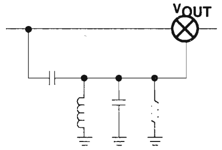


Figure 9.

$$V_O = \frac{C_S}{C_P + C_S} \bullet \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \bullet V_{IN} \qquad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \qquad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \qquad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = t_g^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1 - \left(\frac{\omega_1}{\omega}\right)^2}\right] \qquad (2)$$

Figure 10 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$ with respect to the V_{IN}.

If $V_{IN} = A \text{ Sin } \omega t \Rightarrow V_O = A$ (3)

$$\text{Sin}\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$V_{IN} \bullet V_O = A^2 \text{ Sin } \omega t$ (4)

$$\text{Sin}\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2}\,A^2\,\text{Cos}\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (5)$$

$$= \frac{1}{2}\,A^2\,\text{Sin}\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1\,\frac{\omega_1}{\omega} = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \quad (6)$$

$$\text{For } \frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5\text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 10) and draw a vertical straight line at

$$\frac{\omega}{\omega_1} = 1.01.$$

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) ⇒ Choose a Q = 20

The internal R of the 624 is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S$ = 174pF and L = 0.7mH.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a C_S = 10pF and C_P = 164pF (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of C_S = 1pF is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Singe the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE624 demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 3) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25µV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22µV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a

91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE624 are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

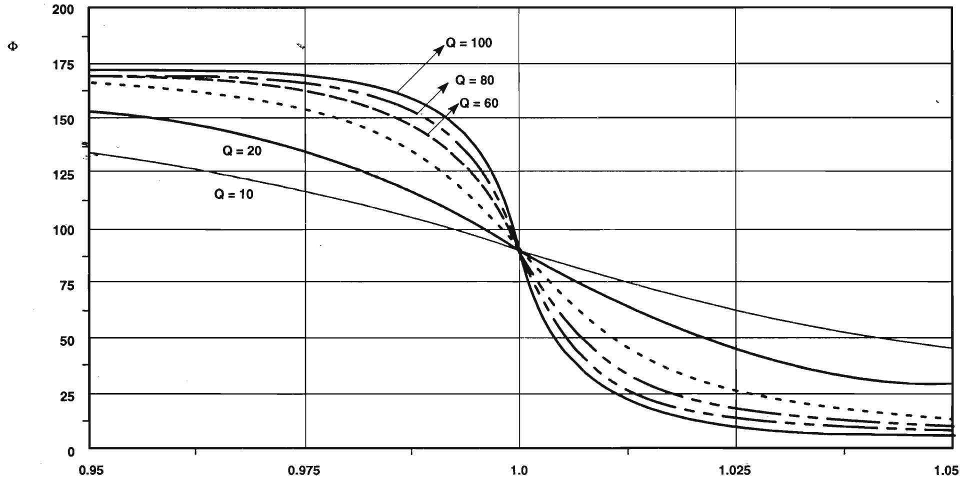


Figure 10. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

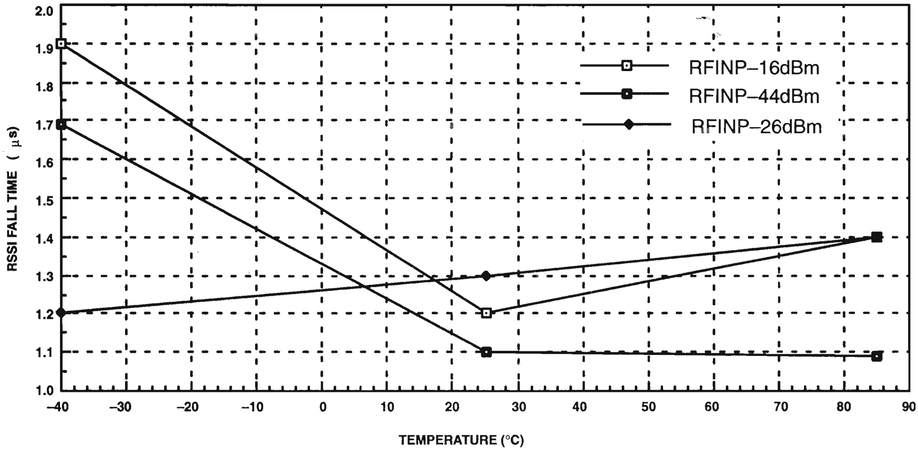


Figure 11. NE/SA624 Rise Time 455kHz IF Frequency

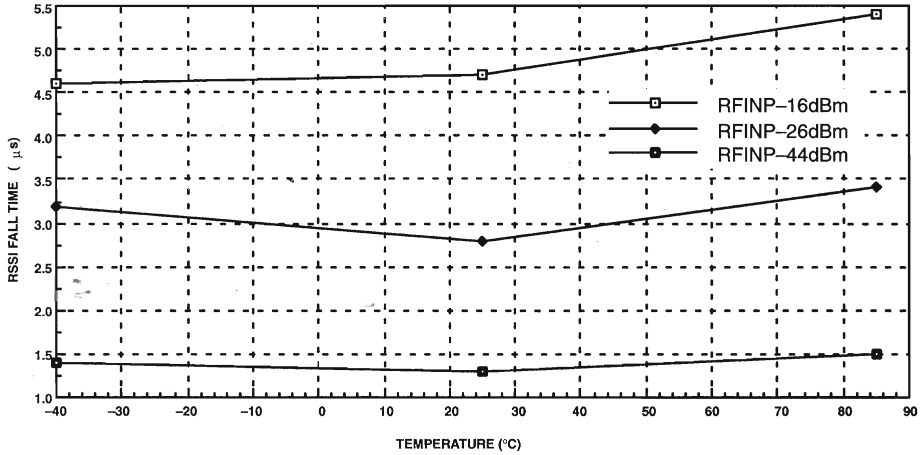


Figure 12. NE/SA624 Fall Time 455kHz IF Frequency

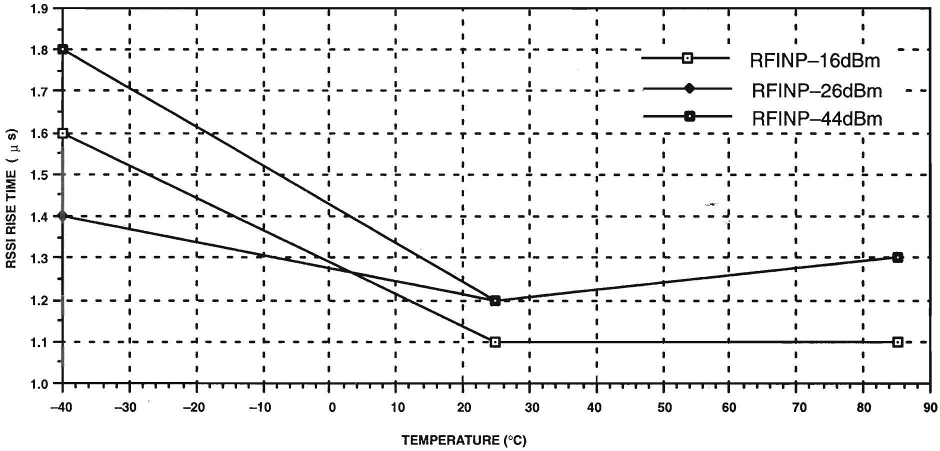


Figure 13. NE/SA624 Rise Time 10.7MHz IF Frequency

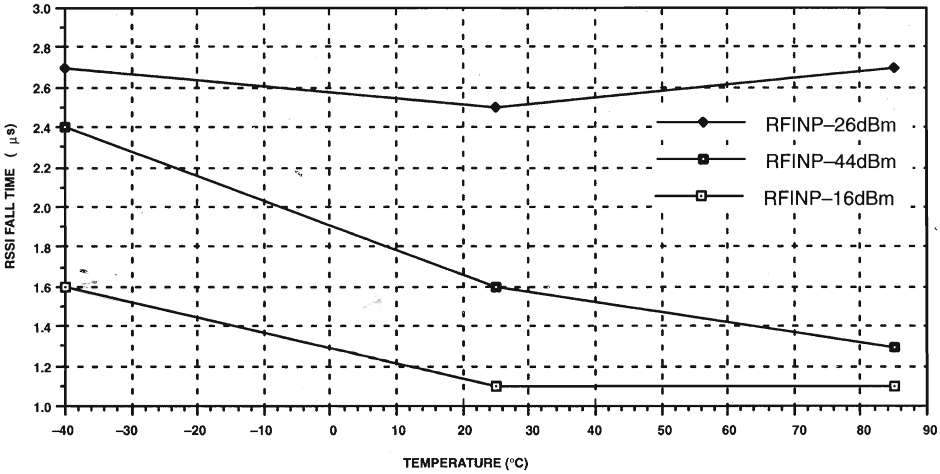


Figure 14. NE/SA624 Fall Time 10.7MHz IF Frequency

High performance low power mixer FM IF system with high-speed RSSI

NE/SA625

DESCRIPTION

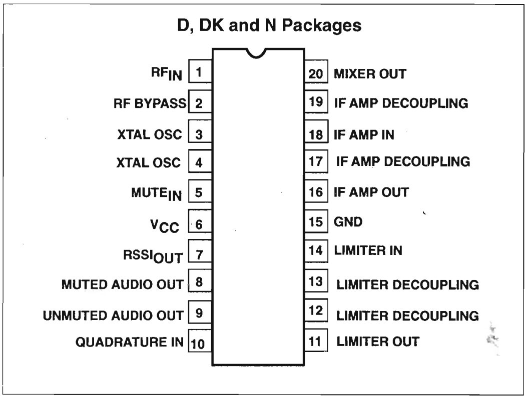
The NE/SA625 is pin-to-pin compatible with the NE/SA605, but has faster RSSI rise and fall times. The NE/SA625 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI) with fast rise and fall time, and voltage regulator. The NE/SA625 combines the functions of Signetics' NE602A and NE624. The NE/SA625 is available in 20-lead dual-in-line plastic and 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

For additional technical information please refer to application notes AN1994, 1995 and 1996, which include example application diagrams, a complete overview of the product and artwork for reference.

FEATURES

- Fast RSSI rise and fall times
- Low power consumption: 5.8mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22µV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA625 meets cellular radio specifications

PIN CONFIGURATION



- ESD hardened

APPLICATIONS

- Digital cellular base stations
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification
- Digital cordless telephones

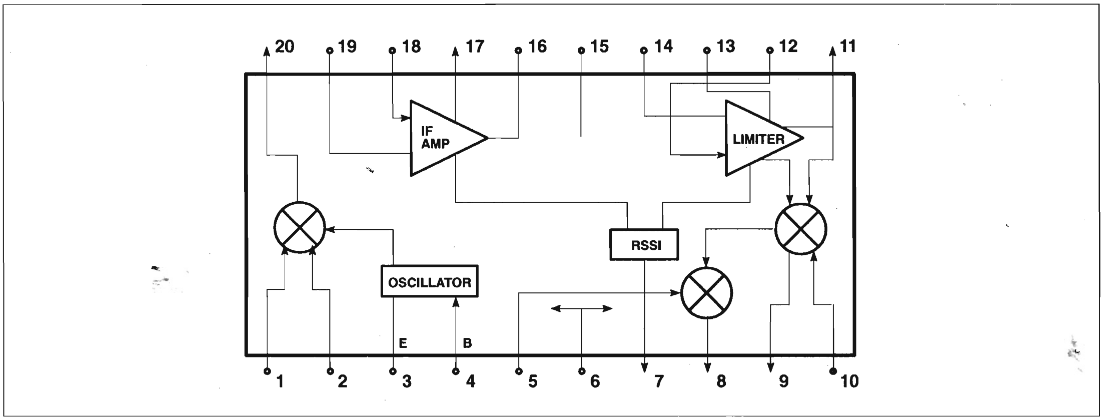
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE625N	0408B
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	0 to +70°C	NE625D	0172D
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	0 to +70°C	NE625DK	1563
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA625N	0408B
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA625D	0172D
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA625DK	1563

High performance low power mixer FM IF system with high-speed RSSI

NE/SA625

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		9	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range	NE625	0 to +70	°C
		SA625	-40 to +85	°C
θ_{JA}	Thermal impedance	D package	90	°C/W
		N package	75	°C/W
		DK package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE625			SA625			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		5.1	5.8	6.7	4.55	5.8	6.75	mA
	Mute switch input threshold (ON)		1.7			1.7			V
	(OFF)				1.0			1.0	V

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = +6V$, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE625			SA625			
			MIN	TYP	MAX	MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)									
f_{IN}	Input signal frequency			500			500		MHz
f_{OSC}	Crystal oscillator frequency			150			150		MHz
	Noise figure at 45MHz			5.0			5.0		dB
	Third-order input intercept point	f1 = 45.0; f2 = 45.06MHz		-10			-10		dBm
	Conversion power gain	Matched 14.5dBV step-up	10.5	13	14.5	10	13	15	dB
		50Ω source		-1.7			-1.7		dB
	RF input resistance	Single-ended input	3.5	4.7		3.0	4.7		kΩ
	RF input capacitance			3.5	4.0		3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.3	1.5		1.25	1.5		kΩ
IF section									
	IF amp gain	50Ω source		39.7			39.7		dB
	Limiter gain	50Ω source		62.5			62.5		dB
	Input limiting -3dB, $R_{17} = 5.1k$	Test at Pin 18		-113			-113		dBm
	AM rejection	80% AM 1kHz	30	34	42	29	34	43	dB
	Audio level, $R_{10} = 100k$	15nF de-emphasis	110	150	250	80	150	260	mV$_{RMS}$
	Unmuted audio level, $R_{11} = 100k$	150pF de-emphasis		480			480		mV
	SINAD sensitivity	RF level -118dB		16			16		dB
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	IF RSSI output, $R_9 = 100kΩ^1$	IF level = -118dBm	0	160	550	0	160	650	mV
		IF level = -68dBm	2.0	2.5	3.0	1.9	2.5	3.1	V
		IF level = -18dBm	4.1	4.8	5.5	4.0	4.8	5.6	V
	IF RSSI output rise time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz							
		RF level = -56dBm		1.2			1.2		μs
		RF level = -28dBm		1.2			1.2		μs
		IF frequency = 10.7MHz							
		RF level = -56dBm		1.2			1.2		μs
		RF level = -28dBm		1.1			1.1		μs
	IF RSSI output fall time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz							
		RF level = -56dBm		2.1			2.1		μs
		RF level = -28dBm		7.6			7.6		μs
		IF frequency = 10.7MHz							
		RF level = -56dBm		2.0			2.0		μs
		RF level = -28dBm		7.3			7.3		μs
	RSSI range	$R_9 = 100kΩ$ Pin 16		90			90		dB
	RSSI accuracy	$R_9 = 100kΩ$ Pin 16		±1.5			±1.5		dB
	IF input impedance		1.40	1.6		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter intput impedance		1.40	1.6		1.40	1.6		kΩ
	Limiter output impedance			300			300		Ω
	Limiter output level with no load			280			280		mV$_{RMS}$

AC ELECTRICAL CHARACTERISTICS(Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE625			SA625			
			MIN	TYP	MAX	MIN	TYP	MAX	
IF section (continued)									
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ
RF/IF section (int LO)									
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450			450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3			4.3		V

NOTE:

1. The generator source impedance is 50Ω, but the NE/SA625 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA625 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA625 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

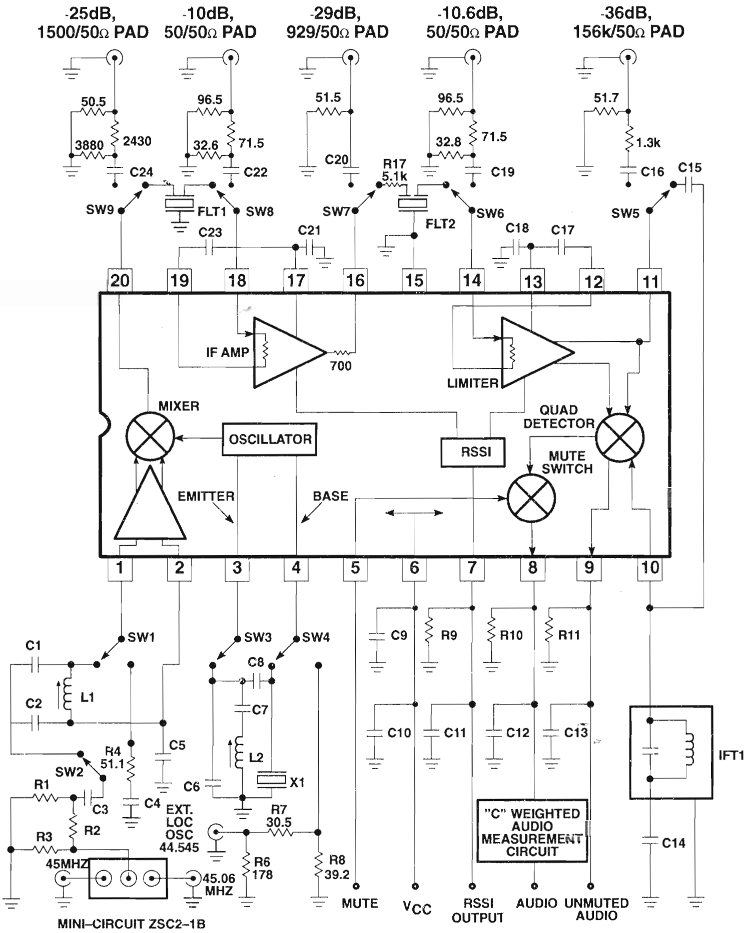
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: dB(v) = 20log V_{OUT}/V_{IN}

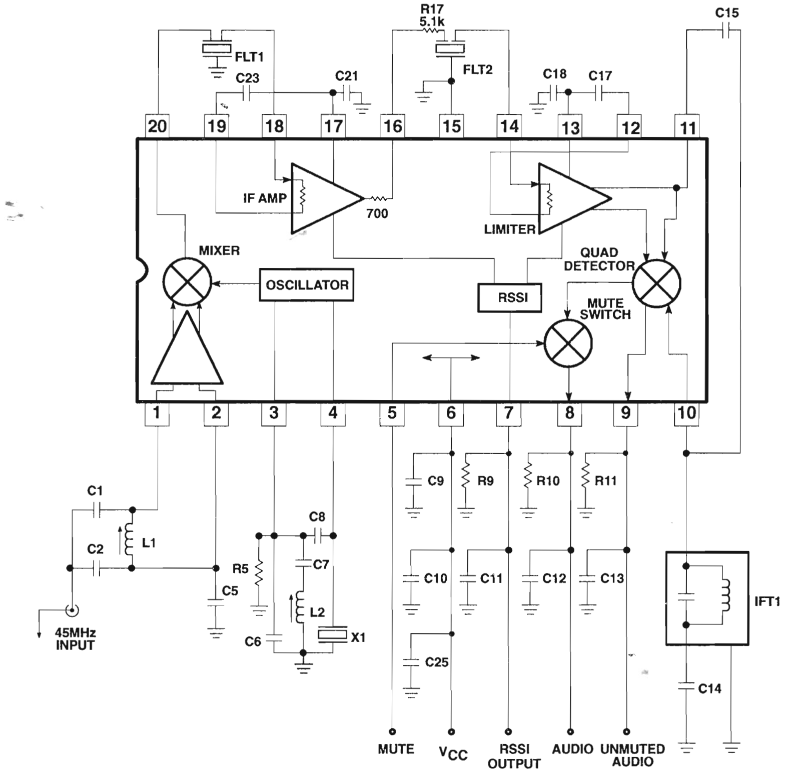


Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8µF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8µH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. NE/SA625 45MHz Test Circuit (Relays as shown)



Application Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8µF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic

C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8µH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R5	Not Used in Application Board (see Note 8)
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

Figure 2. NE/SA625 45MHz Application Circuit

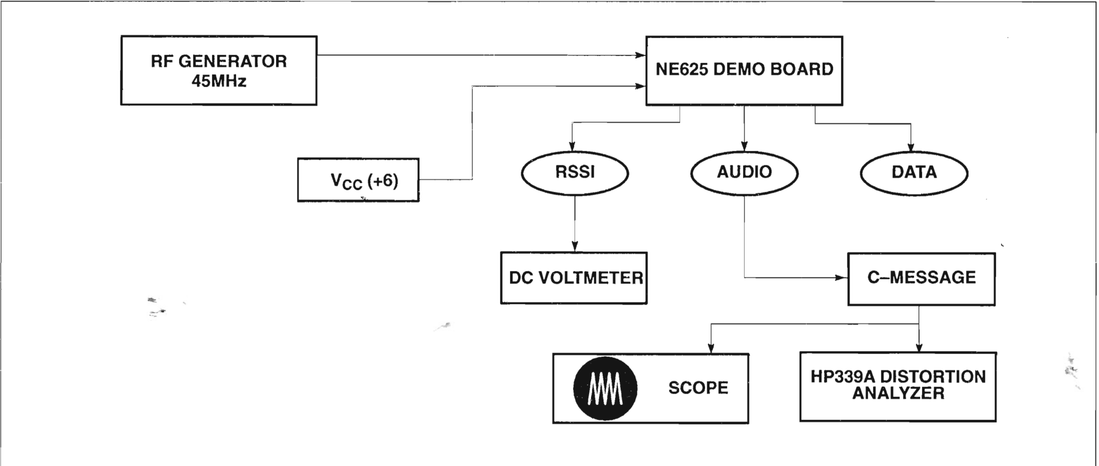


Figure 3. NE/SA625 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22µV or -120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

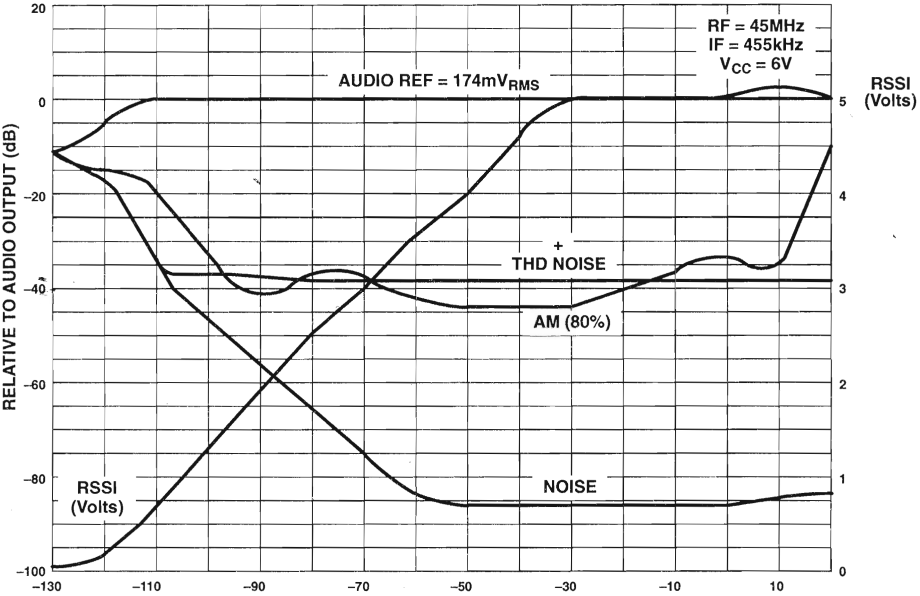


Figure 4. NE625 Application Board at 25°C

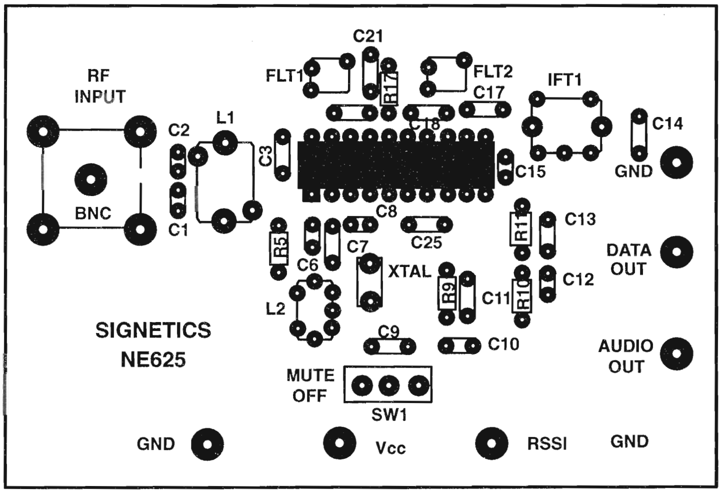
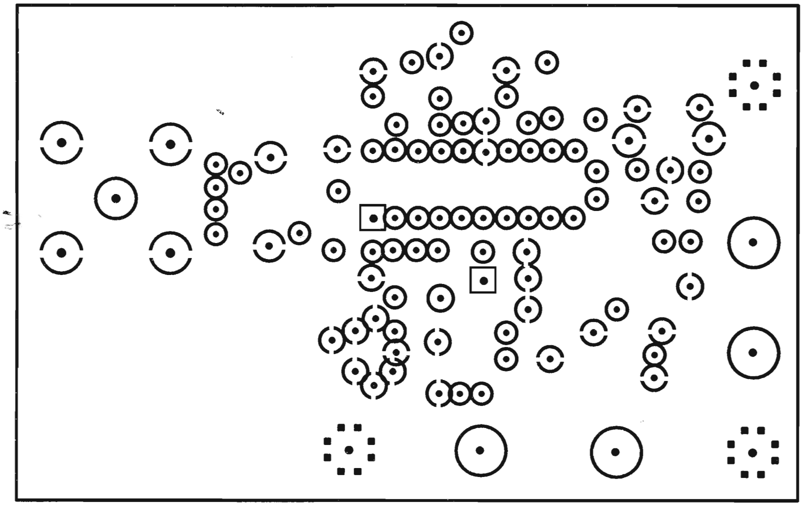
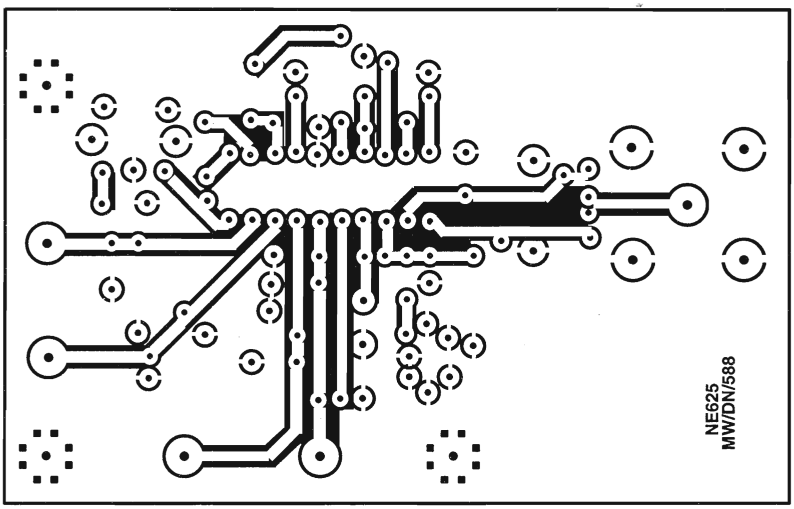


Figure 5. Component Placement for NE625 Application Circuit



TOP VIEW



BOTTOM VIEW

Figure 6. Layout for NE/SA625 Application Board

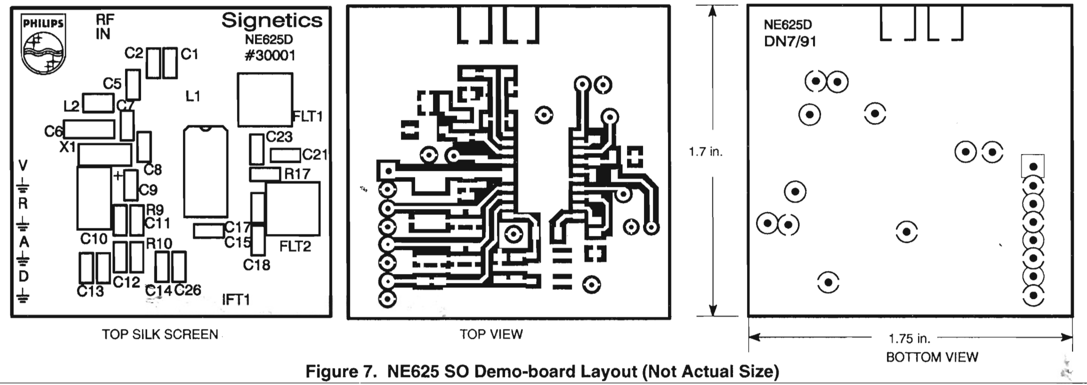


Figure 7. NE625 SO Demo-board Layout (Not Actual Size)

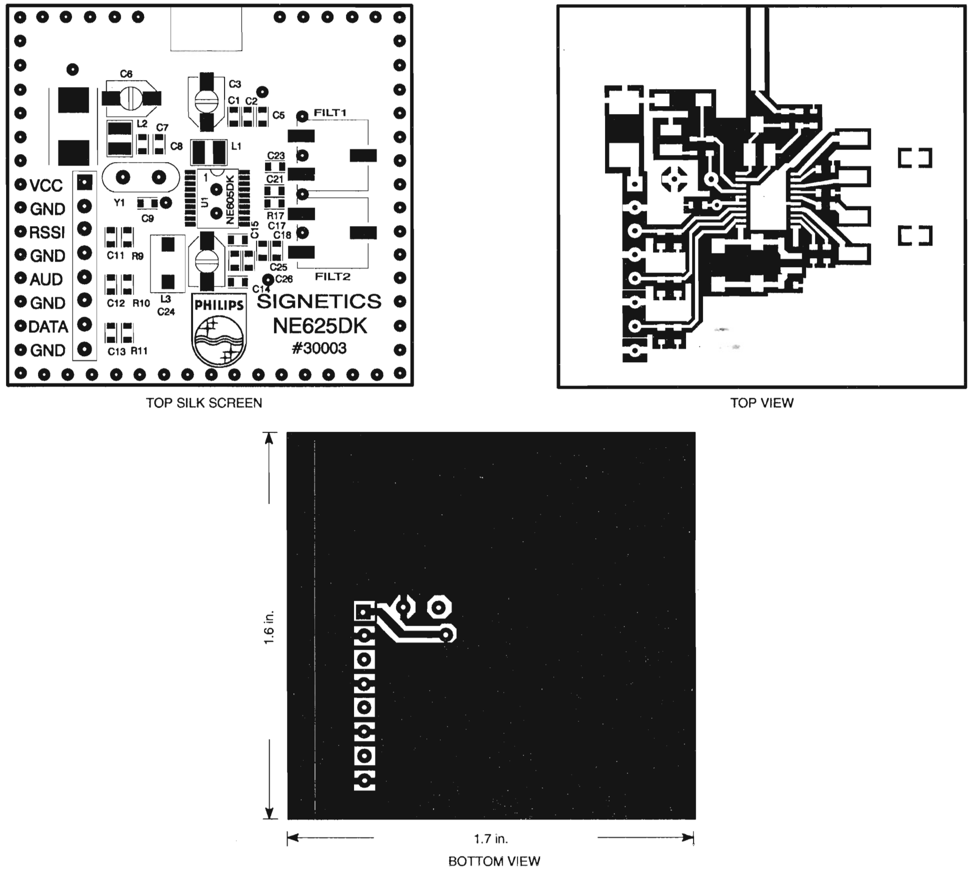


Figure 8. NE625 SSOP Demo-board Layout (Not Actual Size)

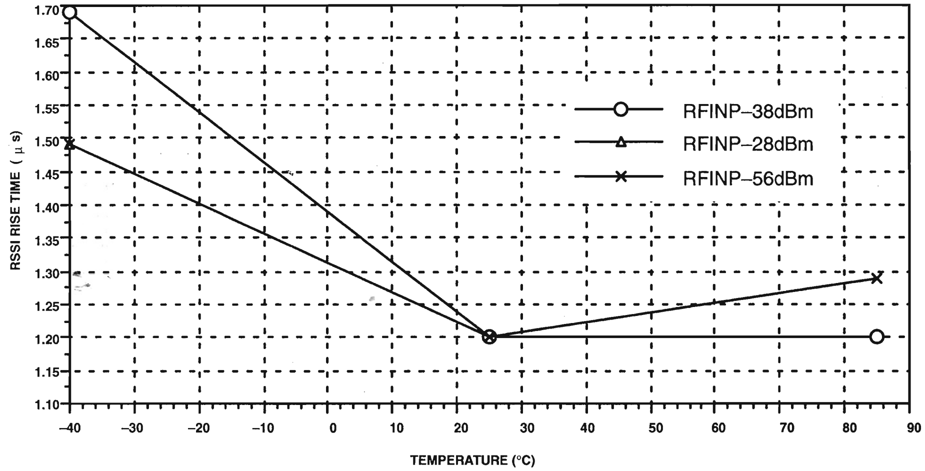


Figure 9. NE/SA625 Rise Time 455kHz IF Frequency

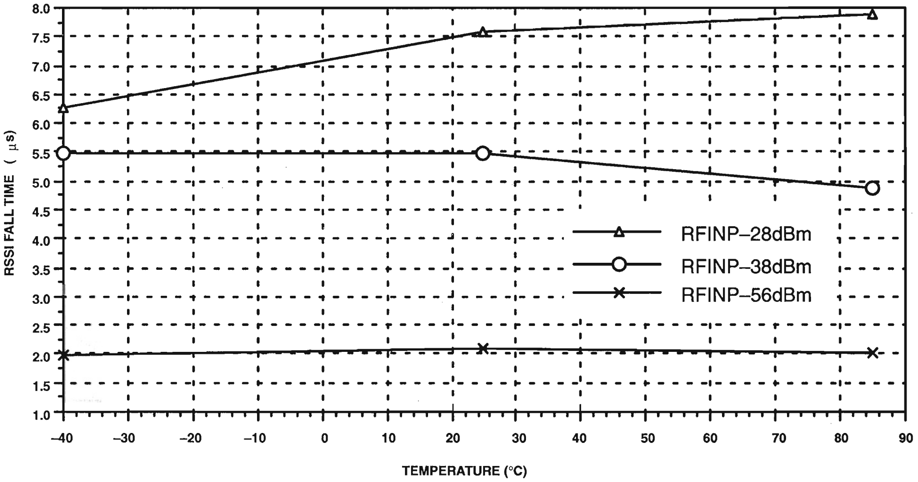


Figure 10. NE/SA625 Fall Time 455kHz IF Frequency

High performance low power mixer FM IF system with high-speed RSSI

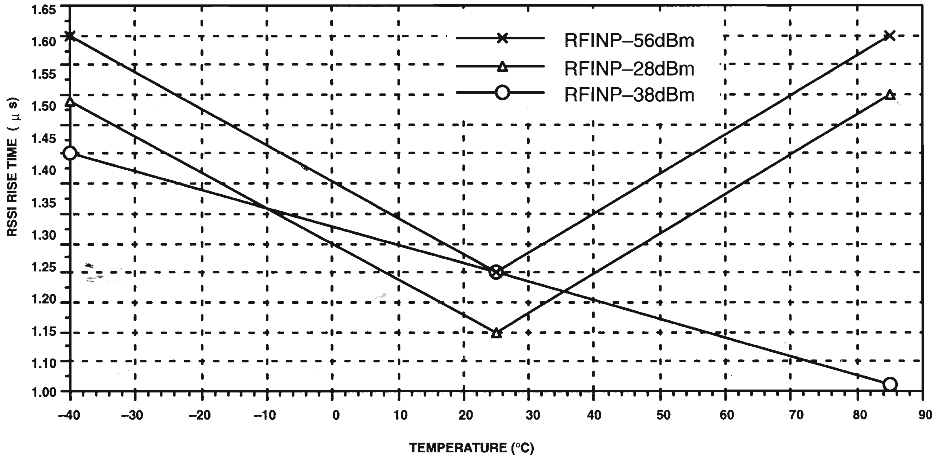


Figure 11. NE/SA625 Rise Time 10.7MHz IF Frequency

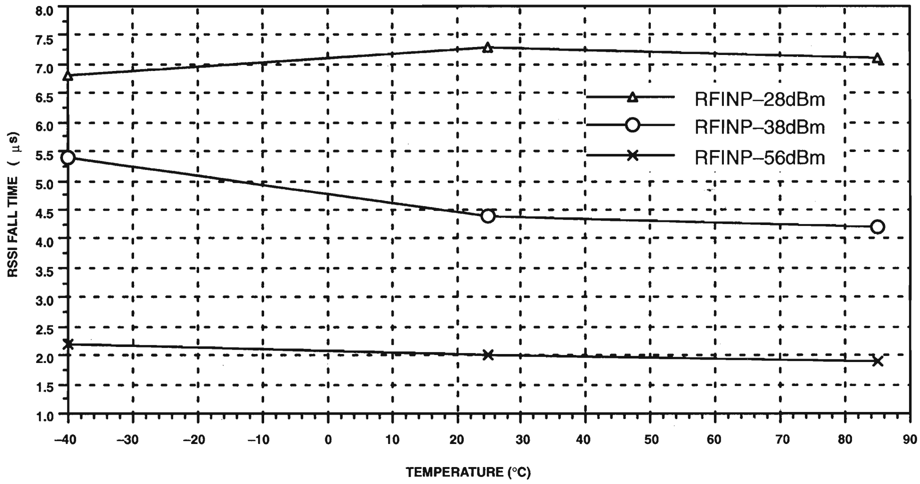


Figure 12. NE/SA625 Fall Time 10.7MHz IF Frequency

Low voltage high performance mixer FM IF system with high-speed RSSI

SA626

DESCRIPTION

The SA626 is a low-voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, high speed logarithmic received signal strength indicator (RSSI), voltage regulator and audio and fast RSSI op amps. The SA626 is available in 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink small outline package).

The SA626 was designed for high bandwidth portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio and RSSI outputs have amplifiers. The RSSI output has access to the feedback pin. This enables the designer to level adjust the outputs or add filtering.

SA626 incorporates a power down mode which powers down the device when Pin 8 is low. Power down logic levels are CMOS and TTL compatible with high input impedance.

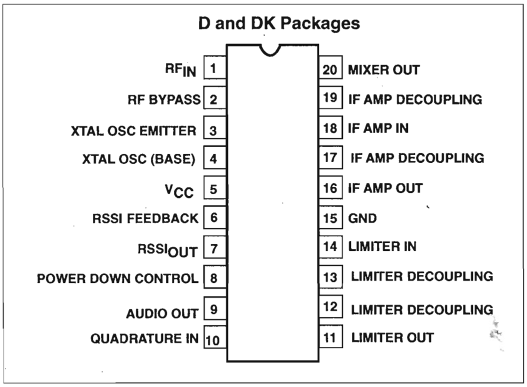
APPLICATIONS

- Digital cordless telephones
- Digital cellular telephones
- Digital cellular base stations
- Portable high performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

FEATURES

- Fast RSSI rise and fall times
- Low power consumption: 6.5mA typ at 3V
- Power down mode (I_{CC} = 200µA)

PIN CONFIGURATION

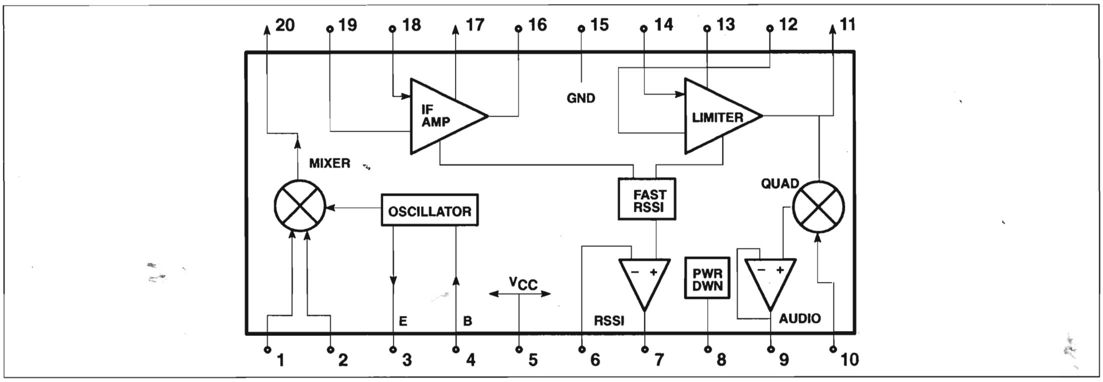


- Mixer input to >500MHz
- Mixer conversion power gain of 11dB at 240MHz
- Mixer noise figure of 14dB at 240MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz, local oscillator can be injected)
- 92dB of IF Amp/Limiter power gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Audio output internal buffer
- RSSI output internal buffer
- Internal op amps with rail-to-rail outputs
- 10.7MHz filter matching (330Ω) reduces external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.54µV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 240MHz and IF at 10.7MHz
- SA626 meets cellular radio specifications
- ESD hardened

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA626D	0172D
20-Pin Plastic Shrink Small Outline Package (Surface-mount)	-40 to +85°C	SA626DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	0.3 to 7	V
V_{IN}	Voltage applied to any other pin	–0.3 to (V_{CC}+0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA626	–40 to +85	°C
θ_{JA}	Thermal impedance D package	90	°C/W
	DK package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

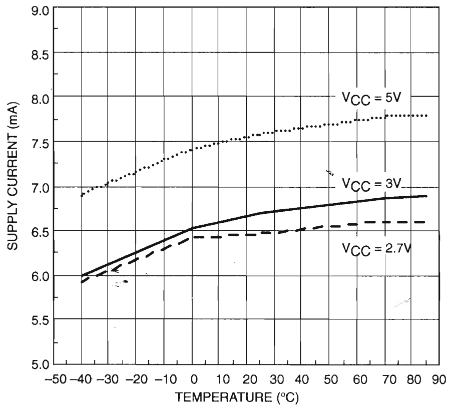
V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA626			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7	3.0	5.5	V
I_{CC}	DC current drain	Pin 8 = HIGH	5.5	6.5	7.5	mA
I_{CC}	Standby	Pin 8 = LOW		0.2	0.5	mA
	Input current	Pin 8 LOW	–10		10	µA
		Pin 8 HIGH	–10		10	µA
	Input level	Pin 8 LOW	0		0.3V_{CC}	V
		Pin 8 HIGH	0.7V_{CC}		V_{CC}	V
t_{ON}	Power up time	RSSI valid (10% to 90%)		10		µs
t_{OFF}	Power down time	RSSI invalid (90% to 10%)		5		µs

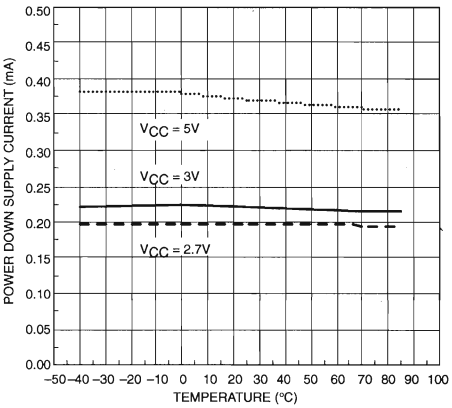
AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = +3V$, unless otherwise stated. RF frequency = 240.05MHz + 14.5dBV RF input step-up; IF frequency = 10.7MHz; RF level = -68dBm; FM modulation = 1kHz with ±125kHz peak deviation. Audio output with C-message weighted filter and de-emphasis filter. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

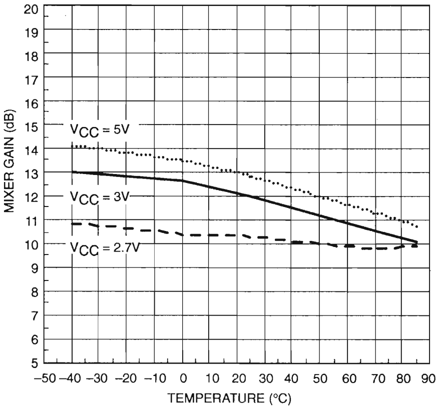
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA626			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 160mV$_{RMS}$)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	External oscillator (buffer)			500		MHz
	Noise figure at 240MHz			14		dB
	Third-order input intercept point	Matched f1=240.05; f2=240.35MHz		-16		dBm
	Conversion power gain	Matched 14.5dBV step-up	8	11	14	dB
	RF input resistance	Single-ended input		700		Ω
	RF input capacitance			3.5		pF
	Mixer output resistance	(Pin 20)		330		Ω
IF section						
	IF amp power gain			38		dB
	Limiter amp power gain			54		dB
	Input limiting -3dB	Test at Pin 18		–105		dBm
	AM rejection	80% AM 1kHz		50		dB
	Audio level	Unity gain	120	160	200	mV$_{RMS}$
	Audio DC level	Pin 9, no signal		1.0		V
	SINAD sensitivity	IF level = -111dBm		16		dB
THD	Total harmonic distortion			-43	–38	dB
S/N	Signal-to-noise ratio	No modulation for noise		60		dB
	IF RSSI output with buffer	IF level = -118dBm		0.2	0.5	V
		IF level = -68dBm	0.3	0.6	1.0	V
		IF level = -10dBm	0.9	1.3	1.8	V
	IF RSSI output rise time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		1.2		μs
	(no RSSI bypass capacitor)	RF level = -28dBm		1.1		μs
	IF RSSI output fall time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		2.0		μs
	(no RSSI bypass capacitor)	RF level = -28dBm		7.3		μs
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance			330		Ω
	IF output impedance			330		Ω
	Limiter input impedance			330		Ω
	Limiter output impedance			300		Ω
	Limiter output level with no load			130		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	RF level = -10dBm		160		mV$_{RMS}$
	System RSSI output	RF level = -10dBm		1.4		V
	System SINAD	RF level = -106dBm		12		dB



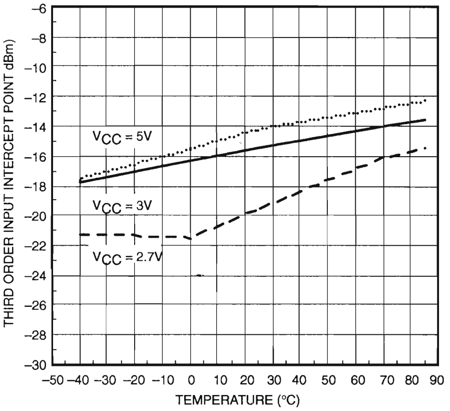
Supply Current vs Temperature and Supply Voltage



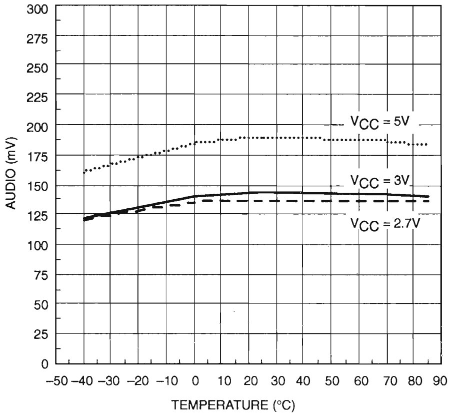
Power Down Supply Current vs Temperature and Supply Voltage



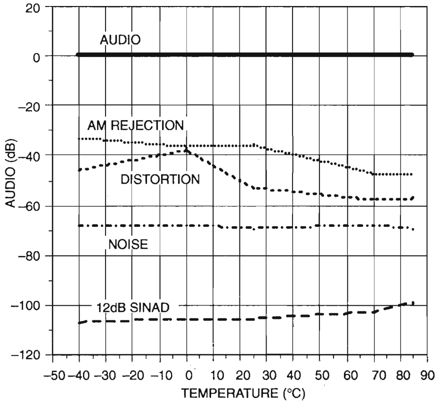
Mixer Power Gain vs Temperature and Supply Voltage



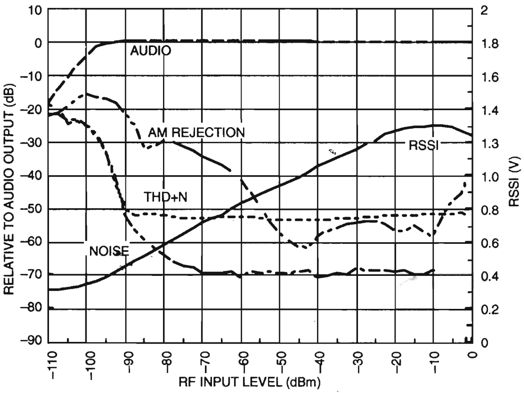
Third Order Input Intercept Point vs Temperature and Supply Voltage



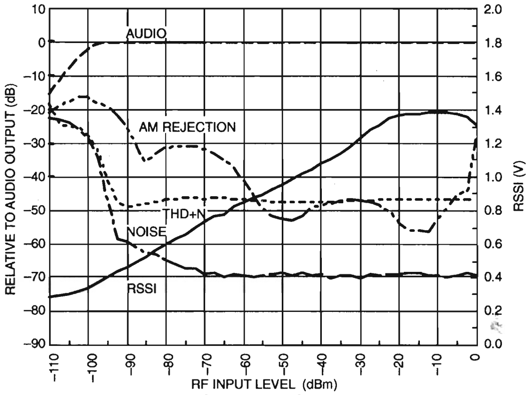
Audio Output Level vs. Temperature and Supply Voltage



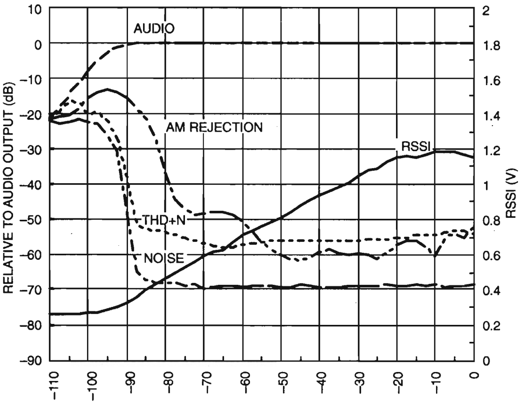
12dB SINAD and Relative Audio, THD, Noise and AM Rejection for VCC = 3V vs Temperature RF = 240MHz, Level = –68dBm, Deviation = 125kHz



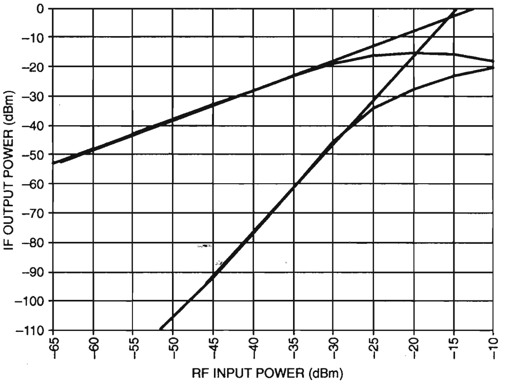
Receiver RF Performance — T = 25°C, Audio Level = 129mV$_{RMS}$



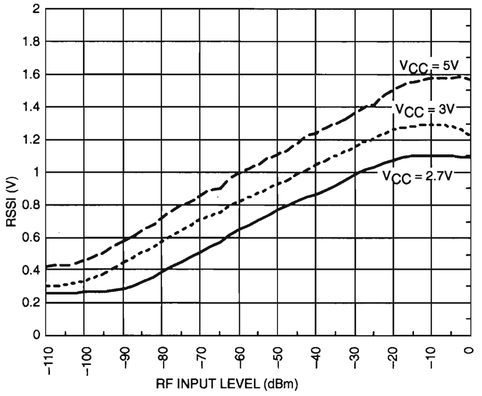
Receiver RF Performance — T = –40°C, Audio Level = 118mV$_{RMS}$



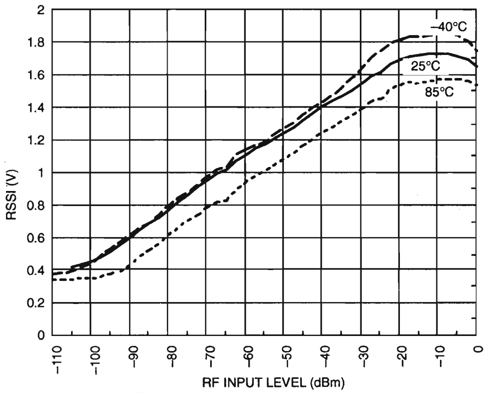
Receiver RF Performance – T = 85°C, Audio Level = 131mV$_{RMS}$



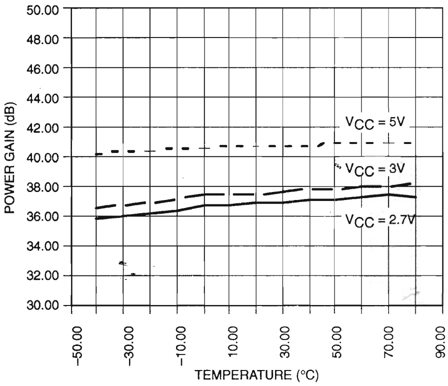
Mixer Third Order Intercept and Compression



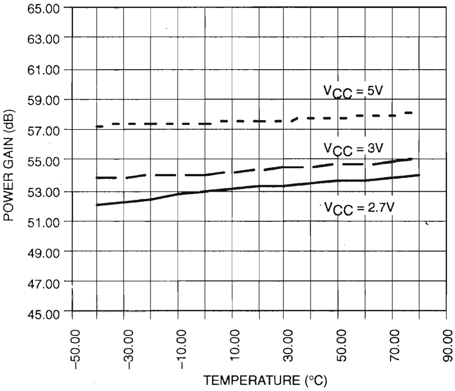
RSSI vs RF Input Level and Supply Voltage



RSSI vs RF Input Level and Temperature



SA626 IF Amplifier Gain vs Temperature vs Supply Voltage



SA626 Limiting Amplifier Gain vs Temperature vs Supply Voltage

CIRCUIT DESCRIPTION

The SA626 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 38dB of power gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 54dB of power gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 10.7MHz, 330Ω source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types, such as cordless and cellular hand-held phones.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 14dB, conversion power gain of 11dB, and input third-order intercept of -16dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 330Ω resistor permitting direct connection to a 10.7MHz ceramic filter. The input resistance of the limiting IF amplifiers is also 330Ω. With most 10.7MHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 3dB insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 3dB insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a power gain of 92dB. For operation at intermediate frequency at 10.7MHz. Special care must be given to layout, termination, and interstage loss to avoid instability.

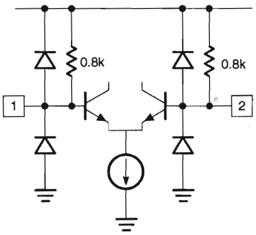
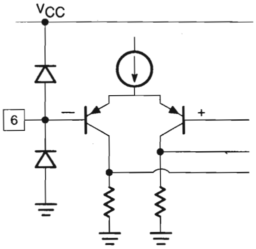
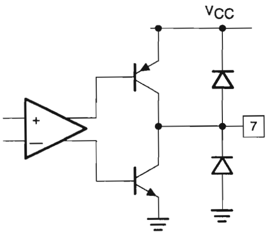
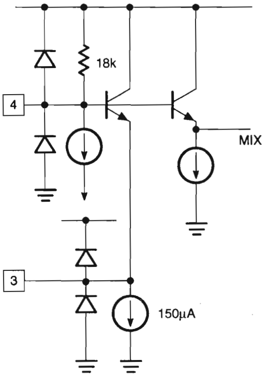
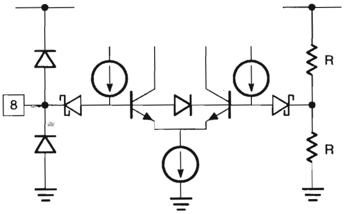
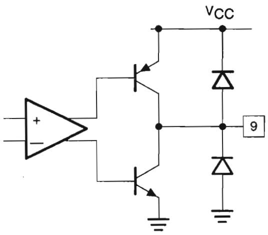
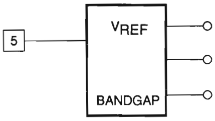
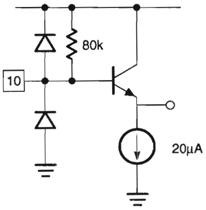
The demodulated output of the quadrature drives an internal op amp. This op amp is configured as a unity gain buffer. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength indicator completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone, and RCR-28 cordless telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

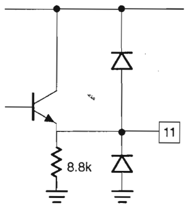
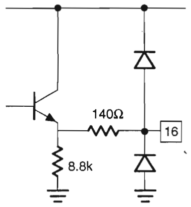
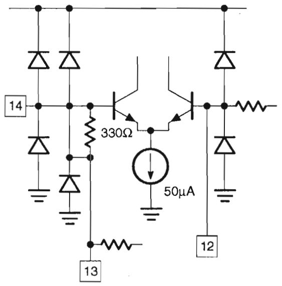
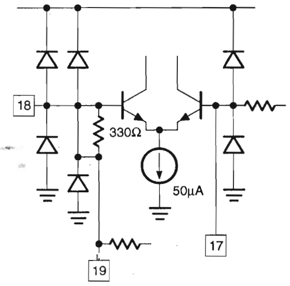
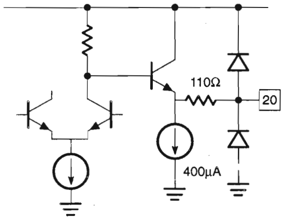
Low voltage high performance mixer FM IF system with high-speed RSSI

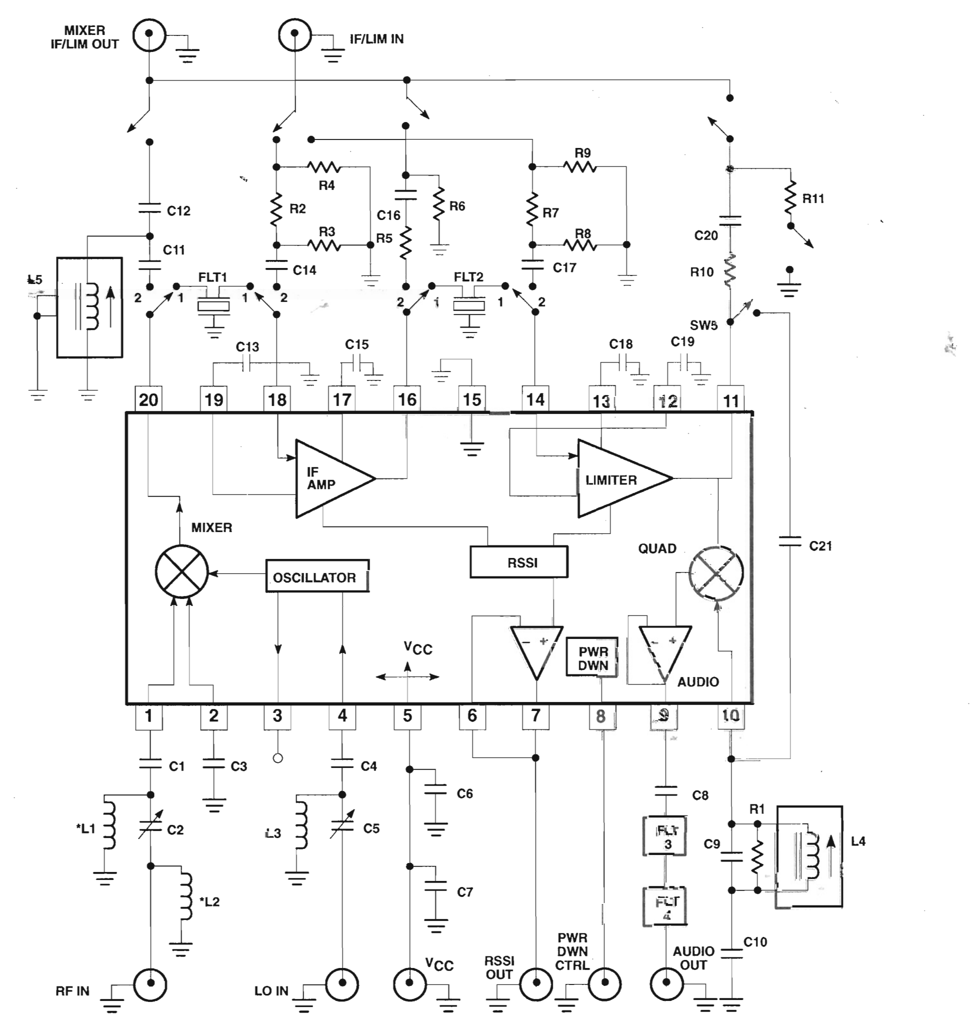
SA626

PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	RF IN	+1.07		6	RSSI FEEDBACK	+0.20	
2	RF BYPASS	+1.07		7	RSSI OUT	+0.20	
3	XTAL OSC	+1.57		8	POWER DOWN	+2.75	
4	XTAL OSC	+2.32		9	AUDIO OUT	+1.09	
5	V_{CC}	+3.00		10	QUAD. IN	+3.00	

PIN FUNCTIONS (continued)

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
11	LIMITER OUT	+1.35		16	IF AMP OUT	+1.22	
12	LIMITER DECOUP	+1.23		17	IF AMP DECOUP	+1.22	
13	LIMITER COUPLING	+1.23		18	IF AMP IN	+1.22	
14	LIMITER IN	+1.23		19	IF AMP DECOUP	+1.22	
15	GND	0		20	MIXER OUT	+1.03	

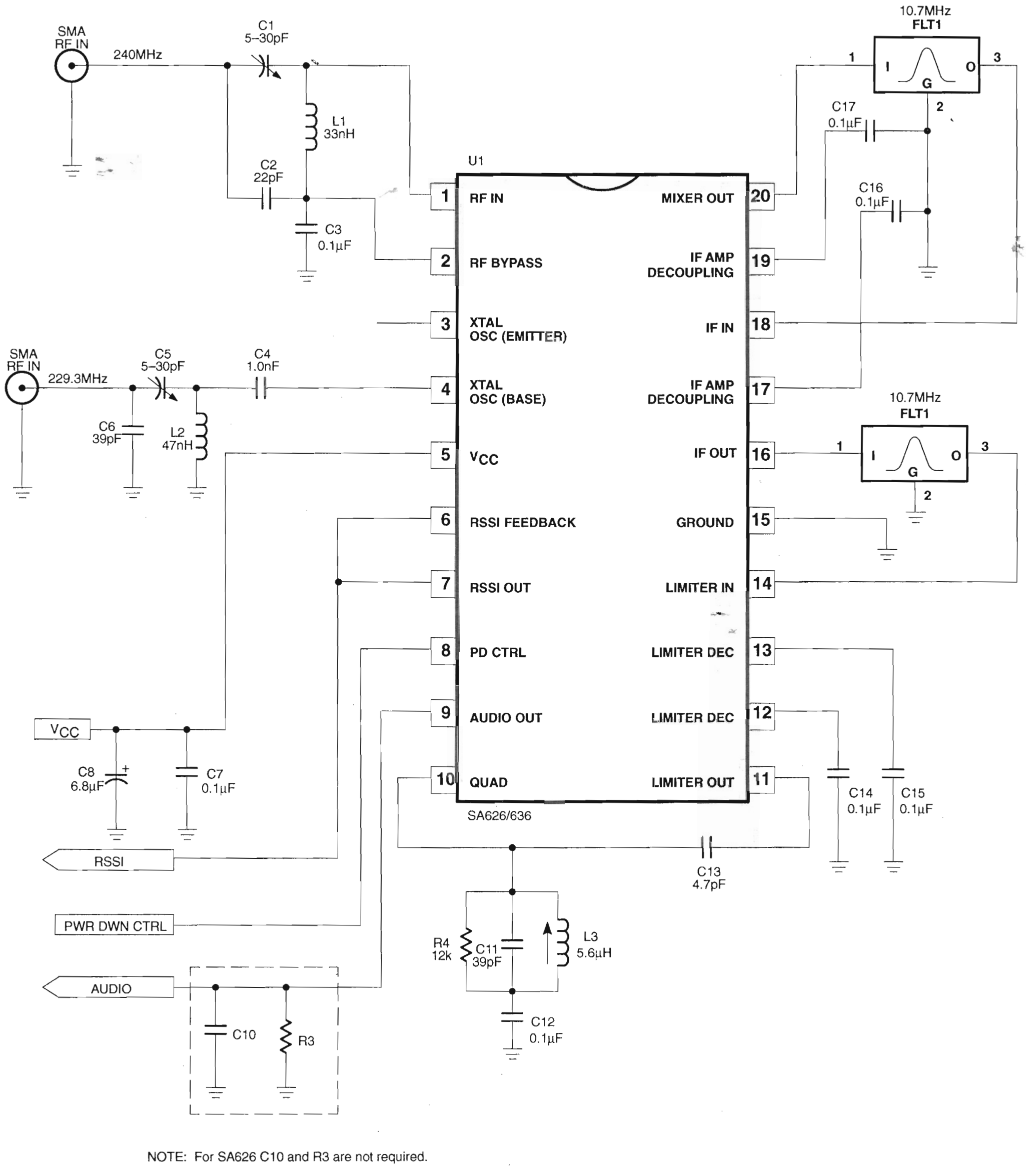


Automatic Test Circuit Component List

R1	8.2kΩ select	C1	0.1µF	C12	160pF select	L1	150nH select for input match
R2	6.42kΩ	C2	1–5pF select for input match	C13	1000pF	L2	22nH select for input match
R3	347.8Ω	C3	0.1µF	C14	0.1µF	L3	47nH select for input match
R4	49.9Ω	C4	0.1µF	C15	1000pF	L4	5.6µH select for input match
R5	1kΩ	C5	1–5pF select for input match	C16	0.1µF	L5	1.27–2.25µH select for mixer output match
R6	49.9Ω	C6	100pF	C17	0.1µF		
R7	6.42kΩ	*C7	6.8µF 10V	C18	1000pF	FLT1	10.7MHz (Murata SFE10.7MA5-A)
R8	347.8Ω	C8	1µF	C19	1000pF	FLT2	10.7MHz (Murata SFE10.7MA5-A)
R9	49.9Ω	C9	39pF select	C20	0.1µF	FLT3	"C" message weighted
R10	1kΩ	C10	0.1µF	C21	1pF	FLT4	Active de-emphasis
R11	49.9Ω	C11	0.1µF				

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. SA626 240.5MHz (RF) / 10.7MHz (IF) Test Circuit



NOTE: For SA626 C10 and R3 are not required.

Figure 2. SA626 240MHz (RF) / 10.7MHz (IF) Application Circuit

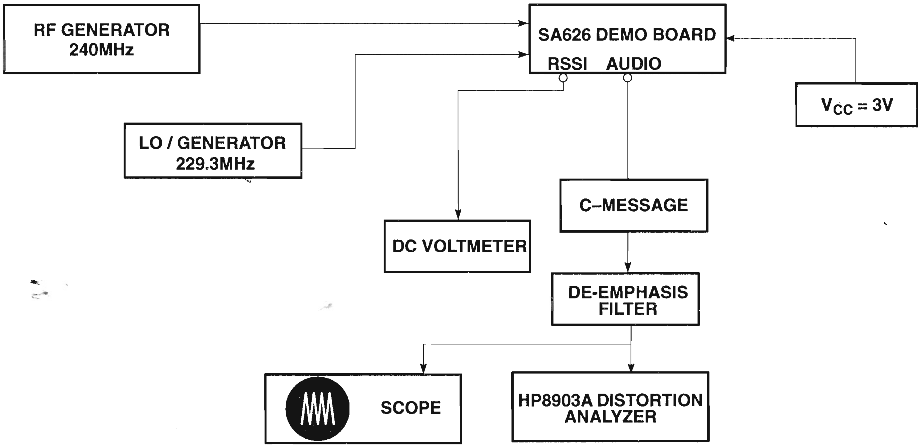


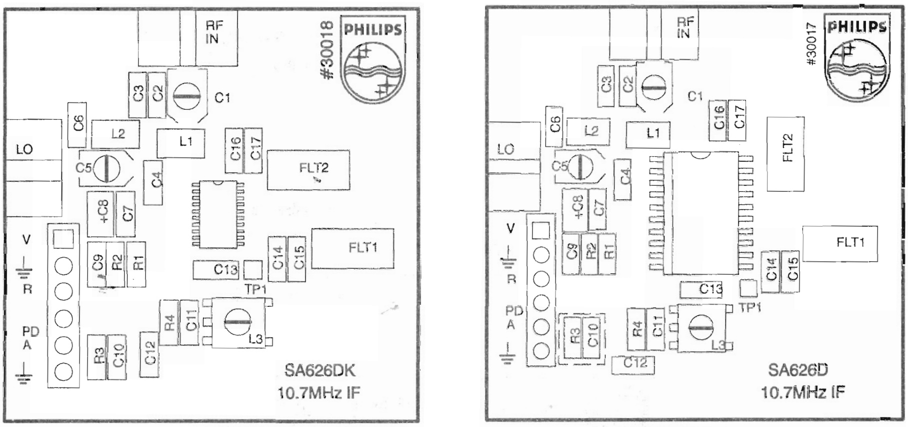
Figure 3. SA626 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP8903A analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filter can be SFE10.7MA5-A made by Murata which has 280kHz IF bandwidth.
3. RF generator: Set your RF generator at 240.000MHz, use a 1kHz modulation frequency and a 125kHz deviation.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.54µV or –112dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 0.1µF bypass capacitor on the supply pin improves sensitivity.

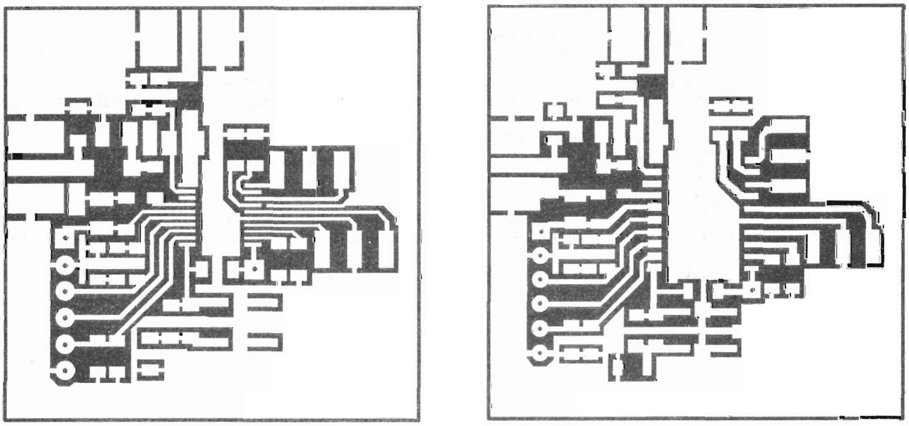
Low voltage high performance mixer FM IF system with high-speed RSSI

SA626



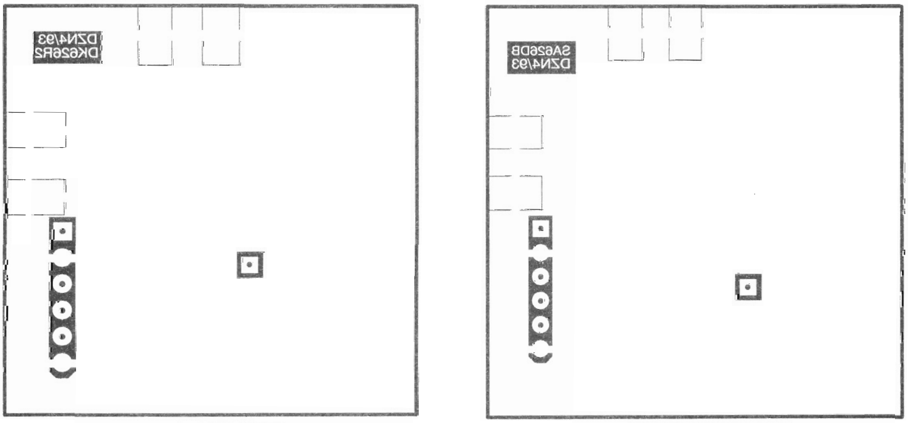
TOP SILK SCREEN (SSOP)

TOP SILK SCREEN (SOL)



TOP VIEW (SSOP)

TOP VIEW (SOL)



BOTTOM VIEW (SSOP)

BOTTOM VIEW (SOL)

Figure 4. SA626 Demoboard Layout (Not Actual Size)

Philips FM/IF systems for GMSK/GFSK receivers

AN1997

Author: Yanpeng Guo

ABSTRACT

To assist Philips Semiconductors customers in digital cellular and wireless/PCS system design, a Philips FM/IF system-based GMSK/GFSK demoboard has been developed based on CT-2 specifications. This application note presents a detailed description of this board including circuits, design information, and measured BER performance. The circuit diagram, component list, and board layout are also included.

INTRODUCTION

In order to meet the rapidly increasing demand for mobile radio and wireless/PCS services, digital cellular and digital wireless systems have become the new generation of mobile communications for higher capacity. It is a new challenge for engineers to find IC solutions for these digital wireless applications.

In worldwide digital cellular, wireless/PCS standards, GMSK/GFSK modulation techniques have been widely employed as illustrated in Table 1. In order to assist the applications of Philips ICs in these digital systems, a Philips FM/IF system-based GMSK/GFSK demoboard has been developed. The purpose of this application note is to provide a detailed description of this board, to help customers achieve the best performance using Philips SA626, and also to provide suggestions for the applications of other Philips FM/IF systems.

Table 1. A Summary of Digital Cellular and Cordless Standards

Standard	Access	Modulation	Bit Rate	Ch. Spacing
IS-54	TDMA	π/4-DQPSK	48 kb/s	30 kHz
GSM	TDMA	GMSK	270 kb/s	200 kHz
CT-2	TDMA	GFSK	72 kb/s	100 kHz
DECT	TDMA	GFSK	1.152 Mb/s	1.728 MHz

This application note is organized as follows:

- Introduction.
- Review of GMSK/GFSK modulation: advantages of GMSK/GFSK modulation techniques and implementation methods.
- Overview of the demoboard: general block diagram and detailed description of each part of the board.
- BER measurements: measurement set-up, procedures, and measured results.
- Questions & Answers.

REVIEW OF GMSK/GFSK MODULATION

GMSK(Gaussian Minimum Shift Keying) is a premodulation Gaussian filtered binary digital frequency modulation scheme with modulation index of 0.5. The following features make GMSK very suitable for digital cellular and wireless applications.

1. Constant envelope: this allows the operation of Class-C RF power amplifiers to achieve higher system power efficiency.
2. Narrow power spectrum: narrow mainlobe and low spectral tails keep the adjacent channel interference to low levels and achieve higher spectral efficiency.
3. Coherent/non-coherent detection capabilities.
4. Good BER performance.

GMSK modulation can be implemented in two ways. The most straightforward way is to transmit the data stream through a Gaussian low-pass filter and apply the resultant wave form to a voltage controlled oscillator (VCO) as shown in Figure 1. The output of the VCO is then a frequency modulated signal with a Gaussian response. The advantage of this scheme is the simplicity, but it is difficult to keep an exact modulation index of 0.5 with this scheme. Therefore, VCO implemented GMSK is usually used in non-coherent detection systems such as DECT and CT2.

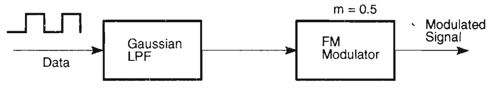


Figure 1. VCO Implemented GMSK Modulator

GMSK signals can also be generated using a quadrature modulation structure. Consider the phase modulated signal given by:

$$s(t) = \cos[\omega_C t + \phi(t)] \qquad \text{(EQ. 1)}$$

This can be expanded into its in-phase and quadrature components,

$$s(t) = \cos[\phi(t)]\cos(\omega_C t) - \sin[\phi(t)]\sin(\omega_C t) \qquad \text{(EQ. 2)}$$

The quadrature modulator is based on Equation (2). The implementation of such a GMSK modulator is shown in Figure 2. The incoming data is used to address two separate ROMs which contain the sampled versions of all possible phase trajectories within a given interval. After D/A conversion, the output of each ROM is applied to the I/Q modulator. The output is the GMSK modulated signal. This implementation scheme provides an exact modulation index of 0.5, which allows coherent detection.

GFSK (Gaussian Frequency Shift Keying) is also a premodulation Gaussian filtered digital FM scheme, but without the restriction of modulation index to be 0.5. The block diagram of GFSK modulator is the same as shown in Figure 1, but the modulation index can be specified according to the applications.

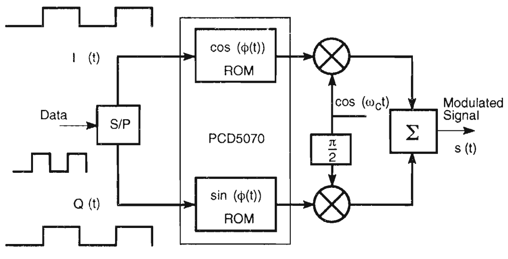


Figure 2. I/Q Implemented GMSK Modulator

GMSK signals can be demodulated in three ways: 1.) FM discriminator detection, 2.) differential detection, and 3.) coherent detection. The coherent detection scheme has the best BER performance, but is only suitable for I/Q structure based GMSK systems (Ref 6.). The differential detection method has BER degradation even with complex implementation (Ref 7.). The limit/frequency discriminator structure is the simplest scheme suitable for both GMSK and GFSK applications. Therefore, the FM discriminator technique is widely used for GMSK/GFSK demodulation in digital cellular/PCS applications. Figure 3 presents the block diagram of an FM discriminator GMSK/GFSK demodulator.

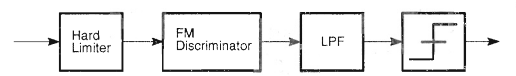


Figure 3. Limit/Frequency Discriminator GMSK/GFSK Demodulator

OVERVIEW OF THE GMSK/GFSK DEMOBOARD

Figure 4 is the block diagram of a VCO/FM discriminator based GMSK/GFSK modem (modulator/demodulator), which also illustrates the structure of the Philips GMSK/GFSK demoboard. The demoboard contains the entire demodulator as well as the Gaussian low-pass filter (LPF) for the modulator. The input data stream is first premodulation filtered by the Gaussian LPF, then the filtered base band wave form is applied to an FM signal generator with specific modulation index. The output is then the GMSK/GFSK modulated signal. After the limit/frequency discriminator detection, a Gaussian LPF is employed to eliminate noise. The output of the threshold detector is the regenerated binary data, which can be sent to a data error analyzer to evaluate the BER performance.

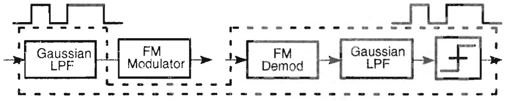


Figure 4. VCO/FM Discriminator GMSK/GFSK Modem (dotted line for the demoboard)

Gaussian LPF

On the demoboard, a 4th-order Gaussian LPF is implemented for both premodulation filtering and post demodulation filtering. The response function of this 4th-order filter can be expressed as (Ref 4.):

$$H(s) = \frac{\omega_1^2}{S^2 + 2\zeta_1\omega_1 S + \omega_1^2} \cdot \frac{\omega_2^2}{S^2 + 2\zeta_2\omega_2 S + \omega_2^2} \qquad \text{(EQ. 3)}$$

By looking up the Gaussian LPF poles table[4], with 3dB bandwidth normalized to unity, we have:

$$\omega_1 = 1.9086, \quad \zeta_1 = 0.7441; \quad \omega_2 = 1.6768, \quad \zeta_2 = 0.9720$$

This 4th-order Gaussian LPF is implemented with switched capacitor filters. The reason for using this scheme is that the LPF's 3dB bandwidth can be controlled by an external clock which allows generating GMSK signals with different BTb. To realize a 4th-order LPF, two stages of LMF100 are cascaded and operated at mode-3[5]. Figure 5 shows the circuit diagram for this mode.

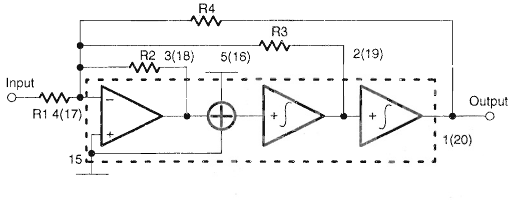


Figure 5. Circuit Diagram of LPF with LMF100 at Mode-3

For mode-3 LPF applications, the following formulas can be used to calculate the resistor values [5]:

$$H_{LP}(s) = \frac{H_{OLP}\omega_0}{S^2 + S\omega_0/Q + \omega_0} \qquad \text{(EQ. 4)}$$

$$\text{where, } H_{OLP} = -\frac{R_4}{R_1} \qquad \text{(EQ. 5)}$$

$$\omega_0 = \left(\frac{f_{CLK}}{100}\right) \cdot \sqrt{\frac{R_2}{R_4}} \qquad \text{(EQ. 6)}$$

$$Q = \left(\frac{R_3}{R_2}\right) \cdot \frac{\sqrt{R_2}}{R_4} \qquad \text{(EQ. 7)}$$

Example:

Step 1. Decide the gain and choose R value:
For unity gain, we have
$H_{OLP} = -R_4/R_1 = -1$, i.e. $R_4 = R_1$.
For the first stage, we choose a convenient value for input resistance: $R_{14} = R_{11} = 22k\Omega$

Step 2. Calculate R_{12}:
Compare (3) with (4), we have:

$$\omega_1 = \left(\frac{f_{CLK}}{100}\right) \cdot \sqrt{\frac{R_{12}}{R_{14}}} \qquad \text{(EQ. 8)}$$

By choosing f_{clk} = 100 times the 3dB bandwidth, we have

$$\omega_1 = \sqrt{\frac{R_{12}}{R_{14}}} \rightarrow R_{12} = 80.14k\Omega$$

Step 3. Calculate R_{13}:
From the comparison of (3) and (4), we also have,

$$Q_1 = \frac{1}{(2\zeta_1)} = \left(\frac{R_{13}}{R_{12}}\right) \cdot \sqrt{\frac{R_{12}}{R_{14}}} = \frac{1}{(2 \cdot 0.7441)} \qquad \text{(EQ. 9)}$$

$R_{13} = 28.22k\Omega$

For the second stage, the resistor values can be calculated by the same procedures. For this example, they are:

$R_{24} = R_{21} = 22k\Omega$
$R_{22} = 61.86k\Omega$
$R_{23} = 18.98k\Omega$

To obtain a good Gaussian LPF, the resistor values have to be adjusted with all input/output circuits connected. Baseband eye-diagrams and modulated power spectrum could be the references for the adjustment. The final values for this example are shown in the circuit diagram.

FM/IF System

The Philips low-voltage high performance monolithic FM/IF system, SA626, is employed for demodulation on the GMSK/GFSK demoboard. SA626 was designed specially for wide bandwidth portable communications applications, incorporating with a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, and audio and RSSI op amps. The RF section is similar to the famous SA605. The audio and RSSI outputs have amplifiers. With power down mode, SA626 will function down to 2.7V. Figure 6 is the block diagram of SA626. Detailed information can be found in the data book and application note [1, 2, 3].

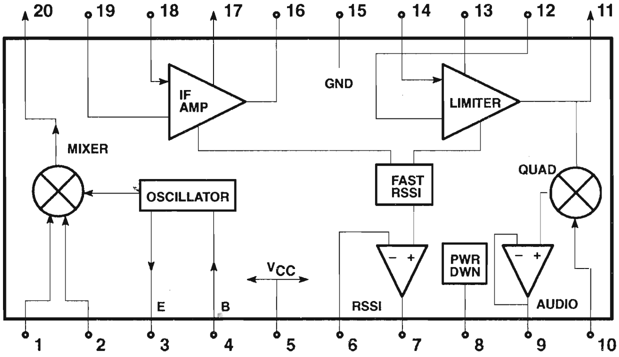


Figure 6. Block Diagram of the FM/IF System SA626

The GMSK/GFSK demoboard is designed for an RF frequency of 45MHz, LO frequency of 55.7 MHz, and intermediate frequency of 10.7MHz. For different RF frequency applications, the step-by-step matching circuits design procedure is presented in Ref. 1.

Although this demoboard is designed with SA626 based on CT-2 specifications, Philips also provides FM/IF solutions for many other GMSK/GFSK systems. SA626 is specially designed for wide bandwidth applications. For lower data rate applications such as CDPD (19.2 kb/s), SA605/625 family is recommended. For DECT and other high data rate applications, SA636 and SA639 are the recommended solutions. Data (audio) output bandwidth is the main limiting factor for high data rate applications. Table 2 presents a summary of the major characteristics of Philips FM/IF systems. The suggested maximum data rate for each part is an approximation based on the baseband eye pattern. Higher data rate could be operated with some modifications or if more BER degradation is allowed.

Table 2. Major Characteristics of the FM/IF Systems

	NE602/604	NE605	NE625	NE626	NE636	NE639*
V_{CC}	4.5 - 8V	4.5 - 8V	4.5 - 8V	2.7 - 5.5V	2.7 - 5.5V	2.7 - 5.5V
I_{CC}	2.4/3.3mA @ 6V	5.7mA @ 6V	5.7mA @ 6V	6.5mA @ 3V	6.5mA @ 3V	8.3mA @ 3V
SINAD	-120dBm/.22µV (RF: 45MHz, IF: 455kHz, 1kHz tone, 8kHz Dev.)	-120dBm/.22µV (RF: 45MHz, IF: 455kHz, 1kHz tone, 8kHz Dev.)	-120dBm/.22µV (RF: 45MHz, IF: 455kHz, 1kHz tone, 8kHz Dev.)	-112dBm/.54µV (RF: 240MHz, IF: 10.7kHz, 1kHz tone, 70kHz Dev.)	-111dBm/.54µV (RF: 240MHz, IF: 10.7kHz, 1kHz tone, 125kHz Dev.)	-111dBm/.54µV (RF: 240MHz, IF: 10.7kHz, 576kHz tone, 288kHz Dev.)
Features	Audio & Data pins IF BW of 25MHz Matching for standard 455kHz IF filters	Audio & Data pins IF BW of 25MHz Matching for 455kHz IF filters	Pin compatible with NE605 Fast RSSI IF BW of 25MHz Matching for 455kHz IF filters	Power down mode Low voltage Fast RSSI IF BW of 25MHz Int. RSSI & Audio op amp Matching for 10.7MHz IF filters	Power down mode Low voltage Fast RSSI IF BW of 25MHz Int. RSSI op amp Wideband data out Matching for 10.7MHz IF filters	Power down mode Low voltage Fast RSSI IF BW of 25MHz Int. RSSI op amp Wideband data out Post detection amp Matching for 10.7MHz IF filters
Data Rate**	100kb/s	100kb/s	100kb/s	300kb/s	1.5Mb/s	2Mb/s
NOTES	* Objective specifications. ** Approximated maximum data rate. With some modifications, higher data rate might be operated.					

Threshold Detector and Data Regeneration

A 2-level threshold detector with sampling time adjustment circuits is implemented for data regeneration as shown in the circuit diagram. The output base band signal (eye-diagrams) from SA626 is first fed into a comparator (LM311) to generate a TTL logic signal which is then sampled with the data clock at the transmitting bit rate. The phase of the data clock can be adjusted manually through a monostable multivibrator (74HC123) to achieve the optimal sampling time. The demoboard is initially adjusted for a bit rate of 72 kb/s. If a different data rate is used, the sampling time has to be re-adjusted.

The symbol timing recovery (STR) circuit is not implemented on this demoboard. The transmitting data clock should be either hard-wire connected from the transmitter, or obtained from a separate STR circuit for operation. The measured performance presented in this paper is conducted with hard-wire connected data clock. However, BER degradation caused by STR should be no more than 1dB (Ref 8.).

PERFORMANCE MEASUREMENTS

The performance of this GMSK/GFSK demoboard including receiver sensitivity and BER is experimentally evaluated. BER performance is evaluated based on CT-2 specifications. Measurement procedures and the measured results are presented in this section.

Measurement Set-up

Figure 7 illustrates the measurement set-up with the GMSK/GFSK demoboard. A data error analyzer is employed to generate a pseudo random binary sequence (PRBS) with length of 10^9 -1 at a data rate of 72kb/s. This data sequence is sent to the Gaussian LPF on the board for premodulation filtering. The output Gaussian filtered base band signal is then applied to an FM signal generator as the modulating signal. To generate a GMSK modulated signal (modulation index = 0.5) at a bit rate of 72kb/s, frequency deviation of the FM signal generator needs to be set at 18kHz. The output from the generator is then a GMSK modulated signal (at 45MHz). Another signal generator is employed to provide an LO signal at 55.7MHz for the FM/IF system detection.

After FM discriminator detection, the output base band signal is fed into another Gaussian LPF on the board to eliminate noise. The 3dB bandwidth of both Gaussian LPFs is controlled by an external clock. This clock should be a square wave signal with TTL level. By controlling the frequency of this clock, different BTb can be achieved for certain bit rate. To have BTb equal 0.5 with bit rate of 72kb/s, the clock signal is set at 3.6MHz (100 times the required 3dB bandwidth). The output from the LPF is then sent to the threshold detector for data regeneration. The data clock signal is taken directly from the data error analyzer. The sampling time can be controlled by adjusting VR2 in the circuit diagram. The recovered data sequence is fed back to the Data Error Analyzer for BER measurement.

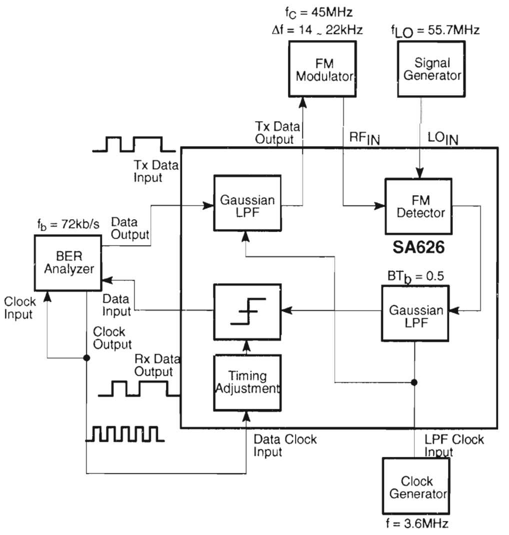


Figure 7. Measurement Set-Up with the GMSK/GFSK Board

Measurement Procedure and Results

1. **Measure SINAD at the audio output of SA626:** use the same set-up as described above, but set RF = 45MHz, fm = 1kHz, Δf = 8kHz; LO = 55.7MHz, -10dBm; the measured typical sensitivity for 12dB SINAD should be about -110dBm. (See Ref 1. for detailed SINAD measurement.)
2. **Check "LPF clock input":** this clock should be a TTL level signal with the frequency of 100 times the desired 3dB bandwidth of the LPF. For the data rate of 72kb/s and BTb = 0.5 LPF, the clock frequency is 3.6MHz (100 × 36kHz).
3. **Check "Tx data input":** 72kb/s baseband NRZ signal.
4. **Measure "Tx data output":** Gaussian low-pass filtered baseband eye-diagram as shown in Figure 8.
5. **Check "data clock input":** 72kHz clock signal.
6. **Adjust sampling position:** by adjusting VR2, set the rising edge of the clock at Pin 11 of Unit 4 (74HC74) to be at the center of the eye-diagram at Pin 2 of Unit 6 (LM311) in the circuit diagram.
7. **Measure BER with high RF level:** set RF input signal level at -80dBm and -90dBm, LO signal level at -10dBm: error free.
8. **Measure BER vs. RF input level curve:** RF level: -94 ~ -104 dBm, LO level: -10dBm, at each point, at least 100 errors have to be measured. Figure 9 presents the measured BER as a reference.

QUESTIONS & ANSWERS

Q. For the SINAD measurement, is it necessary to connect the whole system?
A. Even though only part of the system is used to measure SINAD, it is recommended to connect the whole system because the RF part should be tested under the operating conditions.

Q. Why is the DC current (I_{CC}) very large when I measure the SINAD on SA626?
A. Check the power supplies. Make sure both +5V and -5V are connected all the time even though only +5V is needed for SA626.

Q. Is it possible that SINAD is good, but BER is not good?
A. Yes, because there are other factors affecting BER .

Q. Is it possible that SINAD is bad, but BER is good?
A. No. Good SINAD is a necessary condition to achieve good BER.

Q. What are the main factors affecting BER?
A. They are:
1. Tx LPF
2. FM deviation and RF signal level
3. RF part sensitivity
4. Rx LPF
5. Threshold detector
6. Sampling time

Q. There are two "Rx Data Output" ports. Which one should be used?
A. Two "Rx Data Output" ports are designed to provide convenience for different measurement conditions. Either one can be used if the BER analyzer has the $Q/\overline{Q}$ detection capability.

Q. What needs to be done for higher RF frequency applications?
A. First, RF and LO input matching circuits have to be redesigned at the desired frequency. Second, the layout of RF and LO input circuits might also need to be re-designed. The inputs should be

further away from each other and in different directions (not in parallel with each other) to provide better isolation.

REFERENCES:

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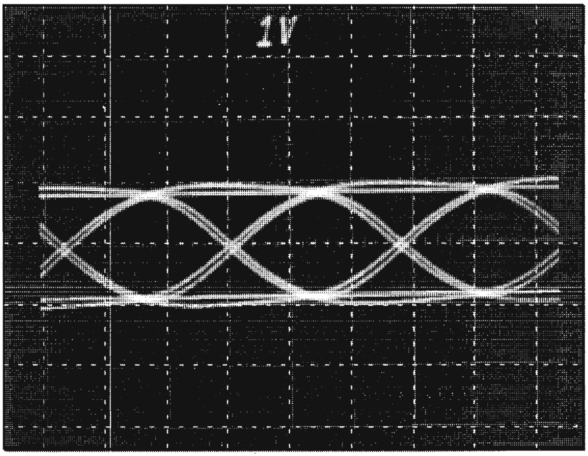


Figure 8. Baseband Eye-Diagram at the Output of Tx Gaussian LPF

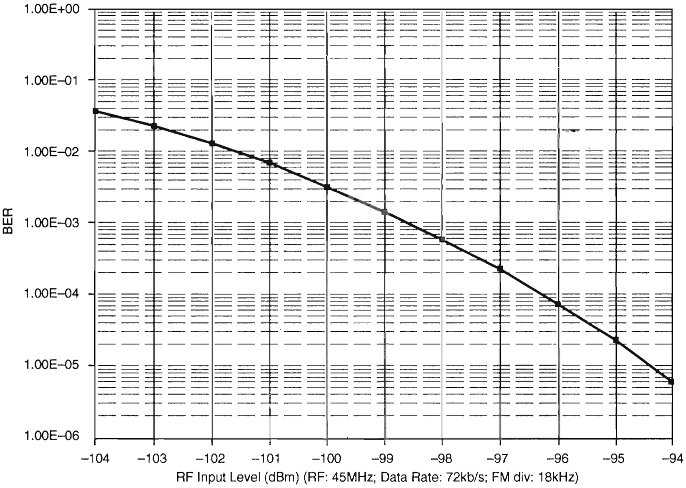


Figure 9. BER of the GMSK/GFSK Demoboard

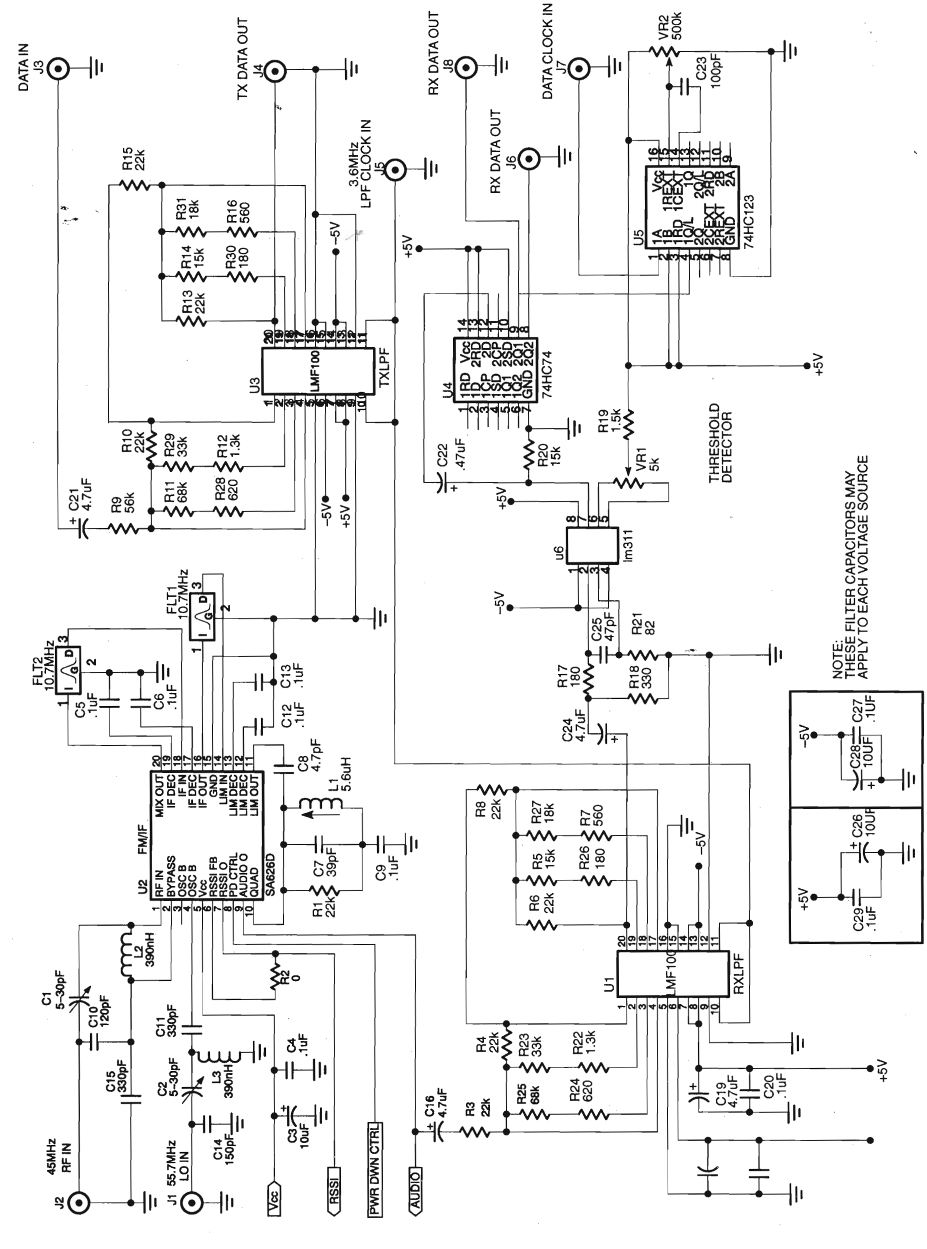


Figure 10. Circuit Diagram of the GMSK/GFSK Demoboard

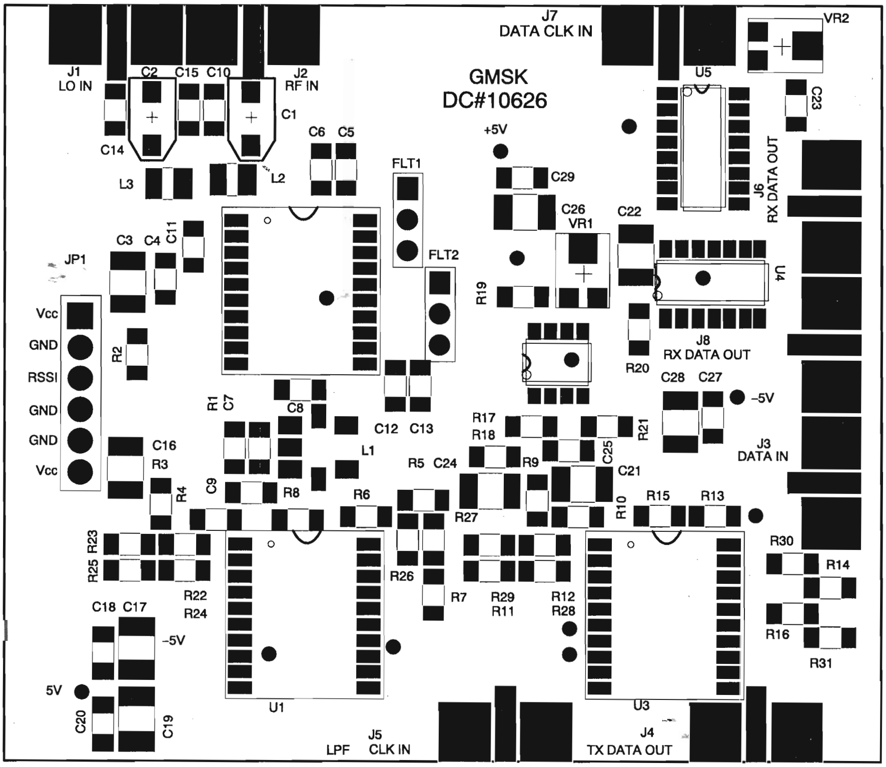
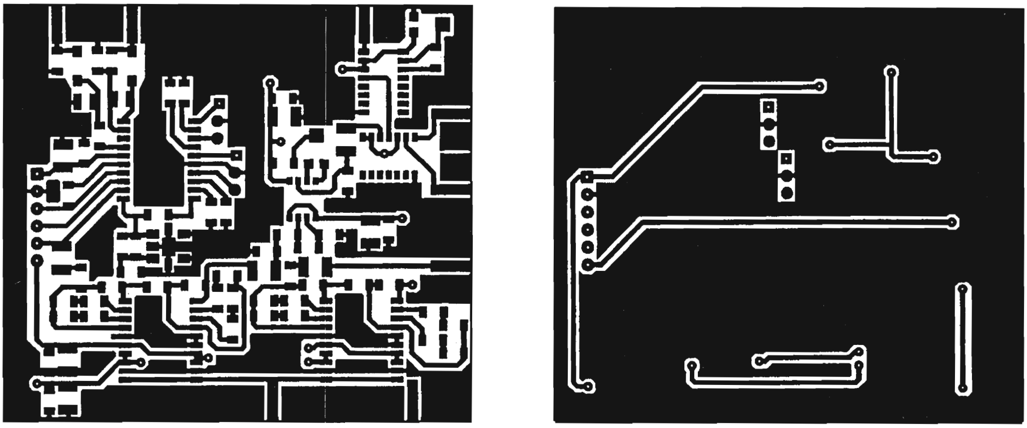


Figure 11. GMSK/GFSK Demoboard Components Layout


TOP VIEW

BOTTOM VIEW

Figure 12. GMSK/GFSK Demoboard Layout

Table 3. Customer Application Component List for GMSK/GFSK Demoboard

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	4.7pF	50V	C8	Cap. cer. 1206 NPO ±0.25pF	Garrett	Rohm	MCH315A4R7CK
1	39pF	50V	C7	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A390JK
1	47pF	50V	C25	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A470JK
1	100pF	50V	C23	Cer. chip cap 1206 NPO ±5%	Garrett	Philips	1206CG101J9BB0
1	120pF	50V	C10	Cer. chip cap 1206 NPO ±5%	Garrett	Philips	1206CG121J9BB0
1	150pF	50V	C14	Cer. chip cap 1206 NPO ±5%	Garrett	Philips	1206CG151J9BB0
2	330pF	50V	C11, C15	Cer. chip cap 1206 NPO ±5%	Garrett	Philips	1206CG331J9BB0
8	0.1μF	50V	C4, C5, C6, C9, C12, C13, C18, C20	Cer. chip cap 1206 X7R ±10%	Garrett	Philips	1206R104K9BB0
1	0.47μF	35V	C22	Tant. chip cap B 3528 ±10%	Garrett	Philips	49MC474B035KOAS
3	4.7μF	10V	C16, C21, C24	Tant. chip cap B 3528 ±10%	Garrett	Philips	49MC475B010KOAS
3	10μF	10V	C3, C17, C19	Tant. chip cap B 3528 ±10%	Jaco	AVX	TAJB106K016R
	Option		C26, C27, C28, C29				
Surface Mount Variable Capacitors							
2	5-30pF		C1, C2	Trimmer capacitor	Kent Elect	Kyocera	CTZ3S-30C-W1
Surface Mount Resistors							
1	0Ω		R2	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW000E
1	82Ω		R21	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW820E
3	180Ω		R17, R26, R30	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW181E
1	330Ω		R18	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW331E
2	560Ω		R7, R16	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW561E
2	620Ω		R24, R28	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW621E
2	1.3kΩ		R12, R22	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW132E
1	1.5kΩ		R19	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW152E
3	15kΩ		R5, R14, R20	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW153E
2	18kΩ		R27, R31	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW183E
1	20kΩ		R1	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW203E
7	22kΩ		R3, R4, R6, R8, R10, R13, R15	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW223E
2	33kΩ		R23, R29	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW333E
1	56kΩ		R9	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW563E
1	68kΩ		R11, R25	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW683E
Surface Mount Variable Resistors							
1	5kΩ		VR1	SM RES TRIM, 1 TRN ±20% J-H	Garrett	Philips	ST-4TA502
1	500kΩ		VR2	SM RES TRIM, 1 TRN ±20% J-H	Garrett	Philips	ST-4TA504
Surface Mount Inductors							
2	0.39μH		L2, L3	Chip Inductors-1800CS series	Coilcraft	Coilcraft	1800CS-391
Surface Mount Variable Inductors							
1	5.6μH		L1	Adjustable SM Inductor 5CCD type	Digikey	TOKO	TKS2251
Filters							
2	10.7MHz		FLT1, FLT2	10.7MHz IF filter 110kHz±30kHz	Murata	Murata	SFE10.7MHY-A
Surface Mount Integrated Circuits							
2			U1, U3	Switched capacitor filter	Hamilton	National	LMF100CIWM
1			U2	Low voltage mixer FM IF high RSSI	Philips	Philips	SA626D
1			U4	Dual D-type flip-flop	Philips	Philips	74HC74
1			U5	Dual re-triggerable monostable	Philips	Philips	74HC123
1			U6	Voltage comparator	Philips	Philips	LM311
Miscellaneous							
8			J1, J2, J3, J4, J5, J6, J7, J8	SMA gold connector	Newark	EF Johnson	142-0701-801
1			JP1	6-pins header straight	Mouser	Molex-Waldem	538-22-05-2061
1				Printed circuit board	Philips	Philips	GMSK/DC#10626
78 Total Parts							

High performance low power mixer FM IF system with high-speed RSSI

NE/SA627

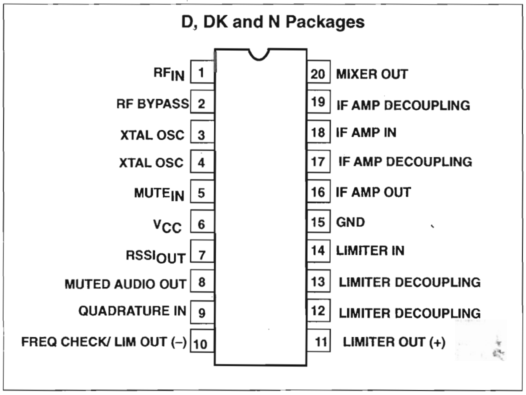
DESCRIPTION

The NE/SA627 has faster RSSI rise and fall times. The NE/SA627 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI) with fast rise and fall time, voltage regulator and frequency check/limiter out (–). The NE/SA627 also has an extra limiter output. This signal is buffered from the output of the limiter and provides a negative (–) limiter output. This can be used to provide a frequency check function. The NE/SA627 is available in 20-lead dual-in-line plastic and 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

FEATURES

- Fast RSSI rise and fall times
- Low power consumption: 5.8mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Audio output - mutable
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22µV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA627 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION



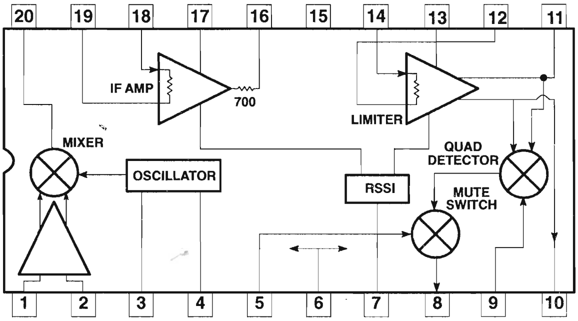
APPLICATIONS

- Digital cellular base stations
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification
- Digital cordless telephones

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE627N	0408B
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	0 to +70°C	NE627D	0172D
20-Pin Plastic SSOP (Surface-mount)	0 to +70°C	NE627DK	1563
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA627N	0408B
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA627D	0172D
20-Pin Plastic Shrink Small Outline Package (SSOP) (Surface-mount)	-40 to +85°C	SA627DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		9	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range	NE627	0 to +70	°C
		SA627	-40 to +85	°C
θ_{JA}	Thermal impedance	D package	90	°C/W
		N package	75	°C/W
		DK package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE627			SA627			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		5.1	5.8	6.7	4.55	5.8	6.75	mA
	Mute switch input threshold (ON)		1.7			1.7			V
	(OFF)				1.0			1.0	V

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = +6V$, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE627			SA627			
			MIN	TYP	MAX	MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)									
f_{IN}	Input signal frequency			500			500		MHz
f_{OSC}	Crystal oscillator frequency			150			150		MHz
	Noise figure at 45MHz			5.0			5.0		dB
	Third-order input intercept point	f1 = 45.0; f2 = 45.06MHz		-10			-10		dBm
	Conversion power gain	Matched 14.5dBV step-up	10.5	13	14.5	10	13	15	dB
		50Ω source		-1.7			-1.7		dB
	RF input resistance	Single-ended input	3.5	4.7		3.0	4.7		kΩ
	RF input capacitance			3.5	4.0		3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.3	1.5		1.25	1.5		kΩ
IF section									
	IF amp gain	50Ω source		39.7			39.7		dB
	Limiter gain	50Ω source		62.5			62.5		dB
	Input limiting -3dB, $R_{17} = 5.1k$	Test at Pin 18		-113			-113		dBm
	AM rejection	80% AM 1kHz	30	34	42	29	34	43	dB
	Audio level, $R_{10} = 100k$	15nF de-emphasis	110	150	250	80	150	260	mV_{RMS}
	SINAD sensitivity	RF level -118dB		16			16		dB
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	IF RSSI output, $R_9 = 100kΩ$[1]	IF level = -118dBm	0	160	550	0	160	650	mV
		IF level = -68dBm	2.0	2.5	3.0	1.9	2.5	3.1	V
		IF level = -18dBm	4.1	4.8	5.5	4.0	4.8	5.6	V
	IF RSSI output rise time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz							
		RF level = -56dBm		1.2			1.2		μs
		RF level = -28dBm		1.2			1.2		μs
		IF frequency = 10.7MHz							
		RF level = -56dBm		1.2			1.2		μs
		RF level = -28dBm		1.1			1.1		μs
	IF RSSI output fall time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz							
		RF level = -56dBm		2.1			2.1		μs
		RF level = -28dBm		7.6			7.6		μs
		IF frequency = 10.7MHz							
		RF level = -56dBm		2.0			2.0		μs
		RF level = -28dBm		7.3			7.3		μs
	RSSI range	$R_9 = 100kΩ$ Pin 16		90			90		dB
	RSSI accuracy	$R_9 = 100kΩ$ Pin 16		±1.5			±1.5		dB
	IF input impedance		1.40	1.6		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.40	1.6		1.40	1.6		kΩ
	Limiter output impedance	Pin 10 or 11		300			300		Ω
	Limiter output level	Pin 10 or 11 with no load 3kΩ load (min)		280 250			280 250		mV_{RMS}

AC ELECTRICAL CHARACTERISTICS(Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE627			SA627			
			MIN	TYP	MAX	MIN	TYP	MAX	
IF section (continued)									
	Muted audio output resistance			58			58		kΩ
RF/IF section (int LO)									
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3			4.3		V

NOTE:

1. The generator source impedance is 50Ω, but the NE/SA627 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA627 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA627 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

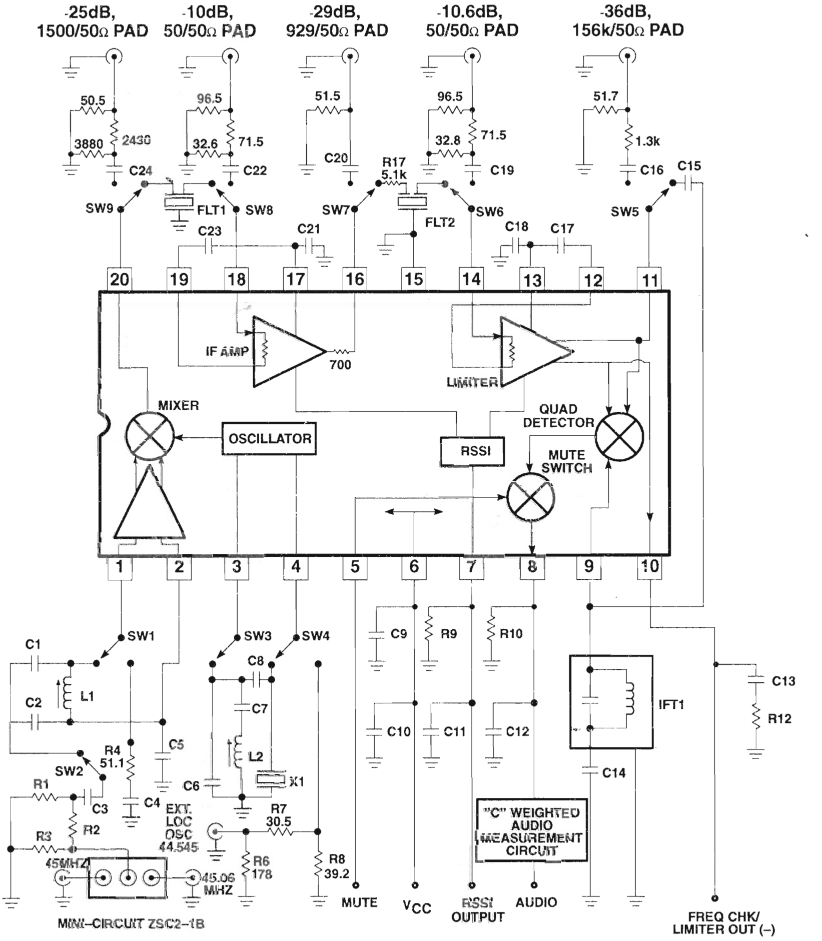
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

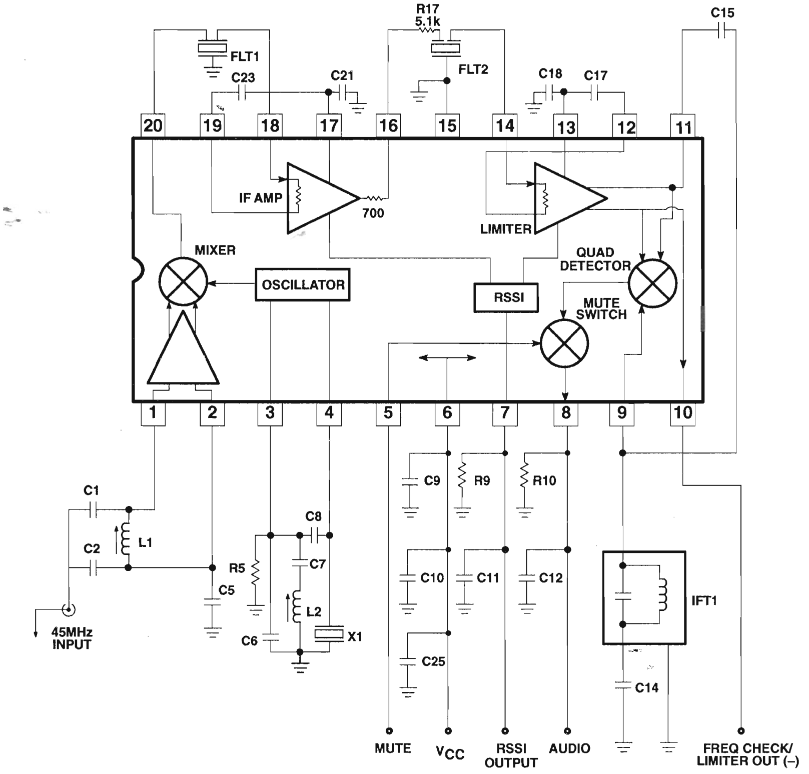


Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum)
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	0.1μF ±10% Monolithic Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8μH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)
R12	3kΩ ±5% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. NE/SA627 45MHz Test Circuit (Relays as shown)



Application Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10µF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8µH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R5	Not Used in Application Board (see Note 8)
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

Figure 2. NE/SA627 45MHz Application Circuit

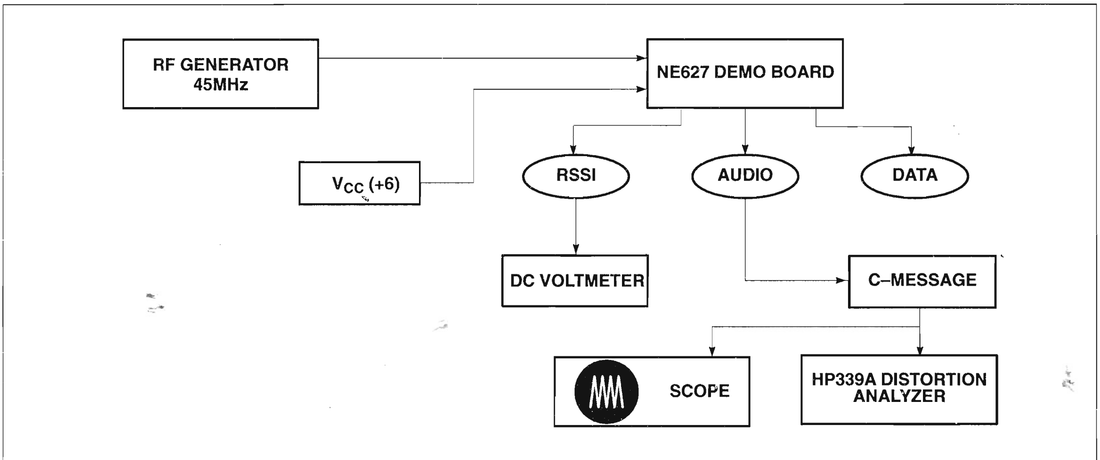


Figure 3. NE/SA627 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22μV or -120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

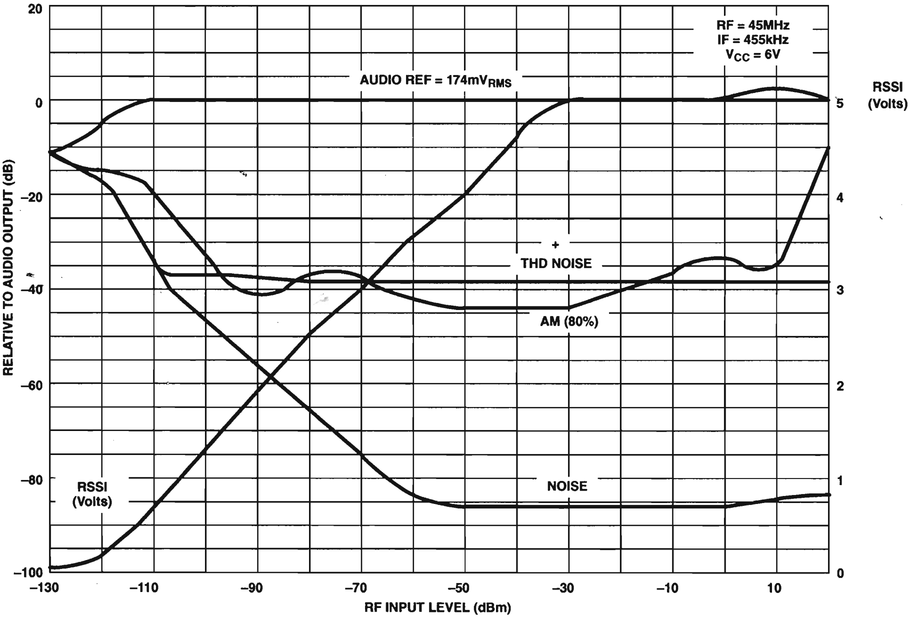


Figure 4. NE627 Application Board at 25°C

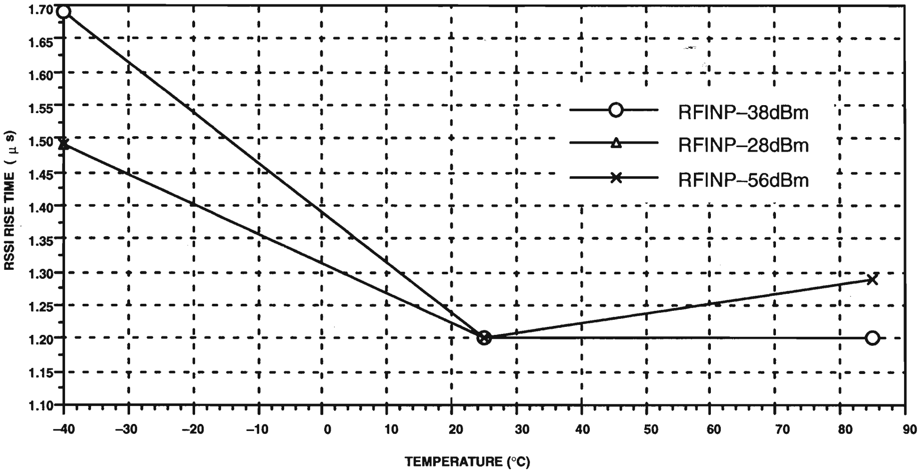


Figure 5. NE/SA627 Rise Time 455kHz IF Frequency

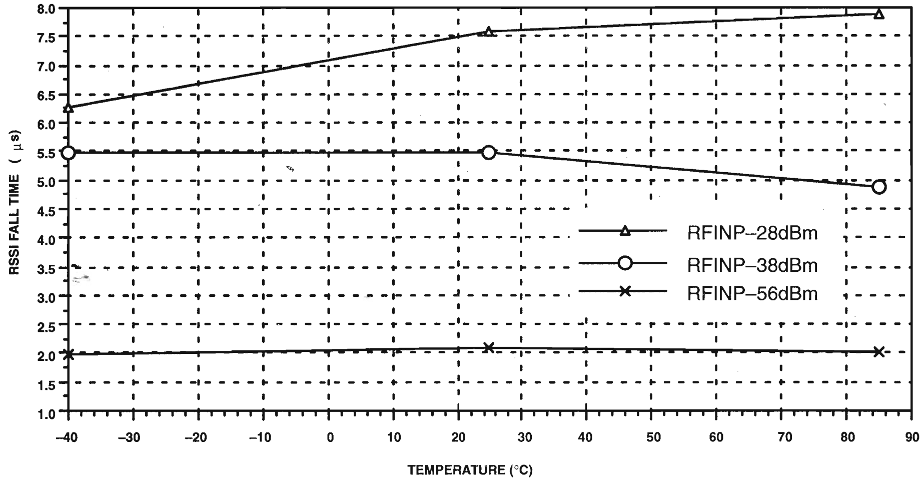


Figure 6. NE/SA627 Fall Time 455kHz IF Frequency

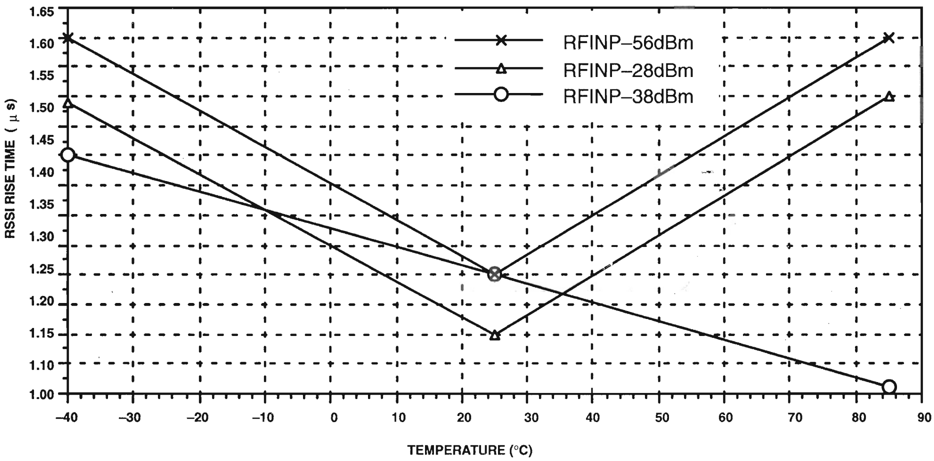


Figure 7. NE/SA627 Rise Time 10.7MHz IF Frequency

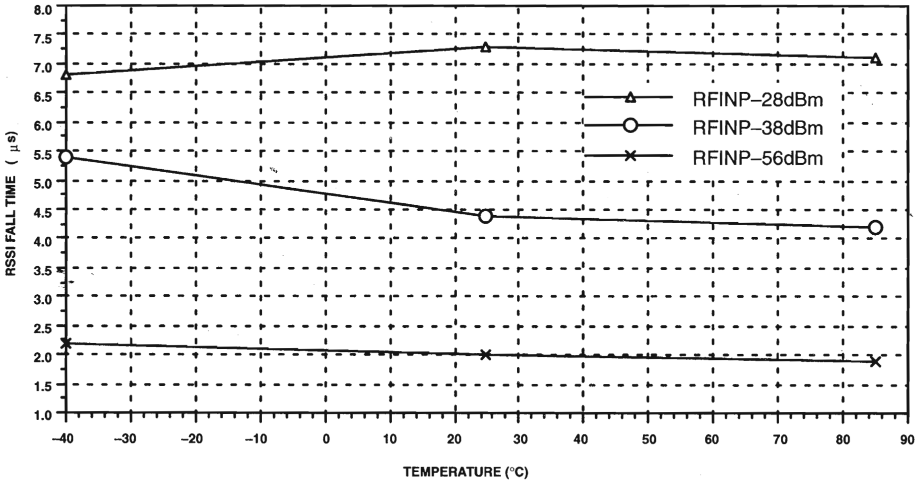


Figure 8. NE/SA627 Fall Time 10.7MHz IF Frequency

Low voltage high performance mixer FM IF system with high-speed RSSI

SA636

DESCRIPTION

The SA636 is a low-voltage high performance monolithic FM IF system with high-speed RSSI incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator, wideband data output and fast RSSI op amps. The SA636 is available in 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink small outline package).

The SA636 was designed for high bandwidth portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The data output has a minimum bandwidth of 600kHz. This is designed to demodulate wideband data. The RSSI output is amplified. The RSSI output has access to the feedback pin. This enables the designer to adjust the level of the outputs or add filtering.

SA636 incorporates a power down mode which powers down the device when Pin 8 is low. Power down logic levels are CMOS and TTL compatible with high input impedance.

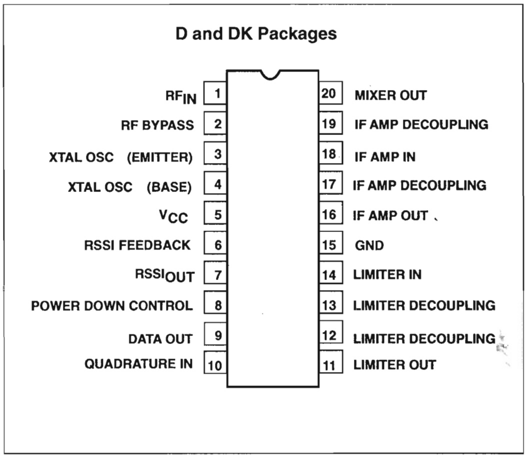
APPLICATIONS

- DECT (Digital European Cordless Telephone)
- Digital cordless telephones
- Digital cellular telephones
- Portable high performance communications receivers
- Single conversion VHF/UHF receivers
- FSK and ASK data receivers
- Wireless LANs

FEATURES

- Wideband data output (600kHz min.)
- Fast RSSI rise and fall times
- Low power consumption: 6.5mA typ at 3V
- Mixer input to >500MHz
- Mixer conversion power gain of 11dB at 240MHz
- Mixer noise figure of 12dB at 240MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 92dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.54µV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 240MHz and IF at 10.7MHz
- ESD hardened
- 10.7MHz filter matching (330Ω)
- Power down mode (I_{CC} = 200µA)

PIN CONFIGURATION


D and DK Packages

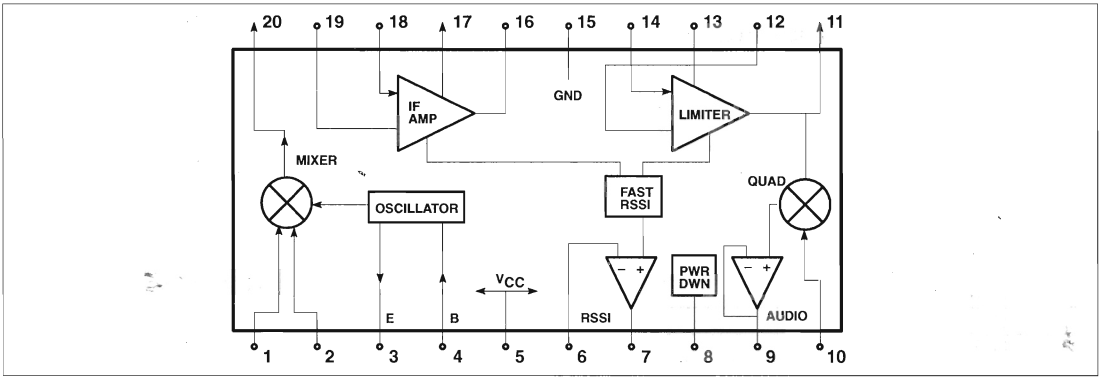
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) package (Surface-mount)	-40 to +85°C	SA636D	0172D
20-Pin Plastic Shrink Small Outline Package (Surface-mount)	-40 to +85°C	SA636DK	1563–

Low voltage high performance mixer FM IF system with high-speed RSSI

SA636

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	0.3 to 7	V
V_{IN}	Voltage applied to any other pin	–0.3 to (V_{CC}+0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA636	–40 to +85	°C

NOTE: θ_{JA}, Thermal impedance

D package	90°C/W
DK package	117°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

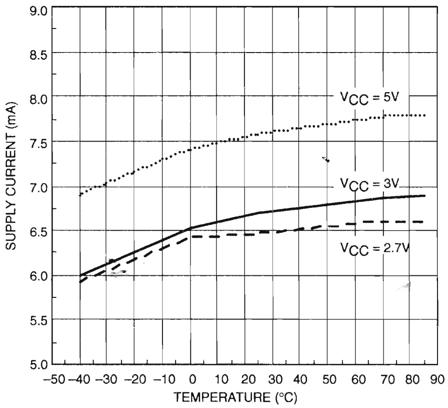
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA636			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7	3.0	5.5	V
I_{CC}	DC current drain	Pin 8 = HIGH	5.5	6.5	7.5	mA
	Input current	Pin 8 LOW	–10		10	µA
		Pin 8 HIGH	–10		10	
	Input level	Pin 8 LOW	0		$0.3V_{CC}$	V
		Pin 8 HIGH	$0.7V_{CC}$		V_{CC}	
I_{CC}	Standby	Pin 8 = LOW		0.2	0.5	mA
t_{ON}	Power up time	RSSI valid (10% to 90%)		10		µs
t_{OFF}	Power down time	RSSI invalid (90% to 10%)		5		µs

AC ELECTRICAL CHARACTERISTICS

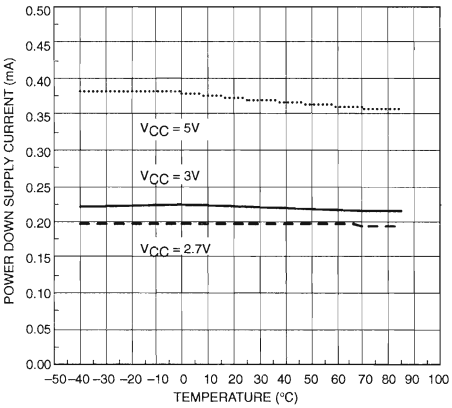
$T_A = 25°C$; $V_{CC} = +3V$, unless otherwise stated. RF frequency = 240.05MHz + 14.5dBV RF input step-up; IF frequency = 10.7MHz; RF level = -45dBm; FM modulation = 1kHz with ±125kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA636			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 160mV$_{RMS}$)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	External oscillator (buffer)			500		MHz
	Noise figure at 240MHz			12		dB
	Third-order input intercept point	Matched f1=240.05; f2=240.35MHz		-16		dBm
	Conversion power gain	Matched 14.5dBV step-up	8	11	14	dB
	RF input resistance	Single-ended input		700		Ω
	RF input capacitance			3.5		pF
	Mixer output resistance	(Pin 20)		330		Ω
IF section						
	IF amp gain	330Ω load		38		dB
	Limiter gain	330Ω load		54		dB
	Input limiting -3dB	Test at Pin 18		–105		dBm
	AM rejection	80% AM 1kHz		50		dB
	Data level	R_{LOAD} = 100kΩ	100	130		mV_{RMS}
	3dB data bandwidth		600	700		kHz
	SINAD sensitivity	RF level = -111dBm		16		dB
THD	Total harmonic distortion			-43	-38	dB
S/N	Signal-to-noise ratio	No modulation for noise		60		dB
	IF RSSI output with buffer	IF level = -118dBm		0.2	0.5	V
		IF level = -68dBm	0.3	0.6	1.0	V
		IF level = -10dBm	0.9	1.3	1.8	V
	IF RSSI output rise time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		1.2		μs
	(no RSSI bypass capacitor)	RF level = -28dBm		1.1		μs
	IF RSSI output fall time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		2.0		μs
	(no RSSI bypass capacitor)	RF level = -28dBm		7.3		μs
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance			330		Ω
	IF output impedance			330		Ω
	Limiter input impedance			330		Ω
	Limiter output impedance			300		Ω
	Limiter output level with no load			130		mV_{RMS}
RF/IF section (int LO)						
	System RSSI output	RF level = -10dBm		1.4		V
	System SINAD	RF level = -106dBm		12		dB

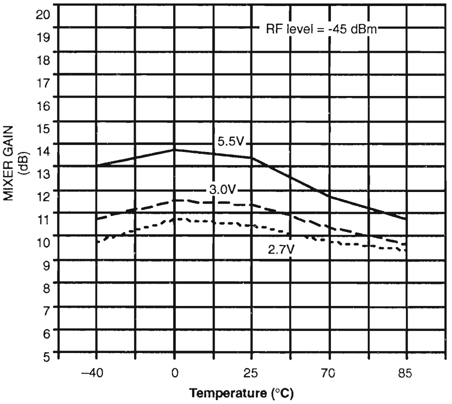
PERFORMANCE CHARACTERISTICS



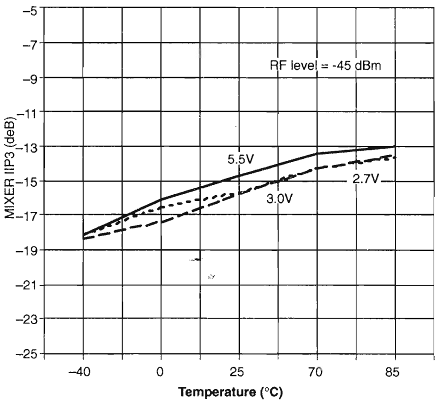
Supply Current vs Temperature and Supply Voltage



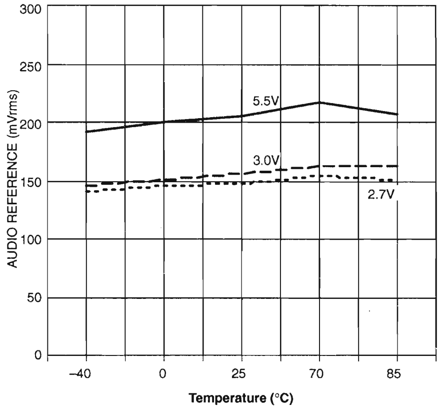
Power Down Supply Current vs Temperature and Supply Voltage



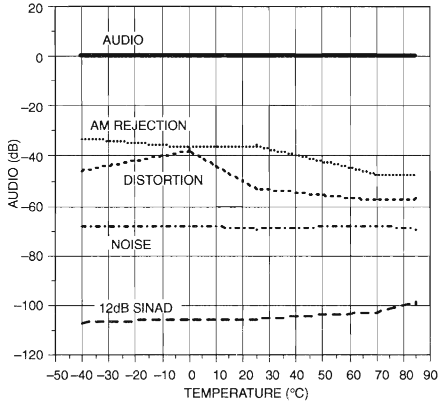
Mixer Power Gain vs Temperature and Supply Voltage



Mixer IIP3 at 240MHz vs Temperature and Supply Voltage

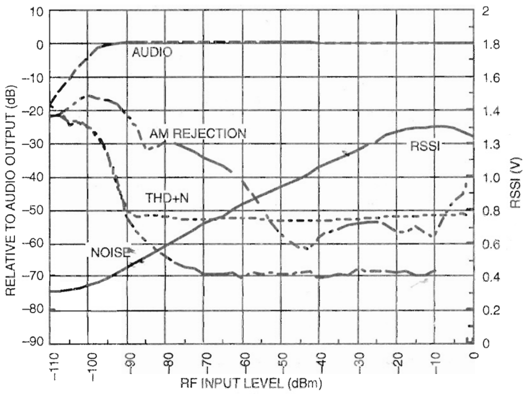


Audio Reference Level vs Temperature and Supply Voltage

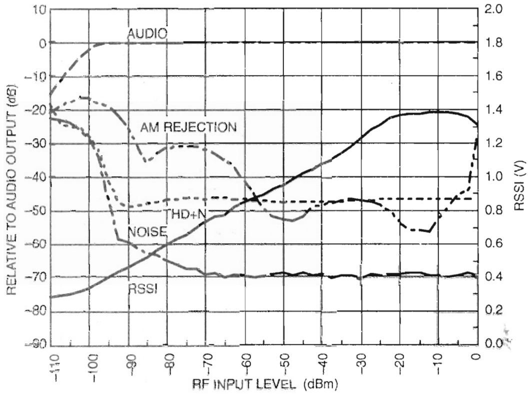


12dB SINAD and Relative Audio, THD, Noise
and AM Rejection for VCC = 3V vs Temperature
RF = 240MHz, Level = −68dBm, Deviation = 125kHz

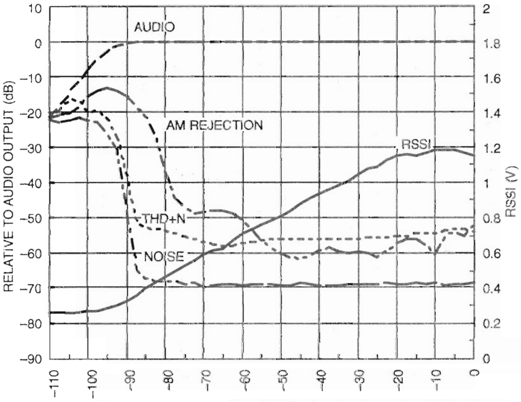
PERFORMANCE CHARACTERISTICS (continued)



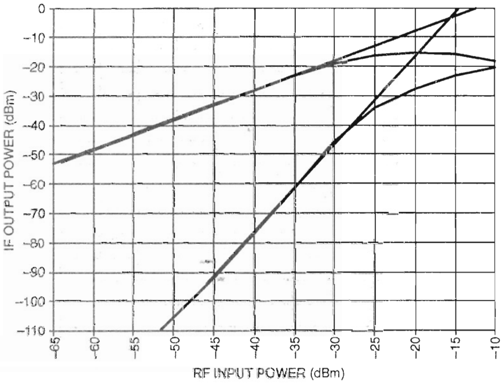
Receiver RF Performance — T = 25°C, Audio Level = 129mV$_{RMS}$



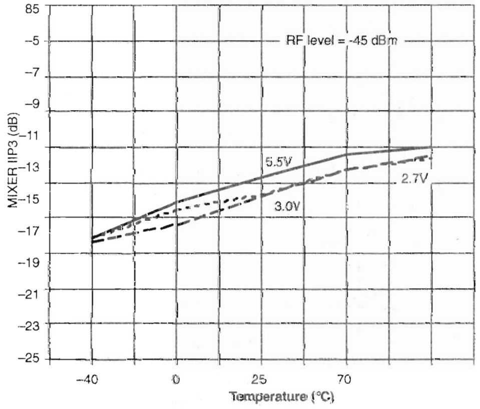
Receiver RF Performance — T = –40°C, Audio Level = 118mV$_{RMS}$



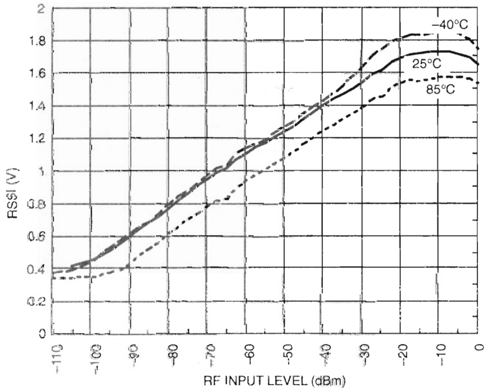
Receiver RF Performance – T = 85°C, Audio Level = 131mV$_{RMS}$



Mixer Third Order Intercept and Compression

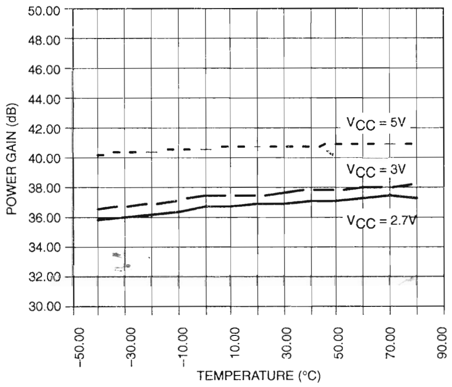


Mixer IIP3 at 240MHz. vs Temperature and Supply Voltage

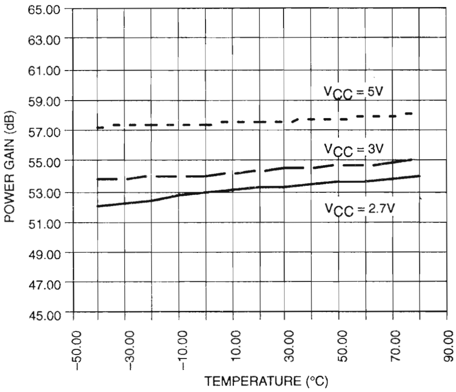


RSSI vs RF Input Level and Temperature

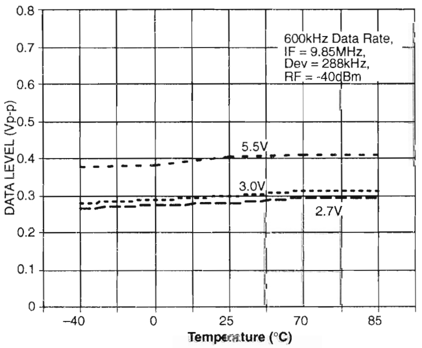
PERFORMANCE CHARACTERISTICS (continued)



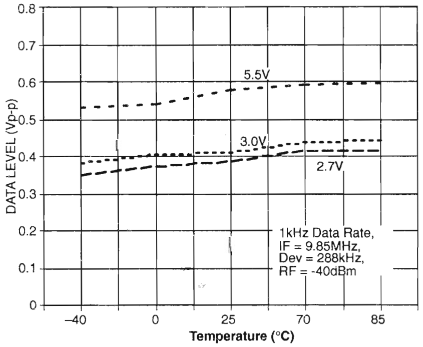
SA626 IF Amplifier Gain vs Temperature vs Supply Voltage



SA626 Limiting Amplifier Gain vs Temperature vs Supply Voltage

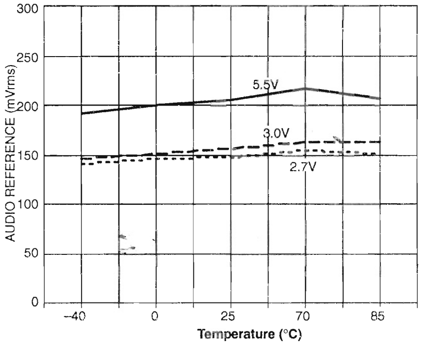


Data Level vs Temperature and Supply Voltage

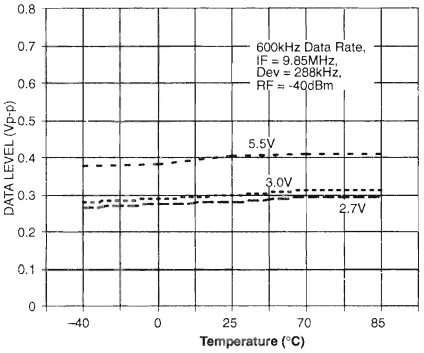


Data Level vs Temperature and Supply Voltage

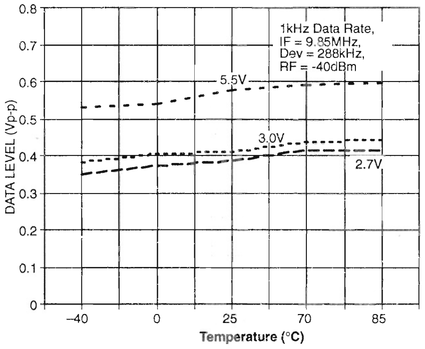
PERFORMANCE CHARACTERISTICS (continued)



Audio Reference Level vs Temperature and Supply Voltage

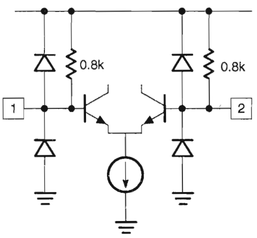
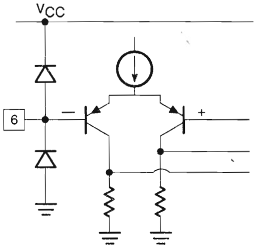
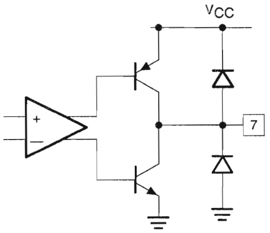
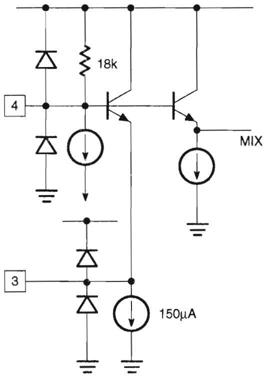
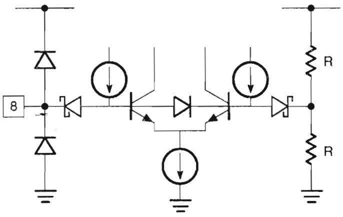
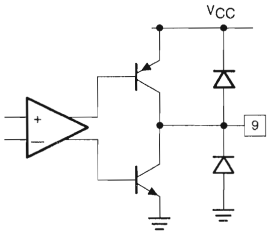
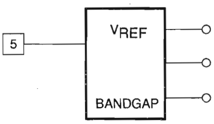
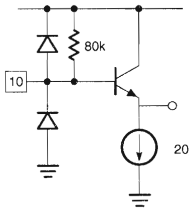


Data Level vs Temperature and Supply Voltage

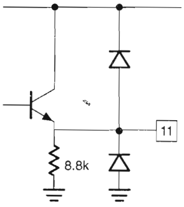
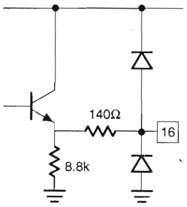
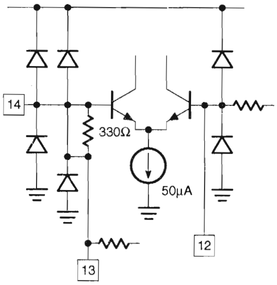
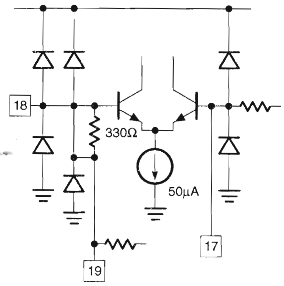
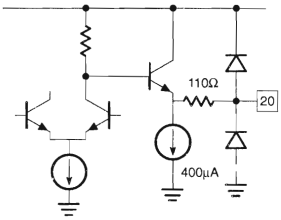


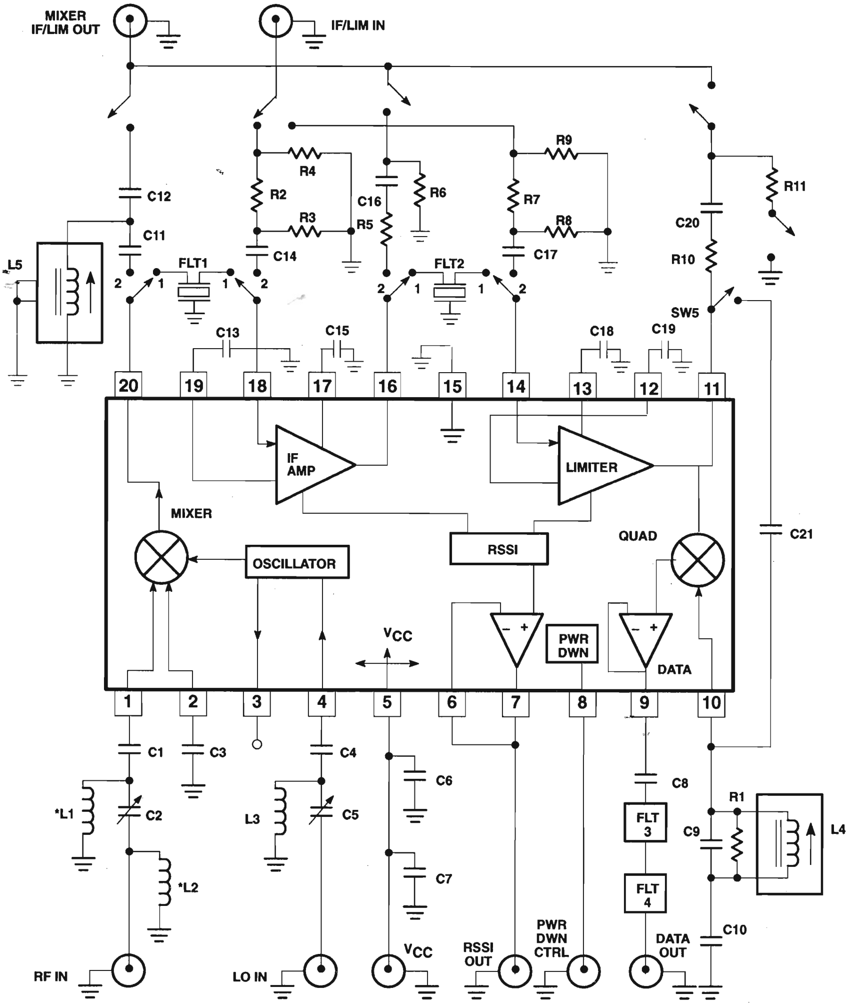
Data Level vs Temperature and Supply Voltage

PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	RF IN	+1.07		6	RSSI FEEDBACK	+0.20	
2	RF BYPASS	+1.07		7	RSSI OUT	+0.20	
3	XTAL OSC	+1.57		8	POWER DOWN	+2.75	
4	XTAL OSC	+2.32		9	DATA OUT	+1.09	
5	V_{CC}	+3.00		10	QUAD. IN	+3.00	

PIN FUNCTIONS (continued)

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
11	LIMITER OUT	+1.35		16	IF AMP OUT	+1.22	
12	LIMITER DECOUP	+1.23		17	IF AMP DECOUP	+1.22	
13	LIMITER COUPLING	+1.23		18	IF AMP IN	+1.22	
14	LIMITER IN	+1.23		19	IF AMP DECOUP	+1.22	
15	GND	0		20	MIXER OUT	+1.03	



Automatic Test Circuit Component List

R1	8.2kΩ select	C1	0.1µF	C12	160pF select	L1	150nH select for input match
R2	6.42kΩ	C2	1–5pF select for input match	C13	1000pF	L2	22nH select for input match
R3	347.8Ω	C3	0.1µF	C14	0.1µF	L3	47nH select for input match
R4	49.9Ω	C4	0.1µF	C15	1000pF	L4	5.6µH select for input match
R5	1kΩ	C5	1–5pF select for input match	C16	0.1µF	L5	1.27–2.25µH select for mixer output match
R6	49.9Ω	C6	100pF	C17	0.1µF		
R7	6.42kΩ	*C7	6.8µF 10V	C18	1000pF	FLT1	10.7MHz (Murata SFE10.7MA5-A)
R8	347.8Ω	C8	1µF	C19	1000pF	FLT2	10.7MHz (Murata SFE10.7MA5-A)
R9	49.9Ω	C9	39pF select	C20	0.1µF	FLT3	"C" message weighted
R10	1kΩ	C10	0.1µF	C21	1pF	FLT4	Active de-emphasis
R11	49.9Ω	C11	0.1µF				

*NOTE: This value can be reduced when a battery is the power source.

Figure 9. SA636 240.05MHz (RF) / 10.7MHz (IF) Test Circuit

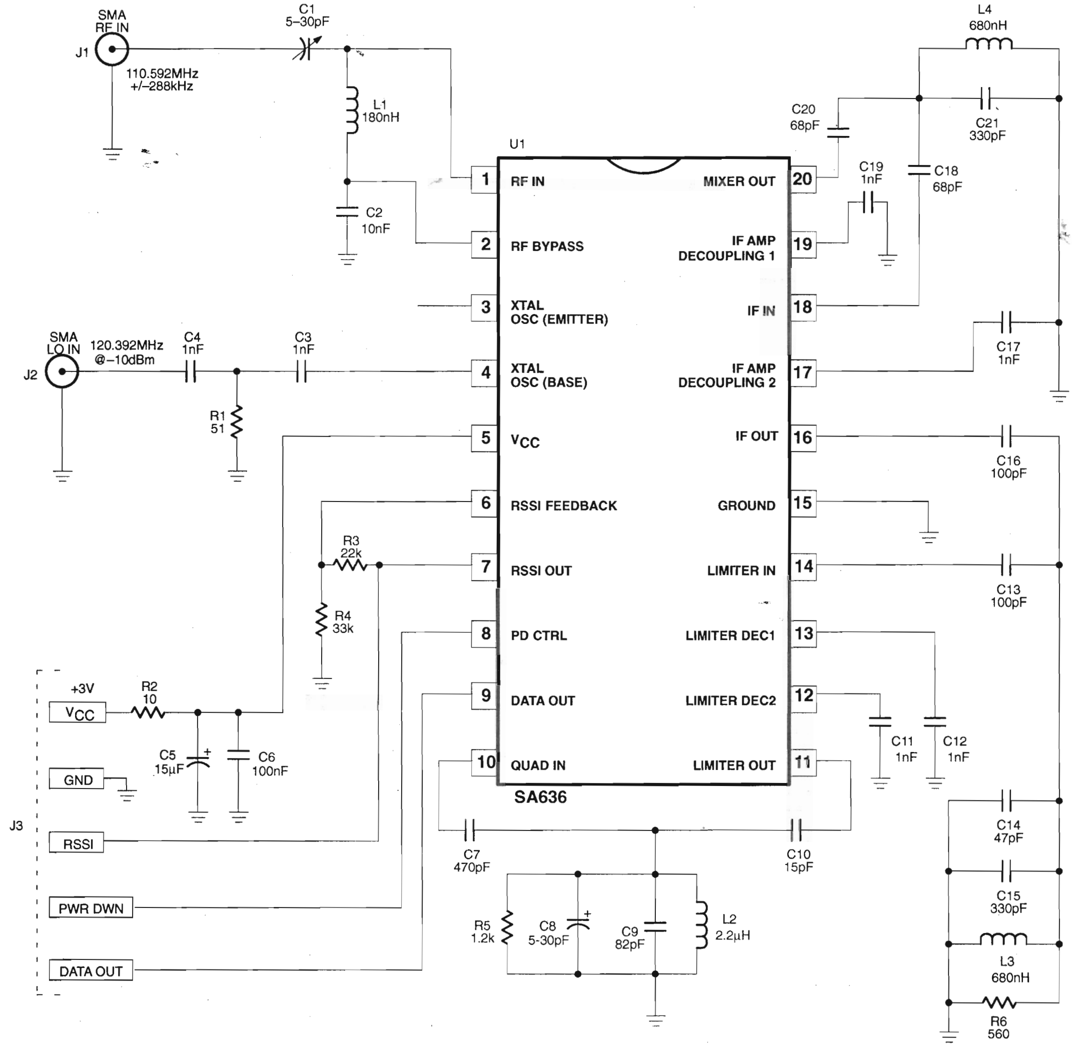


Figure 10. SA636 110.592MHz (RF) / 9.8MHz (IF) DECT Application Circuit

Table 1. DECT Application Circuit Electrical Characteristics

RF frequency = 110.592MHz; IF frequency = 9.8MHz; RF level = -45dBm; FM modulation = 100kHz with ±288kHz peak deviation.

SYMBOL	PARAMETER	TEST CONDITIONS	TYPICAL	UNITS
Mixer/Osc section (ext LO = 160mV$_{RMS}$)				
PG	Conversion power gain		13	dB
NF	Noise Figure at 110MHz		12	dB
IIP3	Third order input intercept	Matched f1 = 110.592; f2 = 110.892MHz	-15	dBm
R_{IN}	RF input resistance		690	Ω
C_{IN}	RF input capacitance		3.6	pF
IF section				
	IF amp gain	330Ω load	38	dB
	Limiter amp gain	330Ω load	54	dB
	Data level	R_{LOAD} = 3kΩ	130	mV$_{RMS}$
	3dB data bandwidth		700	kHz
RF/IF section (internal LO)				
	System RSSI output	RF level = -10dBm	1.4	V
	System S/N[1]	RF level = -83dBm	10	dB

NOTE:

1. 10dB S/N corresponds to BER = 10^{-3}.

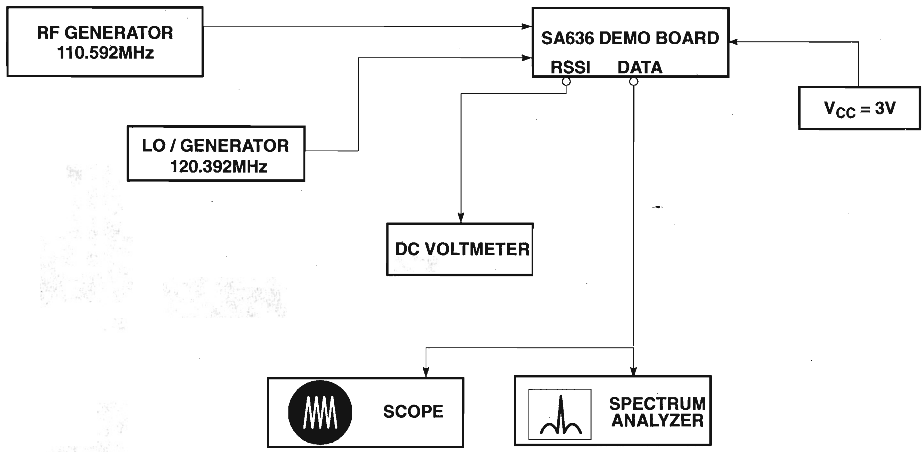
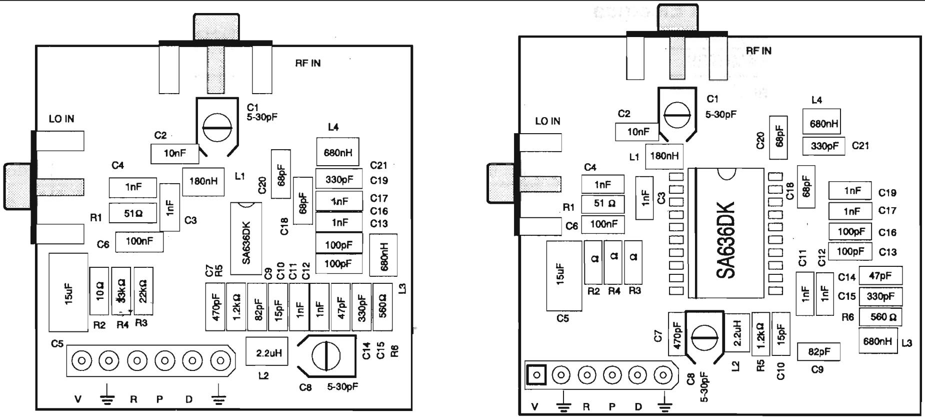


Figure 11. SA636 Application Circuit Test Set Up

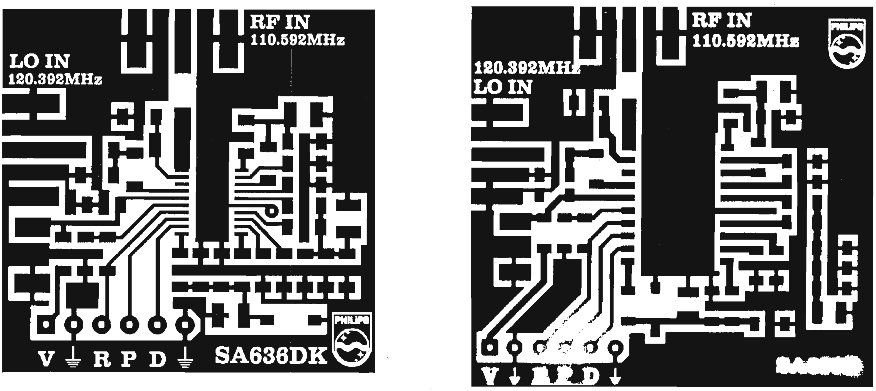
NOTES:

1. RF generator: Set your RF generator at 110.592MHz, use a 100kHz modulation frequency and a ±288kHz deviation.
2. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
3. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
4. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 0.1µF bypass capacitor on the supply pin improves sensitivity.



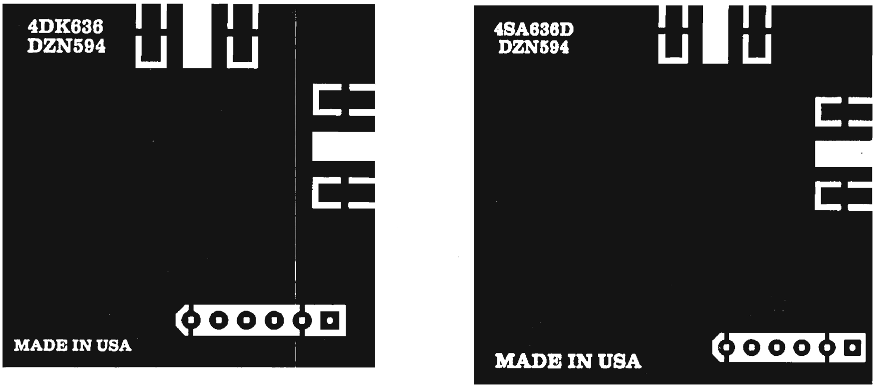
TOP SILK SCREEN (SSOP)

TOP SILK SCREEN (SOL)



TOP VIEW (SSOP)

TOP VIEW (SOL)



BOTTOM VIEW (SSOP)

BOTTOM VIEW (SOL)

Figure 12. SA636 Demoboard Layout (Not Actual Size)

CIRCUIT DESCRIPTION

The SA636 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 38dB of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 54dB of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 10.7MHz, 330Ω source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types, such as cordless and cellular hand-held phones.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 14dB, conversion gain of 11dB, and input third-order intercept of -16dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 330Ω resistor permitting direct connection to a 10.7MHz ceramic filter for narrowband applications. The input resistance of the limiting IF amplifiers is also 330Ω. With most 10.7MHz ceramic filters and many crystal filters, no impedance matching network is necessary. For applications requiring wideband IF filtering, such as DECT, external LC filters are used (see Figure 10). To achieve optimum linearity of the log signal strength indicator, there must be a 6dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 6dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequency at 10.7MHz. Special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output (DATA) of the quadrature is a voltage output. This output is designed to handle a minimum bandwidth of 600kHz. This is designed to demodulate wideband data, such as in DECT applications.

A Receive Signal Strength Indicator (RSSI) completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPS or TACS cellular telephone, DECT and RCR-28 cordless telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

Low-voltage digital IF receiver SA637

DESCRIPTION

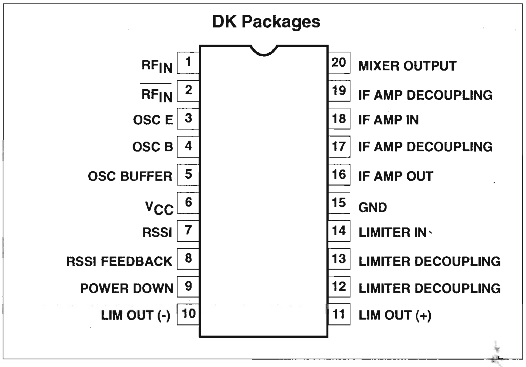
The SA637 is a low-voltage high performance monolithic digital system with high-speed RSSI incorporating a mixer, oscillator with buffered output, two limiting intermediate frequency amplifiers, fast logarithmic received signal strength indicator (RSSI), voltage regulator, RSSI op amp and power down pin. The SA637 is available in SSOP (shrink small outline package).

The SA637 was designed for portable digital communication applications and will function down to 2.7V. The limiter amplifier has differential outputs with 2MHz small signal bandwidth. The RSSI output has access to the feedback pin. This enables the designer to level adjust the outputs or add filtering.

FEATURES

- V_{CC} = 2.7 to 5.5V
- Low power receiver (3.8mA @ 3V)
- Power down mode (I_{CC} = 110µA)
- Fast RSSI rise and fall times
- Extended RSSI range with temperature compensation
- RSSI op amp
- 2MHz limiter small signal bandwidth
- 455kHz filter matching (1.5kΩ)
- Differential limiter output
- Oscillator buffer
- SSOP-20 package

PIN CONFIGURATION



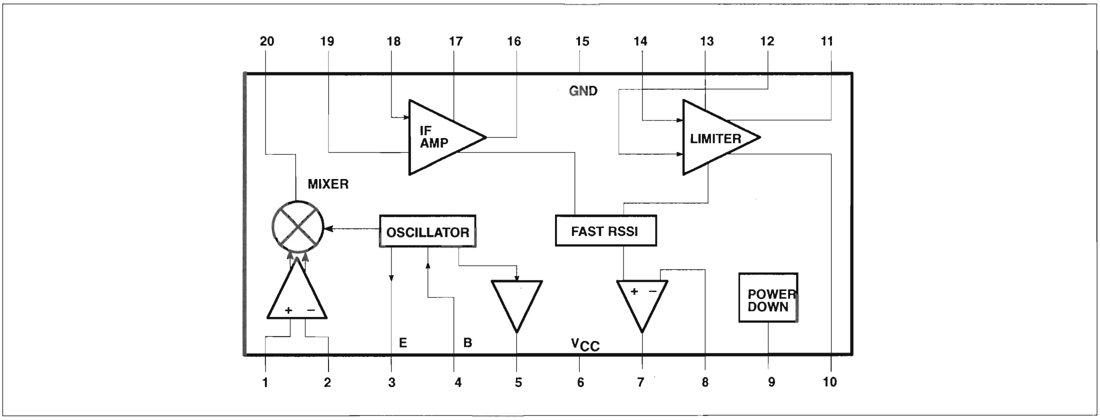
APPLICATIONS

- ADC (American Digital Cellular)
- Digital receiver systems
- Cellular radio

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (Surface-mount)	-40 to +85°C	SA637DK	1563–

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C

NOTE: Thermal impedance (θ_{JA}) = 117°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		5.5	V
I_{CC}	DC current drain	Pin 9 = HIGH or OPEN		3.8	4.5	mA
		V_{CC} = 4.7V		4.4	5.5	mA
	Standby	Pin 9 = LOW		0.11	0.5	mA
	Input current	Pin 9 = LOW	-10		10	µA
		Pin 9 = HIGH	-10		10	
	Input level	Pin 9 = LOW	0		0.3V_{CC}	µA
		Pin 9 = HIGH	0.7V_{CC}		V_{CC}	
t_{ON}	Power up time	RSSI valid (10% to 90%)		10		µs
t_{OFF}	Power down time	RSSI invalid (90% to 10%)		5		µs

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 90MHz; RF input step-up = +14.5dBV; IF frequency = 455kHz; RF level = -68dBm. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Mixer/Osc section						
f_{IN}	Input signal frequency			200		MHz
f_{OSC}	Crystal oscillator frequency			200		MHz
NF	Noise figure at 90MHz	Matched input and output		6.2		dB
TOI	Third-order input intercept point	Input matched to 50Ω source		-17		dBm
P1dB	Input 1dB compression point			-27		dBm
	Conversion power gain	Matched 50Ω		7		dB
R_{IN}	Mixer input resistance			2.5		kΩ
C_{IN}	Mixer input capacitance			2.2		pF
R_{OUT}	Mixer output resistance			1.87		kΩ
	Buffered LO output level	LO = 447mV_{P-P}, 1kΩ AC load	100	300	500	mV_{P-P}
IF section						
	IF amp power gain	50Ω source		36		dB
	Limiter power gain	50Ω source		60		dB
IF_{BW}	IF amp bandwidth			2.5		MHz

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
	RF RSSI output	RF level = -118dBm	.01	0.2	.65	V
		RF level = -68dBm	.4	0.9	1.7	V
		RF level = -28dBm	1.0	1.7	2.3	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	RSSI ripple			30		mV_{P-P}
	RSSI speed Rise time	No interstage filter		2.5		µs
		With interstage filter		22		µs
	RSSI speed Fall time	No interstage filter		10		µs
		With interstage filter		50		µs
	IF input impedance			1.5		kΩ
	IF output impedance			1.5		kΩ
	Limiter input impedance			1.5		kΩ
	Limiter output impedance	(Pin 10, Pin 11)		200		Ω
	Limiter output signal level	(Pin 10, Pin 11) 1.5kΩ AC load		280		mV_{P-P}
	Limiter output DC level			1.27		V
	Differential output matching			±6		mV
	Differential output offset			±30		mV

CIRCUIT DESCRIPTION

Mixer

The mixer has a balanced input and is capable of being driven single-ended. The input impedance is 2.5kΩ in parallel with a 2.2pF cap at 90MHz RF. The mixer output can drive a 1500Ω ceramic filter at 455kHz or 600kHz directly without any matching required. The mixer conversion power gain is 7dB when both input and output are matched and optimum LO level is used to drive the internal mixer core.

Oscillator and Buffer

The on-board oscillator supplies the signal for the mixer down-conversion. The internally biased transistor can be configured as a Colpitts or Butler overtone crystal oscillator. The transistor's bias current can be increased if desired by adding a shunt resistor from Pin 3 to ground. The oscillator's buffered output (Pin 5) can be used as a feedback signal to lock the oscillator to an appropriate reference.

IF Amplifier and IF Limiter

The IF strip provides more than 95dB of power gain for the down converted signal. Its overall bandwidth is limited to 2MHz. The input and output impedance of the IF amplifier and the input impedance of the IF limiter are set to 1500Ω (match to 455kHz filter). A second filter is connected between the IF amplifier and the limiter for improved channel selectivity and reduced instability. This ceramic filter provides 3dB interstage insertion loss which results in optimal RSSI linearity. The overall gain can be reduced if desired by adding an external attenuator after the IF amplifier. The differential limiter outputs (Pins 10 and 11) are available for demodulator circuits.

RSSI

The received signal strength indicator provides a linear voltage indication of the received signal strength in dB for a range in excess of 90dB. The response time to a change in input signal is less than a few microseconds and the delay is kept to a minimum because of the use of a minimum phase shift circuit. Because of the speed of the RSSI circuit, the RSSI rise and fall time may, in practice, be dominated by the bandwidth of the external bandpass filter that is placed between the mixer and the IF, and the external filter placed between the IF amplifier and limiter. Since the RSSI function requires the signal to propagate through the whole IF strip, and the rise and fall time of the filters are inversely proportional to their bandwidth, there is a trade-off between channel selectivity and RSSI response. A possible solution is to use a second SA637 with wider band external filters for faster RSSI response.

The RSSI curve is temperature compensated and in addition is designed for improved consistency from unit to unit.

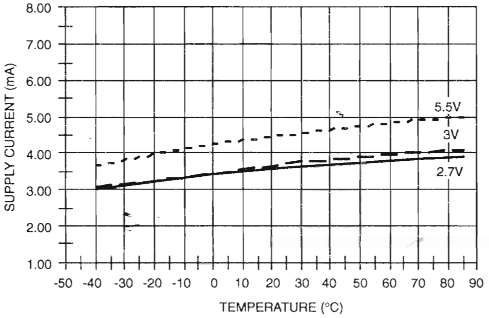
The RSSI circuit drives an on-chip low power op amp with rail-to-rail output which can be connected as a unity gain RSSI buffer or a gain stage or even a comparator.

DC Power Supply

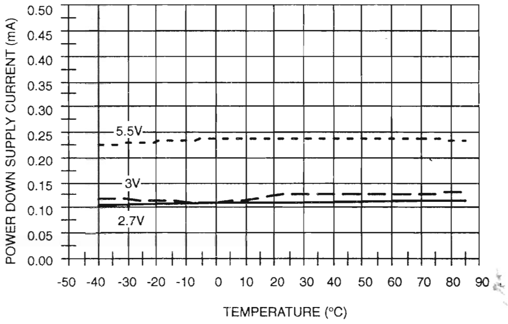
The IC is designed for operation between 2.7 and 5.5V. A power supply dependent biasing scheme is used in the mixers to benefit from the large headroom available at higher V_{CC}s.

PERFORMANCE CHARACTERISTICS

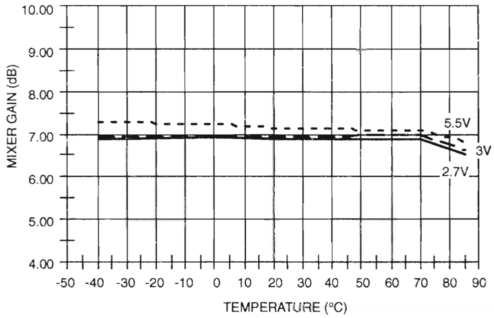
Supply Current vs Temperature and Supply Voltage



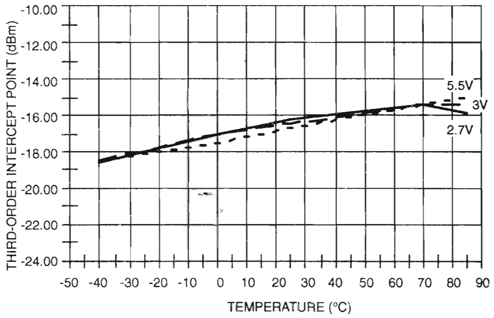
Power Down Supply Current vs Temperature and Supply Voltage



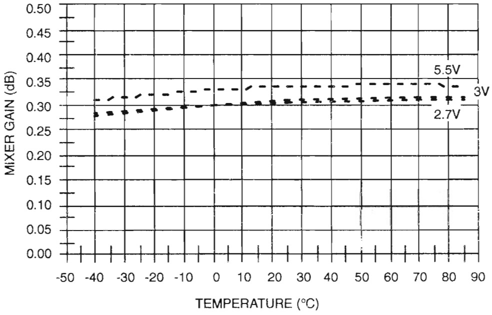
Mixer Power Gain vs Temperature and Supply Voltage



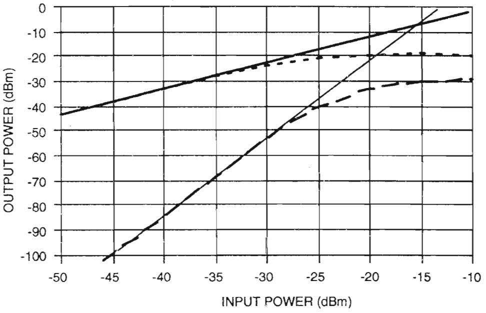
Mixer Third Order Input Intercept Point vs Temperature and Supply Voltage



Oscillator Buffer Output Level vs Temperature and Supply Voltage

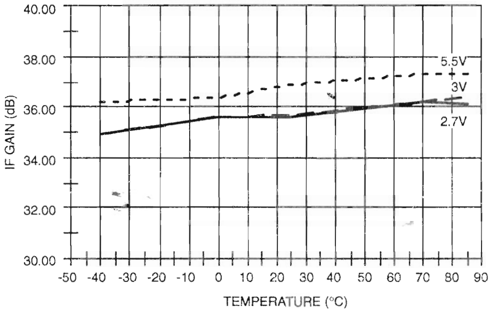


Mixer Third Order Intercept and Compression vs Input Power – Vcc=3V, T=25°C

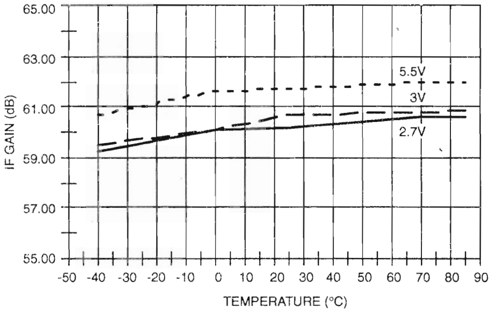


PERFORMANCE CHARACTERISTICS (cont.)

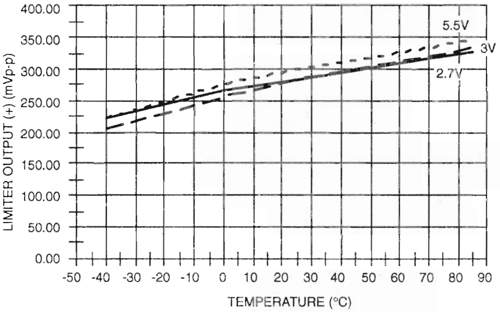
IF Power Gain vs Temperature and Supply Voltage



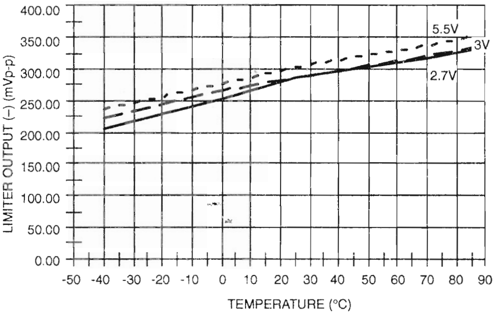
Limiter Power Gain vs Temperature and Supply Voltage



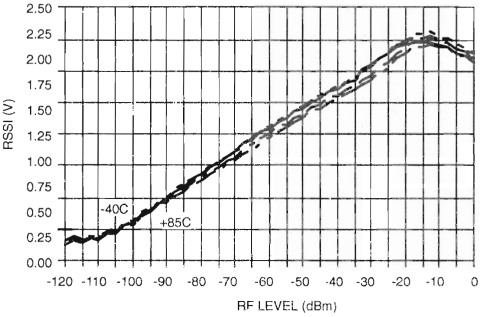
Limiter Output (+) Level vs Temperature and Supply Voltage



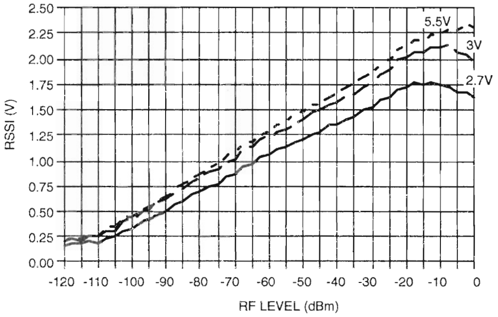
Limiter Output (–) Level vs Temperature and Supply Voltage



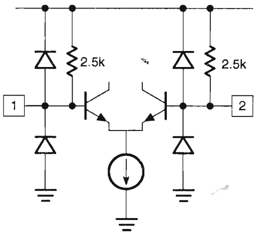
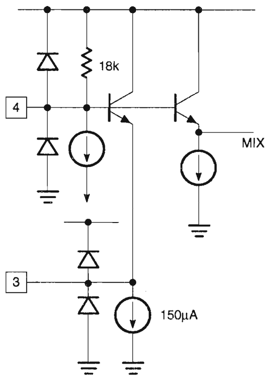
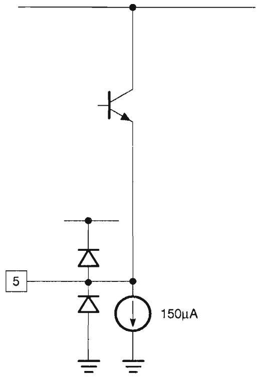
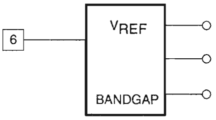
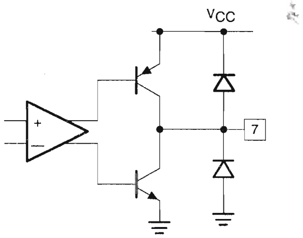
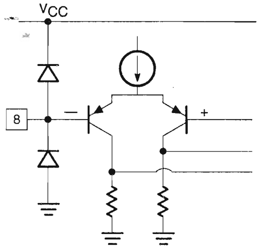
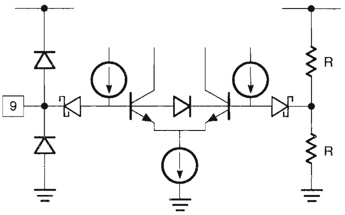
RSSI vs RF Level and Temperature – V_{CC} = 3V



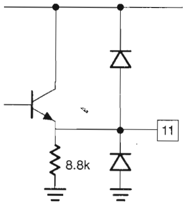
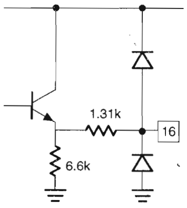
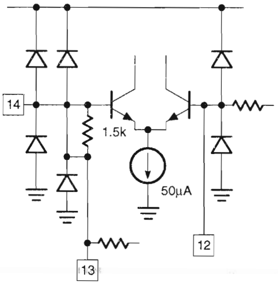
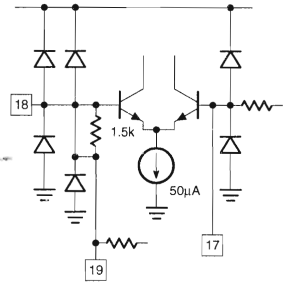
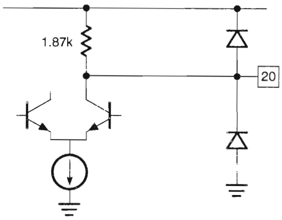
RSSI vs RF Level and Supply Voltage – Temperature = 25°C

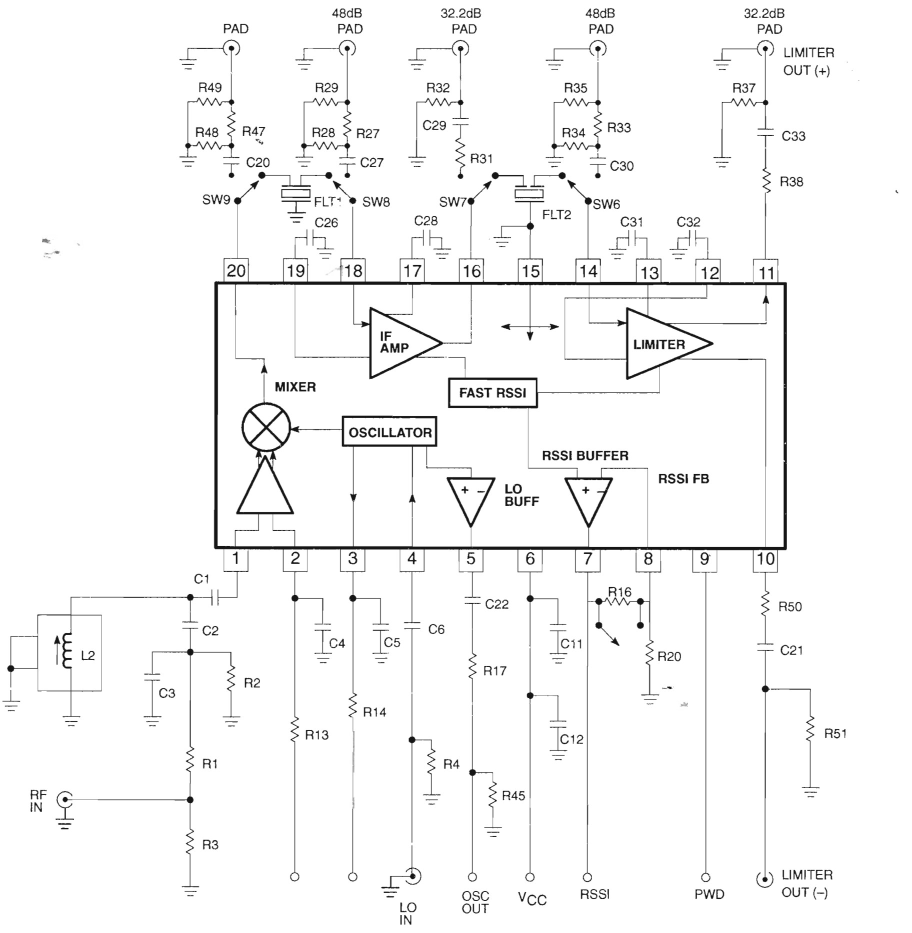


PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	RF IN	+1.40	
2	RF BYPASS	+1.40	
3	OSC E	+1.79	
4	OSC B	+2.56	
5	OSC BUFFER	+1.79	
6	V_{CC}	+3.00	
7	RSSI OUT	+0.20	
8	RSSI FEEDBACK	+0.20	
9	POWER DOWN	+2.00	

PIN FUNCTIONS (continued)

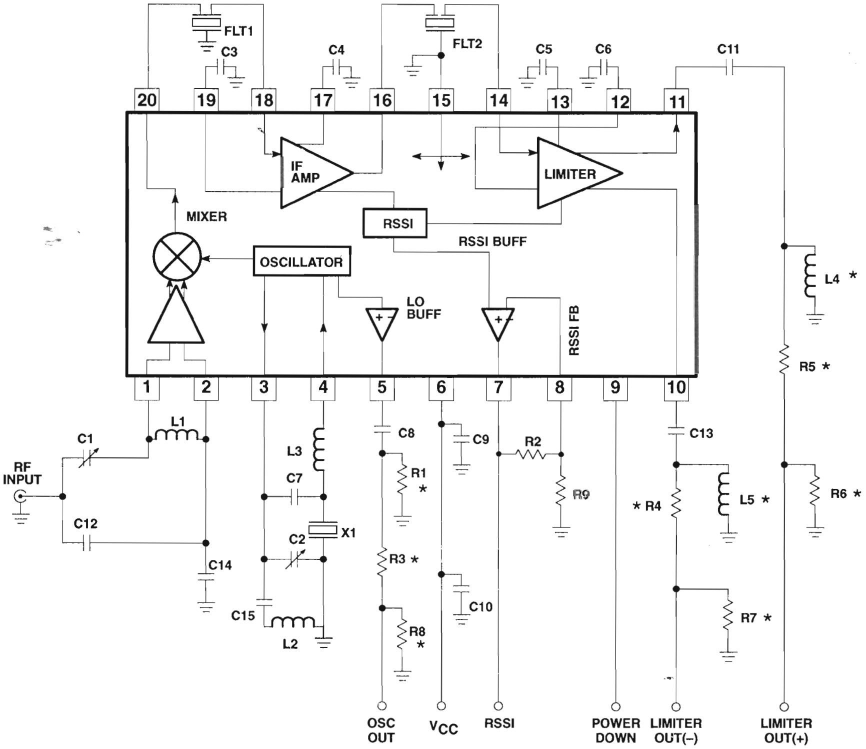
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
10 11	LIMITER OUT	+1.25		16	IF AMP OUT	+1.28	
12	LIMITER DECOUP	+1.28		17	IF AMP DECOUP	+1.28	
13	LIMITER COUPLING	+1.28		18	IF AMP IN	+1.28	
14	LIMITER IN	+1.28		19	IF AMP DECOUP	+1.28	
15	GND	0		20	MIXER OUT	+2.03	



Automatic Test Circuit Component List

C1	10nF	C27	100nF	R4	49.9Ω	R32	49.9Ω	R32	49.9Ω
C2	91pF	C28	100nF	R13	10kΩ	R33	13.7kΩ	R50	1kΩ
C3	620pF	C29	100nF	R14	10kΩ	R34	1.68kΩ	R51	49.9Ω
C4	100nF	C30	100nF	R16	10kΩ	R35	49.9Ω	L2	62nH
C5	100nF	C31	100nF	R17	1kΩ	R38	1kΩ		
C6	10nF	C32	100nF	R20	10kΩ	R39	49.9Ω		
C11	100nF	C33	100nF	R27	13.7kΩ	R45	49.9Ω		
C20	100nF	R1	249Ω	R28	1.68kΩ	R47	2.43kΩ		
C21	100nF	R2	60.4Ω	R29	49.9Ω	R48	39.2kΩ		
C26	100nF	R3	60.4Ω	R31	1kΩ	R49	49.9Ω		

Figure 1. SA637 Automatic Test Circuit



Component List

C1	5-30pF	C9	0.1µF	R1	OPEN	L1	0.15µH PM20-R15M
C2	5-30pF	C10	1.0µF	R2	0Ω (short)	L2	0.15µH PM20-R15M
C3	0.1µF	C11	0.1µF	R3	1kΩ	L3	0.47µH PM20-R47M
C4	0.1µF	C12	68pF	R4	1.0kΩ	L4	OPEN
C5	0.1µF	C13	0.1µF	R5	2.0kΩ	L5	OPEN
C6	0.1µF	C14	0.1µF	R6	51Ω	FLT1	455kHz SFGCC 455BX-TC
C7	10pF	C15	1000pF	R7	100Ω	FLT2	455kHz SFGCC 455BX-TC
C8	0.1µF			R8	100Ω	X1	82.705MHz CTS XTAL 020-3249-042
				R9	OPEN		

* NOTE: These components are optional and depend on user matching requirements.
Pads are provided on the demo board.
R2 and R9 set the RSSI buffer gain. For unity gain short R2 (Pin 7 to Pin 8)
and leave R9 open.

Figure 2. SA637 Application Circuit

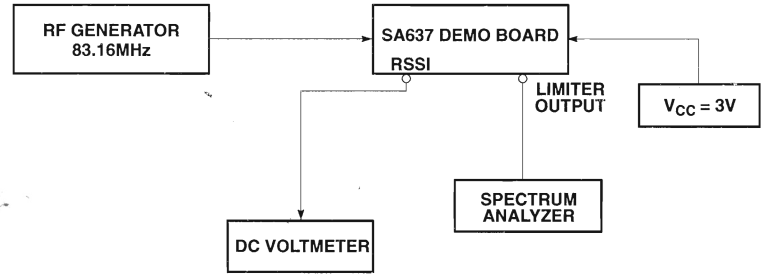
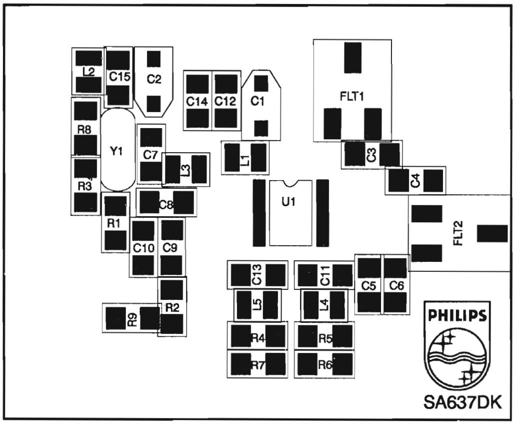
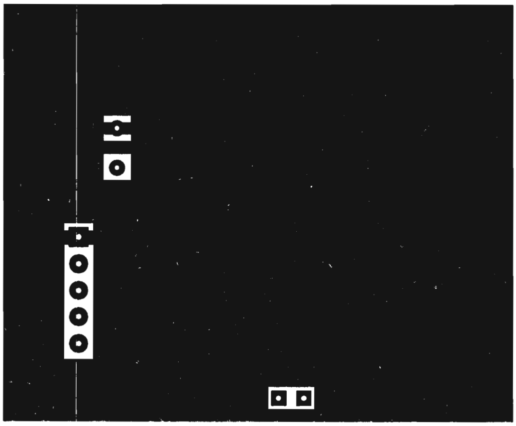


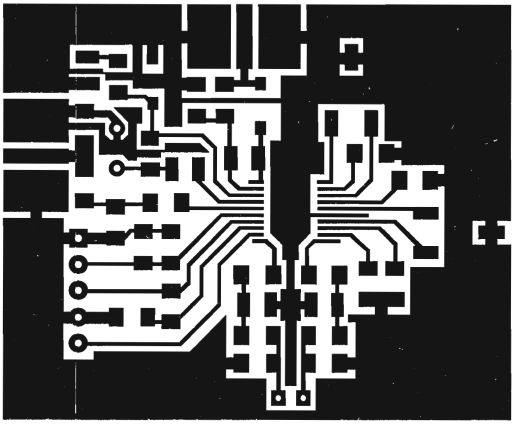
Figure 3. SA637 Application Circuit Test Set Up

NOTES:

1. Carrier-to-Noise (C/N): Connect a spectrum analyzer to Pin 10 or 11; set your RF generator to 83.16MHz or 455kHz above your LO frequency, modulation off; set the spectrum analyzer resolution bandwidth to 300Hz; and adjust your RF input level until the C/N = 26dB. Use video averaging. Assure that LIMOUT(+) and LIMOUT(–) are matched symetrically.
2. Ceramic filters: The ceramic filter can be SFGCC455BX-TC made by Murata which has 30kHz IF bandwidth.
3. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.45µV or -114dBm at the RF input.
4. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
5. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
6. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 0.1µF bypass capacitor on the supply pin improves sensitivity.


L2
C15
C2
C14
C12
C1
FLT1
R8
Y1
C7
L3
L1
C3
C4
R3
C8
U1
R1
C10
C9
FLT2
C13
C11
C5
C6
R9
R2
L5
L4
PHILIPS
R4
R5
R7
R6
SA637DK





Low voltage mixer FM IF system with filter amplifier and data switch

SA639

DESCRIPTION

The SA639 is a low-voltage high performance monolithic FM IF system with high-speed RSSI incorporating a mixer/oscillator, two wideband limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), fast RSSI op amps, voltage regulator, wideband data output, post detection filter amplifier and data switch. The SA639 is available in 24-lead TSSOP (Thin shrink small outline package).

The SA639 was designed for high bandwidth portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The data output provides a minimum bandwidth of 1MHz to demodulate wideband data. The RSSI output is amplified and has access to the feedback pin. This enables the designer to level adjust the outputs or add filtering.

The post-detection amplifier may be used to realize a low pass filter function. A programmable data switch routes a portion of the data signal to an external integration circuit that generates a data comparator reference voltage.

SA639 incorporates a power down mode which powers down the device when Pin 8 is high. Power down logic levels are CMOS and TTL compatible with high input impedance.

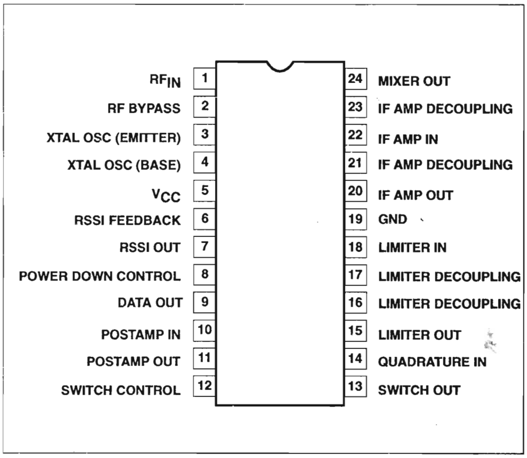
APPLICATIONS

- DECT (Digital European Cordless Telephone)
- FSK and ASK data receivers

FEATURES

- V_{CC} = 2.7 to 5.5V
- Low power consumption: 8.3mA typ at 3V
- Wideband data output (1MHz min.)
- Fast RSSI rise and fall times
- Mixer input to >500MHz
- Mixer conversion power gain of 12dB and noise figure of 11dB at 110MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 92dB of IF Amp/Limiter power gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- RSSI output internal op amp
- Post detection amplifier for filtering
- Programmable data switch
- Excellent sensitivity: 2.24µV into 50Ω matching network for 10dB SNR (Signal to Noise Ratio) with RF at 110MHz and IF at 9.8MHz
- ESD hardened
- Power down mode

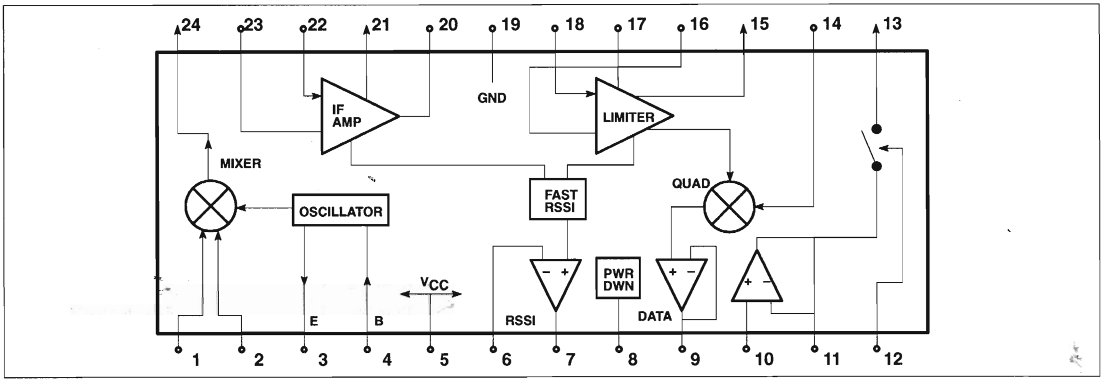
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic TSSOP (Thin Shrink Small Outline Package)	-40 to +85°C	SA639	SOT-355

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	-0.3 to 6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC}+0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA639	-40 to +85	°C

NOTE: θ_{JA} Thermal impedance (DH package) 117°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA639			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7	3.0	5.5	V
I_{CC}	DC current drain	Pin 8 = LOW, Pin 12 = HIGH		8.5		mA
I_{CC}	Standby	Pin 8 = HIGH, Pin 12 = HIGH		140	200	µA
	Input current	Pin 8 = LOW			10	µA
		Pin 8 = HIGH			4	
	Input level	Pin 8 = LOW	0		0.3V_{CC}	V
		Pin 8 = HIGH[1]	0.7V_{CC}		6	
t_{ON}	Power up time	RSSI valid (10% to 90%)		10		µs
t_{OFF}	Power down time	RSSI invalid (90% to 10%)		5		µs
	Power up settling time	Data output valid		100	200	µs
Data Switch Control Input						
	Switch closed	Pin 12 = LOW, PIN 8 = LOW	0		0.3 V_{CC}	V
	Switch open (output tri-state)	Pin 12 = HIGH	0.7 V_{CC}		6	V
	Input current	Pin 12 = LOW			10	µA
		Pin 12 = HIGH			4	
	Switch activation time			0.5	1	µs

NOTE:
1. When the device is forced in power down mode via Pin 8, the Data Switch will output a voltage close to 1.6V and the state of the switch control input will have no effect.

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = +3V$, unless otherwise stated. RF frequency = 110.592MHz + 14.5dBV RF input step-up;LO frequency = 120.392MHz; IF frequency = 9.8MHz; RF level = -45dBm; FM modulation = 576kHz with ±288kHz peak deviation, discriminator tank circuit Q=4. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA639			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 160mV$_{RMS}$)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	External oscillator (buffer)		0.2	500		MHz
	Noise figure at 110MHz			11	12	dB
	Third-order input intercept point	Matched f1=110.592MHz; f2=110.852MHz	-15	-12.5		dBm
	Conversion power gain	Matched 14.5dBV step-up	11	12		dB
	RF input resistance	Single-ended input		800		Ω
	RF input capacitance			3.5		pF
	Mixer output resistance	(Pin 24)		330		Ω
IF section						
	IF amp gain		34	38		dB
	Limiter gain		50	54		dB
	Input limiting -3dB	Test at Pin 22		–105		dBm
	AM rejection	RF level = -45dBm, 80% AM 1kHz	30	34		dB
	Data level	$R_L = 10kΩ$, $C_L = 30pF$ (see application circuit)	300	400	450	mV_{P-P}
	Data bandwidth		1	2		MHz
S/N	Signal-to-noise ratio	RF level = -45dBm, no modulation for noise		60		dB
	IF RSSI output with buffer	IF level = -100dBm	0	0.2	0.5	V
		IF level = -45dBm	0.3	0.6	1.0	
		IF level = -18dBm	0.9	1.3	1.8	
	IF RSSI output rise time	IF frequency = 9.8MHz				
	(10kHz pulse, no 9.8MHz filter)	RF level = -45dBm		1.2		µs
	(no RSSI bypass capacitor)	RF level = -28dBm		1.1		
	IF RSSI output fall time	IF frequency = 9.8MHz				
	(10kHz pulse, no 9.8MHz filter)	RF level = -45dBm		2.0		µs
	(no RSSI bypass capacitor)	RF level = -28dBm		7.3		
	RSSI range		85	90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance			330		Ω
	IF output impedance			330		Ω
	Limiter input impedance			330		Ω
	Limiter output impedance			300		Ω
	Limiter output level with no load			130		mV_{RMS}
RF/IF section (int LO)						
	System RSSI output	RF level = -27dBm	1.0	1.2	1.5	V
	System SINAD	RF level = -85dBm		12		dB
	System S/N	RF level = -100dBm		10		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA639			
			MIN	TYP	MAX	
Post detection filter amplifier						
	Amplifier 3dB bandwidth	AC coupled: $R_L = 10k\Omega$, $C_L = 30pF$	4			MHz
	Amplifier gain	AC coupled: $R_L = 10k\Omega$, $V_{OUT\ DC} = 1.6V$	-1	-0.2	0	dB
	Slew rate	AC coupled: $R_L = 10k\Omega$, $C_L = 30pF$	1			V/µs
	Input resistance		300			kΩ
	Input capacitance				3	pF
	Output impedance			250	500	Ω
	Output load resistance	AC coupled	5			kΩ
	Output load capacitance[1]	AC coupled		30		pF
	DC output level[2]		1.6	1.7	1.8	V
Data switch						
	DC input voltage range[3]		1.2	1.6	2.0	V
	AC input swing			400		mV_{P-P}
	Input impedance		100			kΩ
	Input capacitance				5	pF
	Output load resistance			500		Ω
Through Mode (Pin 12 = LOW)						
	AC voltage gain[4]		-2	-1.5		dB
	Output drive capability	Sink/source, $V_{OUT\ DC} = 1.6V$	3			mA
	Slew rate	$V_{OUT\ DC} = 1.6V$	1			V/µs
	Input offset voltage$_5$	$V_{IN\ DC} = 1.2$ to $2.0V$			±5	mV
Tri-State Mode (Pin 12 = HIGH)						
	Output leakage current	$V_{OUT\ DC} = 1.2$ to $2.0V$			100	nA

NOTES:

1. Includes filter feedback capacitance, comparator input capacitance. PCB stray capacitances and switch input capacitance.
2. Demodulator output DC coupled with Post Detection Filter Amplifier input and the demodulator tank exactly tuned to center frequency.
3. Includes DC offsets due to frequency offsets between Rx and Tx carrier and demodulator tank offset due to mis-tuning.
4. With a $400mV_{P-P}$ sinusoid at 600kHz driving Pin 10. Output load resistance 500Ω in series with 10nF.
5. With a DC input and capacitor in the RC load fully charged.

CIRCUIT DESCRIPTION

The SA639 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 44dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 58dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 10.7MHz, 330Ω source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types, such as digital cordless phones.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 11dB, conversion power gain of 12dB, and input third-order intercept of -12.5dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 330Ω resistor permitting direct connection to a 10.7MHz ceramic filter. The input resistance of the limiting IF amplifiers is also 330Ω. With most 10.7MHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 6dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 6dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequency at 10.7MHz. Special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output (DATA) of the quadrature is a low impedance voltage output. This output is designed to handle a minimum bandwidth of 1MHz. This is designed to demodulate wideband data, such as in DECT applications.

Post Detection Filter Amplifier

The filter amplifier may be used to realize a group delay optimized low pass filter for post detection. The filter amplifier can be configured for Sallen & Key low pass with Bessel characteristic and a 3dB cut frequency of about 800kHz.

The filter amplifier provides a gain of 0dB. The output impedance is less than 500Ω in order to reduce frequency response changes as a result of amplifier load variations. The filter amplifier has a 3dB bandwidth of at least 4 MHz in order to keep the amplifier's frequency response influence on the filter group delay characteristic at a minimum. At the center of the carrier it is mandatory to provide a filter output DC bias voltage of 1.6V in order to be within the input common mode range of the external data comparator. The filter output DC bias voltage specification holds for an exactly center tuned demodulator tank and for the demodulator output connected to the filter amplifier input.

Data Switch

The SA639 incorporates an active data switch used to derive the data comparator reference voltage by means of an external integration circuit. The data switch is typically closed for 10µs before and during reception of the synchronization word pattern, and is otherwise open. The external integration circuit is formed by an R/C low pass with a time constant of 5 to 10µs.

The active data switch provides excellent tracking behavior over a DC input range of 1.2 to 2.0V. For this range with an RC load (no static current drawn), the DC output voltage will not differ more than ±5mV from the input voltage. Since the active data switch is designed to behave like a non-linear charge pump (to allow fast tracking of the input signal without slew rate limitations under dynamic conditions of a 600kHz input signal with $400mV_{P-P}$ and the RC load), the output signal will have a $340mV_{P-P}$ output with a DC average that will not vary from the input DC average by more than ±15mV.

The data switch is able to sink/source 3mA from/to the external integration circuit in order to minimize the settling time after long power-down periods (DECT paging mode). In addition, during power-down conditions a reference voltage of approximately 1.6V will be used as the input to the switch. The switch will be in a low current mode to maintain the voltage on the external RC load. This will further reduce the settling time of the capacitor after power-up. It should be noted that during power-down the switch can only source and sink a trickle current (10µA). Thus, the user should make sure that other circuits (like the data comparator inputs) are not drawing current from the RC circuit.

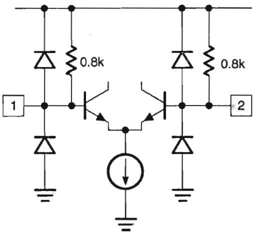
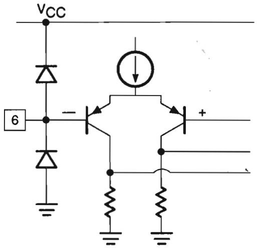
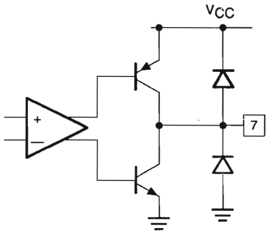
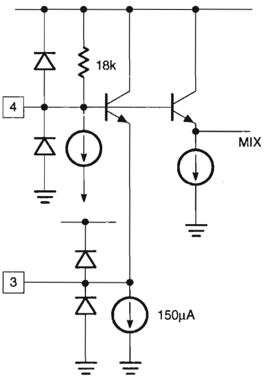
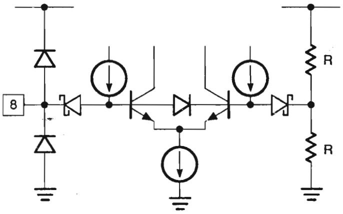
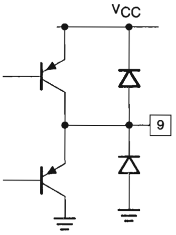
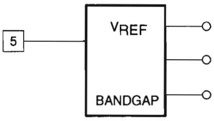
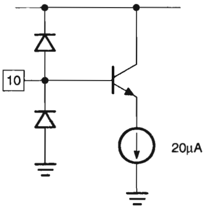
The data switch provides a slew rate better than 1V/µs in order to track with system DC offset from receive slot to receive slot (DECT idle lock or active mode). When the data switch is opened the output is in a tri-state mode with a leakage current of less than 100nA. This reduces discharge of the external integration circuit. When powered-down, the data switch will output a reference of approximately 1.6V to maintain a charge on the external RC circuit.

A Receive Signal Strength Indicator (RSSI) completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for DECT cordless telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

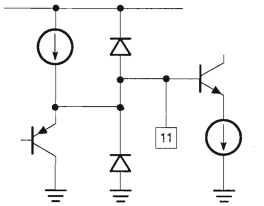
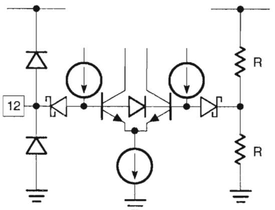
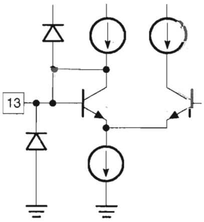
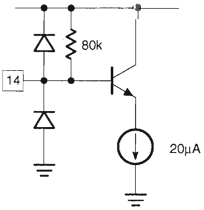
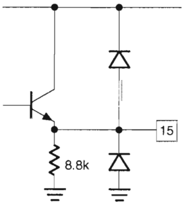
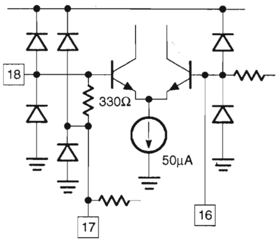
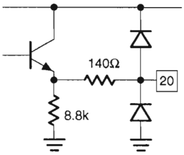
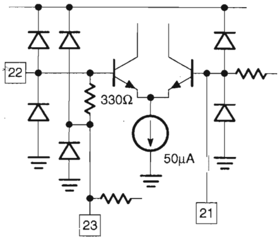
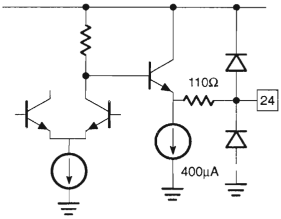
NOTE: dB(v) = 20log V_{OUT}/V_{IN}

PIN FUNCTIONS

All DC voltages measured with Pin 8 = Pin 12 = Pin 19 = 0V, Pin 5 = 3V and Pin 9 connected to Pin 10 (see Figure 4).

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	RF IN	+1.07		6	RSSI FEEDBACK	+0.20	
2	RF BYPASS	+1.07		7	RSSI OUT	+0.20	
3	XTAL OSC	+1.57		8	POWER DOWN	0.00	
4	XTAL OSC	+2.32		9	DATA OUT	+1.7	
5	VCC	+3.00		10	POST AMP IN	+1.70	

PIN FUNCTIONS (continued)

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
11	POST AMP OUT	+1.70	
12	SWITCH CONTROL	0.00	
13	SWITCH OUT	+1.70	
14	QUAD IN	+3.00	
15	LIMITER OUT	+1.35	
16	LIMITER DECOUP	+1.23	
17	LIMITER COUPLING	+1.23	
18	LIMITER IN	+1.23	
19	GND	0	
20	IF AMP OUT	+1.22	
21	IF AMP DECOUP	+1.22	
22	IF AMP IN	+1.22	
23	IF AMP DECOUP	+1.22	
24	MIXER OUT	+1.03	

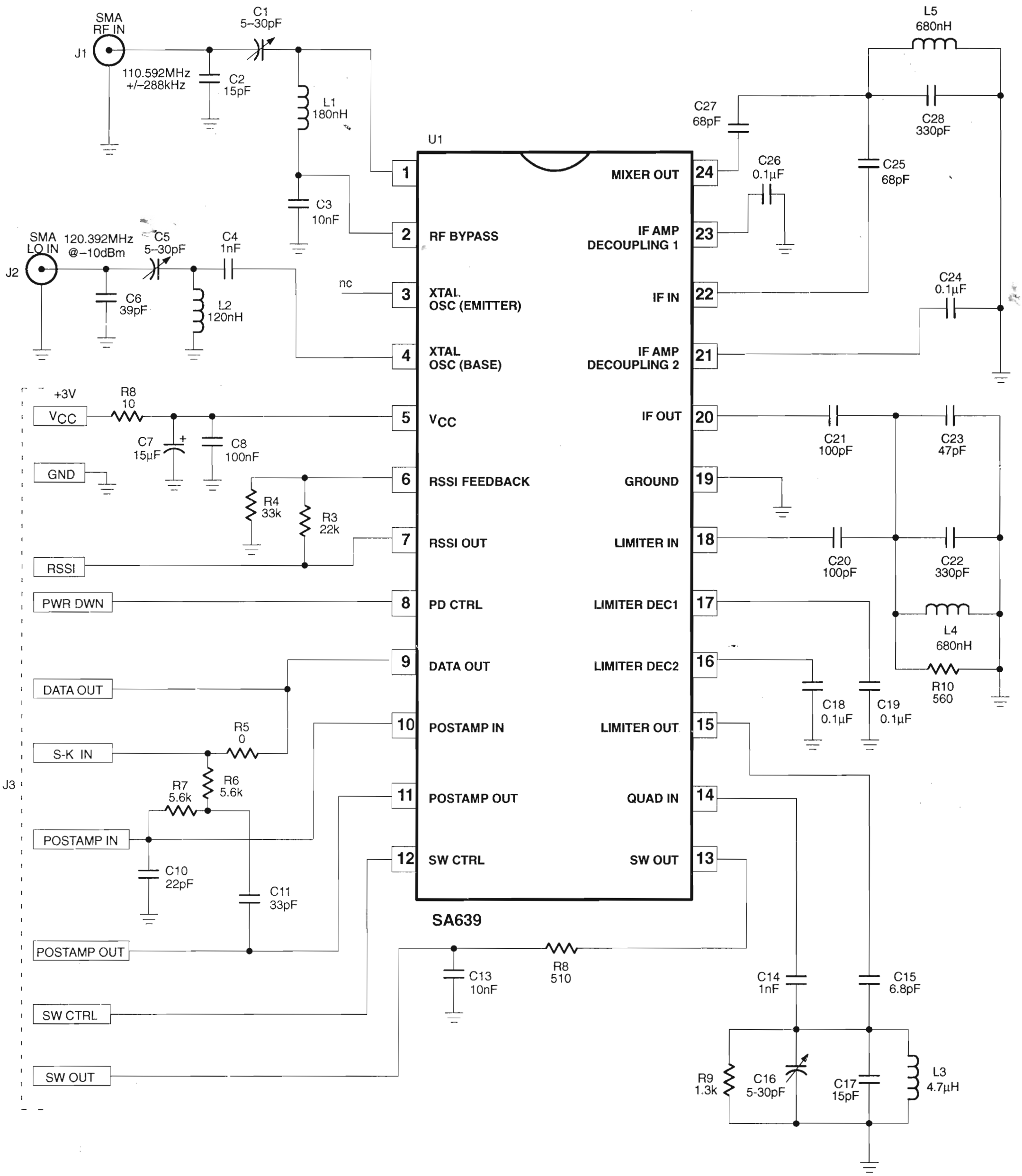


Figure 4. SA639 110.592MHz (RF) / 9.8MHz (IF) DECT Application Circuit

Low-voltage mixer FM IF system SA676

DESCRIPTION

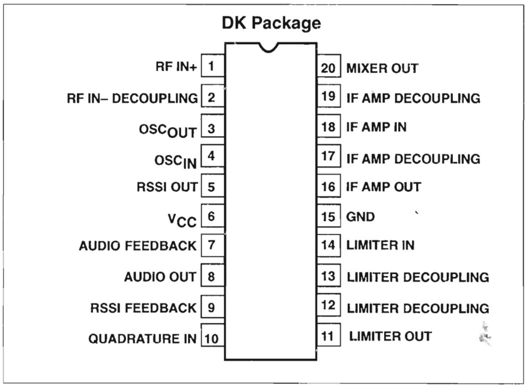
The SA676 is a low-voltage monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA676 is available in a 20-pin SSOP (shrink small outline package).

The SA676 was designed for cordless telephone applications in which efficient and economic integrated solutions are required and yet high performance is desirable. Although the product is not targeted to meet the stringent specifications of high performance cellular equipment, it will exceed the needs for analog cordless phones. The minimal amount of external components and absence of any external adjustments makes for a very economical solution.

FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >100MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 100MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz IF amp/limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 70dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Audio output internal op amp
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

PIN CONFIGURATION



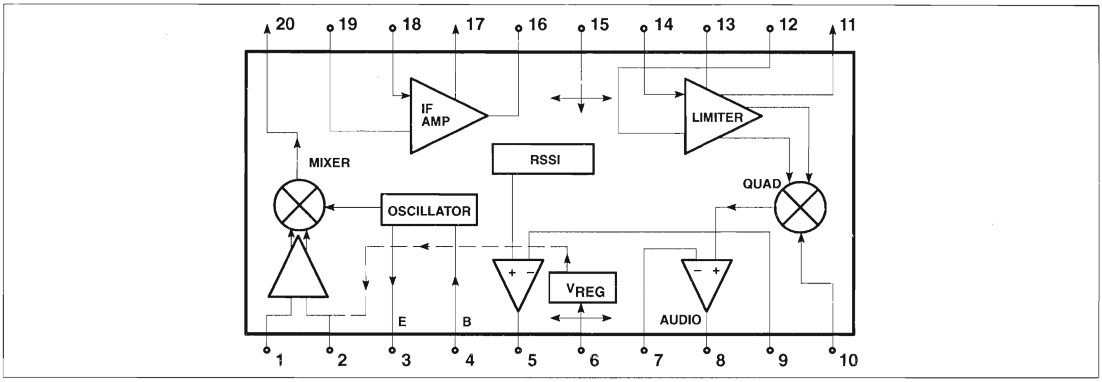
APPLICATION

- Cordless phones

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (Surface-mount)	-40 to +85°C	SA676DK	1563–

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range	–40 to +85	°C
θ_{JA}	Thermal impedance DK package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA676 MIN	LIMITS SA676 TYP	LIMITS SA676 MAX	UNITS
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	5.0	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz; +14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4kΩ and R18 = 3.3kΩ; RF level = –45dBm; FM modulation = 1kHz with ±5kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			100		MHz
f_{OSC}	Crystal oscillator frequency			100		MHz
	Noise figure at 45MHz			7.0		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF level = –52dBm		–10		dBm
	Conversion power gain	Matched 14.5dBV step–up	10	17		dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	AM rejection	30% AM 1kHz		50		dB
	Audio level	Gain of two	60	120		mV
	SINAD sensitivity	IF level –110dBm		17		dB
THD	Total harmonic distortion			–55		dB
S/N	Signal–to–noise ratio	No modulation for noise		60		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –110dBm		0.5	.90	V
		IF level = –50dBm		1.7	2.2	V
	RSSI range			70		dB
	IF input impedance	Pin 18	1.3	1.5		kΩ
	IF output impedance	Pin 16		0.3		kΩ
	Limiter input impedance	Pin 14	1.3	1.5		kΩ
	Limiter output impedance	Pin 11		0.3		kΩ
	Limiter output voltage	Pin 11		130		mV$_{RMS}$

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
RF/IF section (int LO)						
	System SINAD sensitivity	RF level = −114dBm		12		dB

NOTE:

1. The generator source impedance is 50Ω, but the SA676 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA676 input (Pin 18) which is about 21dB less than the “available power” at the generator.

CIRCUIT DESCRIPTION

The SA676 is an IF signal processing system suitable for second IF systems with input frequency as high as 100MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 7.0dB, conversion gain of 17dB, and input third-order intercept of −10dBm. The oscillator will operate in excess of 100MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations.

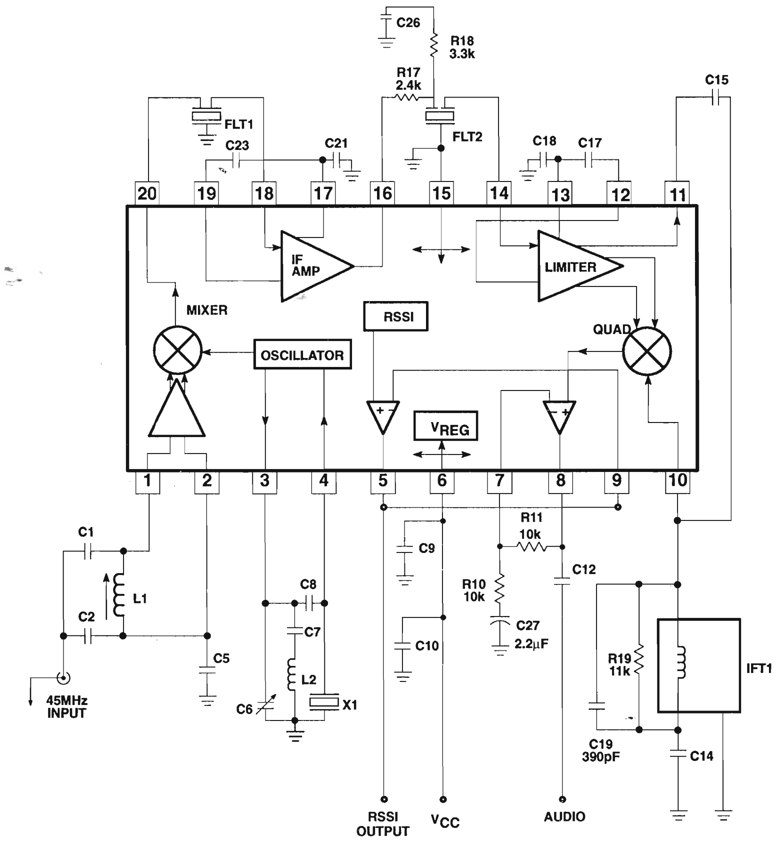
The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 44dB of gain and 5.5MHz bandwidth. The IF limiter has 58dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 10kΩ with a rail-to-rail output.

A log signal strength indicator completes the circuitry. The output range is greater than 70dB and is temperature compensated. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



SA676DK Demoboard
Application Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	5-30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2μF Tantalum
FLT 1	Ceramic Filter Murata SFG455A3 or equiv
FLT 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330μH TOKO 303LN-1130
L1	330nH Coilcraft UNI-10/142-04J08S
L2	0.8μH nominal TOKO 292CNS-T1038Z
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

* NOTE: This value can be reduced when a battery is the power source.

Figure 1. SA676 45MHz Application Circuit

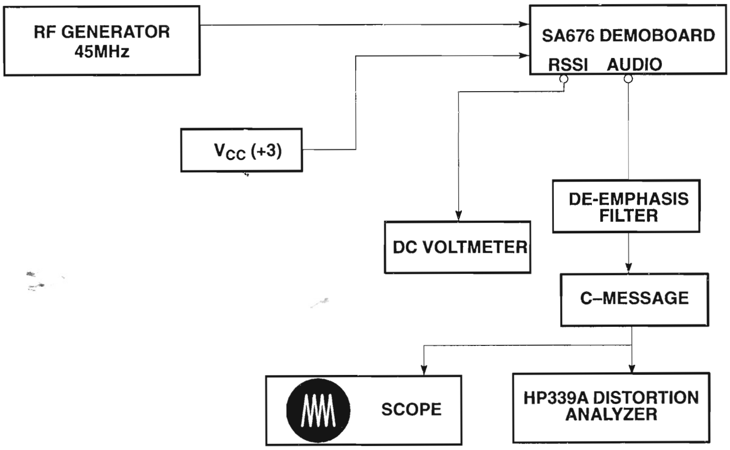


Figure 2. SA676 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339A analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All specifications and testing are done with the wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.45µV or –114dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15µF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1µF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

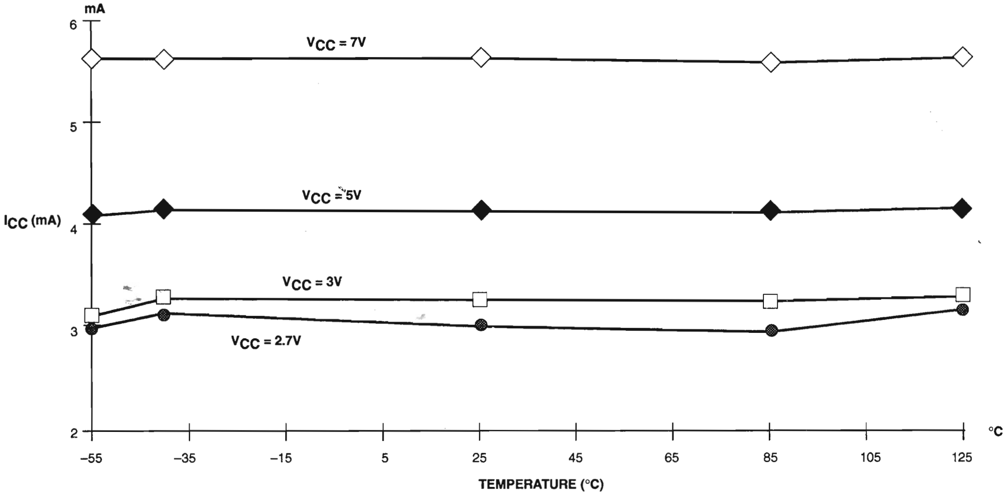


Figure 3. I_{CC} vs Temperature and Supply Voltage

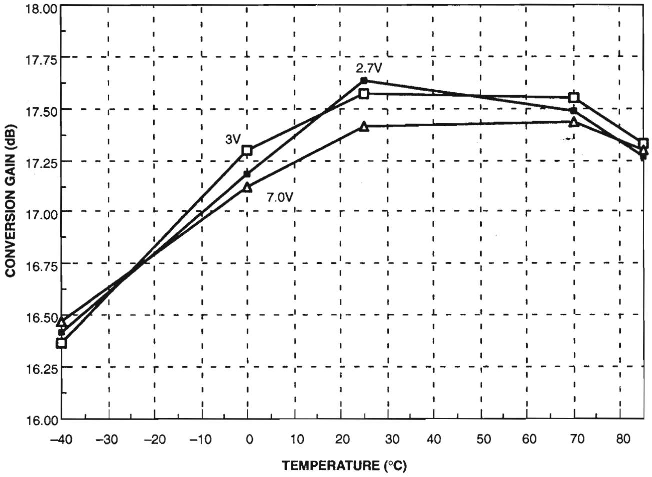
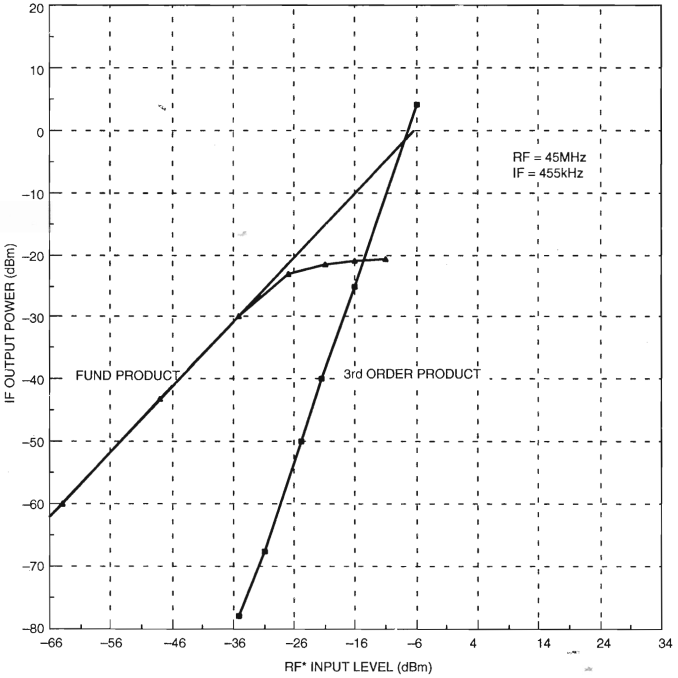


Figure 4. Conversion Gain vs Temperature and Supply Voltage



*50Ω INPUT

Figure 5. Mixer Third Order Intercept and Compression

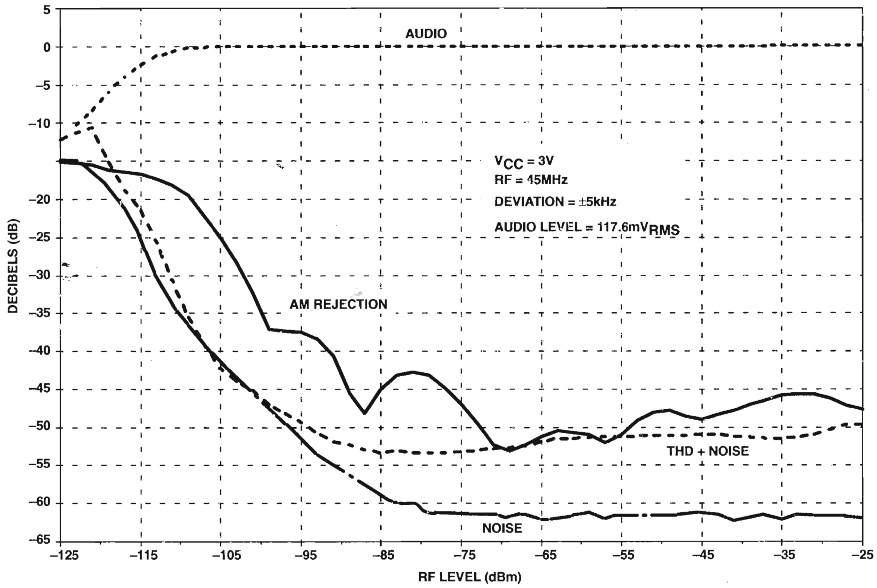


Figure 6. Sensitivity vs RF Level (+25°C)

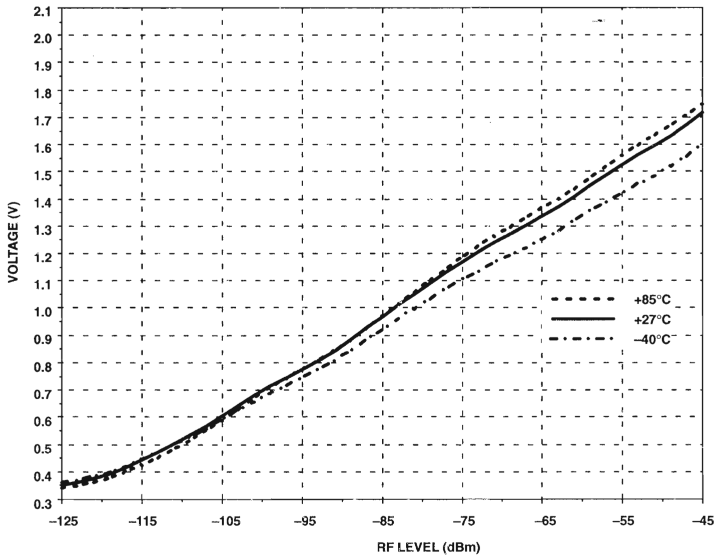


Figure 7. RSSI vs RF Level and Temperature - V_{CC} = 3V

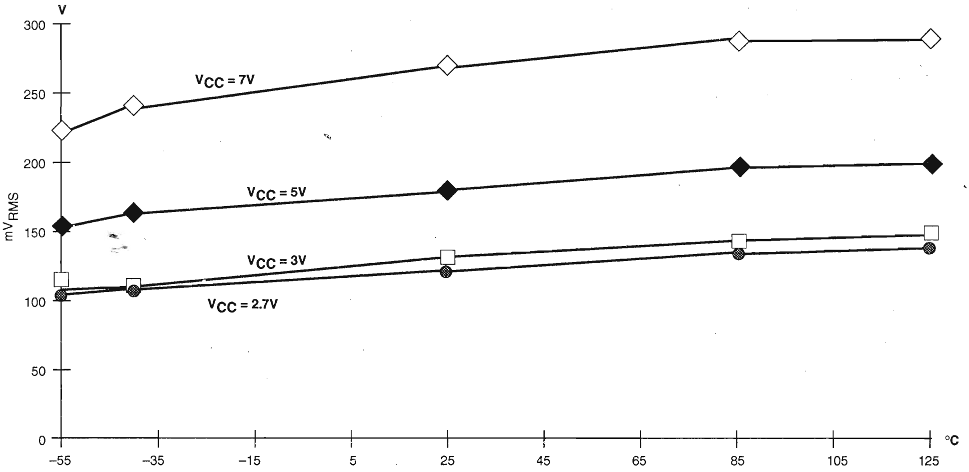


Figure 8. Audio Output vs Temperature and Supply Voltage

Low voltage IF I/Q transceiver
SA1638

DESCRIPTION

The SA1638 is a combined Rx and Tx IF I/Q circuit. The receive path contains an IF amplifier, a pair of quadrature down-mixers, and a pair of baseband filters and amplifiers. A second pair of mixers in the transmit path transposes a quadrature baseband input up to the IF frequency. An external VCO signal is divided down internally and buffered to provide quadrature local oscillator signals for the mixers. A further divider chain, reference divider and phase detector are provided to avoid the need for an external IF synthesizer. Rx or Tx path or the entire circuit may be powered down by logic inputs. On-board voltage regulators are provided to allow direct connection to a battery supply.

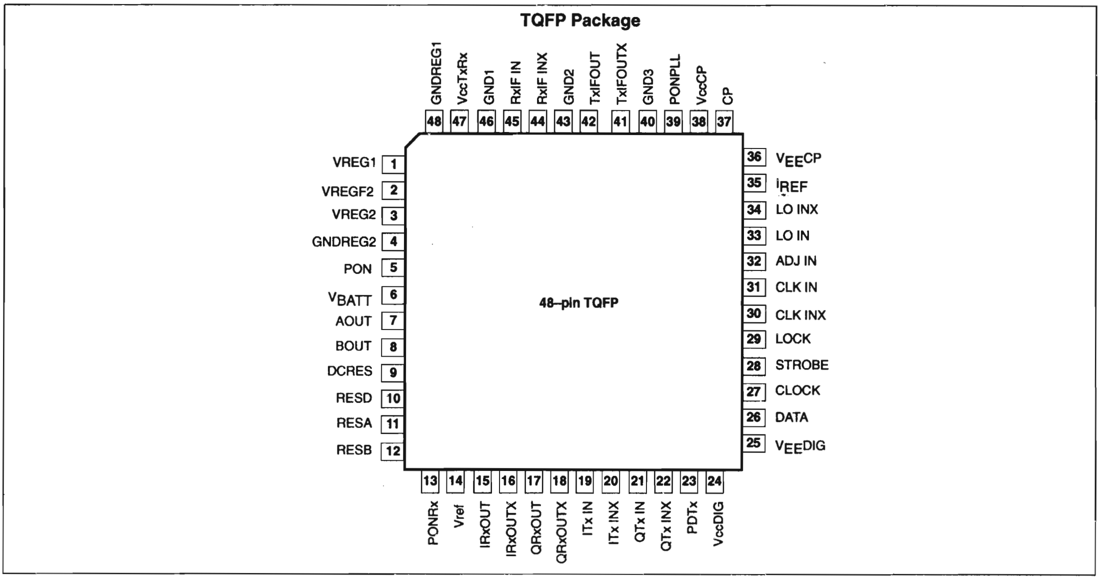
FEATURES

- Direct supply: 3.3V to 7.5V
- Two DC regulators giving 3.0V output
- Low current consumption: 14mA for Rx or 18mA for Tx
- Input/output IF frequency from 70-500MHz
- Internal IF PLL for synthesizing the local oscillator signal
- High performance on-board integrated receive filters with bandwidth tunable between 50kHz to 1MHz
- Switchable alternative bandwidth setting available to allow channel bandwidth flexibility in operation
- Designed for a widely used I and Q baseband GSM interface
- Control registers power up in a default state
- Optional DC offset trim capability to <200mV
- Only a standard reference input frequency required, choice of 13, 26, 39 or 52MHz
- Fully compatible with SA1620 GSM RF front-end

APPLICATIONS

- IF circuitry for GSM 900MHz hand-held units
- IF circuitry for PCN (DCS1800) hand-held units
- Quadrature up and down mixer stage

PIN CONFIGURATION



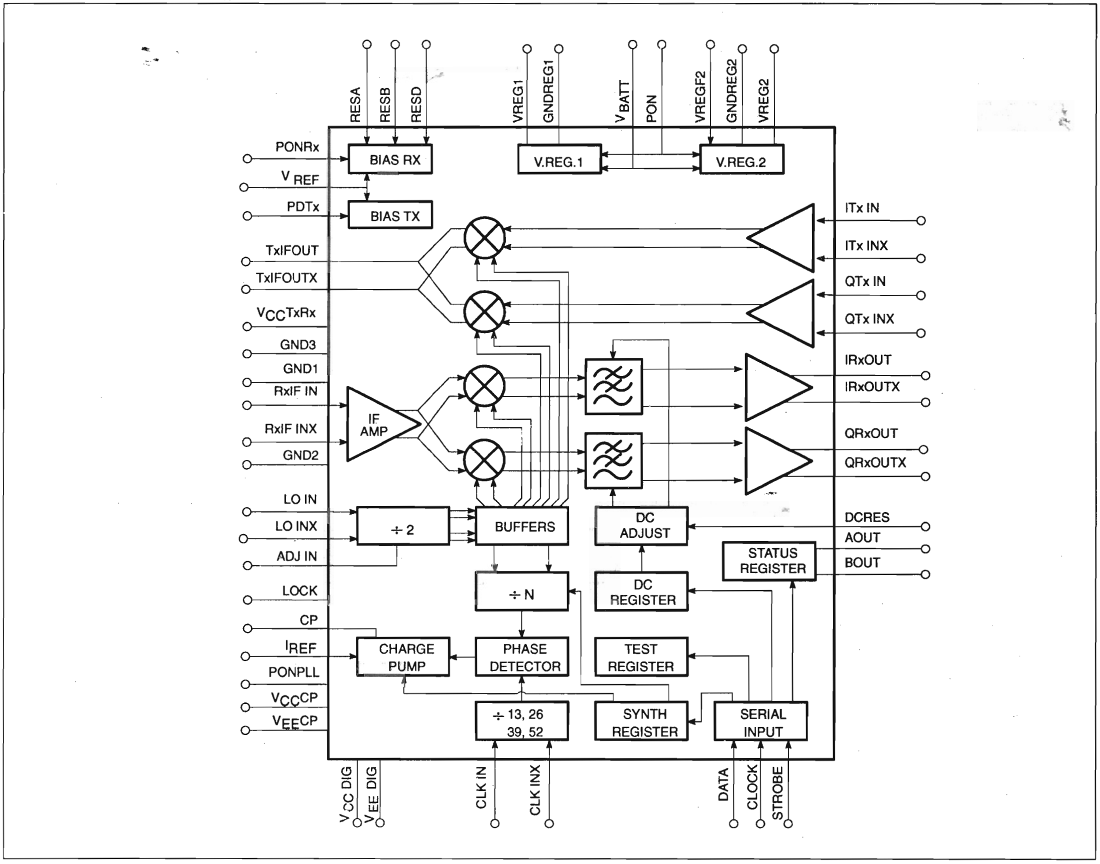
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48-Pin Thin Quad Flat Pack (TQFP)	-40 to +85°C	SA1638BE	1706B

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXXX}	Supply voltages	2.7 to 5.5	V
$V_{CC}CP$	Charge pump supply voltage	2.9 to 5.5	V
V_{BATT}	Battery voltage	3.3 to 7.5	V
T_A	Operating ambient temperature range	-40 to +85	°C

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin Name	Description
1	VREG1	Output voltage of regulator 1
2	VREGF2	Feedback of regulator 2
3	VREG2	Output voltage of regulator 2
4	GNDREG2	Ground of regulator 2
5	PON	Power-on input for voltage regulators 1 and 2 (active high)
6	V_{BATT}	Input voltage for regulators 1 and 2
7	AOUT	Control output (for SA1620 attenuation select A pin)
8	BOUT	Control output (for SA1620 attenuation select B pin)
9	DCRES	Reference resistor for DC offset circuit
10	RESD	Additional external current defining resistor for filters
11	RESA	Principal external current defining resistor for filters
12	RESB	Principal external current defining resistor for filters
13	PONRx	Power-on input for Rx (active high)
14	V_{REF}	Reference voltage
15	IRxOUT	In-phase differential receive baseband output
16	IRxOUTX	In-phase differential receive baseband output
17	QRxOUT	Quadrature differential receive baseband output
18	QRxOUTX	Quadrature differential receive baseband output
19	ITx IN	In-phase differential transmit baseband input
20	ITx INX	In-phase differential transmit baseband input
21	QTx IN	Quadrature differential transmit baseband input
22	QTx INX	Quadrature differential transmit baseband input
23	PDTx	Power-on for transmitter (active low)
24	V_{CC}DIG	Digital circuit supply
25	V_{EE}DIG	Digital ground
26	DATA	Serial data input
27	CLOCK	Serial clock input
28	STROBE	Serial strobe input
29	LOCK	Test control/synthesizer lock indicator
30	CLK INX	Differential reference divider input
31	CLK IN	Differential reference divider input
32	ADJ IN	Used for test only
33	LO IN	Differential LO input
34	LO INX	Differential LO input
35	I_{REF}	Reference current for charge pump
36	V_{EE}CP	Charge pump ground
37	CP	Charge pump output
38	V_{CC}CP	Charge pump circuit supply
39	POnPLL	Power-on input for synthesizer circuits (active high)
40	Gnd3	Ground (internal connection to GND1 and GND2)
41	TxIFOUTX	Differential transmit IFoutput
42	TxIFOUT	Differential transmit IFoutput
43	GND2	Ground (internal connection to GND1 and GND3)
44	RxIF INX	Differential receive IF input
45	RxIF IN	Differential receive IF input
46	GND1	Ground (internal connection to GND2 and GND3)
47	V_{CC}TxRx	Transmit and receive circuits supply voltage (also feedback of Regulator 1)
48	GNDREG1	Ground of regulator 1

NOTE: There are no ESD protection diodes at Pins 41 and 42. Thus, open collector outputs may have increased DC voltage or higher AC peak voltage.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CCXX}	Supply voltages	-0.3 to +6.0	V
V_{BATT}	Battery voltage	-0.3 to +8.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CCXX}+0.3)	V
ΔVG	Any GND pin to any other GND pin	0	V
P_D	Power dissipation, T_A = 25°C (still air)	300	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}. 48-pin TQFP: θ_{JA} = 67°C/W.

Voltage Regulators

T_A = 25°C, P_{ON} = 3V, P_{ON}RX = 0V, PDTX = 3V, PDPLL = 0V, V_{BATT} = 3.3V, I_{LOAD} = 15mA, $V_{REG}1$ connected to V_{CC}TxRx, $V_{REG}2$ connected to V_{REG}F2; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
$V_{REG}1$, $V_{REG}2$	Nominal V_{OUT}		2.85		3.15	V
V_{BATT}			3.3		7.5	V
I_{LOAD}[1]	$V_{REG}1$ or $V_{REG}2$				30	mA
I_{BATT}		I_{LOAD} = 0mA		7		mA
$I_{BATT\ PD}$	P_{ON} = 0V	I_{LOAD} = 0mA			75	µA
$C_{REG}1$[2]	$V_{REG}1$ cap load		0.1		1000	µF
$C_{REG}2$[2]	$V_{REG}2$ cap load		0.1		500	µF
BW	Bandwidth		100			kHz
LINEREG	Line regulation	DC, V_{BATT} = 3.3V to 7.5V	–0.4		0.4	%
LOADREG	Load regulation	I_{LOAD} = 15mA to 30mA	–5		5	%

NOTES:
1. At $T_j \geq$ 150°C a thermal switch reduces the output current.
2. Recommended load capacitors: In every case $C_{REG}1$ = $C_{REG}2$ = 100nF to ground with series resistance ≤0.1Ω. Additional capacitor optional ≤1000µF with series resistance ≤5Ω.
3. Feedthrough attenuation from the logic input P_{ON} to the outputs $V_{REG}1$ and $V_{REG}2$: ≥40dB.

DC ELECTRICAL CHARACTERISTICS

V_{CC}XXX = PONRx = PONPLL = +3V; V_{EE}XXX = GND1 = GND2 = GND3 = PDTx = 0V; T_A = 25°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{CC}	Supply current					mA
	Rx and IF synthesizer active	PONRx = PONPLL = PDTx = Hi		14	17	
	Tx and IF synthesizer active	PONRx = PDTx = Low; PONPLL = Hi		18	21	
	Power-down mode	PONRx = PONPLL = Low; PDTx = Hi		.007		
V_{REF}	Reference voltage	Generated internally		1.5		V
IV_{REF}	V_{REF} I_{SINK} I_{SOURCE}				100 250	µA
Digital inputs (PDTx, P_{ON}Rx, P_{ON}PLL, P_{ON})						
V_{IH}	High level input voltage range		2.0		V_{CC}TxRx	V
V_{IL}	Low level input voltage range		0		0.8	V
Digital inputs (Clock, Data, Strobe)						
V_{IH}	High level input voltage range		0.7 × V_{CC}DIG		V_{CC}Dig	V
V_{IL}	Low level input voltage range		0		0.3 × V_{CC}DIG	V
Digital outputs (LOCK, AOUT, BOUT)						
V_{OH}	Output voltage HIGH	I_O = -2mA	V_{CC}DIG – 0.4			V
V_{OL}	Output voltage LOW	I_O = 2mA			0.4	V

AC ELECTRICAL CHARACTERISTICS

V_{CC}XXX = P_{ON}Rx = P_{ON}PLL =+3V; V_{EE}XXX = GND1 = GND2 = GND3 = PDTx = 0V; f_{LO} = 800MHz; T_A = 25°C unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
IF Transmit Modulator						
BW	Input modulation bandwidth	200Ω source impedance		2		MHz
	Input signal amplitude	Centered on V_{REF} (V)		V_{REF}/2	V_{REF}/1.75	V_{PK}
THD	Total harmonic distortion[1]	I ITxIn I = I ITxInX I = I QTxIn I = I QTxInX I = ±V_{REF}/2		-50		dBc
R_{INTx}	Input resistance	Between pins: ITxIn and ITxInX or QTxIn and QTxInX	10			kΩ
C_{INTx}	Input capacitance	At ITxIn, ITxInX, QTxIn, QTxInX			10	pF
	Output saturation limit				V_{CC}TxRx-0.3	V
	DC output current	At pins TxIFOUT and TxIFOUTX		2.0		mA
	Offset between DC output currents	At pins TxIFOUT and TxIFOUTX		tbd		µA
	Output current	I ITxIn I = I ITxInX I = I QTxIn I = I QTxInX I = ±V_{REF}/2		0.25		mA_{RMS}
S_{LO}	LO suppression	I ITxIn I = I ITxInX I = I QTxIn I = I QTxInX I = ±V_{REF}/2		-36		dB
SSB	Sideband suppression	I ITxIn I = I ITxInX I = I QTxIn I = I QTxInX I = ±V_{REF}/2		-42		dB
	Equivalent input noise	at 10kHz		tbd		nV/√Hz
t_{ON}	Turn ON time			5		µs
t_{OFF}	Turn OFF time			5		µs

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
IF Receiver						
RInRx	Differential input impedance	f_{IN} = 400MHz		5		kΩ
ROutRx	Output impedance			1		kΩ
	Output common mode voltage			V_{REF}		V
f3dB	Low pass filter -3dB bandwidth	68kΩ resistor between pins RESA and RESB	72	80	88	kHz
	Low pass filter attenuation: 200kHz 400kHz 600kHz 6.5MHz 13.0MHz	68kΩ external resistor between RESA and RESB		34 64 80 >80 >80		dB
VG	Voltage gain	Differential output PD into GSM baseband relative to 1200Ω source EMF	43	50	58	dB
NF	Noise figure at minimum gain	1200Ω source and external matching resistor and inductor		5.8		dB
	Channel matching: Gain Phase			1.0 5.0		dB degrees
	Output DC offset[2]	Differential		200		mV
P_{-1dB}	Input 1dB compression point: In band 200kHz 400kHz 600kHz	1200Ω source EMF		-52 -41 -41 -41		dBV
t_{ON}	Turn-On time	POnRx = V_{EE}		5		μs
t_{OFF}	Turn-off time	POnRx = V_{EE}		5		μs
IF Synthesizer						
f_{LO}	Local oscillator input frequency range		140		1000	MHz
Z_{LOIN}	Differential input impedance	Between pins LO_{IN} and $LO_{IN}X$		tbd		Ω ǁ pF
	LO input range	Referred to 50Ω	300		550	mV_{P-P}
	Programmable divider: Division range Step size		64	1	511	
f_{CLK}	Reference clock input frequency		13, 26, 39 or 52			MHz
Z_{CLKIN}	Differential input impedance	Between pins ClkIn and ClkInX		10 ǁ 1.0		kΩ ǁ pF
	CLK input sensitivity	Referred to 50Ω		200		mV_{P-P}
I_{REF}	Charge pump input reference current			31.2		μA
$\lvert I_{CP} \rvert$	Charge pump output current: C0...C2 = 000 C0...C2 = 111 Step size	I_{REF} =31.2μA, $V_{CP} = V_{CC}CP/2$		0.5 1.0 0.071		mA
$\frac{\Delta I_{CP}}{I_{CP}}$	Relative output current variation[3]	I_{REF} =31.2μA			±10	%
ΔI_{CP_M}	Output current matching[4]	I_{REF} =31.2μA, $V_{CP} = V_{CC}CP/2$			±50	μA

NOTES:

1. Parameter measured relative to modulation sideband amplitude.
2. After programming the DC offset register for minimum offset.
3. The relative output current variation is defined thus: $\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{|(I_2 + I_1)|}$; with $V_1 = 0.3V$, $V_2 = V_{CC}CP - 0.3V$ (see Figure 1).
4. The output current matching is measured when both (positive current and negative current) sections of the output charge pumps are on.

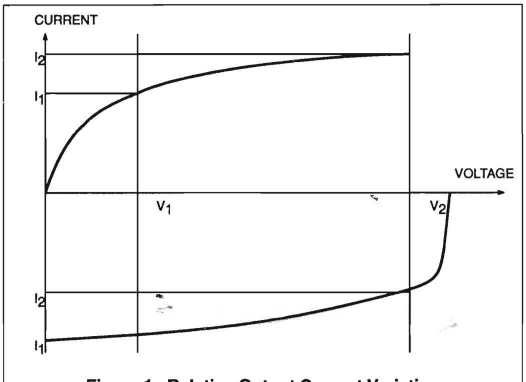


Figure 1. Relative Output Current Variation

FUNCTIONAL DESCRIPTION

Serial Programming Input

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program the counter ratios, charge pump current, status- and DC-offset register, mode select and test register. The programming data is structured into two 21-bit words; each word includes 4 chip address bits and 1 subaddress bit. Figure 2 shows the timing diagram of the serial input. When the STROBE = L, the clock driver is enabled and on the positive edges of the CLOCK the signal on DATA input is clocked into a shift register. When the STROBE = H, the clock is disabled and the data in the shift register remains stable. Depending on the value of the subaddress bit the data is latched into different working registers. Table 1 shows the contents of each word.

Default States

Upon power up (V_{CC}DIG is applied) a reset signal is generated, which sets all registers to a default state. These default states are shown in Table 1.

Reference Divider

The reference divider can be programmed to four different division ratios (:13, :26, :39, :52), see registers r0, r1; default setting: divide by 13.

Main Divider

The external VCO signal, applied to the LO_{IN} and LO_{IN}X inputs, is divided by two and then fed to the main divider (:N). The main divider is a programmable 9 bit divider, the minimum division ratio is divide by 64. The division ratio is binary coded and set in the registers n0 to n8. The default setting is a divide by 400.

At the completion of a main divider cycle, a main divider output is generated which will drive the phase detector.

Phase Detector

The phase detector is a D-type flip-flop phase and frequency detector shown in Figure 3. The flip-flops are set by the negative edges of the output signals of the dividers. The rising edge of the signal L will reset the flip-flops after both flip-flops have been set. Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or deadband around zero phase error. The flip-flops drive on-chip charge pumps. A source current from the charge pump indicates the VCO frequency will be increased; a sink current indicates the VCO frequency will be decreased.

Current Setting

The charge pump current is defined by the current set between the pin I_{REF} and V_{SS}. The current value to be set there is 31.2µA. This current can be set by an external resistor to be connected between the pin I_{REF} and V_{SS}. The typical value R_{EXT} (current setting resistor) can be calculated with the formula

$$R_{EXT} = \frac{V_{CC}CP - 1.4V}{31.2\mu A}$$

The current can be set to zero by connecting the pin I_{REF} to V_{CC}CP.

Charge Pumps

The charge pumps at pin CP are driven by the phase dectector and the current value is determined by the binary value of the charge pumps register CN = c0, c1, c2, default 1mA. The active charge pump current is typically:

$$|I_{CP}| = CN \cdot 71\mu A + 500\mu A$$

Lock Detect

The output LOCK is H when the phase detector indicates a lock condition. This condition is defined as a phase difference of less than ±1 cycle on the reference input CLK_{IN}, CLK_{IN}X.

Test Modes

The LOCK output is selectable as a test output. Bits x0, x1 control the selection, the default setting is normal lock output as described in the Lock detect section. The selection of a Bit x0, x1 combination has a twofold effect: First it routes a divider output signal to the LOCK pin, second it disables mixer stages in the transmit path:

x0	x1	signal at LOCK pin	Transmit Mixer	
			I-mixer	Q-mixer
0	0	normal lock detect	on	on
1	0	CLK_{IN} divided by reference divider ratio	off	on
0	1	LOIN divided by 2 * (main divider ratio)	on	off
1	1	main divider output, that goes to the phase detector	off	off

Power Down Modes

There are 4 power-on pins in the SA1638: P_{ON}, P_{ON}Rx, P_{ON}Tx, P_{ON}PLL.

P_{ON} = H powers up both voltage regulators $V_{REG}1$ and $V_{REG}2$. P_{ON} should be set to L, if these internal voltage regulators are not to be used.

P_{ON}Rx = H powers up the receiver part.

P_{ON}Tx = L powers up the transmitter part.

P_{ON}PLL = H powers up the synthesizer part. As it also powers up the first divide by 2 stage for generating the 0/90 degree phase shifted signals for the transmit and receive mixers, it also has to be set H if either the transmit part or the receive part is used. P_{ON}PLL = L powers down the dividers, resets the phase detector and disconnects the current setting pin I_{REF}. In P_{ON}PLL = L mode, the values in the serial input registers are still kept and the part still can be reprogrammed.

Low voltage IF I/Q transceiver

SA1638

Table 1. Definition of SA1638 Serial Registers

First data word: (shown with default values)

Address SA1638				Sub Adr	N-Divider									Ref ÷ Reg		Charge-Pump			Synth Test	
MSB																				LSB
a0	a1	a2	a3	sa	n0	n1	n2	n3	n4	n5	n6	n7	n8	r0	r1	c0	c1	c2	x0	x1
1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	1	1	1	0	0

Address:	4 bits, a0...a3, fixed to 1110
Sub:Address:	1 bit, sa, fixed to 0 for first data word
N-Divider:	9 bits, n0...n8, values 64 (00100 0000) to 511 (111111111) allowed for IF-choice, default 400
Reference Divider Register:	2 bits, r0...r1, 00 = ÷13, 01 = ÷26, 10 = ÷39, 11 = ÷52. Default: 00
Charge-Pump Register:	3 bits, c0...c2, Binary current setting factor for charge pumps, values 000 = minimum current to 111 = maximum current, default maximum charge pump current
Synthesizer-Test Register:	2 bits, x0...x1, default 00 00 lock detect at LOCK pin 10 reference signal divided by the reference divider ratio at LOCK pin 01 main input signal divided by 2 × (main divider ratio) at LOCK pin 11 main divider output signal going to the phase detector at LOCK pin

Second data word: (shown with default values)

Address SA1638				Sub Adr	Status Reg		DC Offset Register								Mode Select Register					
							I-Channel				Q-Channel									
MSB																				LSB
a0	a1	a2	a3	sa	s0	s1	i0	i1	i2	i3	q0	q1	q2	q3	t0	t1	t2	t3	t4	t5
1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address:	4 bits, a0...a3, fixed to 1110
Sub:Address:	1 bit, sa, fixed to 1 for second data word
Status Register:	2 bits, s0...s1, controls gain/attenuation settings of SA1620 data sheet, see Table 4, Gain Control Logic for LNA1 and LNA2 of the SA1620 data sheet.
DC Offset Register:	4 bits per channel, i0...i3 and q0...q3, no correction as default i0 and q0 switches offset polarity, 0 to lower voltage, 1 to higher voltage il...i3 and q1...q3, 000 no correction to 111 max. correction enabled
Mode Select Register:	6 bits, t0...t5, 000000 = normal GSM-Operation as default 0xxxxx = Rx internal path AC coupled 1xxxxx = Rx internal path DC coupled x0xxxx = Rx LO input applied x1xxxx = Rx LO input replaced by DC offset xx00xx = LLL on xx01xx = LLL on with medium external tune (ADJ IN) xx10xx = LLL off xx11xx = LLL on with fine external tune (ADJ IN) xxxx00 = Rx LP filter 3dB BW = 80kHz (GSM) xxxx11 = Rx LP filter 3dB BW = 580kHz

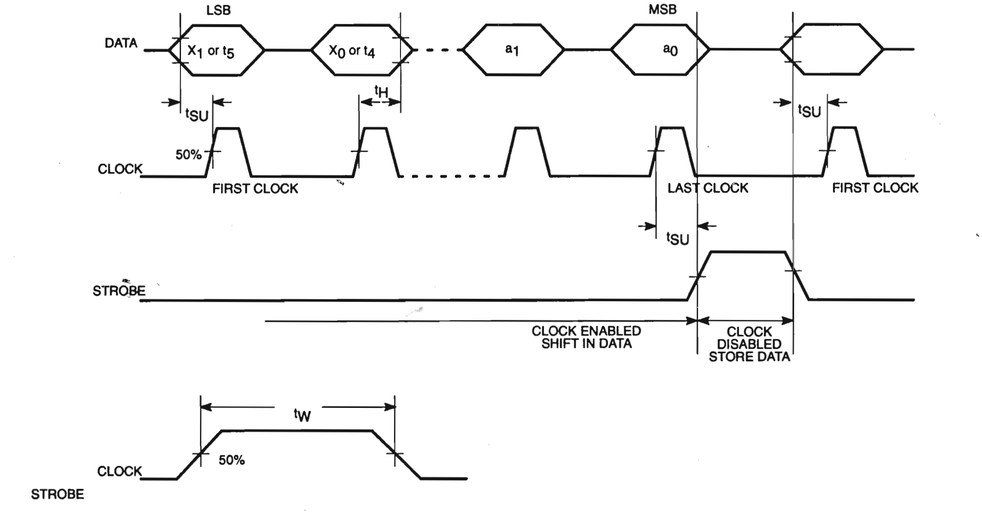


Figure 2. Serial Input Timing Sequence

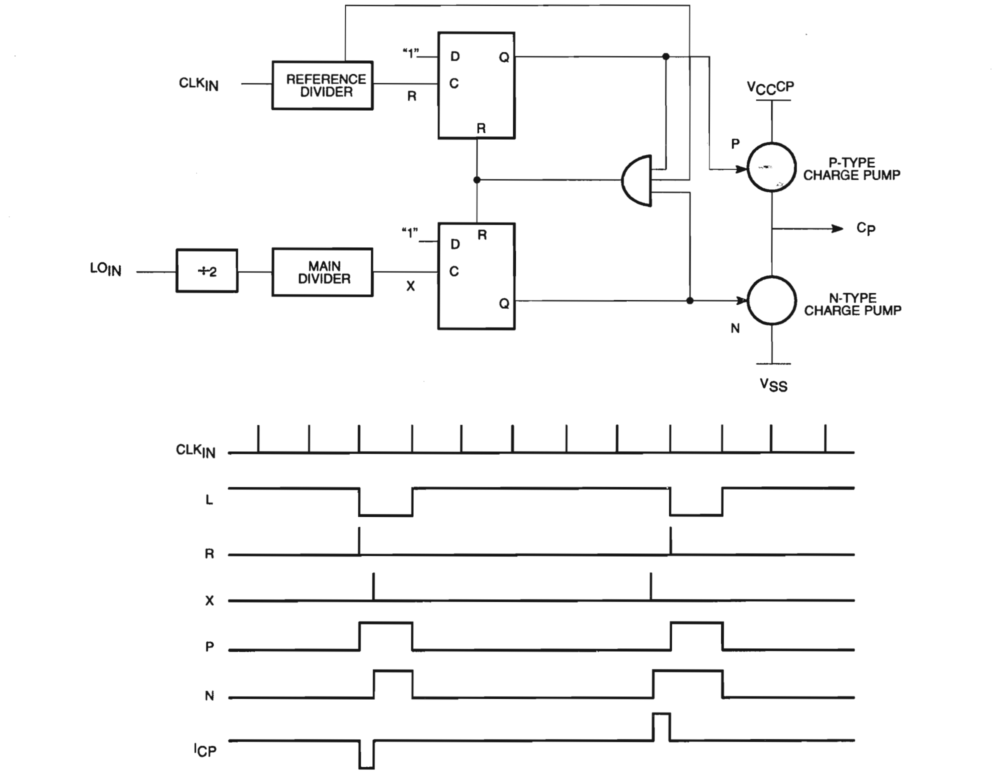
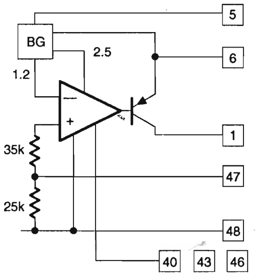
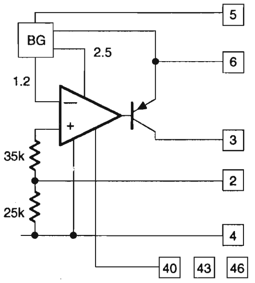
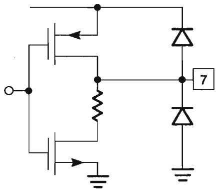
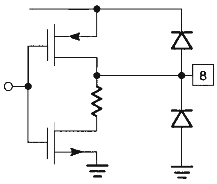
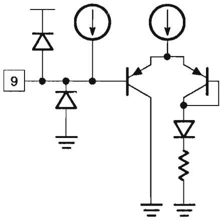
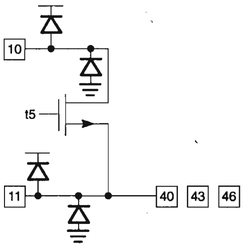
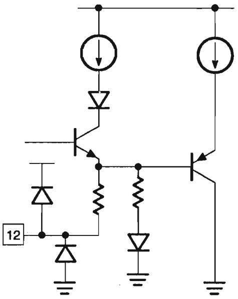
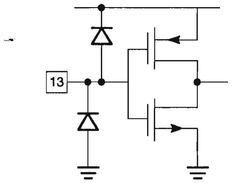
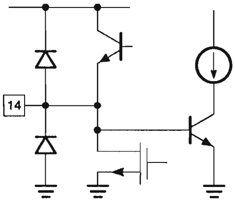
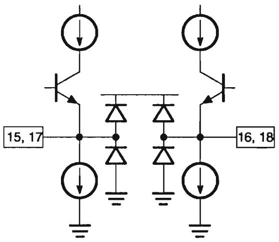


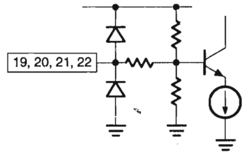
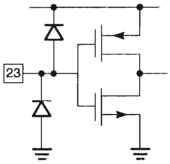
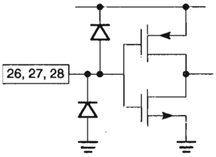
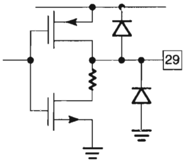
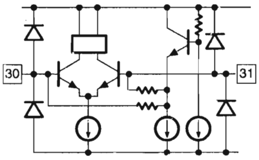
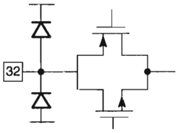
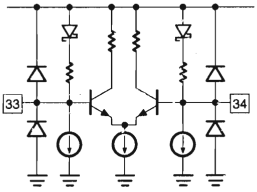
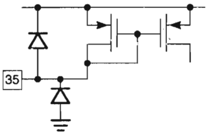
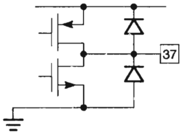
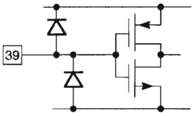
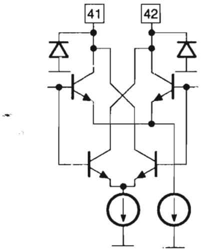
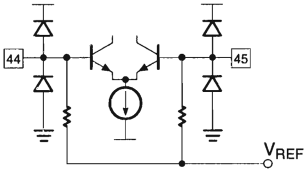
Figure 3. Phase Detector Structure with Timing

PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
47	$V_{CC}TxRx$	3.0	 5 BG 2.5 6 1.2 1 35k 47 25k 48 40 43 46
48	$GND_{REG}1$	0.0	
1	$V_{REG}1$	3.0	
2	$V_{REG}F2$	3.0	 5 BG 2.5 6 1.2 3 35k 2 25k 4 40 43 46
3	$V_{REG}2$	3.0	
4	$GND_{REG}2$	0.0	
5	P_{ON}	3.3	
6	V_{BATT}	3.3	
7	A_{OUT}		
8	B_{OUT}		
9	DC_{RES}		

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
10	RES_D		
11	RES_A	0.00	
12	RES_B		
13	$P_{ON}Rx$		
14	V_{REF}	1.5	
15	IRX_{OUT}	1.5	
16	$IRX_{OUT}X$	1.5	
17	QRX_{OUT}	1.5	
18	$QRX_{OUT}X$	1.5	

PIN FUNCTIONS (continued)

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
19	ITX$_{IN}$	1.5	
20	ITX$_{IN}$X	1.5	
21	QTX$_{IN}$	1.5	
22	QTX$_{IN}$X	1.5	
23	PdTx		
24	V$_{CC}$DIG	3.0	
25	V$_{EE}$DIG	3.0	
26	DATA		
27	CLOCK		
28	STROBE		
29	LOCK		
30	CLK$_{IN}$	2.0	
31	CLK$_{IN}$X	2.0	
32	ADJ$_{IN}$	2.0	
33	LO$_{IN}$	2.0	
34	LO$_{IN}$X	2.0	
35	I$_{REF}$	1.6	
36	V$_{EE}$CP	0.0	
37	CP		
38	V$_{CC}$CP	3.0	
39	P$_{ON}$PLL		
40	GND3	0.0	
41	TXIF$_{OUT}$X	OPEN COLLECTOR	
42	TXIF$_{OUT}$X	OPEN COLLECTOR	
43	GND2	0.0	
44	RxIF$_{IN}$X	1.5	
45	RxIF$_{IN}$	1.5	
46	GND1	0.0	
47	V$_{CC}$TxRx	3.0	
48	GND$_{REG}$1	0.0	

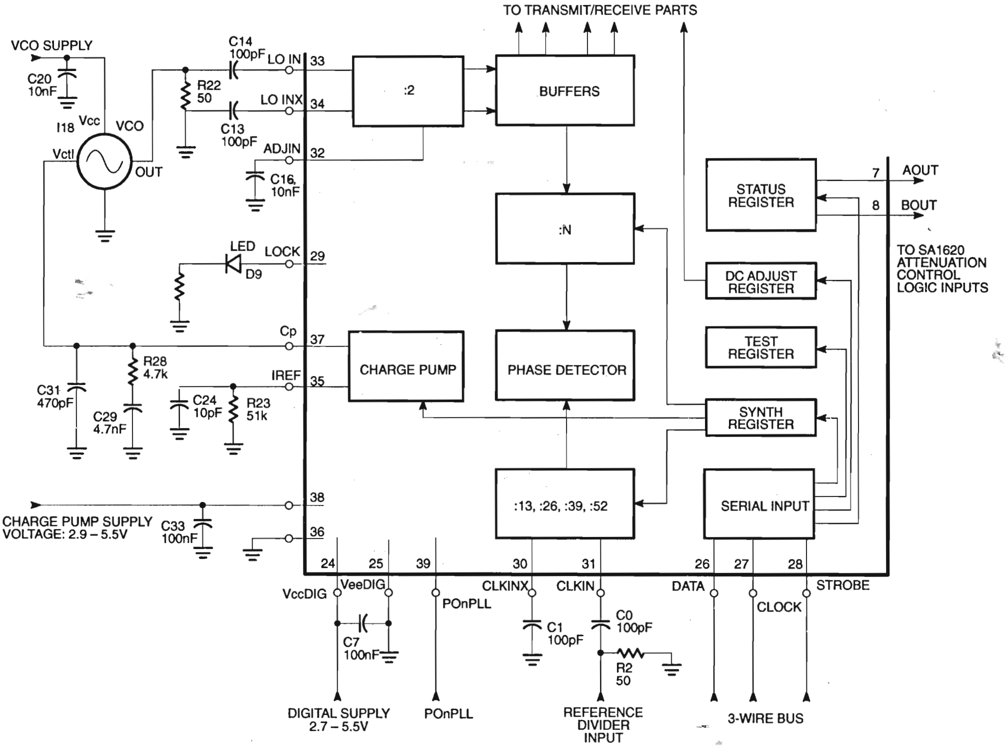


Figure 4. Recommended Application of the Synthesizer Part of SA1638

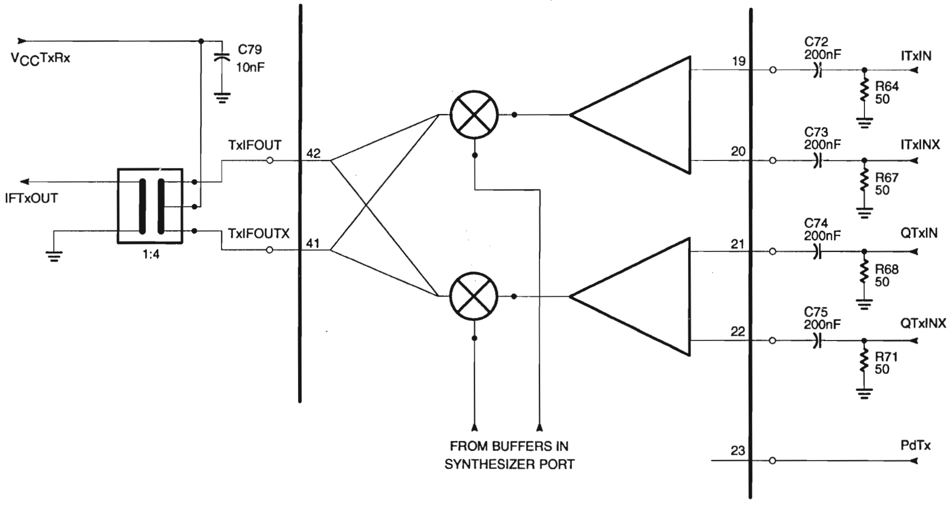


Figure 5. Recommended Application of the Transmit Part of SA1638

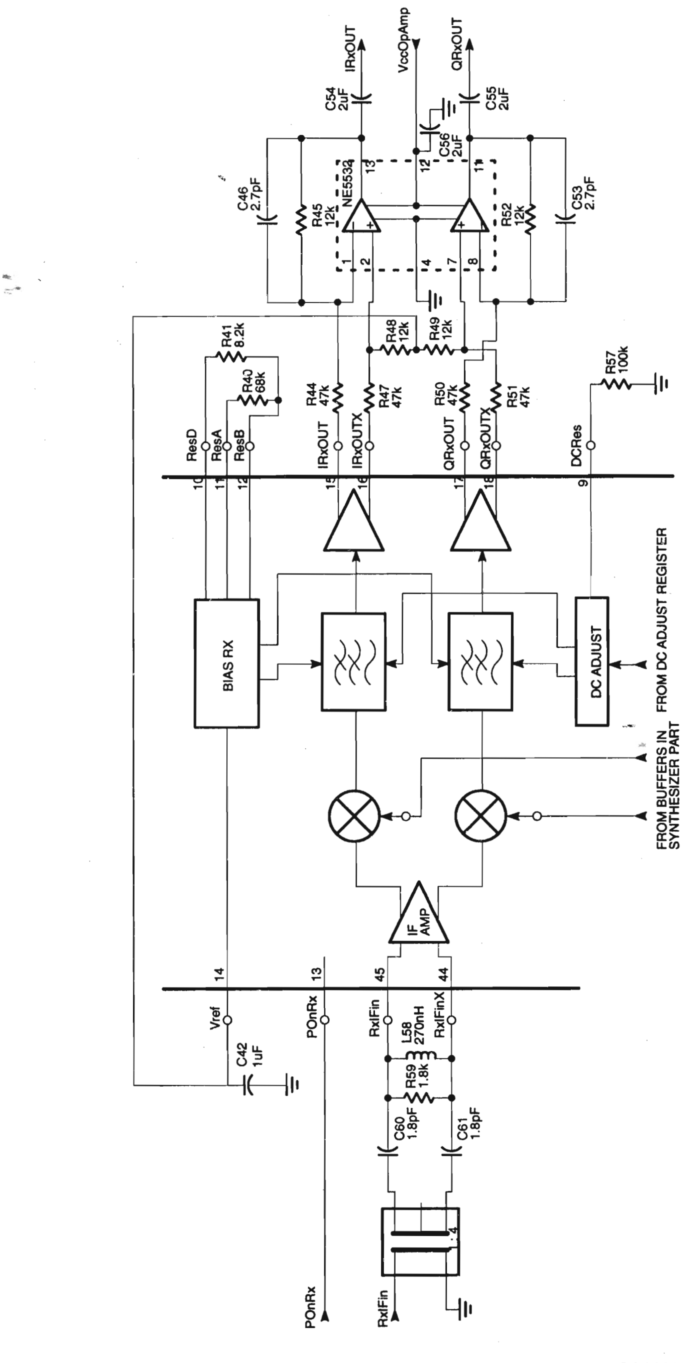
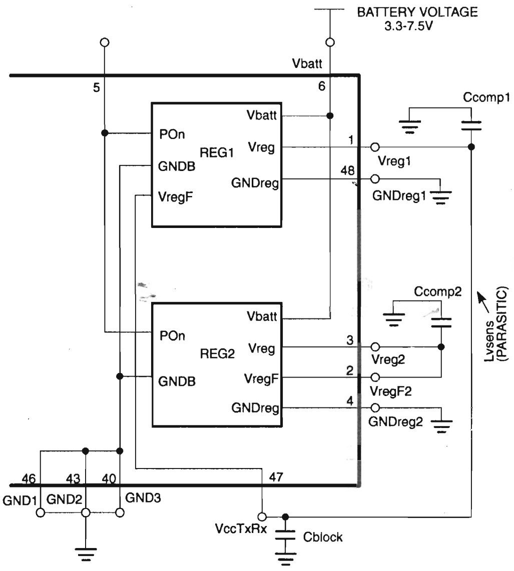


Figure 6. Recommended Application of the Receive Part of the SA1638



$C_{COMP1} = C_{COMP2}$ = 100nF (min) with lowest ≤0.1Ω
L_{VSENS} ≤ 20nH (recommended <10nH)
C_{BLOCK} ≤10μF

Figure 7. Recommended Application of Voltage Registers of the SA1638

Overview of Dual GSM/PCN Architecture

The SA1620 RF front-end and SA1638 IF transceivers form a dual conversion architecture which uses a common IF and standard I/Q baseband interface for both transmit and receive paths. This approach avoids the screening difficulties of direct modulation in the transmit direction and the mass production and practical performance issues related to direct conversion in the receive direction. The time division multiplex nature of the GSM system permits integration of the transmit and receive functions together on the one RF and one IF chips. This simplifies the distribution of local oscillator signals, maximizes circuitry commonality, and reduces power consumption.

The SA1620 and SA1638 allow considerable flexibility to optimize the transceiver design for particular price/size/performance requirements, through choice of appropriate RF and IF filters. The IF may be chosen freely in the range 70–500MHz. The same IF can be used in the transmit and receive directions. Alternately, different IFs can be used if the SA1638 synthesizer frequency is switched between transmit and receive timeslots. The comparison frequency of the SA1638 PLL is high in order to provide fast switching time.

With suitable choice of the IF, an identical SA1638 IF receiver design can be used for both 900MHz GSM and 1800MHz PCN (DCS1800) equipment.

General Benefits/Advantages

- 2.7V operation. Compatible with 3V digital technology and portable applications. (Higher voltage operation also possible, if desired.)
- Excellent dynamic range. The availability of two LNAs in the SA1620 allows flexibility in receiver dynamic design for portable and mobile GSM spec. applications with appropriate filters. If for a particular application a GaAs or discrete front-end is desired, one of the LNAs can be left unpowered. Placing the AGC gain switches at the front results in some attenuation most of the time, further increasing typical dynamic performance beyond that specified by GSM.
- High power transmit output driver, delivering +7.5dBm output. This is sufficient to drive a filter and power amplifier input, without a driver amplifier. To avoid unnecessary current consumption, the output power can be reduced to an appropriate level by choice of an external resistor.
- DC offsets generated in the receive channel are independent of the AGC setting, and correctable by software to prevent erosion of signal handling dynamic range by DC offsets. Independence of DC from AGC setting is achieved by putting the gain switches in the RF front-end.
- Minimal high-quality filter requirements. As a result of the integration in the SA1638 of high quality channel selectivity filters, only sufficient filtering is needed in the receive path to provide blocking protection for the second mixers. This reduces receiver cost and size.
- Operation at a high IF allows RF image reject filter requirements to be relaxed. For example, at a 400MHz IF, the natural gain roll-off in the SA1620 LNAs and mixer suppresses the image signal in the 1800MHz band by typically 28dB below the desired 900MHz band signal.

DC Offset Correction

DC offset correction is provided by two DACs each feeding into one of the two Rx channels. The step size of both DACs is set by the value of the external resistor between DCRES and ground. With a resistor value of 120kΩ, the step size is 200mV. The actual offset of each DAC is controlled independently by 4 bits within a DC register. For each DAC 1 bit controls the polarity of the offset and the other 3 bits control the magnitude of the offset. Thus any original offset less than 1.5V magnitude in either channel can be reduced to the specified level by selecting the appropriate DAC setting via the serial interface.

Integrated Receive Filters

The low-pass characteristics of the Rx channel are determined by two low-pass responses. The first of these is the output of the quadrature mixers and the second is the low-pass filters which follow the post-mixer amplifiers. These specifications refer only to the response of the default state, but this may be switched by the control register to an alternative setting with a nominal 3dB point of 792kHz. In this alternative bandwidth setting, the performance of the circuit is not specified.

The corner frequency of the low pass filters can be adjusted over a wide range by varying the value of the external resistor between RESA and RESB. The range of feasible corner frequencies extends at least between 50kHz and 500kHz. As with the alternative bandwidth setting on the mixer outputs, the performance of the circuit is not specified when the alternative low-pass filter bandwidth is active.

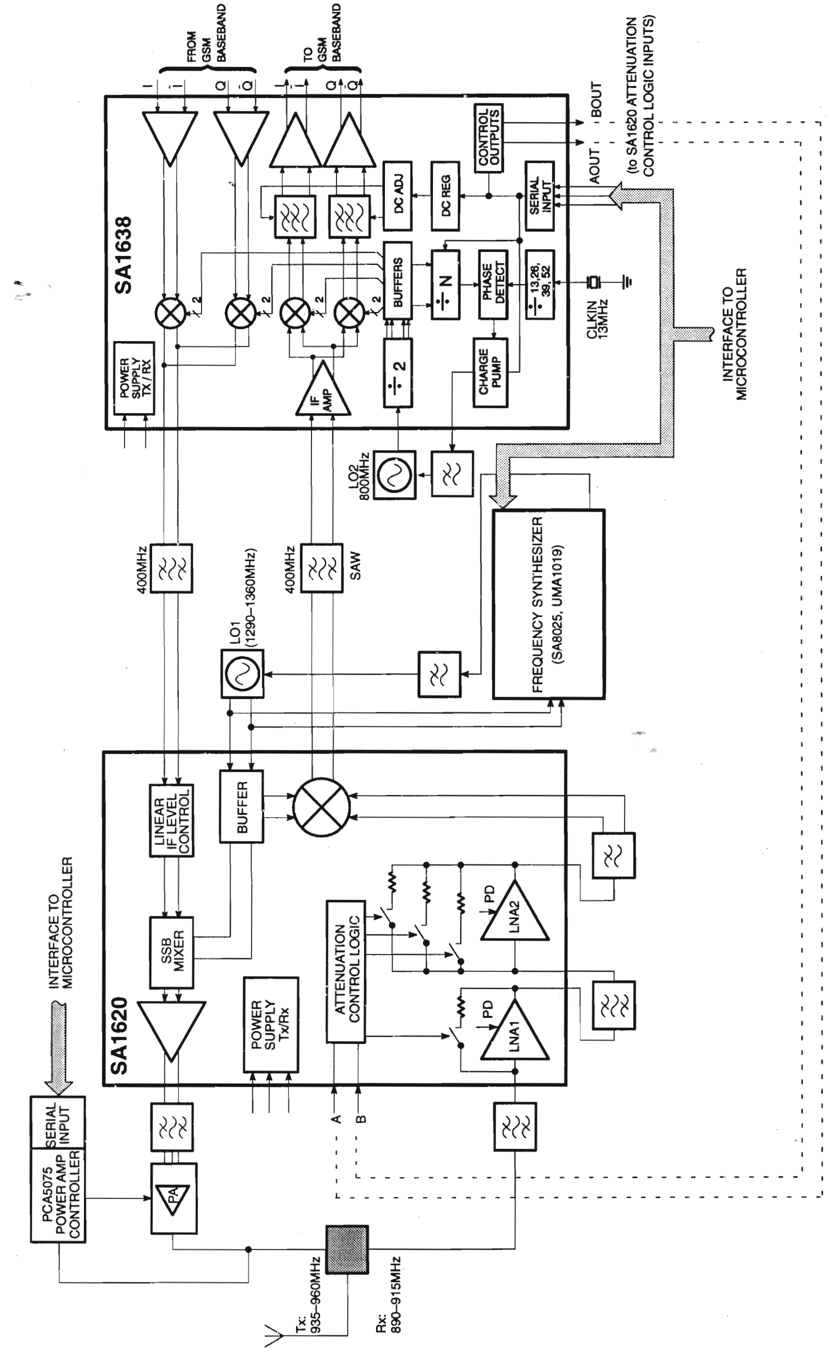

SA1638
FROM GSM BASEBAND
I
Ī
Q
Q̄
TO GSM BASEBAND
I
Ī
Q
Q̄
CONTROL OUTPUTS
AOUT
BOUT
(to SA1620 ATTENUATION CONTROL LOGIC INPUTS)
SERIAL INPUT
DC ADJ
DC REG
BUFFERS
÷ N
PHASE DETECT
÷ 13, 26, 39, 52
CLKIN 13MHz
INTERFACE TO MICROCONTROLLER
÷ 2
CHARGE PUMP
IF AMP
POWER SUPPLY TX / RX
2
LO2 800MHz
FREQUENCY SYNTHESIZER (SA8025, UMA1019)
400MHz
400MHz
SAW
LO1 (1290–1360MHz)
SA1620
LINEAR IF LEVEL CONTROL
BUFFER
SSB MIXER
POWER SUPPLY Tx/Rx
ATTENUATION CONTROL LOGIC
PD
LNA2
PD
LNA1
A
B
INTERFACE TO MICROCONTROLLER
SERIAL INPUT
PCA5075 POWER AMP CONTROLLER
PA
Tx: 935–960MHz
Rx: 890–915MHz

Figure 8.

FM/IF amplifier/demodulator circuit TDA1576T

FEATURES

- Fully balanced 4-stage limiting IF amplifier
- Symmetrical quadrature demodulator
- Field-strengh indication output for 1 mA ammeter
- Detune detector for side response and noise attenuation
- Detune voltage output
- Internal muting circuit
- 0° and 180° AF output signals
- Reference voltage output
- Electronic smoothing of the supply voltage

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)	7.5	8.5	15	V
I_P	supply current	10	16	23	mA
V_{iIF}	input sensivity (RMS value)				
	–3 dB before limiting	14	22	35	μV
	S/N = 26 dB	-	10	-	μV
	S/N = 46 dB	-	55	-	μV
V_{oAF}	AF output signal (RMS value)	-	67	-	mV
THD	total harmonic distortion with double resonant circuits	-	0.02	-	%
S/N	signal-to-noise ratio (V_i > 1 mV)	-	72	-	dB
α_{AM}	AM suppression	-	50	-	dB
RR	ripple rejection (f = 100 Hz)	43	48	-	dB
I_{15}	maximum indicator output current	-	-	2	mA
T_{amb}	operating ambient temperature	–30	-	+80	°C

GENERAL DESCRIPTION

The TDA1576T is a monolithic integrated FM-IF amplifier circuit for use in mono and stereo FM-receivers of car radios or home sets.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1576T	20	mini-pack	plastic	SOT163A

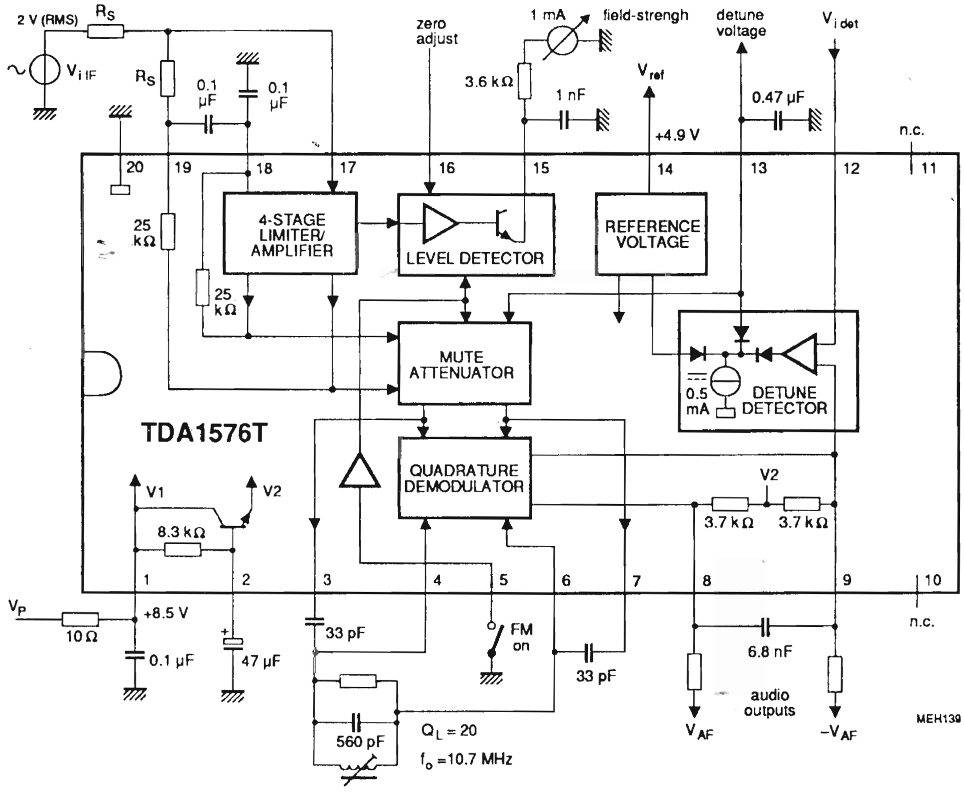


Fig.1 Block diagram and application circuit.

FM/IF amplifier/demodulator circuit TDA1576T

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
C_{PS}	2	smoothing capacitor of power supply
IF1	3	IF signal to resonant circuit
RES1	4	resonant circuit
FMON	5	FM-ON, standby switch
RES2	6	resonant circuit
IF2	7	IF signal to resonant circuit
$V_{o\ AF1}$	8	AF output voltage (0° phase)
$V_{o\ AF2}$	9	AF output voltage (180° phase)
n.c.	10	not connected
n.c.	11	not connected
$V_{i\ det}$	12	detune detector input for external audio reference
$V_{o\ det}$	13	detune detector output voltage
V_{ref}	14	reference voltage output
V_F	15	level output for field-strengh
$V_{F\ o}$	16	zero adjust for field-strengh
$V_{i\ IF}$	17	FM-IF input signal
IN2	18	input 2 of differential IF amplifier
IFLV	19	IF input level
GND	20	ground (0 V)

PIN CONFIGURATION

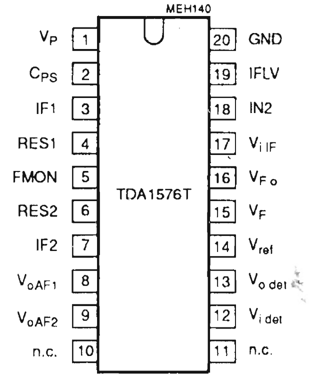


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	0	15	V
$V_{2,\ 5,\ 16}$	voltage on pins 2, 5 and 16	0	V_P	V
P_{tot}	total power dissipation	0	450	mW
T_{stg}	storage temperature range	–55	150	°C
T_{amb}	operating ambient temperature range	–30	+85	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air		85	K/W

CHARACTERISTICS

V_P = 8.5 V; $f_{i\ ZF}$ = 10.7 MHz; R_S = 60 Ω; f_m = 400 Hz with Δf = ±22.5 kHz; 50 µs de-emphasis ($C_{8\text{-}9}$ = 6.8 nF); T_{amb} = 25 °C and measurements taken in Fig.1, unless otherwise specified. The demodulator circuit is adjusted at minimum second harmonic distortion for $V_{i\ ZF}$ = 1 mV and a deviation Δf = ±75 kHz.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 1)		7.5	8.5	15	V
I_P	supply current	$V_5 = V_9 = V_{13} = 0$	10	16	23	mA
Reference voltage						
V_{ref}	reference voltage (pin 14)	$I_{14} = -1$ mA	-	4.9	-	V
ΔV_{ref}	reference voltage dependence on temperature	$\Delta V_{14} / V_{14} \cdot \Delta T$	-	0.3	-	%/K
I_{14}	maximum output current	short-circuit current	4	6	7.5	mA
R_{14}	output resistor ($\Delta V_{14} / \Delta I_{14}$)	$I_{14} < 1.2$ mA	-	60	150	Ω
IF amplifier						
$V_{i\ IF}$	input sensivity (RMS value, pin 17)	−3 dB before limiting	14	22	35	µV
$R_{17\text{-}18}$	input resistance	$V_{i\ IF}$ = 200 mV (RMS)	10	-	-	kΩ
$C_{17\text{-}18}$	input capacitance	$V_{i\ IF}$ = 200 mV (RMS)	-	5	-	pF
$V_{o\ IF}$	output signal at pins 3 and 7 (peak-to-peak value)	$Z_{3,\ 7}$ = 10 pF // 1MΩ	610	680	750	mV
$R_{3\text{-}7}$	output impedance		200	250	300	Ω
Demodulator						
$R_{4\text{-}6}$	input resistance		20	30	40	kΩ
$C_{4\text{-}6}$	input capacitance		-	1	2.5	pF
$R_{8,\ 9}$	output impedance		2.9	3.7	4.5	kΩ
$V_{8,\ 9}$	DC offset voltage on output pins at $V_{4\text{-}6} = 0$	$V_5 > 3$ V or $V_{3\text{-}7} = 0$ or $V_{13} < 0.3$ V	-	0	±100	mV
$\Delta V / \Delta\varphi$	demodulator efficiency	$\Delta V_{8\text{-}9} / \Delta\varphi$	-	40	-	mV/ °
	demodulator efficiency dependent on supply voltage (note 1)	K	-	6.2	-	mV/ °
V/V	DC voltage ratio	$V_8 + V_9 / 2 \cdot V_2$	0.653	0.667	0.680	V/V
ΔV/ΔT	dependence on temperature	$\Delta(V_8 + V_9 / 2 \cdot V_2)/\Delta T$	-	10^{-5}	-	1/K
Field-strength output						
V_{15}	output voltage (Fig.4)	$V_{i\ IF} = 0$	0	0.1	0.25	V
		$V_{i\ IF}$ = 1 mV (RMS)	1.1	1.5	1.9	V
		$V_{i\ IF}$ = 250 mV (RMS)	3.2	3.6	4.1	V
S	control steepness	Fig.4	-	0.85	-	V/dec
R_{15}	output resistance		-	150	200	Ω
ΔV/ΔT	dependence on temperature	$V_{i\ IF} = \Delta V_{15} / (\Delta T \cdot V_{15})$	-	0.3	-	%/K
I_{15}	stand-by operational cut-off current	$V_5 \geq 3$ V; V_{15} = 0 to 5 V	-	-	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero level adjustment						
V_{16}	internal bias voltage		-	260	-	mV
R_{16}	input resistance		-	19	-	kΩ
S	control steepness	$V_{i\ IF} = 100$ mV; $A = \Delta V_{15} / \Delta V_{16}$	0.87	1.0	1.2	V/V
Detuning detector						
I_{12}	input bias current		-	20	100	nA
R_{12}	input resistance (Fig.5)	$5\ V/\Delta I_{12}$	6	30	-	MΩ
V_{13}/V_{14}	output voltage ratio for $\Delta\varphi = \varphi$ (pins 3-7) $- \varphi$ (pins 4-6) $-90°$; (Fig.6)	$V_1 = V_2 = 7.5$ V $R_{13\text{-}14} = 10$ kΩ; pins 9 and 12 short-circuit				
	$\Delta\varphi = 9.2°$ (43 kHz), Q = 20	$V_{9,\ 12} = 334$ mV	0.45	0.5	0.55	V/V
	$\Delta\varphi = 3.5°$ (16 kHz), Q = 20	$V_{9,\ 12} = 138$ mV	0.75	0.8	0.85	V/V
	$\Delta\varphi = 14°$ (65 kHz), Q = 20	$V_{9,\ 12} = 501$ mV	0.335	0.345	0.355	V/V
I_{13}	maximum output current (Fig.7)	$V_{13} = 6$ V	0.4	0.5	0.6	mA
	cut-off current	$V_{13} = 2.5$ V; $V_{9,\ 12} = 0$	-	-	−100	nA
Internal audio attenuation						
V_{13}/V_{14}	output voltage ratio (Fig.8)	α = attenuation factor				
	for $\alpha = 1$ dB		0.11	0.12	0.13	
	for $\alpha = 7.2$ dB		0.095	0.1	0.105	
	for $\alpha \geq 40$ dB		-	0.06	-	
I_{13}	input current	$V_{13} / V_{13} \leq 0.1$	-	-	−225	nA
Stand-by switch						
V_5	input voltage for FM-on	$V_{3,\ 7} / V_{3,\ 7(max)} = 0.9$	2.4	2.5	-	V
	input voltage for FM-off	$V_{19} = 0.3$ V	-	2.9	3	V
	linear range (Fig 9)		-	350	-	mV
I_5	input current	$V_5 = 0$ to 2 V	-	-	−100	μA
		$V_5 = 3.5$ to 15 V	-	-	1	μA
$V_5/\Delta T$	temperature dependence	FM-on ($3.5V_{BE}$)	-	7	-	mV/K
		FM-off ($5V_{BE}$)	-	10	-	mV/K
Supply voltage smoothing						
$V_{1\text{-}2}$	internal voltage drop	proportional to $V_1 - 3V_{BE}$	80	210	400	mV
$R_{1\text{-}2}$	internal resistor		5.8	8.3	10.8	kΩ

OPERATING CHARACTERISTICS

$V_P = 8.5$ V; $f_{i\ ZF} = 10.7$ MHz; $R_S = 60\ \Omega$; $f_m = 400$ Hz with $\Delta f = \pm 22.5$ kHz; 50 μs de-emphasis ($C_{8\text{-}9} = 6.8$ nF); $T_{amb} = 25$ °C and measurements taken in Fig.1, unless otherwise specified. The demodulator circuit is adjusted at minimum second harmonic distortion with $V_{i\ ZF} = 1$ mV.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF amplifier and demodulator						
$V_{i\ IF}$	input sensivity (RMS value, pin 17)	–3 dB before AF limiting	14	22	35	μV
	input signal for S/N = 26 dB	f = 250 to 15000 Hz	-	10	-	μV
	input signal for S/N = 46 dB	f = 250 to 15000 Hz	-	55	-	μV
$V_{o\ AF}$	output signal at (RMS value, pins 8 and 9)		60	67	75	mV
$V_{o\ N}$	noise voltage for $V_{i\ IF} = 0$ (RMS value, pins 8 and 9)	$R_S = 300\ \Omega$ f = 250 to 15000 Hz	-	900	-	μV
	weighted noise voltage according to	DIN 45405	-	2	-	mV
S/N	signal-to-noise ratio Fig.3 (pin 8 and 9)	$V_{i\ IF} = 1$ mV (RMS)	-	72	-	dB
α_{AM}	AM suppression	$V_{i\ IF} = 0.5$ to 200 mV FM: 70 Hz, ±15 kHz AM: 1 kHz, m = 30%	-	50	-	dB
α_{FM}	FM rejection for FM-off	$V_{i\ IF} = 500$ mV; $V_5 = 3$V	80	-	-	dB
$\Delta V_{8,\ 9}$	AFC shift in relation to minimum second harmonic distortion α_{2H}	$V_{i\ IF} = 0.03$ to 500 mV	-	25	-	mV
	DC offset at second harmonic distortion	operating	-	0	±100	mV
		mute or FM-off	-	0	±50	mV
α_{3H}	distortion for third harmonic		-	0.65	-	%
RR	ripple rejection $V_{ripple} = 200$ mV on V_P	f = 100 Hz	43	48	-	dB

Note to the characteristics

1. $V_{8\text{-}9} / \Delta\varphi = K(V_P - 3\ V_{BE})$

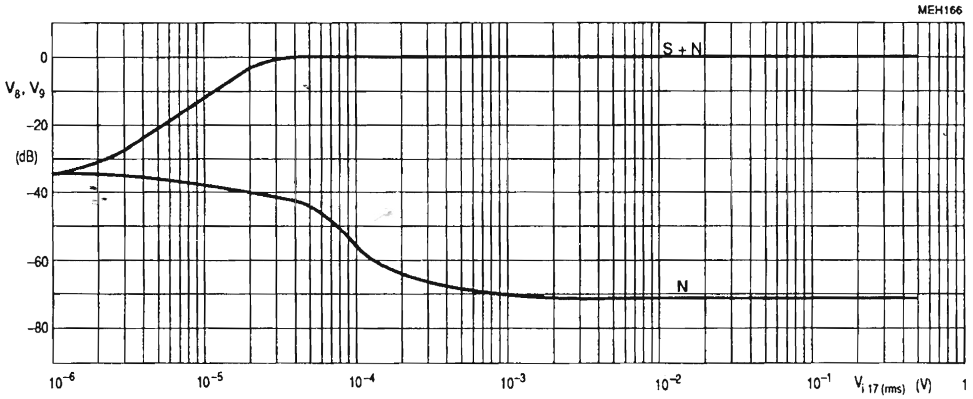


Fig.3 AF output voltage level on pins 8 and 9 as a function of $V_{i\,IF}$ at $V_P = 8.5$ V; $f_m = 1$ kHz; $Q_L = 20$ and with de-emphasis. S = signal; N = noise.

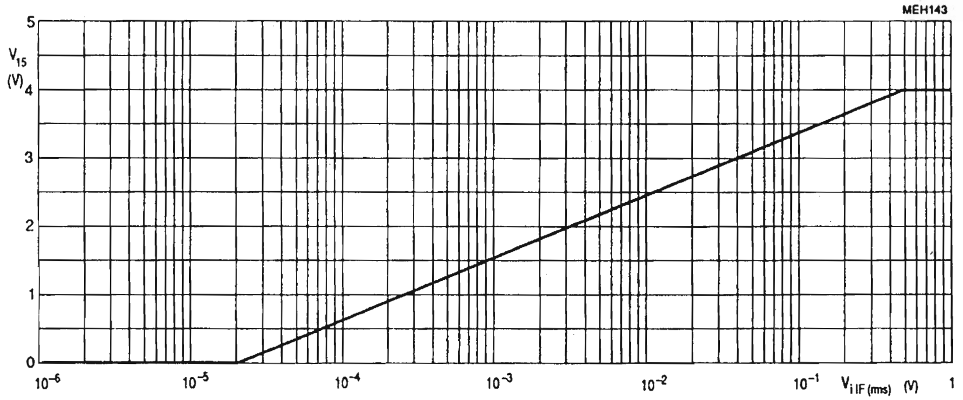


Fig.4 Field-strengh output ($I_{16} = 0$).

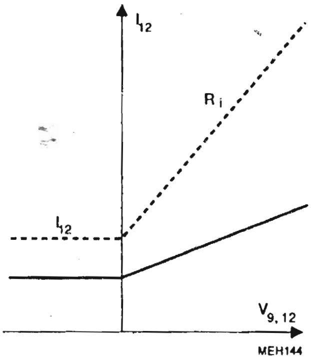


Fig.5 Detuning input impedance.

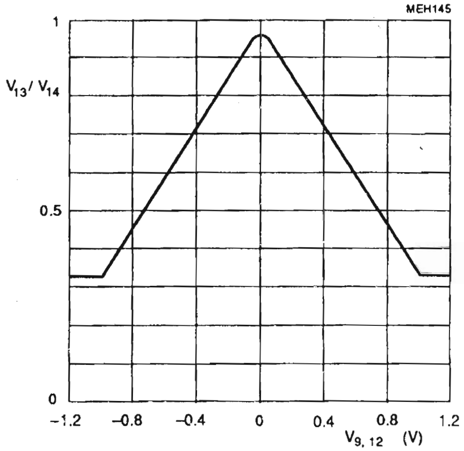


Fig.6 Detuning curve.

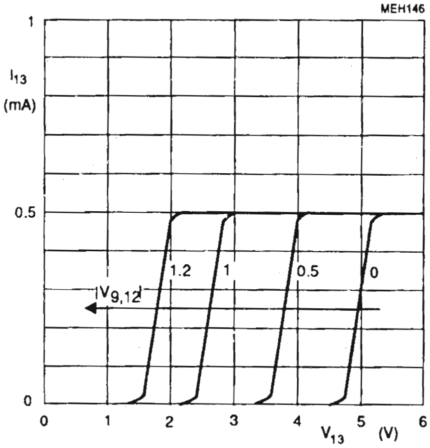


Fig.7 Detuning output.

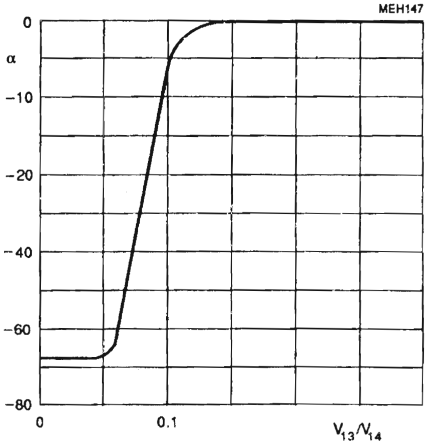


Fig.8 Internal audio attenuation.

Single-chip FM radio circuit

TDA7000

GENERAL DESCRIPTION

The TDA7000 is a monolithic integrated circuit for mono FM portable radios, where a minimum on peripheral components is important (small dimensions and low costs).

The IC has an FLL (Frequency-Locked-Loop) system with an intermediate frequency of 70 kHz. The i.f. selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too noisy input signals. Special precautions are taken to meet the radiation requirements.

The TDA7000 includes the following functions:

- R.F. input stage
- Mixer
- Local oscillator
- I.F. amplifier/limiter
- Phase demodulator
- Mute detector
- Mute switch

QUICK REFERENCE DATA

Supply voltage range (pin 5)	V_P		2,7 to 10	V
Supply current at $V_P = 4{,}5$ V	I_P	typ.	8	mA
R.F. input frequency range	f_{rf}		1,5 to 110	MHz
Sensitivity for −3 dB limiting (e.m.f. voltage) (source impedance: 75 Ω; mute disabled)	EMF	typ.	1,5	μV
Signal handling (e.m.f. voltage) (source impedance: 75 Ω)	EMF	typ.	200	mV
A.F. output voltage at $R_L = 22$ kΩ	V_o	typ.	75	mV

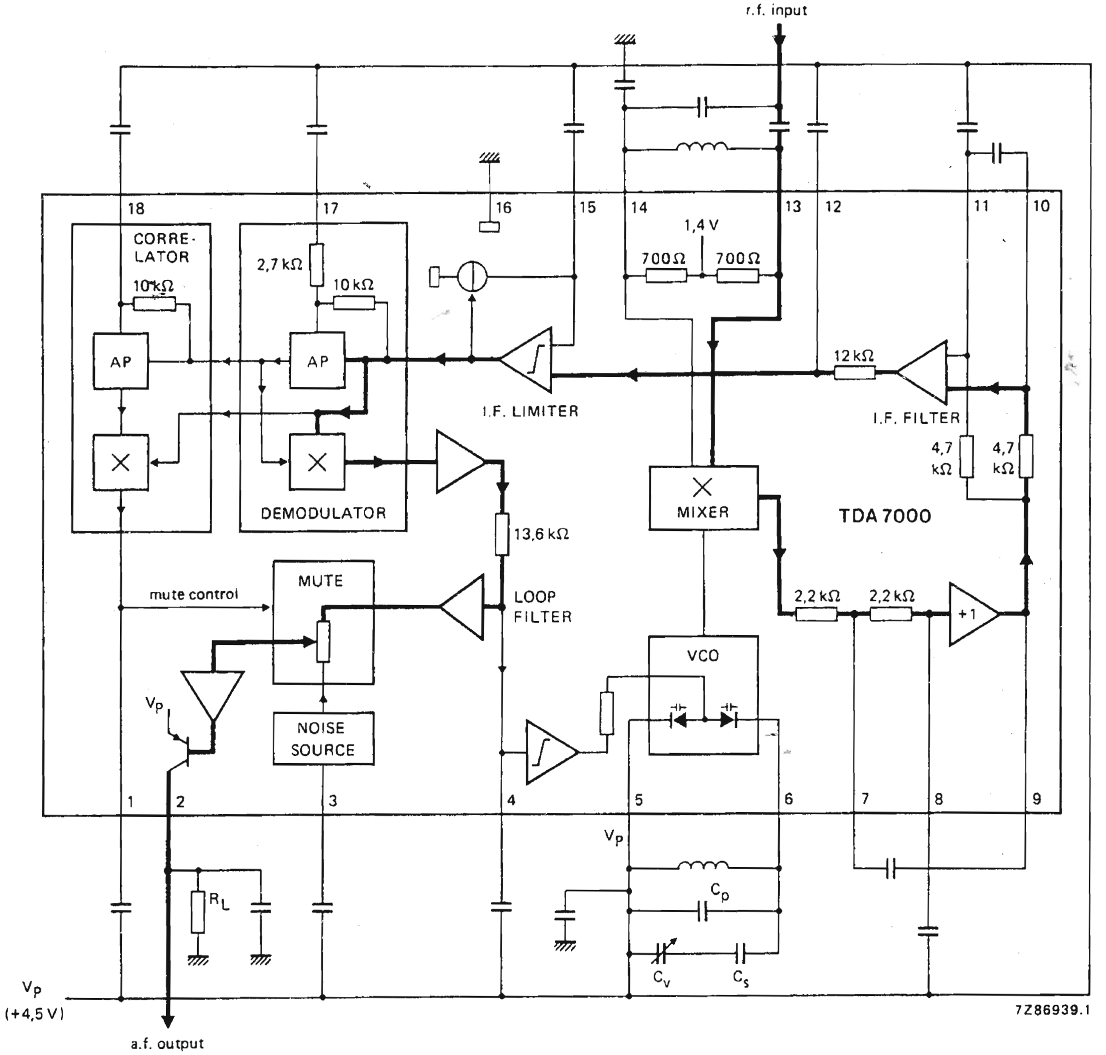


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 5)	V_P	max.	12 V
Oscillator voltage (pin 6)	$V_{6\text{-}5}$	V_P–0,5 to V_P +0,5	V
Total power dissipation	see derating curve Fig. 2		
Storage temperature range	T_{stg}	−55 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to +60	°C

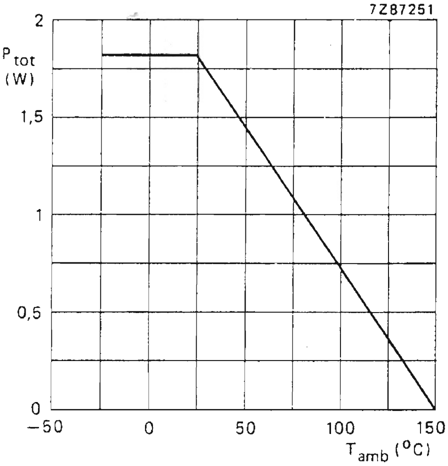


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 5)	V_P	2,7	4,5	10	V
Supply current at V_P = 4,5 V	I_P	–	8	–	mA
Oscillator current (pin 6)	I_6	–	280	–	μA
Voltage at pin 14	$V_{14\text{-}16}$	–	1,35	–	V
Output current at pin 2	I_2	–	60	–	μA
Voltage at pin 2; R_L = 22 kΩ	$V_{2\text{-}16}$	–	1,3	–	V

A.C. CHARACTERISTICS

V_P = 4,5 V; T_{amb} = 25 °C; measured in Fig. 4 (mute switch open, enabled); f_{rf} = 96 MHz (tuned to max. signal at 5 μV e.m.f.) modulated with Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 0,2 mV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Sensitivity (see Fig. 3) (e.m.f. voltage)					
for −3 dB limiting; muting disabled	EMF	–	1,5	–	μV
for −3 dB muting	EMF	–	6	–	μV
for S/N = 26 dB	EMF	–	5,5	–	μV
Signal handling (e.m.f. voltage) for THD < 10%; Δf = ± 75 kHz	EMF	–	200	–	mV
Signal-to-noise ratio	S/N	–	60	–	dB
Total harmonic distortion					
at Δf = ± 22,5 kHz	THD	–	0,7	–	%
at Δf = ± 75 kHz	THD	–	2,3	–	%
AM suppression of output voltage (ratio of the AM output signal referred to the FM output signal) FM signal: f_m = 1 kHz; Δτ = ± 75 kHz AM signal: f_m = 1 kHz; m = 80%	AMS	–	50	–	dB
Ripple rejection (ΔV_P = 100 mV; f = 1 kHz)	RR	–	10	–	dB
Oscillator voltage (r.m.s. value) at pin 6	$V_{6\text{-}5(rms)}$	–	250	–	mV
Variation of oscillator frequency with supply voltage (ΔV_P = 1 V)	Δf_{osc}	–	60	–	kHz/V
Selectivity	S_{+300}	–	45	–	dB
	S_{-300}	–	35	–	dB
A.F.C. range	Δf_{rf}	–	± 300	–	kHz
Audio bandwidth at ΔV_o = 3 dB measured with pre-emphasis (t = 50 μs)	B	–	10	–	kHz
A.F. output voltage (r.m.s. value) at R_L = 22 kΩ	$V_{o(rms)}$	–	75	–	mV
Load resistance					
at V_P = 4,5 V	R_L	–	–	22	kΩ
at V_P = 9,0 V	R_L	–	–	47	kΩ

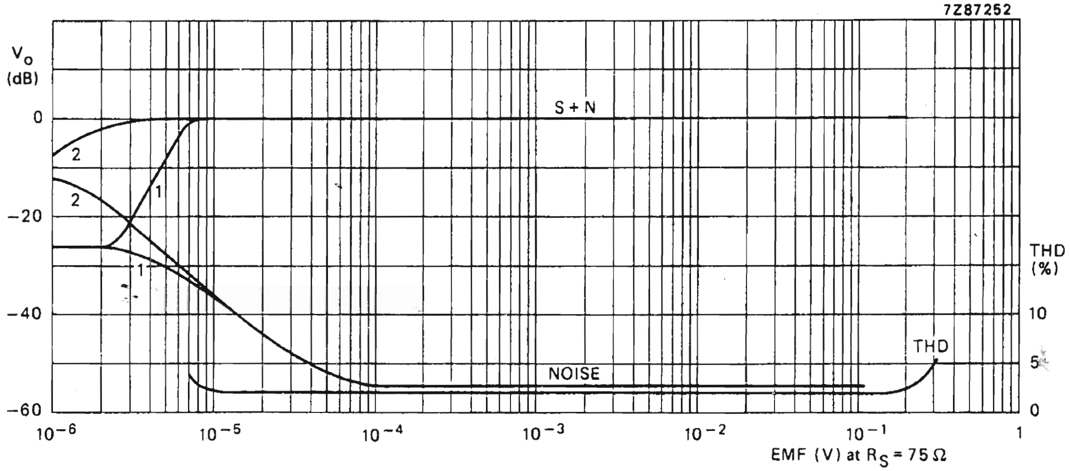


Fig. 3 A.F. output voltage (V_o) and total harmonic distortion (THD) as a function of the e.m.f. input voltage (EMF) with a source impedance (R_S) of 75 Ω: (1) muting system enabled; (2) muting system disabled.

Conditions: 0 dB = 75 mV; f_{rf} = 96 MHz.
for S + N curve: Δf = ± 22,5 kHz; f_m = 1 kHz.
for THD curve: Δf = ± 75 kHz; f_m = 1 kHz.

Notes

1. The muting system can be disabled by feeding a current of about 20 μA into pin 1.
2. The interstation noise level can be decreased by choosing a low-value capacitor at pin 3. Silent tuning can be achieved by omitting this capacitor.

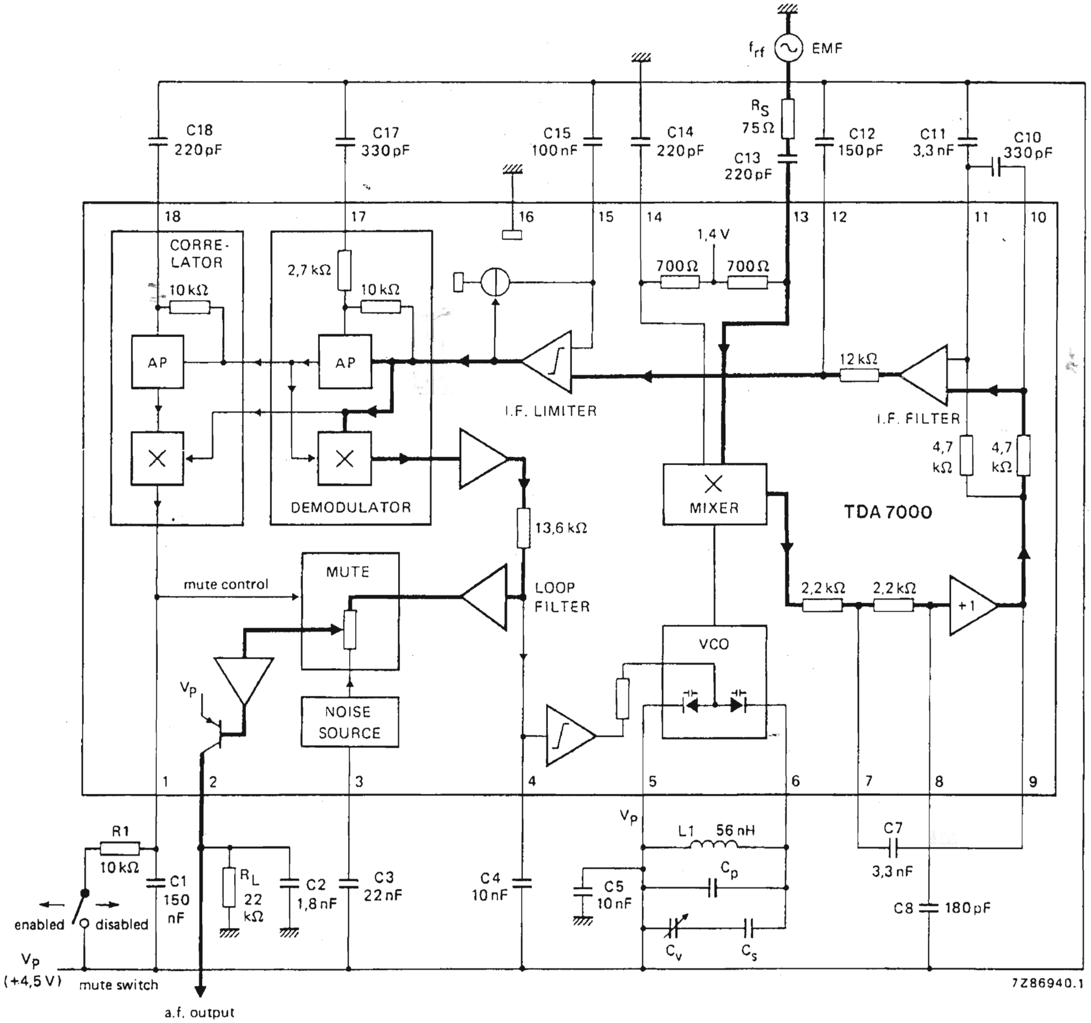
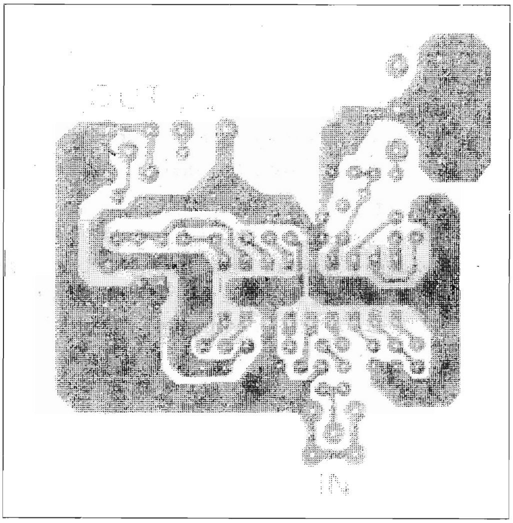


Fig. 4 Test circuit; for printed-circuit boards see Figs 5 and 6.



Track side of printed-circuit board used for the circuit of

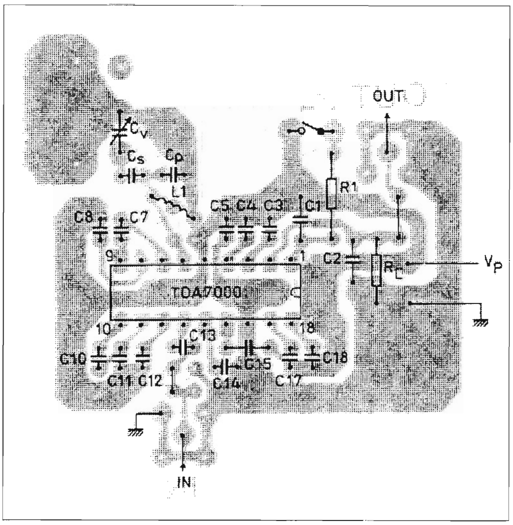


Fig. 6 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

Single-chip FM radio circuit TDA7021T

GENERAL DESCRIPTION

The TDA7021T integrated radio receiver circuit is for portable radios, stereo as well as mono, where a minimum of periphery is important in terms of small dimensions and low cost. It is fully compatible for applications using the low-voltage micro tuning system (MTS). The IC has a frequency locked loop (FLL) system with an intermediate frequency of 76 kHz. The selectivity is obtained by active RC filters. The only function to be tuned is the resonant frequency of the oscillator. Interstation noise as well as noise from receiving weak signals is reduced by a correlation mute system.

Special precautions have been taken to meet local oscillator radiation requirements. Because of the low intermediate frequency, low pass filtering of the MUX signal is required to avoid noise when receiving stereo. 50 kHz roll-off compensation, needed because of the low pass characteristic of the FLL, is performed by the integrated LF amplifier. For mono application this amplifier can be used to directly drive an earphone. The field-strength detector enables field-strength dependent channel separation control.

Features

- RF input stage
- Mixer
- Local oscillator
- IF amplifier/limiter
- Frequency detector
- Mute circuit
- MTS compatible
- Loop amplifier
- Internal reference circuit
- LF amplifier for
  - mono earphone amplifier or
  - MUX filter
- Field-strength dependent channel separation control facility

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)		$V_P = V_{4-3}$	1,8	—	6,0	V
Supply current	$V_P = 3$ V	I_4	—	6,3	—	mA
RF input frequency		f_{rf}	1,5	—	110	MHz
Sensitivity (e.m.f.) for −3 dB limiting	source impedance = 75 Ω; mute disabled	EMF	—	4	—	μV
Signal handling (e.m.f.)	source impedance = 75 Ω	EMF	—	200	—	mV
AF output voltage		V_o	—	90	—	mV

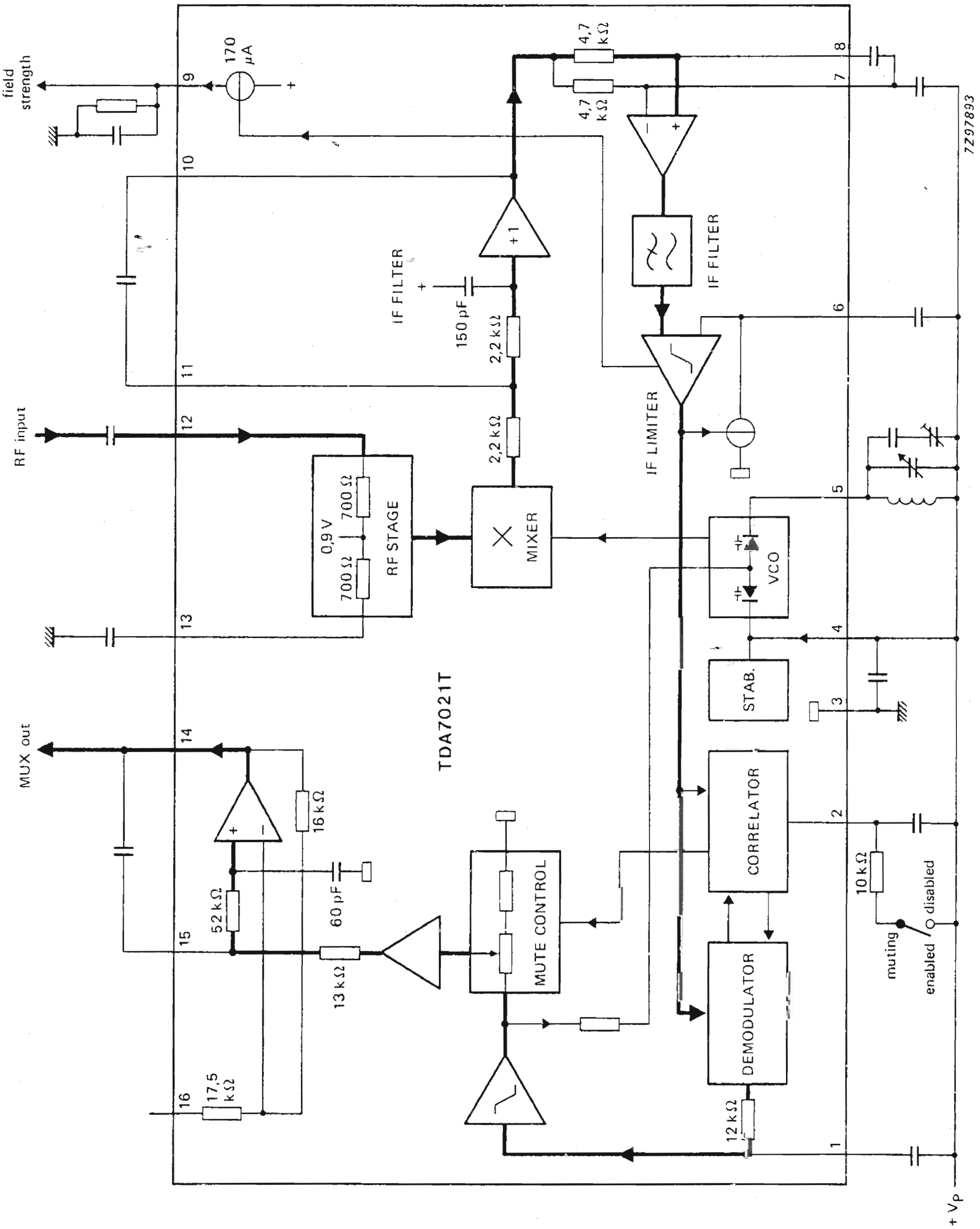


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage (pin 4)		$V_P = V_{4\text{-}3}$	–	7,0	V
Oscillator voltage		$V_{5\text{-}4}$	V_P–0,5	V_P + 0,5	V
Storage temperature range		T_{stg}	–55	+150	°C
Operating ambient temperature range		T_{amb}	–10	+70	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 300 K/W

DC CHARACTERISTICS

V_P = 3 V, T_{amb} = 25 °C, measured in circuit of Fig. 4, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 4)		$V_P = V_{4\text{-}3}$	1,8	3,0	6,0	V
Supply current	V_P = 3 V	I_4	–	6,3	–	mA
Oscillator current		I_5	–	250	–	µA
Voltage at pin 13		$V_{13\text{-}3}$	–	0,9	–	V
Output voltage (pin 14)		$V_{14\text{-}3}$	–	1,3	–	V

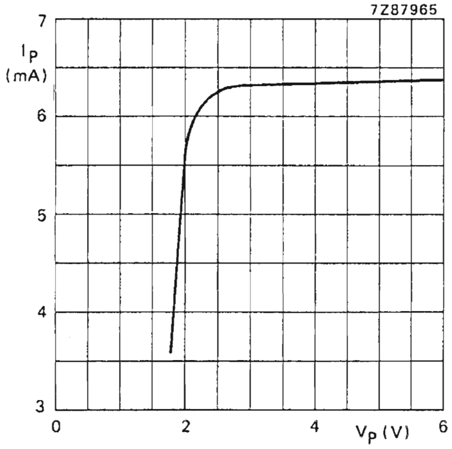


Fig. 2 Supply current as a function of the supply voltage.

AC CHARACTERISTICS (MONO OPERATION)

V_P = 3 V; T_{amb} = 25 °C; measured in Fig. 5; f_{rf} = 96 MHz modulated with Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 0,3 mV (e.m.f. at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Sensitivity (e.m.f.)	see Fig. 3					
for −3 dB limiting	muting disabled	EMF	–	4,0	–	µV
for −3 dB muting		EMF	–	5,0	–	µV
for (S+N)/N = 26 dB		EMF	–	7,0	–	µV
Signal handling (e.m.f.)	THD < 10%; Δf = ± 75 kHz	EMF	–	200	–	mV
Signal-to-noise ratio		(S+N)/N	–	60	–	dB
Total harmonic distortion	Δf = ± 22,5 kHz	THD	–	0,7	–	%
	Δf = ± 75 kHz	THD	–	2,3	–	%
AM suppression of output voltage	ratio of AM signal (f_m = 1 kHz; m = 80%) to FM signal (f_m = 1 kHz; Δf = 75 kHz)	AMS	–	50	–	dB
Ripple rejection	ΔV_P = 100 mV; f = 1 kHz	RR	–	30	–	dB
Oscillator voltage (r.m.s. value)		$V_{5\text{-}4(rms)}$	–	250	–	mV
Variation of oscillator frequency with temperature	V_P = 1 V	$\frac{\Delta f_{osc}}{\Delta T_{amb}}$	–	5	–	kHz/°C
Selectivity	see Fig. 9; no modulation	S_{+300}	–	46	–	dB
		S_{-300}	–	30	–	dB
AFC range		$\pm\Delta f_{rf}$	–	160	–	kHz
Mute range		$\pm\Delta f_{rf}$	–	120	–	kHz
Audio bandwidth	ΔV_o = 3 dB; measured with 50 µs pre-emphasis	B	–	10	–	kHz
AF output voltage (r.m.s. value)	R_L (pin 14) = 100 Ω	$V_{o(rms)}$	–	90	–	mV
AF output current						
max. d.c. load		$I_{o(dc)}$	−100	–	+100	µA
max. a.c. load (peak value)	THD = 10%	$I_{o(ac)}$	–	3	–	mA

Single-chip FM radio circuit

TDA7021T

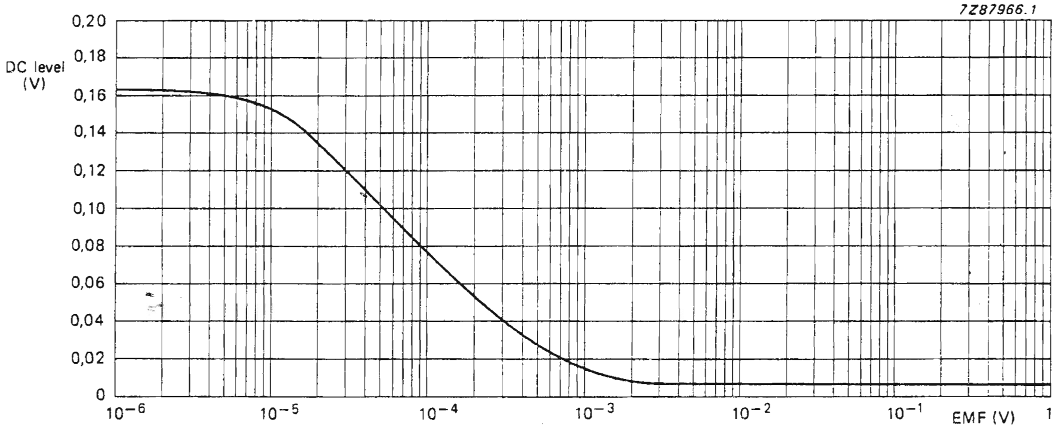


Fig. 3 Field strength voltage ($V_{9\text{-}3}$) at R_{source} = 1 kΩ; f = 96,75 MHz; Vp = 3 V.

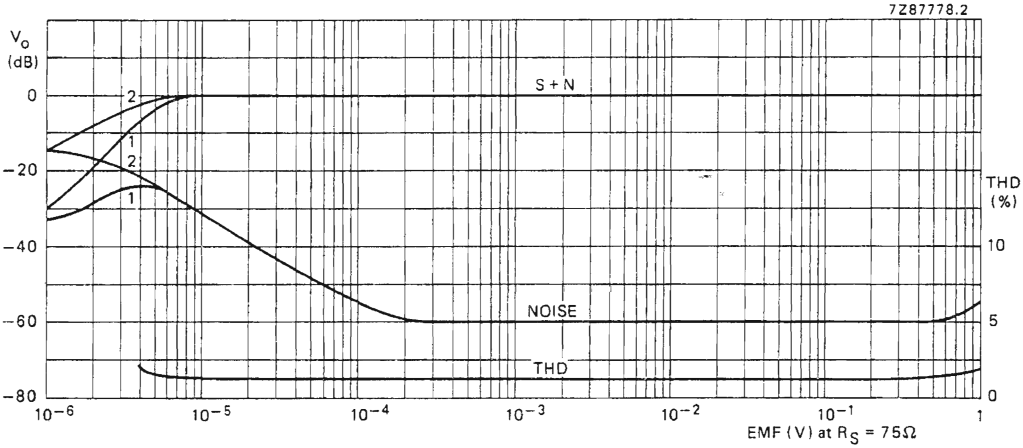
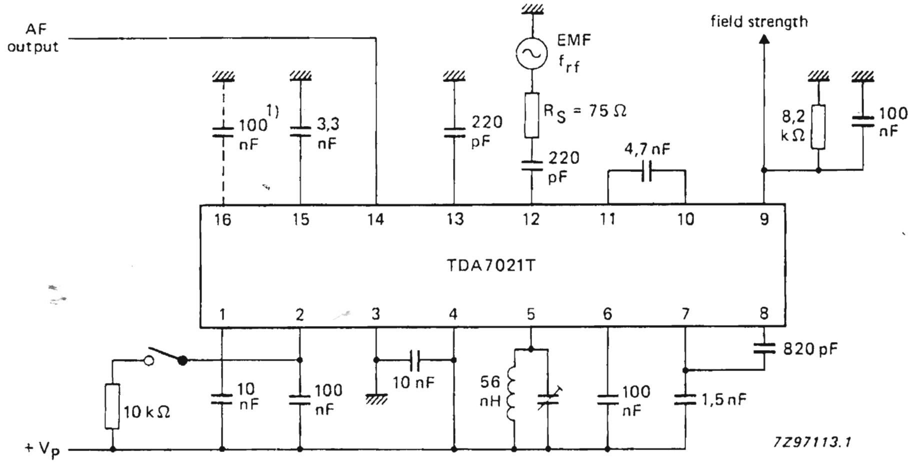


Fig. 4 Mono operation: AF output voltage (V_o) and total harmonic distortion (THD) as functions of input e.m.f. (EMF); R_{source} = 75 Ω; f_{rf} = 96 MHz; 0 dB = 90 mV. For S+N and noise curves (1) is with muting enabled and (2) is with muting disabled; signal Δf = ± 22,5 kHz and f_m = 1 kHz. For THD curve, Δf = ± 75 kHz and f_m = 1 kHz.



1) The AF output can be decreased by disconnecting the 100 nF capacitor from pin 16.

Fig. 5 Test circuit for mono operation.

AC CHARACTERISTICS (STEREO OPERATION)

V_P = 3 V; T_{amb} = 25 °C; measured in Fig. 8; f_{rf} = 96 MHz modulated with pilot Δf = ± 6,75 kHz and AF signal Δf = ± 22,5 kHz; f_m = 1 kHz; EMF = 1 mV (e.m.f. at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Sensitivity (e.m.f.) for (S+N)/N = 26 dB	see Fig. 8; pilot off	EMF	–	11	–	μV
Selectivity	see Fig. 9; no modulation	S_{+300}	–	40	–	dB
		S_{-300}	–	22	–	dB
Signal-to-noise ratio		(S+N)/N	–	50	–	dB
Channel separation	V_i = L-signal; f_m = 1 kHz; pilot on: at f_{rf} = 97 MHz	α	–	26	–	dB
	at f_{rf} = 87,5 MHz and 108 MHz	α	–	14	–	dB

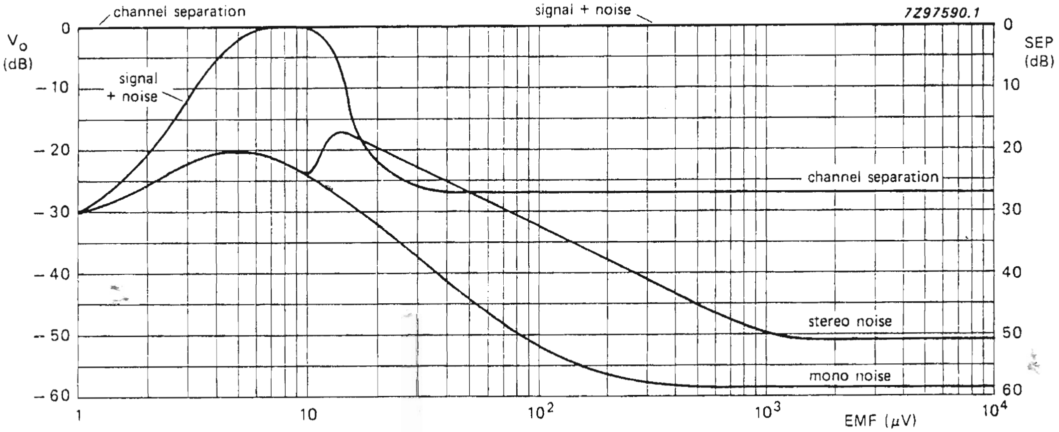


Fig. 6 Stereo operation: signal/noise and channel separation of TDA7021T when used in the circuit of Fig. 8.

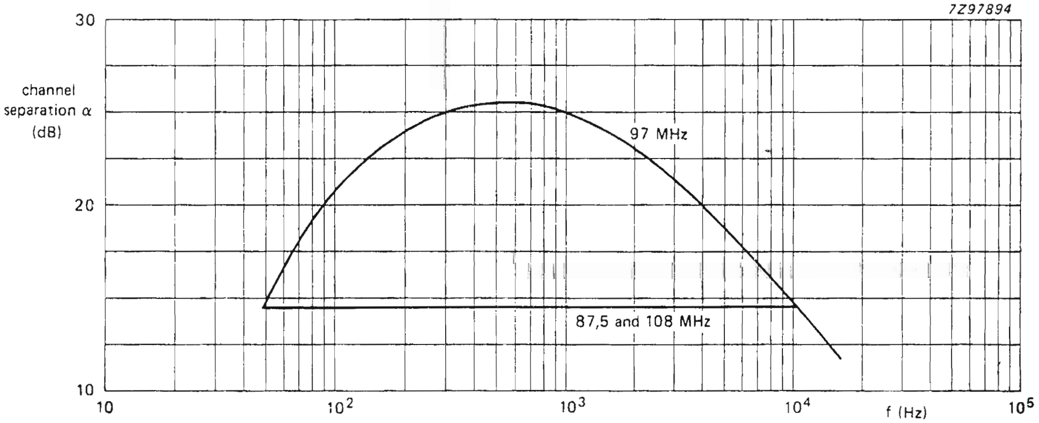


Fig. 7 Stereo operation: channel separation as a function of audio frequency in the circuit of Fig. 8.

Single-chip FM radio circuit

TDA7021T

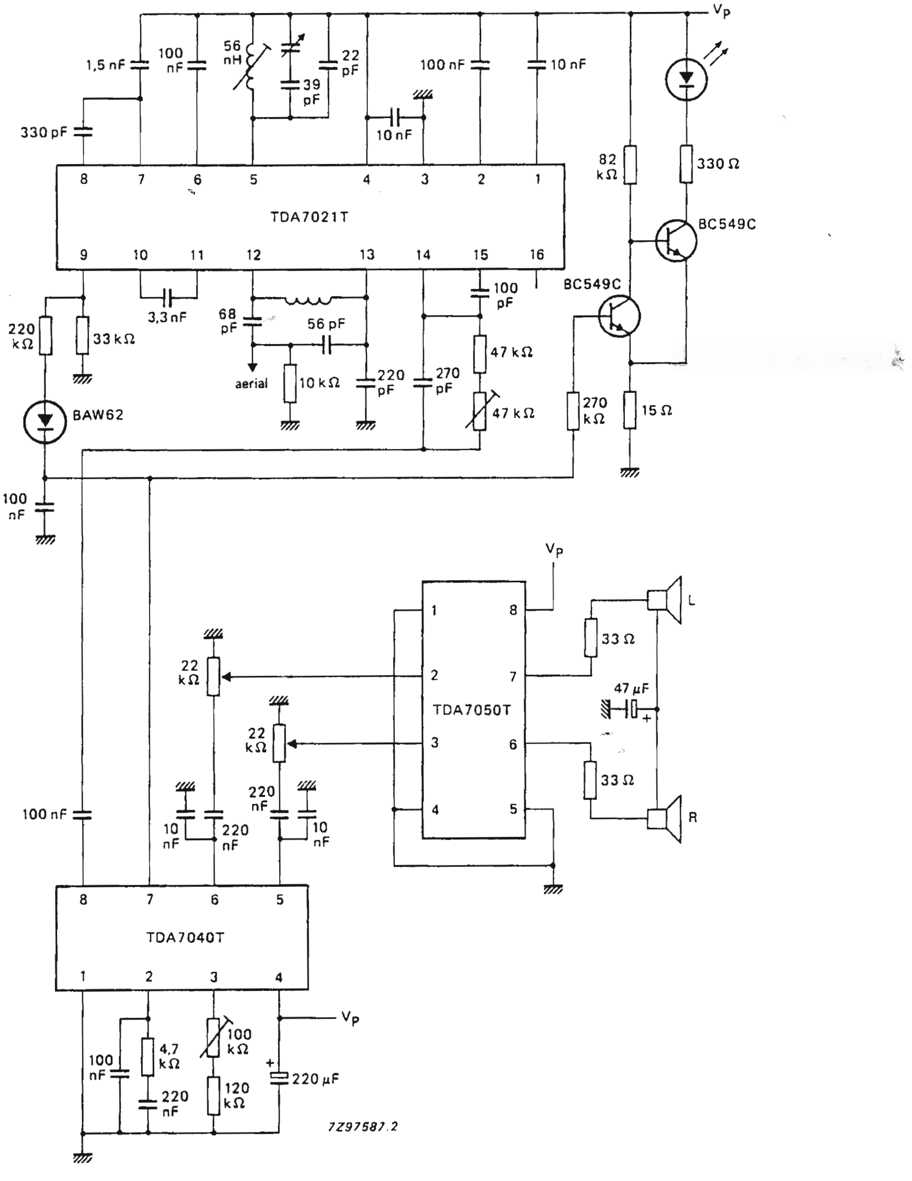


Fig. 8 Stereo application in combination with a low voltage PLL stereo decoder (TDA7040T) and a low voltage mono/stereo power amplifier (TDA7050T).

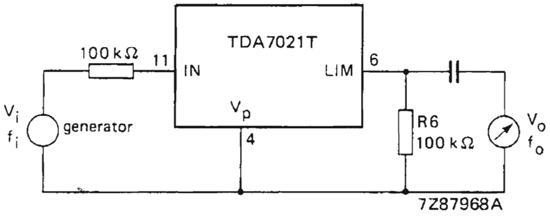


Fig. 9 Test set-up; V_i = 30 mV; f_i = 76 kHz; selective voltmeter at output has $R_i \geqslant 1$ MΩ and $C_i \leqslant 8$ pF; $f_o = f_i$.

Note to Fig. 9

This test set-up is to incorporate the circuit of Fig. 5 for mono operation or the circuit of Fig. 8 for stereo operation. For either circuit, replace the 100 nF capacitor at pin 6 with R6 (100 kΩ) as shown above.

Selectivity

$$S_{+300} = 20 \log \frac{V_o \mid (300\,\text{kHz} - f_i)}{V_o \mid f_i} \qquad S_{-300} = 20 \log \frac{V_o \mid (300\,\text{kHz} + f_i)}{V_o \mid f_i}$$

Section 5

Frequency Synthesizers and Prescalers

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Frequency Synthesizer Selector Guide 734
SA701 Divide by: 128/129-64/65 dual modulus low power ECL prescaler 735
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SA7025 Low-voltage 1GHz fractional-N synthesizer 756
SA8025 Low-voltage 2GHz fractional-N synthesizer 774
AN1891 SA8025 Fractional-N synthesizer for 2GHz band applications 792
TDD1742T CMOS frequency synthesizer 806
TSA6057/T Radio tuning PLL frequency synthesizer 828
TSA5511 1.3GHz bi-directional I^{2}C bus controlled synthesizer 837
UMA1005T Dual low-power frequency synthesizer 848
UMA1014 Low-power frequency synthesizer for mobile radio communications 866
SCO/AN91004 Application report for the UMA1014T frequency synthesizer 879
UMA1015M Low-power dual frequency synthesizer for radio communications 907
UMA1017M Low-voltage frequency synthesizer for radiotelephones 923
UMA1018M Low-voltage dual frequency synthesizer for radio telephones 934
UMA1019AM Low-voltage frequency synthesizer for radio telephones 946
UMA1019M Low-voltage dual frequency synthesizer for radio telephones 957
UMA1020AM Low-voltage dual frequency synthesizer for radio telephones 968
UMA1020M Low-voltage dual frequency synthesizer for radio telephones 980

Frequency Synthesizer Selector Guide

The Philips Family of High Performance Frequency Synthesizers

	Vcc	Icc	Pins	Pkg	Max RF/Input Frequency	Channel Spacing	Fractional-N Divider	Auxiliary Synthesizer	Applications
Fractional-N Frequency Synthesizers									
SA7025DK	2.7 to 5.5V	7.5mA@3V	20	SSOP20	1.0GHz (main) 150MHz (aux) 40MHz (aux)	10-5000kHz (main) 40-20,000kHz (aux) 10-5000kHz (aux)	✓	✓	NADC (IS-54), PDC, GSM digital cellular
SA8025DK	2.7 to 5.5V	11mA@3V	20	SSOP20	1.8GHz (main) 150MHz (aux) 40MHz (aux)	10-5000kHz (main) 40-20,000kHz (aux) 10-5000kHz (aux)	✓	✓	PHS digital cordless, PDC digital cellular
UMA1005T	2.9 to 5.5V	5mA@3V	20	SSOP20	30MHz (main) 90MHz (aux) 30MHz (aux)	10-5000kHz (main) 40-20,000kHz (aux) 10-5000kHz (aux)	✓	✓	NADC (IS-54), PDC, GSM digital cellular
Frequency Synthesizers									
UMA 1014T	4.5 to 5.5V	13mA@5V	16	SO16	1.1GHz	5-100kHz			AMPS/TACS cellular, cordless
UMA1015M	2.7 to 5.5V	9.6mA@3V	20	SSOP20	1.1GHz 1.1GHz	8.5-375kHz		✓ (Dual)	CT1/CT1 + cordless AMPS/TACS NMT cellular
UMA1016xT	4.5 to 5.5V	10mA@5V	16	SO16	1.0GHz	100-1000kHz			cordless spread spectrum
UMA1017M	2.7 to 5.5V	8.5mA@3V	20	SSOP20	1200MHz	10-2000kHz			GSM digital cellular, spread spectrum
UMA1018M	2.7 to 5.5V	8.5mA@3V	20	SSOP20	1200MHz (main) 300MHz (aux)	10-2000kHz (main) 10-1000kHz (aux)		✓	GSM digital cellular
UMA1019AM	2.7 to 5.5V	12mA@3V	20	SSOP20	1750 MHz	10-2000kHz			DECT digital cordless, DCS 1800
UMA1020M	2.7 to 5.5V	12mA@3V	20	SSOP20	2400MHz (main) 300MHz (aux)	10-2000kHz (main) 10-2000kHz (aux)		✓	DECT digital cordless, DCS1800

	Vcc	Icc	Pins	Pkg	Max Input Frequency	Max Compare Frequency	Input Sensitivity	Divide Ratio
Prescalers								
SA701N, D	2.7 to 6V	4.5mA@3V	8	DIP, S08	1.1GHz	65kHz/270kHz	-35dBm	128/129, 64/65
SA702N, D	2.7 to 6V	4.5mA@3V	8	DIP, S08	1.1GHz	1000kHz	-35dBm	64/65/72
SA703N, D	2.7 to 6V	4.5mA@3V	8	DIP, S08	1.1GHz	335kHz	-35dBm	128/129/144

Divide by: 128/129-64/65 dual modulus low power ECL prescaler

SA701

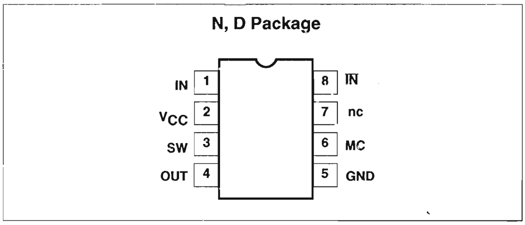
DESCRIPTION

The SA701 is an advanced dual modulus (Divide By 128/129 or 64/65) low power ECL prescaler. The minimum supply voltage is 2.7V and is compatible with the CMOS UMA1005 synthesizer from Philips and other logic circuits. The low supply current allows application in battery operated low-power equipment. Maximum input signal frequency is 1.1GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the QUBiC process. The circuit will be available in an 8-pin SO package with 150 mil package width and in 8-pin dual in-line plastic package, and is pin compatible with Fujitsu MB501, Plessey SP8704 and Motorola MC12022.

FEATURES

- Low voltage operation
- Low current consumption
- Operation up to 1.1GHz
- ESD hardened

PIN CONFIGURATION



APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

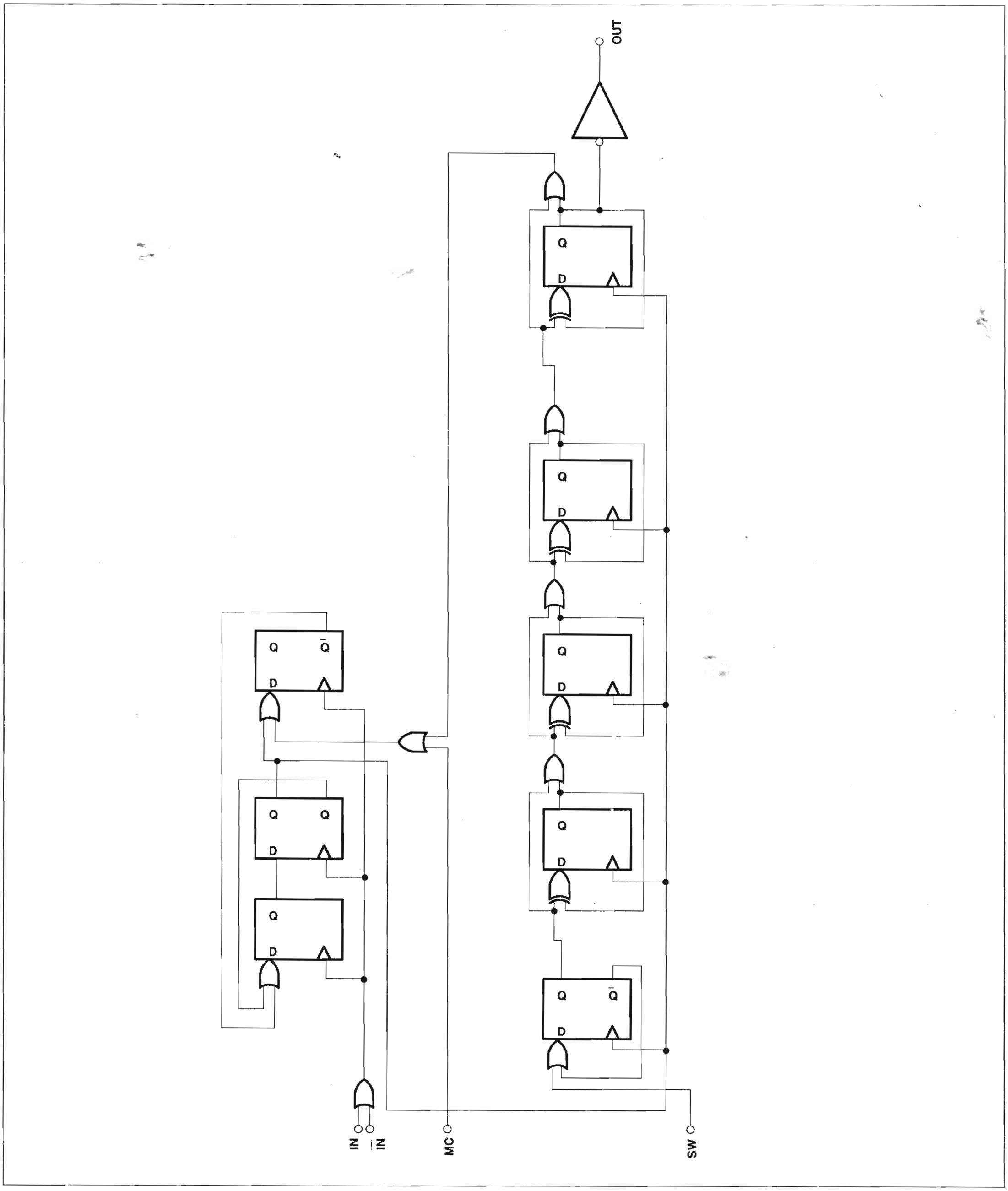
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA701N	0404B
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA701D	0174C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +7.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance D package N package	158 108	°C/W

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for $T_A = 25°C$ and $V_{CC} = 3.0V$; unless otherwise stated. Test circuit Figure 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range	f_{IN} = 1GHz, input level = 0dBm	2.7		6.0	V
I_{CC}	Supply current	No load		4.5		mA
V_{OH}	Output high level	I_{OUT} = 1.2mA	V_{CC}-1.4			V
V_{OL}	Output low level			V_{CC}-2.6		V
V_{IH}	MC input high threshold		2.0		V_{CC}	V
V_{IL}	MC input low threshold		–0.3		0.8	V
V_{IH}	SW input high threshold		2.0		V_{CC}	V
V_{IL}	SW input low threshold		–0.3		0.8	V
I_{IH}	MC input high current	$V_{MC} = V_{CC} = 6V$		0.1	50	µA
I_{IL}	MC input low current	$V_{MC} = 0V$, $V_{CC} = 6V$	–100	–30		µA
I_{IH}	SW input high current	$V_{SW} = V_{CC} = 6V$		35	100	µA
I_{IL}	SW input low current	$V_{SW} = 0V$, $V_{CC} = 6V$	–50	–0.1		µA

AC ELECTRICAL CHARACTERISTICS

The following AC specifications are valid for $V_{CC} = 3.0V$, f_{IN} = 1GHz, input level = 0dBm, $T_A = 25°C$; unless otherwise stated. Test circuit Fig. 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude[1]	1000pF input coupling	0.05		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input[2]	0		1.1	GHz
		1000pF input coupling			1.1	GHz
R_{ID}	Differential input resistance	DC measurement		5		kΩ
V_O	Output voltage	$V_{CC} = 5.0V$		1.6		V_{P-P}
		$V_{CC} = 3.0V$		1.2		V_{P-P}
t_S	Modulus set-up time[1]				5	ns
t_H	Modulus hold time[1]				0	ns
t_{PD}	Propagation time			10		ns

NOTES:

1. Maximum limit is not tested, however, it is guaranteed by design and characterization.
2. For $f_{IN} < 50MHz$, minimum input slew rate of 32V/µs is required.

DESCRIPTION OF OPERATION

The SA701 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for SW (Modulus Set Switch) input to be set low and MC (Modulus Control) input to be set high in which case the circuit comprises a divide by 128. For divide by 129 the MC signal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the synchronous counter. Similarly, for divide by 64 and 65 the SA701 will generate those respective moduli with the SW signal forced high, in which the fourth stage of the synchronous divider is bypassed. A truth table for the modulus values is given below:

Table 1.

Modulus	MC	SW
128	1	0
129	0	0
64	1	1
65	0	1

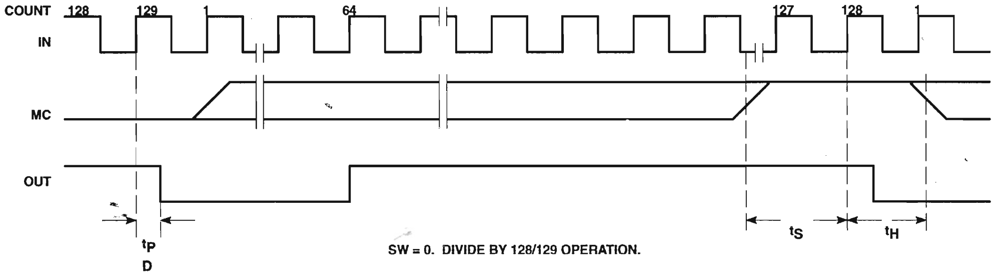
For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 64 for modulus 128/129 or count 32 for modulus 64/65 with delay t_{PD}. The SW input is not designed for synchronous switching.

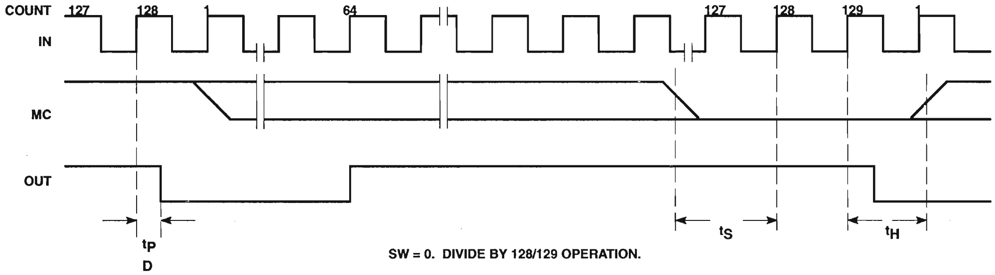
The MC and SW inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed. The SW input has an internal pull-down simplifying modulus group selection. With SW open the divide by 128/129 mode is selected and with SW connected to V_{CC} divide by 64/65 is selected.

The prescaler input is differential and ECL compatible. The output is single-ended ECL compatible.

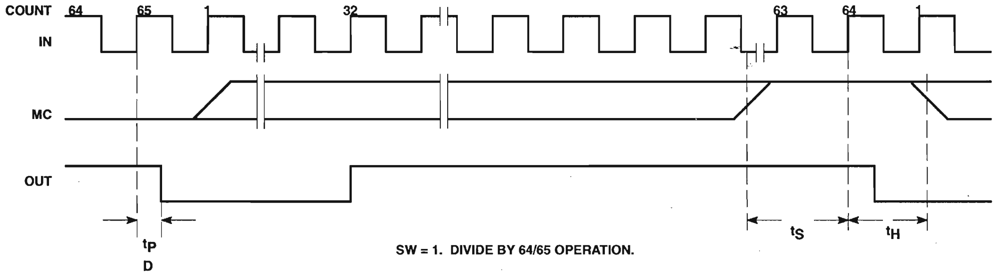
AC TIMING CHARACTERISTICS



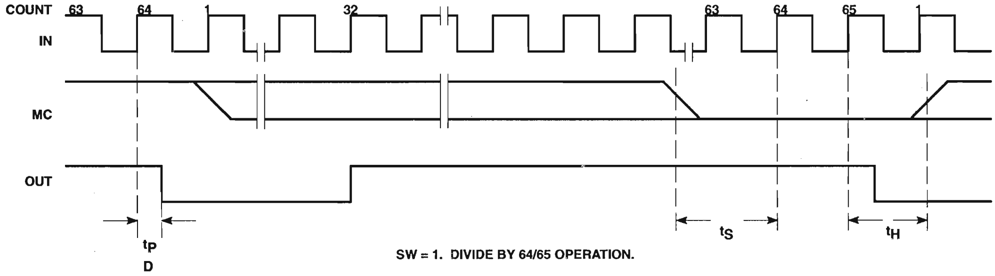
SW = 0. DIVIDE BY 128/129 OPERATION.



SW = 0. DIVIDE BY 128/129 OPERATION.



SW = 1. DIVIDE BY 64/65 OPERATION.



SW = 1. DIVIDE BY 64/65 OPERATION.

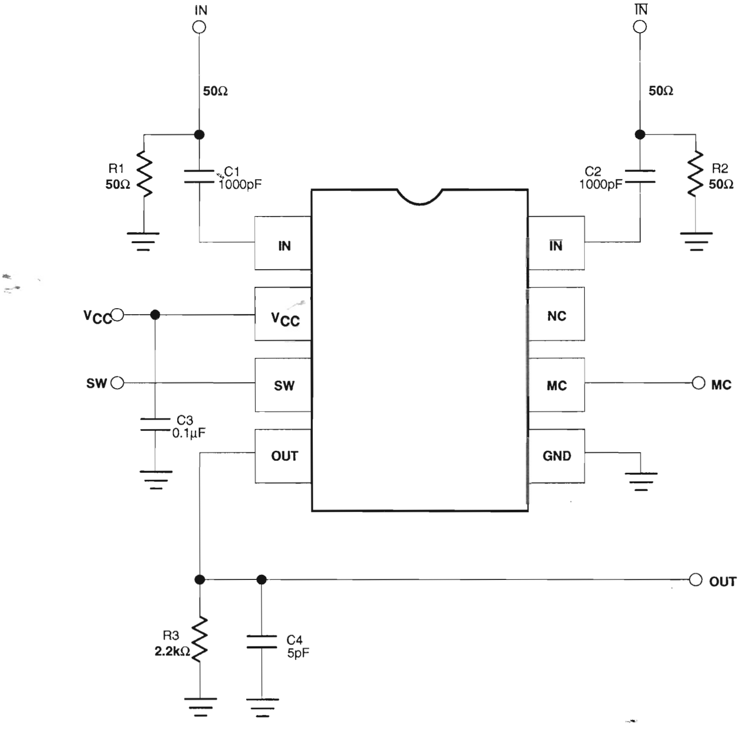


Figure 1. SA701 Test Circuit

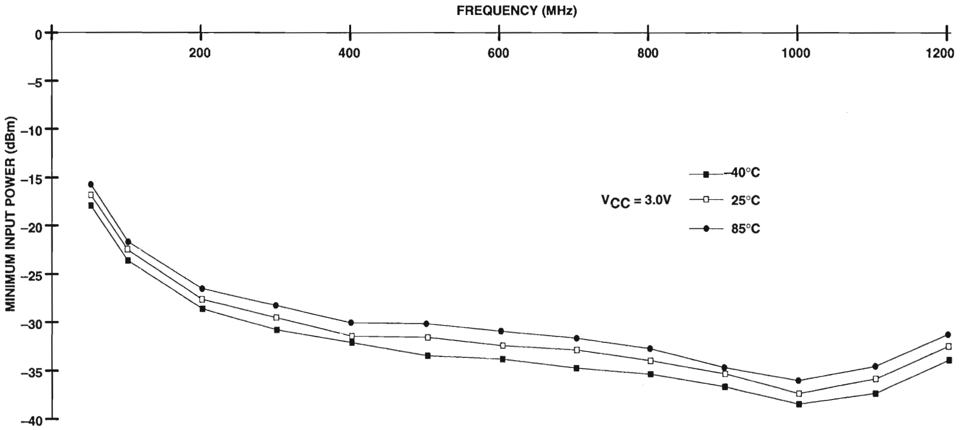


Figure 2. Minimum Input Power vs Frequency and Temperature

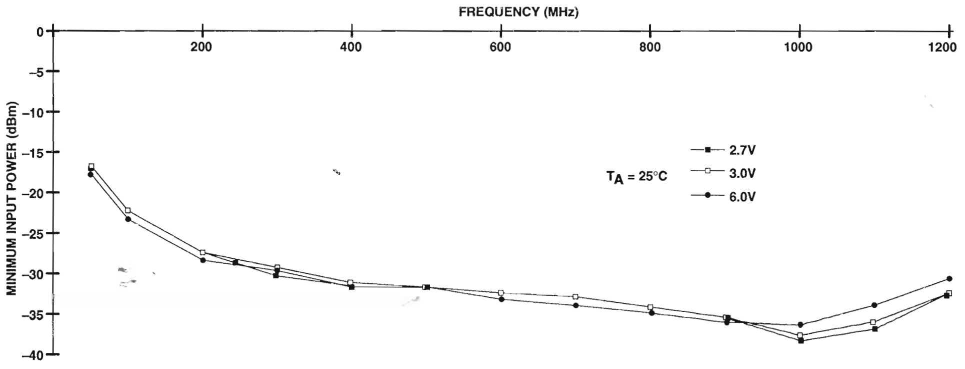


Figure 3. Minimum Input Power vs Frequency and V_{CC}

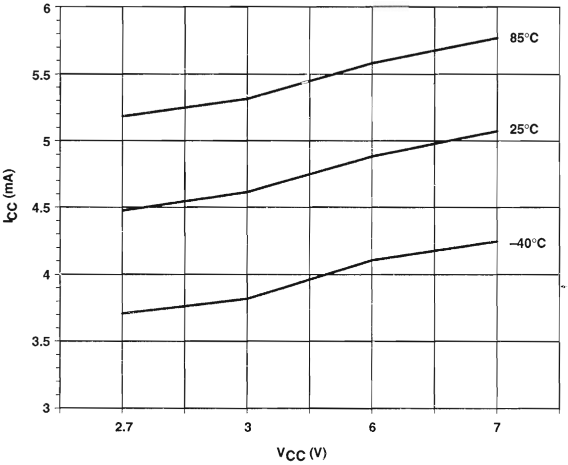


Figure 4. Supply Current vs Supply Voltage and Temperature With No Load

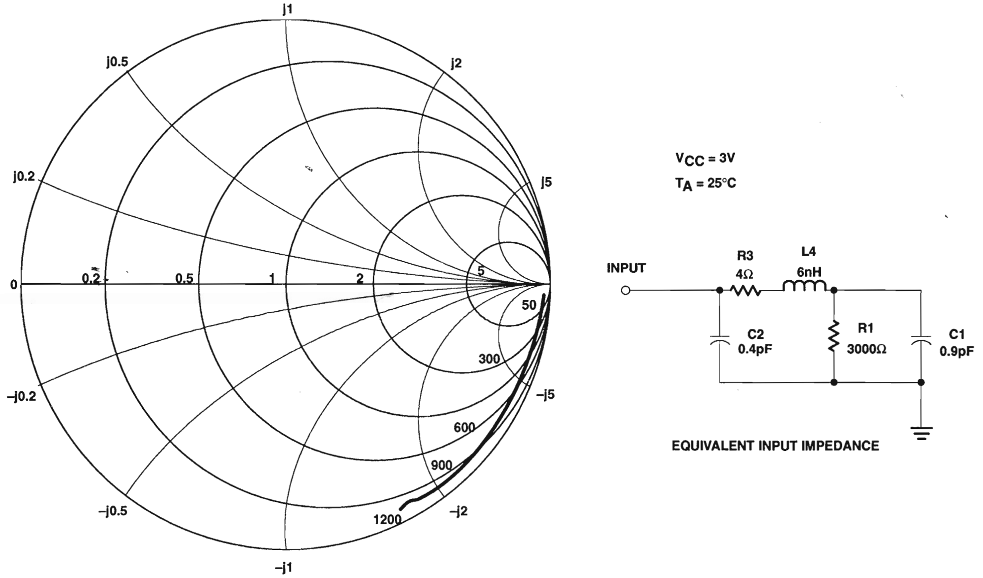


Figure 5. Typical N Package Input Impedance

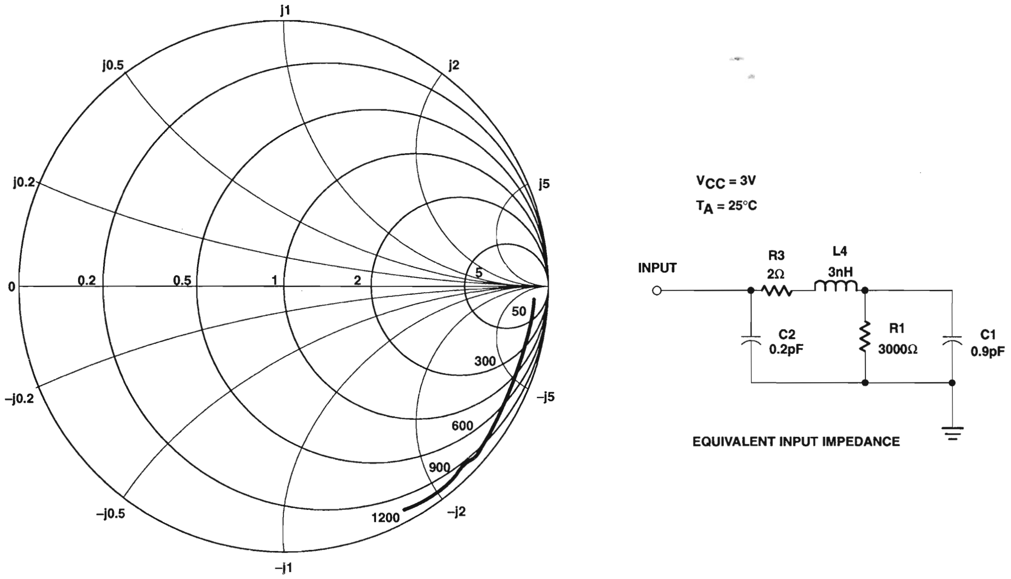


Figure 6. Typical D Package Input Impedance

Divide by: 64/65/72 triple modulus low power ECL prescaler

SA702

DESCRIPTION

The SA702 triple modulus (Divide By 64/65/72) low power ECL prescaler is used in synthesizer systems to achieve low phase lock time, broad operating range, high reference frequency and small frequency step sizes. The minimum supply voltage is 2.7V and is compatible with the CMOS UMA1005 synthesizer from Philips and other logic circuits. The low supply current allows application in battery operated low-power equipment. Maximum input signal frequency is 1.1GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the QUBiC process. The circuit will be available in an 8-pin SO package with 150 mil package width and in 8-pin dual in-line plastic package.

FEATURES

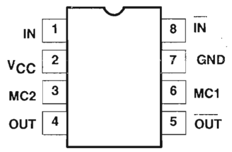
- Low voltage operation
- Low current consumption
- Operation up to 1.1GHz
- ESD hardened

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

PIN CONFIGURATION

N, D Package



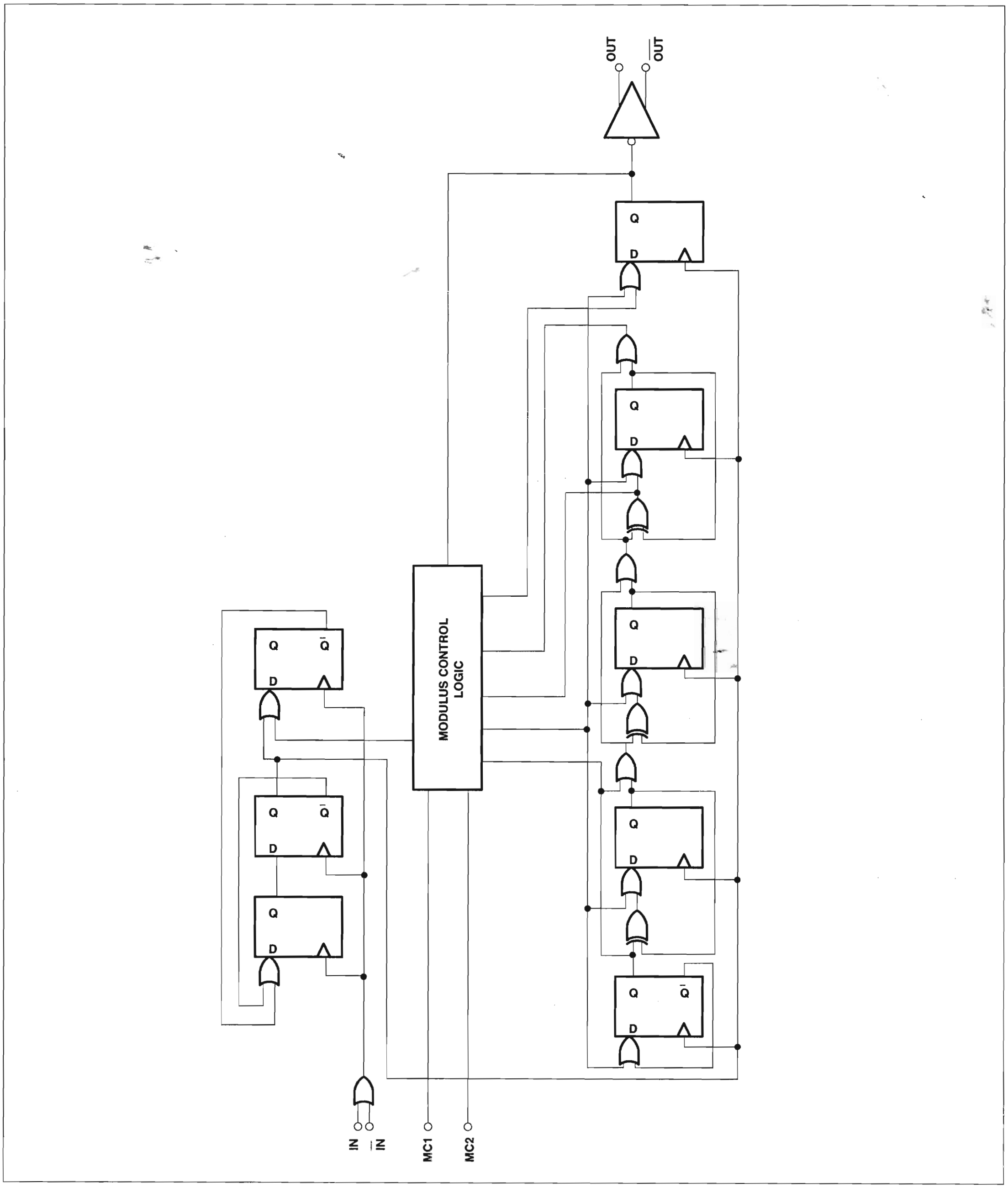
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA702N	0404B
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA702D	0174C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +7.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance D package N package	158 108	°C/W

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for $T_A = 25°C$ and $V_{CC} = 3.0V$; unless otherwise stated. Test circuit Figure 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range	f_{IN} = 1GHz, input level = 0dBm	2.7		6.0	V
I_{CC}	Supply current	No load		4.5		mA
V_{OH}	Output high level	$I_{OUT} = 1.2mA$	V_{CC}-1.4			V
V_{OL}	Output low level			V_{CC}-2.6		V
V_{IH}	MC1 input high threshold		2.0		V_{CC}	V
V_{IL}	MC1 input low threshold		–0.3		0.8	V
V_{IH}	MC2 input high threshold		2.0		V_{CC}	V
V_{IL}	MC2 input low threshold		–0.3		0.8	V
I_{IH}	MC1 input high current	$V_{MC1} = V_{CC} = 6V$		0.1	50	μA
I_{IL}	MC1 input low current	$V_{MC1} = 0V$, $V_{CC} = 6V$	–100	–30		μA
I_{IH}	MC2 input high current	$V_{MC2} = V_{CC} = 6V$		0.1	50	μA
I_{IL}	MC2 input low current	$V_{MC2} = 0V$, $V_{CC} = 6V$	–100	–30		μA

AC ELECTRICAL CHARACTERISTICS

These AC specifications are valid for f_{IN} = 1GHz, input level = 0dBm, $V_{CC} = 3.0V$ and $T_A = 25°C$; unless otherwise stated. Test circuit Fig. 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude[1]	1000pF input coupling	0.05		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input[2]	0		1.1	GHz
		1000pF input coupling			1.1	
R_{ID}	Differential input resistance	DC measurement		5		kΩ
V_O	Output voltage	$V_{CC} = 5.0V$		1.6		V_{P-P}
		$V_{CC} = 3.0V$		1.2		
t_S	Modulus set-up time[1]				5	ns
t_H	Modulus hold time[1]				0	ns
t_{PD}	Propagation time			10		ns

NOTES:
1. Maximum limit is not tested, however, it is guaranteed by design and characterization.
2. For f_{IN} < 50MHz, minimum input slew rate of 32V/μs is required.

DESCRIPTION OF OPERATION

The SA702 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for MC1 (Modulus Control) to be set high and MC2 input to be set low in which case the circuit comprises a divide by 64. For divide by 65 the MC1 singal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the synchronous counter. For divide by 72, MC2 is set high configuring the prescaler to divide by 4 and the counter to divide by 18. A truth table for the modulus values is given below:

Table 1.

Modulus	MC1	MC2
64	1	0
65	0	0
72	0	1
72	1	1

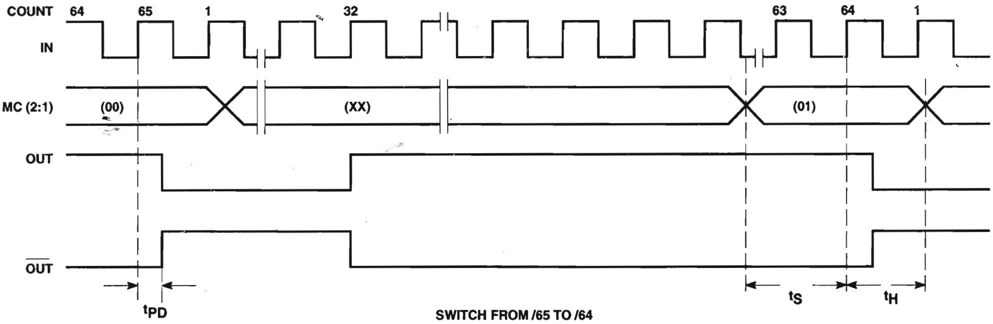
For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 32 with delay t_{PD}.

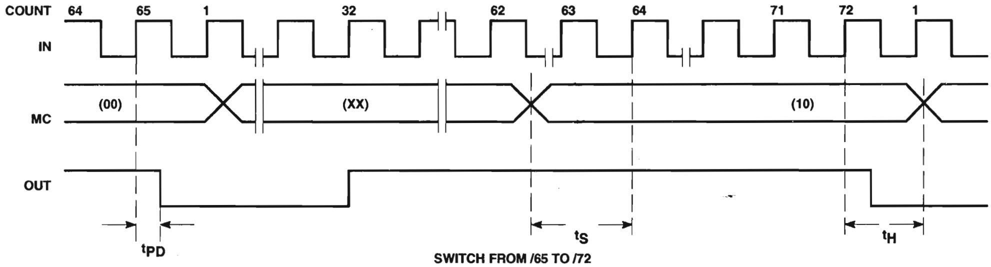
The MC1 and MC2 inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed.

The prescaler input is differential and ECL compatible. The output is differential ECL compatible.

AC TIMING CHARACTERISTICS



SWITCH FROM /65 TO /64



SWITCH FROM /65 TO /72

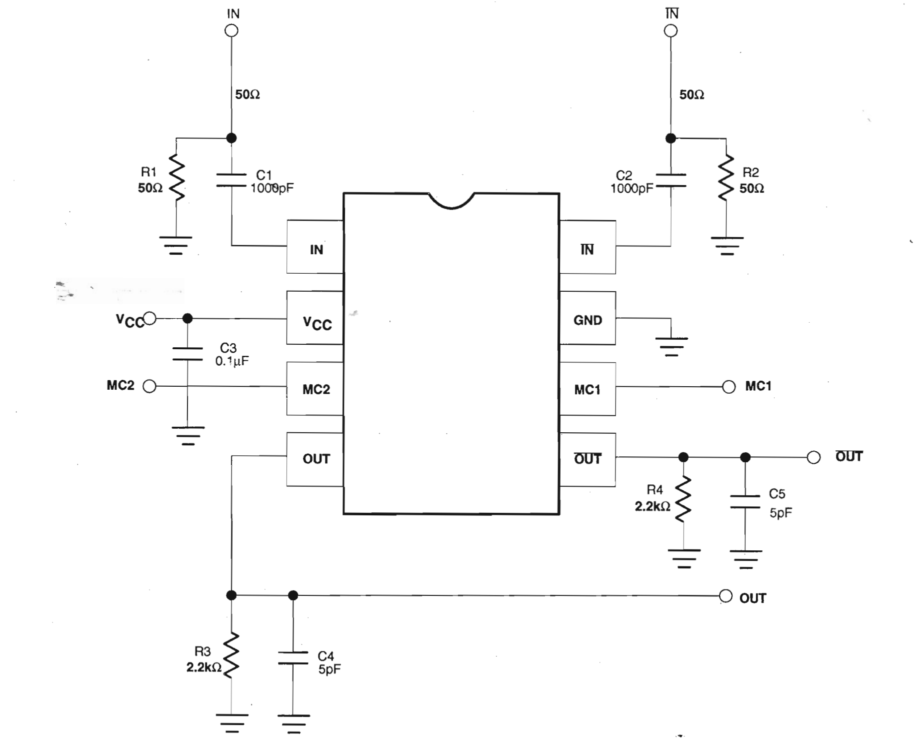


Figure 1. SA702 Test Circuit

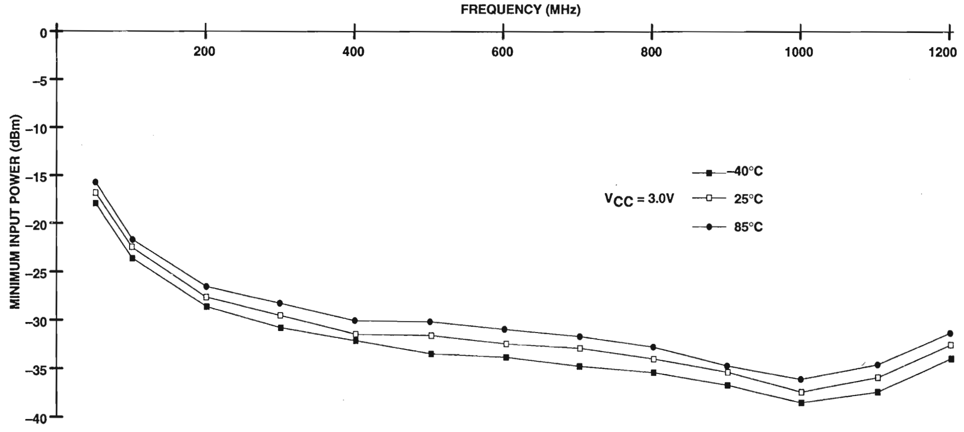


Figure 2. Minimum Input Power vs Frequency and Temperature

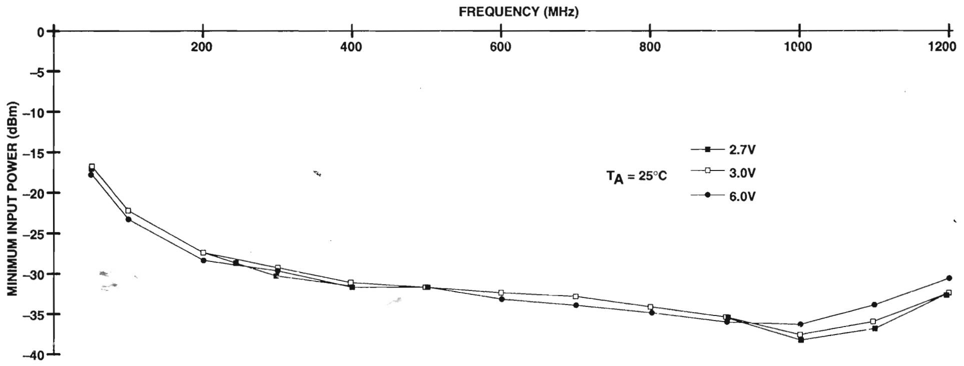


Figure 3. Minimum Input Power vs Frequency and V_{CC}

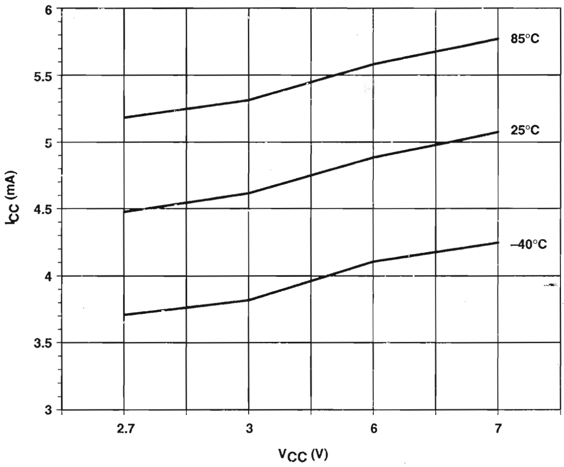


Figure 4. Supply Current vs Supply Voltage and Temperature With No Load

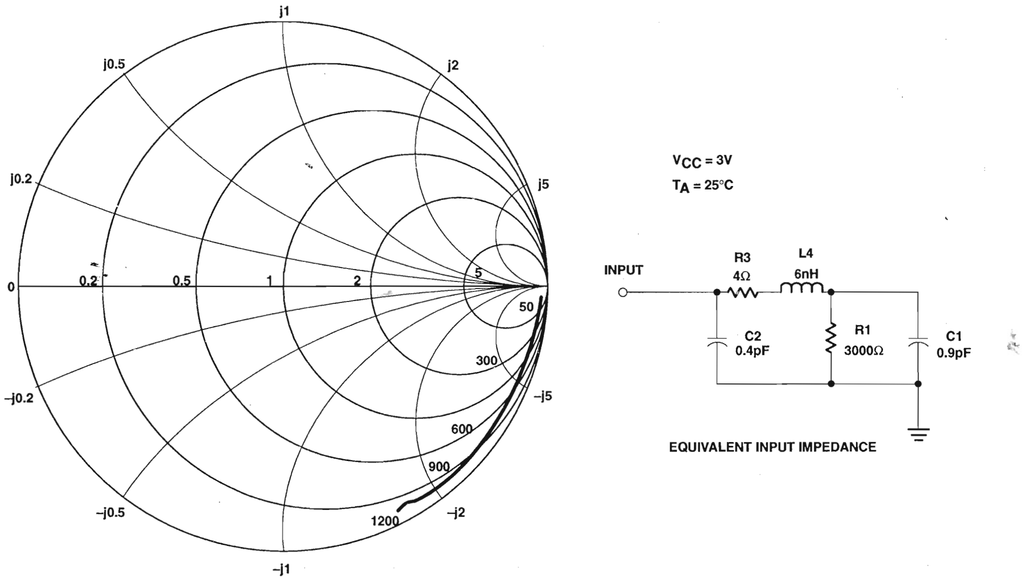


Figure 5. Typical N Package Input Impedance

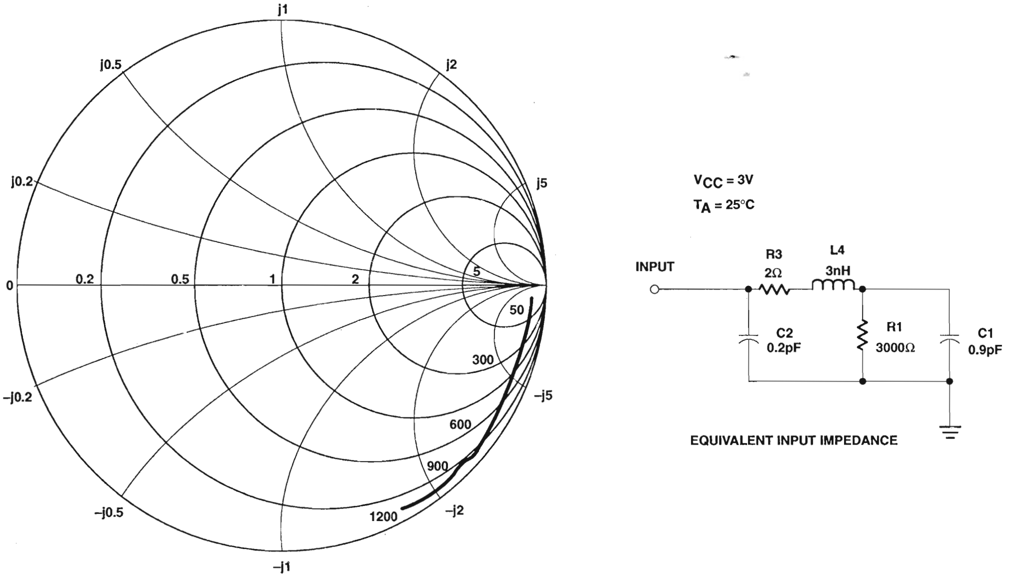


Figure 6. Typical D Package Input Impedance

Divide by: 128/129/144 triple modulus low power ECL prescaler

SA703

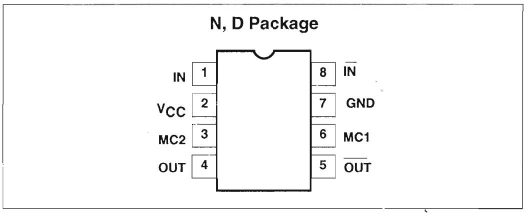
DESCRIPTION

The SA703 triple modulus (Divide By 128/129/144) low power ECL prescaler is used in synthesizer systems to achieve low phase lock time, broad operating range, high reference frequency and small frequency step sizes. The minimum supply voltage is 2.7V and is compatible with the UMA1005 synthesizer from Philips and other logic circuits. The low supply current allows application in battery operated low-power equipment. Maximum input signal frequency is 1.1GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the QUBiC process. The circuit will be available in an 8-pin SO package with 150 mil package width and in 8-pin dual in-line plastic package.

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

PIN CONFIGURATION



FEATURES

- Low voltage operation
- Low current consumption
- Operation up to 1.1GHz
- ESD hardened

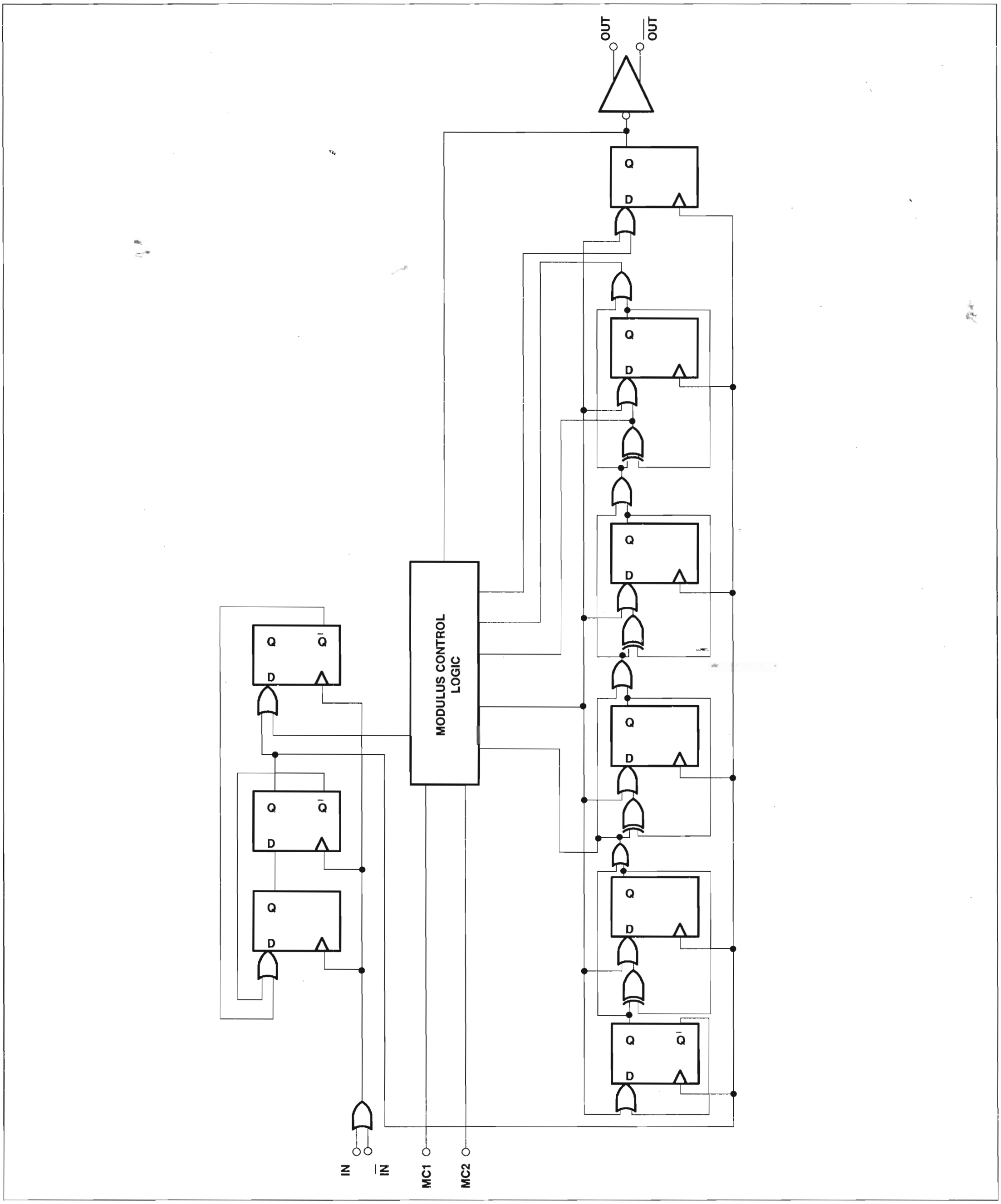
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA703N	0404B
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA703D	0174C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +7.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance D package N package	158 108	°C/W

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for $T_A = 25°C$ and $V_{CC} = 3.0V$; unless otherwise stated. Test circuit Figure 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range	f_{IN} = 1GHz, input level = 0dBm	2.7		6.0	V
I_{CC}	Supply current	No load		4.5		mA
V_{OH}	Output high level	I_{OUT} = 1.2mA	V_{CC}-1.4			V
V_{OL}	Output low level			V_{CC}-2.6		V
V_{IH}	MC1 input high threshold		2.0		V_{CC}	V
V_{IL}	MC1 input low threshold		–0.3		0.8	V
V_{IH}	MC2 input high threshold		2.0		V_{CC}	V
V_{IL}	MC2 input low threshold		–0.3		0.8	V
I_{IH}	MC1 input high current	$V_{MC1} = V_{CC} = 6V$		0.1	50	µA
I_{IL}	MC1 input low current	$V_{MC1} = 0V$, $V_{CC} = 6V$	–100	–30		µA
I_{IH}	MC2 input high current	$V_{MC2} = V_{CC} = 6V$		0.1	50	µA
I_{IL}	MC2 input low current	$V_{MC2} = 0V$, $V_{CC} = 6V$	–100	–30		µA

AC ELECTRICAL CHARACTERISTICS

These AC specifications are valid for $V_{CC} = 3.0V$, $f_{IN} = 1GHz$, input level = 0dBm, $T_A = 25°C$; unless otherwise stated. Test circuit Fig. 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude[1]	1000pF input coupling	0.05		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input[2]	0		1.1	GHz
		1000pF input coupling			1.1	
R_{ID}	Differential input resistance	DC measurement		5		kΩ
V_O	Output voltage	$V_{CC} = 5.0V$		1.6		V_{P-P}
		$V_{CC} = 3.0V$		1.2		
t_S	Modulus set-up time[1]				5	ns
t_H	Modulus hold time[1]				0	ns
t_{PD}	Propagation time			10		ns

NOTES:

1. Maximum limit is not tested, however, it is guaranteed by design and characterization.
2. For f_{IN} < 50MHz, minimum input slew rate of 32V/µs is required.

DESCRIPTION OF OPERATION

The SA703 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for MC1 (Modulus Control) to be set high and MC2 input to be set low in which case the circuit comprises a divide by 128. For divide by 129 the MC1 singal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the synchronous counter. For divide by 144, MC2 is set high configuring the prescaler to divide by 4 and the counter to divide by 36. A truth table for the modulus values is given in Table 1.

For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 64 with delay t_{PD}.

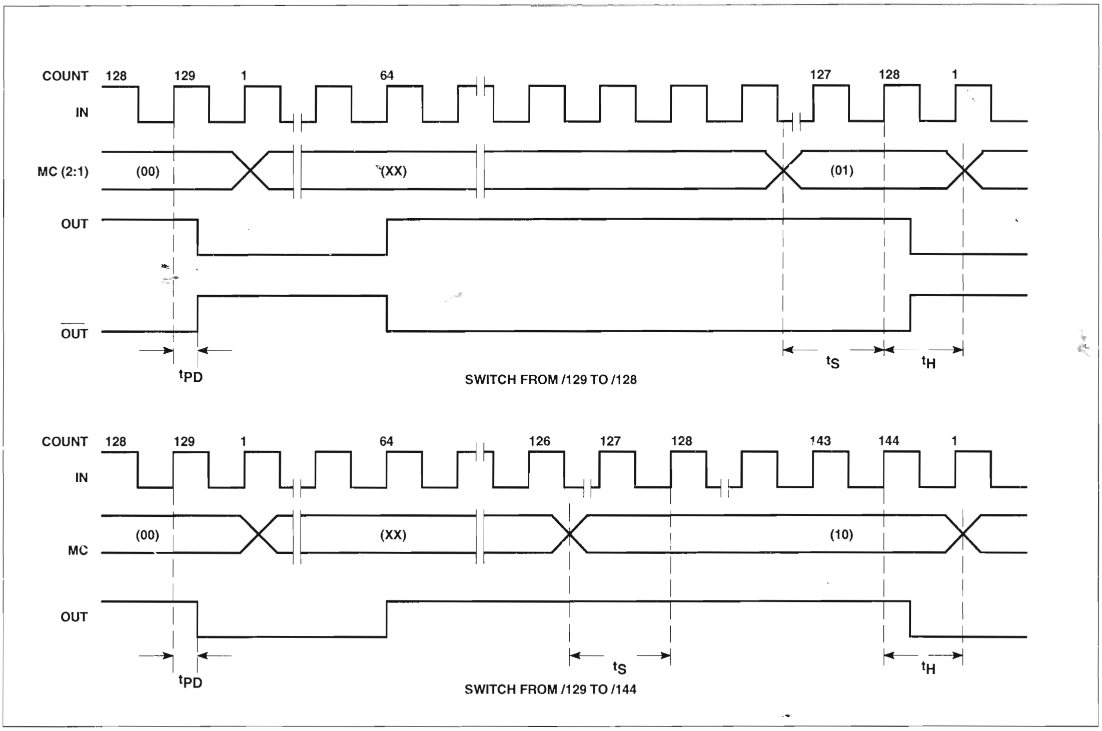
The MC1 and MC2 inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed.

The prescaler input is differential and ECL compatible. The output is differential ECL compatible.

Table 1.

Modulus	MC1	MC2
128	1	0
129	0	0
144	0	1
144	1	1

AC TIMING CHARACTERISTICS



SWITCH FROM /129 TO /128

SWITCH FROM /129 TO /144

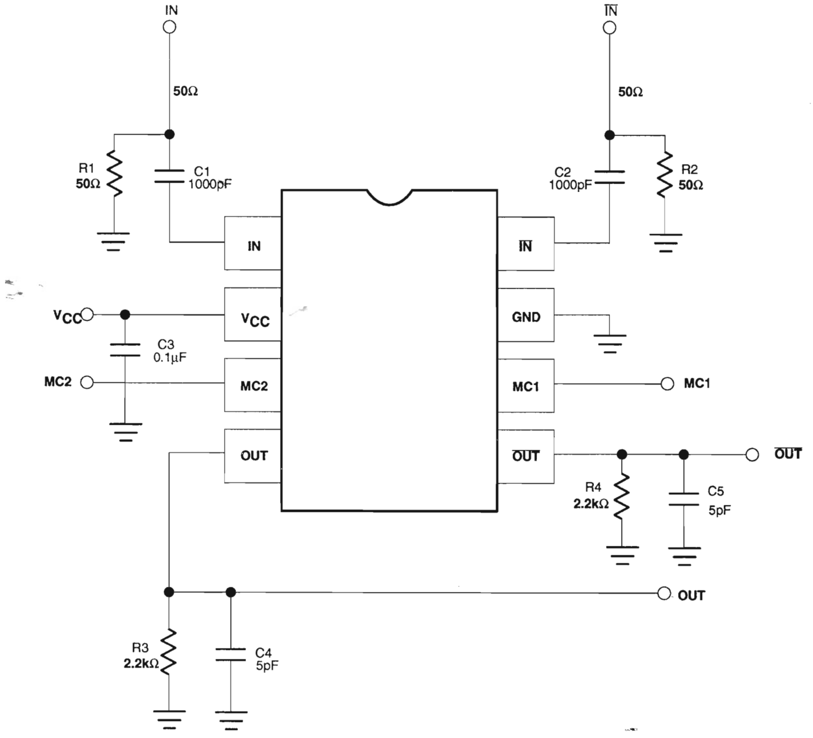


Figure 1. SA703 Test Circuit

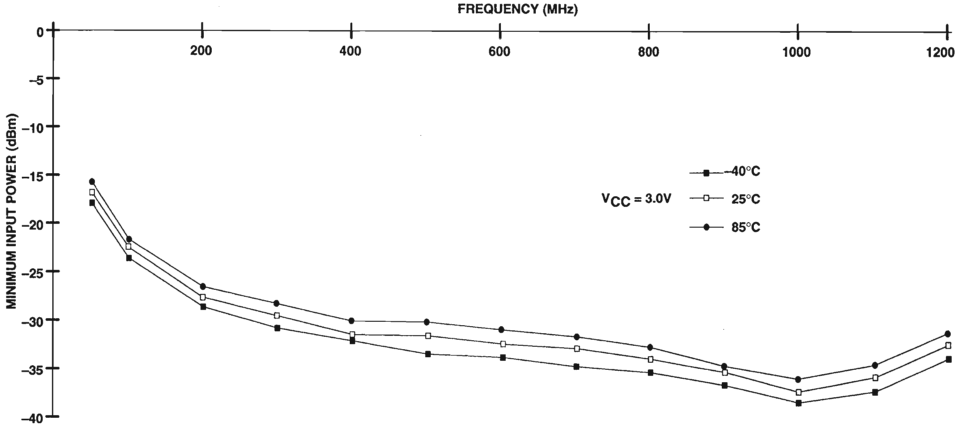


Figure 2. Minimum Input Power vs Frequency and Temperature

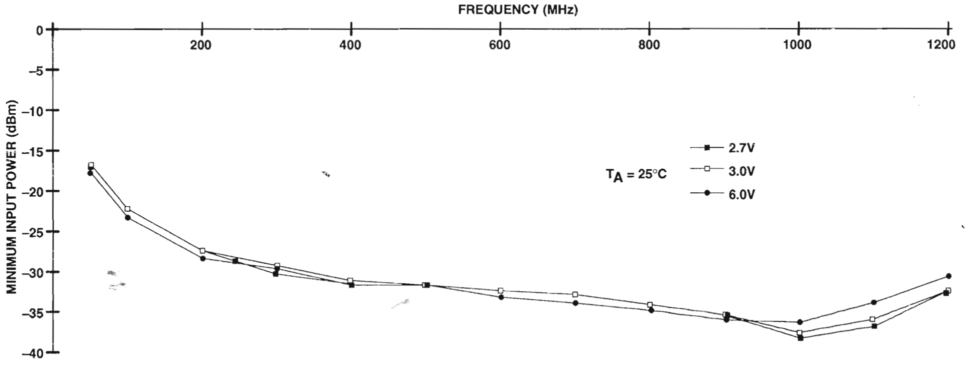


Figure 3. Minimum Input Power vs Frequency and V_{CC}

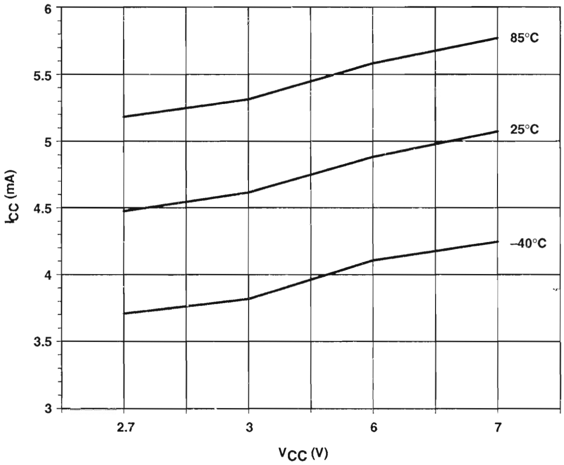


Figure 4. Supply Current vs Supply Voltage and Temperature With No Load

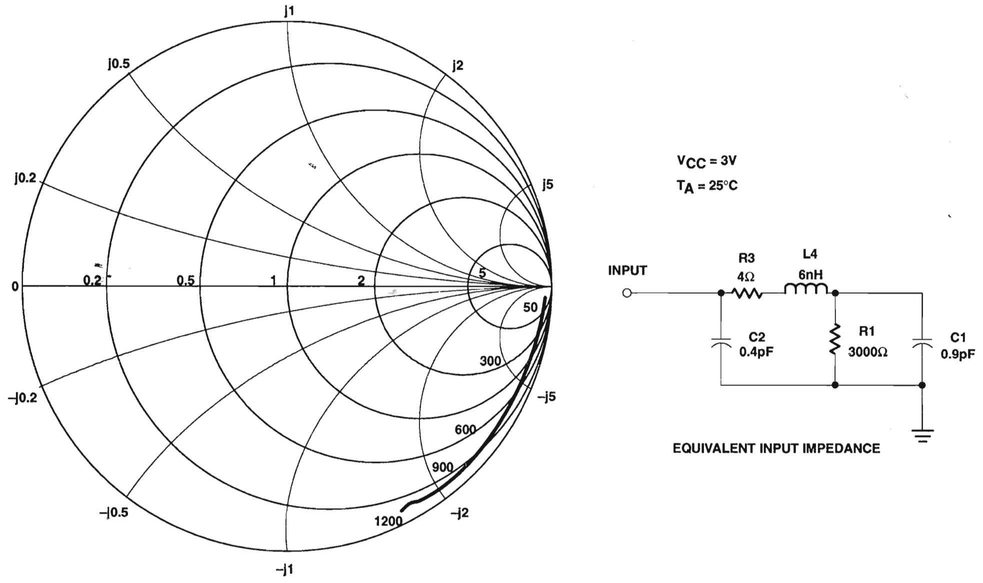


Figure 5. Typical N Package Input Impedance

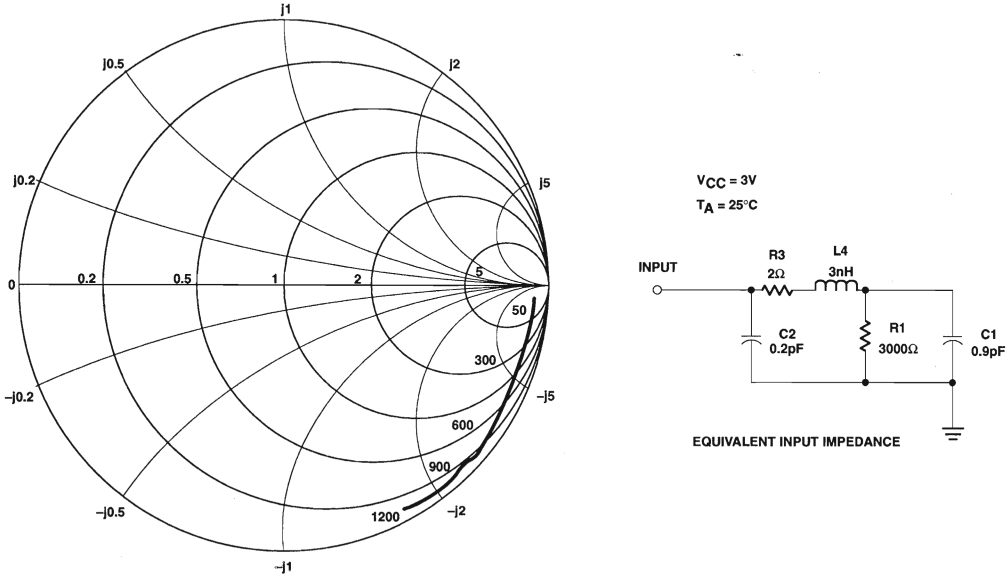


Figure 6. Typical D Package Input Impedance

Low-voltage 1GHz fractional-N synthesizer SA7025

DESCRIPTION

The SA7025 is a monolithic low power, high performance dual frequency synthesizer fabricated in QUBiC BiCMOS technology. Featuring Fractional-N division with selectable modulo 5 or 8 implemented in the Main synthesizer to allow the phase detector comparison frequency to be five or eight times the channel spacing. This feature reduces the overall division ratio yielding a lower noise floor and faster channel switching. The phase detectors and charge pumps are designed to achieve phase detector comparison frequencies up to 5MHz. A triple modulus prescaler (divide by 64/65/72) is integrated on chip with a maximum input frequency of 1.0GHz. Programming and channel selection are realized by a high speed 3-wire serial interface.

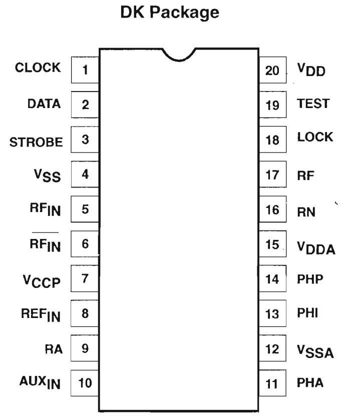
FEATURES

- Operation up to 1.0GHz
- Fast locking by “Fractional-N” divider
- Auxiliary synthesizer
- Digital phase comparator with proportional and integral charge pump output
- High speed serial input
- Low power consumption
- Programmable charge pump currents
- Supply voltage range 2.7 to 5.5V
- Excellent input sensitivity:
  $V_{RF_IN} = -20$dBm

APPLICATIONS

- ADC (American Digital Cellular)
- Cellular radio
- Spread-spectrum receivers
- Portable communication systems

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (SSOP)	–40 to +85°C	SA7025DK	1563

ABSOLUTE MAXIMUM RATINGS

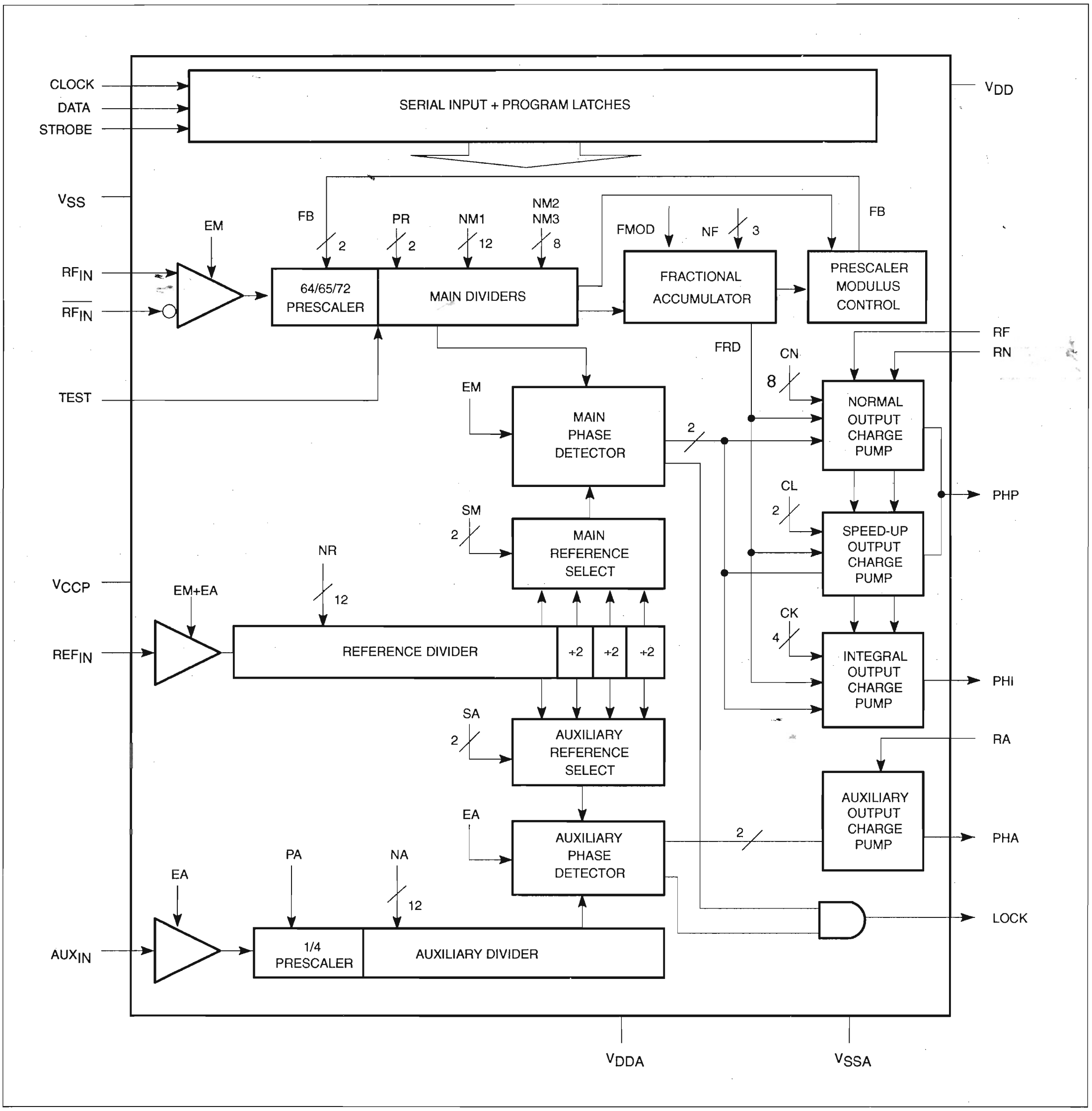
SYMBOL	PARAMETER	RATING	UNITS
V	Supply voltage, V_{DD}, V_{DDA}, V_{CCP}	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{DD} + 0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C

NOTE: Thermal impedance (θ_{JA}) = 117°C/W.

PIN DESCRIPTIONS

Symbol	Pin	Description
CLOCK	1	Serial clock input
DATA	2	Serial data input
STROBE	3	Serial strobe input
V_{SS}	4	Digital ground
RF_{IN}	5	Prescaler positive input
$\overline{RF_{IN}}$	6	Prescaler negative input
V_{CCP}	7	Prescaler positive supply voltage. This pin supplies power to the prescaler and RF input buffer
REF_{IN}	8	Reference divider input
RA	9	Auxiliary current setting; resistor to V_{SSA}
AUX_{IN}	10	Auxiliary divider input
PHA	11	Auxiliary phase detector output
V_{SSA}	12	Analog ground
PHI	13	Integral phase detector output
PHP	14	Proportional phase detector output
V_{DDA}	15	Analog supply voltage. This pin supplies power to the charge pumps, Auxiliary prescaler, Auxiliary and Reference buffers.
RN	16	Main current setting; resistor to V_{SSA}
RF	17	Fractional compensation current setting; resistor to V_{SSA}
LOCK	18	Lock detector output
TEST	19	Test pin; connect to V_{DD}
V_{DD}	20	Digital supply voltage. This pin supplies power to the CMOS digital part of the device

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{CCP} = 3V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
$I_{STANDBY}$	Standby supply currents	$V_{RA} = V_{RF} = V_{RN} = V_{DDA}$, EM = EA = 0		100		µA
I_{AUX}	Operational supply currents[5]	EM = 0, EA = 1		3.5		mA
I_{MAIN}	Operational supply currents[5]	EM = 1, EA = 0		5.5		mA
I_{TOTAL}	Operational supply currents[5]	EM = EA = 1		7.5		mA
Digital inputs CLK, DATA, STROBE						
V_{IH}	High level input voltage range		$0.7 \times V_{DD}$		V_{DD}	V
V_{IL}	Low level input voltage range		0		$0.3 \times V_{DD}$	V
Digital outputs LOCK						
V_{OL}	Output voltage LOW	$I_O = 2mA$			0.4	V
V_{OH}	Output voltage HIGH	$I_O = -2mA$	$V_{DD}-0.4$			V
Charge pump PHA						
$\|I_{PHA}\|$	Output current PHA	$I_{RA} = -62.5µA$; $V_{PHA} = V_{DDA}/2$[13]	400	500	600	µA
		$I_{RA} = -25µA$; $V_{PHA} = V_{DDA}/2$	160	200	240	
$\frac{\Delta I_{PHP\_A}}{\|I_{PHP\_A}\|}$	Relative output current variation PHA	$I_{RA} = -62.5µA$[2, 13]		2	6	%
ΔI_{PHA_M}	Output current matching	$I_{RA} = -62.5µA$; $V_{PHA} = V_{DDA}/2$[4, 13]			±50	µA
Charge pump PHP, normal mode[1, 4, 6] $V_{RF} = V_{DDA}$						
$\|I_{PHP\_N}\|$	Output current PHP	$I_{RN} = -62.5µA$; $V_{PHP} = V_{DDA}/2$[13]	440	550	660	µA
		$I_{RN} = -25µA$; $V_{PHP} = V_{DDA}/2$	175	220	265	
$\frac{\Delta I_{PHP\_N}}{I_{PHP\_N}}$	Relative output current variation PHP	$I_{RN} = -62.5µA$[2, 13]		2	6	%
$\Delta I_{PHP\_N\_M}$	Output current matching	$I_{RN} = -62.5µA$; $V_{PHP} = V_{DDA}/2$[4, 13]			±50	µA
Charge pump PHP, speed-up mode [1, 4, 7] $V_{RF} = V_{DDA}$						
$\|I_{PHP\_S}\|$	Output current PHP	$I_{RN} = -62.5µA$; $V_{PHP} = V_{DDA}/2$[13]	2.20	2.75	3.30	mA
		$I_{RN} = -25µA$; $V_{PHP} = V_{DDA}/2$	0.85	1.1	1.35	
$\frac{\Delta I_{PHP\_S}}{I_{PHP\_S}}$	Relative output current variation PHP	$I_{RN} = -62.5µA$[2, 13]		2	6	%
$\Delta I_{PHP\_S\_M}$	Output current matching	$I_{RM} = -62.5µA$; $V_{PHP} = V_{DDA}/2$[4, 13]			±250	µA
Charge pump PHI, speed-up mode [1, 4, 8] $V_{RF} = V_{DDA}$						
$\|I_{PHI}\|$	Output current PHI	$I_{RN} = -62.5µA$; $V_{PHI} = V_{DDA}/2$[13]	4.4	5.5	6.6	mA
		$I_{RN} = -25µA$; $V_{PHI} = V_{DDA}/2$	1.75	2.2	2.65	
$\frac{\Delta I_{PHI}}{I_{PHI}}$	Relative output current variation PHI	$I_{RN} = -62.5µA$[2, 13]		2	8	%
ΔI_{PHI_M}	Output current matching	$I_{RN} = -62.5µA$; $V_{PHI} = V_{DDA}/2$[4, 13]			±500	µA
Fractional compensation PHP, normal mode [1, 9] $V_{RN} = V_{DDA}$, $V_{PHP} = V_{DDA}/2$						
$I_{PHP\_F\_N}$	Fractional compensation output current PHP vs F_{RD}[3]	$I_{RF} = -62.5µA$; F_{RD} = 1 to 7[13]	−675	−500	−325	nA
		$I_{RF} = -25µA$; F_{RD} = 1 to 7	−270	−200	−130	
Fractional compensation PHP, speed up mode [1, 10] $V_{PHP} = V_{DDA}$, $V_{RN} = V_{DDA}$						
$I_{PHP\_F\_S}$	Fractional compensation output current PHP vs F_{RD}[3]	$I_{RF} = -62.5µA$; F_{RD} = 1 to 7[13]	−3.35	−2.5	−1.65	µA
		$I_{RF} = -25µA$; F_{RD} = 1 to 7	−1.35	−1.0	−0.65	
Fractional compensation PHI, speed up mode [1, 11] $V_{PHP} = V_{DDA}/2$, $V_{RN} = V_{DDA}$						
I_{PHI_F}	Fractional compensation output current PHI vs F_{RD}[3]	$I_{RF} = -62.5µA$; F_{RD} = 1 to 7[13]	−5.4	−4.0	−2.6	µA
		$I_{RF} = -25µA$; F_{RD} = 1 to 7	−2.15	−1.6	−1.05	

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Charge pump leakage currents, charge pump not active						
I_{PHP_L}	Output leakage current PHP; normal mode[1]	V_{PHP} = 0.7 to V_{DDA} – 0.8		0.1	10	nA
I_{PHI_L}	Output leakage current PHI; normal mode[1]	V_{PHI} = 0.7 to V_{DDA} – 0.8		0.1	10	nA
I_{PHA_L}	Output leakage current PHA	V_{PHA} = 0.7 to V_{DDA} – 0.8		0.1	10	nA

AC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{CCP} = 3V$; $T_A = 25°C$; f_{RF_IN} = 1GHz, input level = –10dBm; unless otherwise specified. Test Circuit, Figure 2. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Main divider						
f_{RF_IN}	Input signal frequency	Direct coupled input[14]	0		1.0	GHz
		1000pF input coupling			1.0	
V_{RF_IN}	Input sensitivity		–20		0	dBm
Reference divider						
f_{REF_IN}	Input signal frequency		0		20	MHz
		$4.5V \leq V_{DDA} \leq 5.5V$	0		30	
V_{REF_IN}	Input signal range, AC coupled		300			mV_{P-P}
Z_{REF_IN}	Reference divider input impedance			100		kΩ
					3	pF
Auxiliary divider						
f_{AUX_IN}	Input signal frequency PA = “0”, prescaler enabled		0		50	MHz
		$4.5V \leq V_{DDA} \leq 5.5V$	0		150	
	Input signal frequency PA = “1”, prescaler disabled		0		30	
		$4.5V \leq V_{DDA} \leq 5.5V$	0		40	
V_{AUX_IN}	Input signal range, AC coupled		200			mV_{P-P}
Z_{AUX_IN}	Auxiliary divider input impedance			100		kΩ
					3	pF
Serial interface[15]						
f_{CLOCK}	Clock frequency				10	MHz
t_{SU}	Set-up time: DATA to CLOCK, CLOCK to STROBE		30			ns
t_H	Hold time; CLOCK to DATA		30			ns
t_W	Pulse width; CLOCK		30			ns
	Pulse width; STROBE	B, C, D, E words	30			
t_{SW}	Pulse width; STROBE	A word, PR = ‘01’	$\frac{1}{f_{VCO}} \cdot (NM2 \cdot 65) + t_W$			ns
		A word, PR = ‘10’	$\frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65) + (NM3 + 1) \cdot 72] + t_W$			

NOTES:

1. When a serial input "A" word is programmed, the main charge pumps on PHP and PHI are in the "speed up mode" as long as STROBE = H. When this is not the case, the main charge pumps are in the "normal mode".
2. The relative output current variation is defined thus:
$$\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{|(I_2 + I_1)|}$$; with $V_1 = 0.7V$, $V_2 = V_{DDA} - 0.8V$ (see Figure 1).
3. F_{RD} is the value of the 3 bit fractional accumulator.
4. Monotonicity is guaranteed with $C_N = 0$ to 255.
5. Power supply current measured with $f_{RF\ IN} = 953.19MHz$, NM1 = 48, NM2 = 3, NM3 = 7, NF = 5, FMOD = 8, N = 3971+5/8, main phase detector frequency = 240kHz, $f_{REF\ IN} = 21.36MHz$, NR = 89, SM = 1, $f_{AUX\ IN} = 82.56MHz$, NA = 86, SA = 2, PA = 0, auxiliary phase detector frequency = 120kHz, IRN = IRA = IRF = 25μA, CN = 160, CL = 0, CK = 0, lock condition, normal mode, $V_{DDA} = 5V$, $V_{DD} = V_{CCP} = 3V$. Operational supply current = $I_{DDA} + I_{DD} + I_{CCP}$.
6. Specification condition: CN = 255
7. Specification conditions:
   1) CN = 255; CL = 1, or
   2) CN = 75; CL = 3
8. Typical output current $|I_{PHI}| = -I_{RN} \times CN \times 2^{(CL+1)} \times CK/32$:
   1) CN = 160; CL = 3; CK = 1, or
   2) CN = 160; CL = 2; CK = 2, or
   3) CN = 160; CL = 1; CK = 4, or
   4) CN = 160; CL = 0; CK = 8
9. Specification condition: F_{RD} = 1 to 7.
10. Specification conditions: F_{RD} = 1 to 7; CL = 1.
11. Specification conditions:
    1) F_{RD} = 1 to 7; CL = 1; CK = 2, or
    2) F_{RD} = 1 to 7; CL = 2; CK = 1.
12. The output current matching is measured when both (positive current and negative current) sections of the output charge pumps are on.
13. Limited analog supply voltage range 4.5 to 5.5V.
14. For f_{IN} < 50MHz, minimum input slew rate of 32V/μs is required.
15. Guaranteed by design.

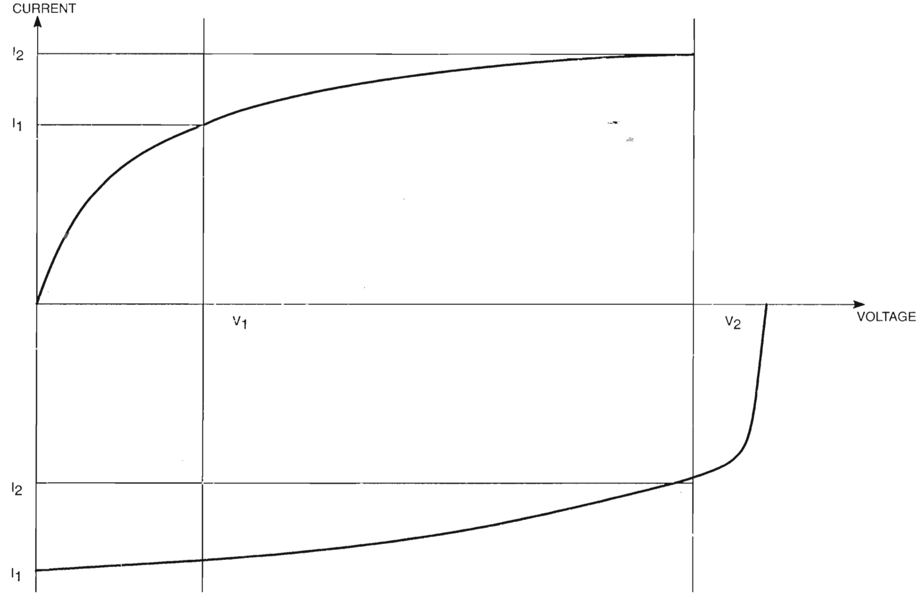


Figure 1. Relative Output Current Variation

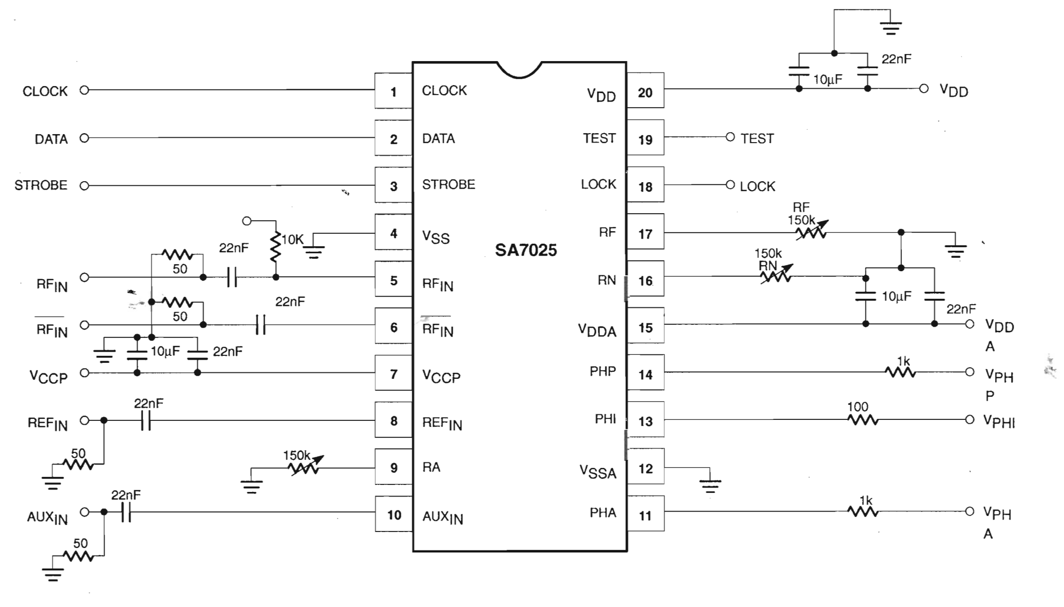


Figure 2. Test Circuit

AC TIMING CHARACTERISTICS

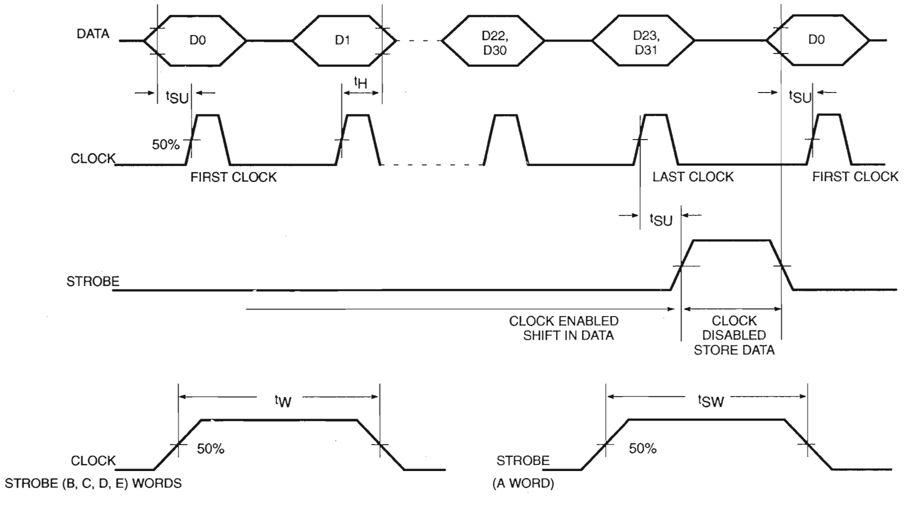


Figure 3. Serial Input Timing Sequence

FUNCTIONAL DESCRIPTION

Serial Input Programming

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program all counter ratios, DACs, selection and enable bits. The programming data is structured into 24 or 32 bit words; each word includes 1 or 4 address bits. Figure 3 shows the timing diagram of the serial input. When the STROBE = L, the clock driver is enabled and on the positive edges of the CLOCK the signal on DATA input is clocked into a shift register. When the STROBE = H, the clock is disabled and the data in the shift register remains stable. Depending on the 1 or 4 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 4 words must be sent: D, C, B and A. Figure 4 and Table 1 shows the format and the contents of each word. The E word is for testing purposes only. The E (test) word is reset when programming the D word. The data for CN and PR is stored by the B word in temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the A word into the work registers which avoids false temporary main divider input. CN is only loaded from the temporary registers when a short 24 bit A0 word is used. CN will be directly loaded by programming a long 32 bit A1 word. The flag LONG in the D word determines whether A0 (LONG = "0") or A1 (LONG = "1") format is applicable. The A word contains new data for the main divider.

Main Divider Synchronization

The A word is loaded only when a main divider synchronization signal is also active in order to avoid phase jumps when reprogramming the main divider. The synchronization signal is generated by the main divider. The signal is active while the NM1 divider is counting down from the programmed value. The new A word will be loaded after the NM1 divider has reached its terminal count; also, at this time a main divider output pulse will be sent to the main phase detector. The loading of the A word is disabled while the NM2 or NM3 dividers are counting up to their programmed values. Therefore, the new A word will be correctly loaded provided that the STROBE signal has been at an active high value for at least a minimum number of VCO input cycles at RF_{IN} or $\overline{RF_{IN}}$.

$$\text{t\_strobe\_min} = \frac{1}{f_{VCO}}(NM_2 \cdot 65) + t_W \text{ for PR} = \text{'01'}$$

$$\text{t\_strobe\_min} = \frac{1}{f_{VCO}}[NM_2 \cdot 65 + (NM_3 + 1) \cdot 72] + t_W \text{ for PR} = \text{'10'}$$

Programming the A word means also that the main charge pumps on output PHP and PHI are set into the speed-up mode as long as the STROBE is H.

Auxiliary Divider

The input signal on AUX_IN is amplified to logic level by a single-ended CMOS input buffer, which accepts low level AC coupled input signals. This input stage is enabled if the serial control bit EA = "1". Disabling means that all currents in the input stage are switched off. A fixed divide by 4 is enabled if PA = "0". This divider has been optimized to accept a high frequency input signal. If PA = "1", this divider is disabled and the input signal is fed directly to the second stage, which is a 12-bit programmable divider with standard input frequency (40MHz). The division ratio can be expressed as:

if PA = "0": N = 4 x NA

if PA = "1": N = NA; with NA = 4 to 4095

Reference Divider

The input signal on REF_IN is amplified to logic level by a single-ended CMOS input buffer, which accepts low level AC coupled input signals. This input stage is enabled by the OR function of the serial input bits EA and EM. Disabling means that all currents in the input stage are switched off. The reference divider consists of a programmable divider by NR (NR = 4 to 4095) followed by a three bit binary counter. The 2 bit SM register (see Figure 5) determines which of the 4 output pulses is selected as the main phase detector input. The 2 bit SA register determines the selection of the auxiliary phase detector signal.

Main Divider

The differential inputs are amplified (to internal ECL logic levels) and provide excellent sensitivity (–20dBm at 1GHz) making the prescaler ideally suited to directly interface to a VCO as integrated on the SA620 RF gain stage, VCO and mixer device. The internal triple modulus prescaler feedback loop FB controls the selection of the divide by ratios 64/65/72, and reduces the minimum system division ratio below the typical value required by standard dual modulus (64/65) devices.

This input stage is enabled when serial control bit EM = "1". Disabling means that all currents in the prescaler are switched off.

The main divider is built up by a 12 bit counter plus a sign bit. Depending on the serial input values NM1, NM2, NM3, and the prescaler select PR, the counter will select a prescaler ratio during a number of input cycles according to Table 2 and Table 3.

The loading of the work registers NM1, NM2, NM3 and PR is synchronized with the state of the main counter, to avoid extra phase disturbance when switching over to another main divider ratio as explained in the Serial Input Programming section.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented with NF. The accumulator works modulo Q. Q is preset by the serial control bit FMOD to 8 when FMOD = "1". Each time the accumulator overflows, the feedback to the prescaler will select one cycle using prescaler ratio R2 instead of R1.

As shown above, this will increase the overall division ratio by 1 if R2 = R1 + 1. The mean division ratio over Q main divider will then be

$$NQ = N + \frac{NF}{Q}$$

Programming a fraction means the prescaler with main divider will divide by N or N + 1. The output of the main divider will be modulated with a fractional phase ripple. This phase ripple is proportional to the contents of the fractional accumulator FRD, which is used for fractional current compensation.

Phase Detectors

The auxiliary and main phase detectors are a two D-type flip-flop phase and frequency detector shown in Figure 6. The flip-flops are set by the negative edges of output signals of the dividers. The rising edge of the signal, L, will reset the flip-flops after both flip-flops have been set. Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or deadband around zero phase error. The flip-flops drive on-chip charge pumps. A source current from the charge pump indicates the VCO frequency will be increased; a sink current indicates the VCO frequency will be decreased.

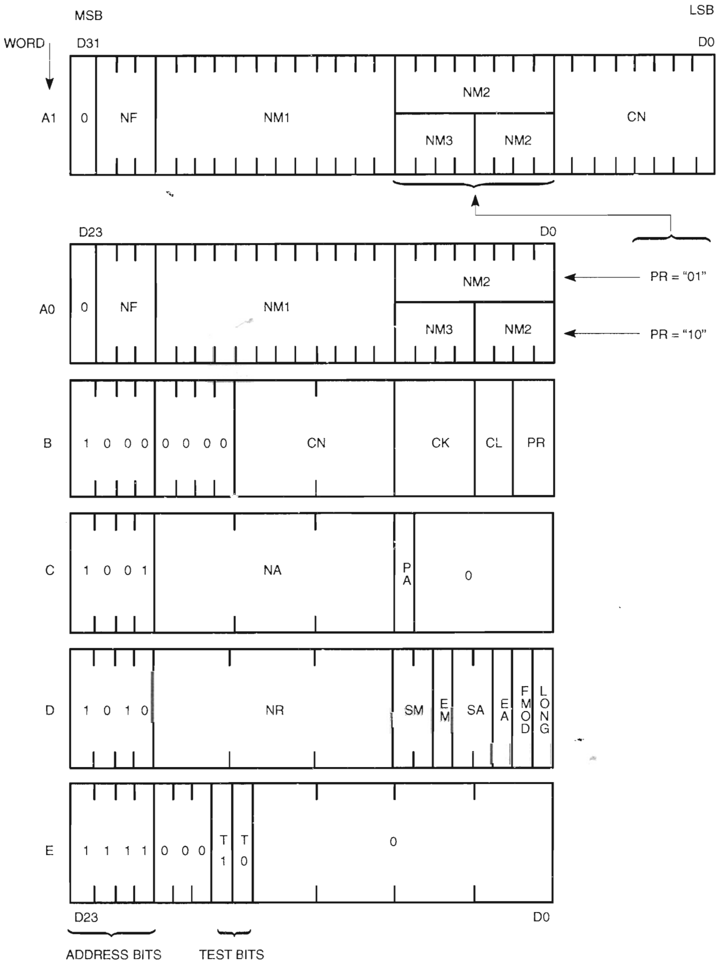


Figure 4. Serial Input Word Format

Current Settings

The SA7025 has 3 current setting pins: RA, RN and RF. The active charge pump currents and the fractional compensation currents are linearly dependent on the current connected between the current setting pin and V_{SS}. The typical value R (current setting resistor) can be calculated with the formula:

$$R = \frac{V_{DDA} - 0.9 - 150\sqrt{I_R}}{I_R}$$

The current can be set to zero by connecting the corresponding pin to V_{DDA}.

Auxiliary Output Charge Pumps

The auxiliary charge pumps on pin PHA are driven by the auxiliary phase detector and the current value is determined by the external resistor RA at pin RA. The active charge pump current is typically:

$$|I_{PHA}| = 8 \cdot I_{RA}$$

Main Output Charge Pumps and Fractional Compensation Currents

The main charge pumps on pin PHP and PHI are driven by the main phase detector and the current value is determined by the current at pin RN and via a number of DACs which are driven by registers of the serial input. The fractional compensation current is determined by the current at pin RF, the contents of the fractional accumulator FRD and a number of DACs driven by registers from the serial input. The timing for the fractional compensation is derived from the reference divider. The current is on during 1 input reference cycle before and 1 cycle after the output signal to the phase comparator. Figure 7 shows the waveforms for a typical case.

Table 1. Function Table

Symbol	Bits	Function
NM1	12	Number of main divider cycles when prescaler modulus = 64*
NM2	8 if PR = “01” 4 if PR = “10”	Number of main divider cycles when prescaler modulus = 65*
NM3	4 if PR = “10”	Number of main divider cycles when prescaler modulus = 72*
PR	2	Prescaler type in use PR = “01”: modulus 2 prescaler (64/65) PR = “10”: modulus 3 prescaler (64/65/72)
NF	3	Fractional-N increment
FMOD	1	Fractional-N modulus selection flag “1”: modulo 8 “0”: modulo 5
LONG	1	A word format selection flag “0”: 24 bit A0 format “1”: 32 bit A1 format
CN	8	Binary current setting factor for main charge pumps
CL	2	Binary acceleration factor for proportional charge pump current
CK	4	Binary acceleration factor for integral charge pump current
EM	1	Main divider enable flag
EA	1	Auxiliary divider enable flag
SM	2	Reference select for main phase detector
SA	2	Reference select for auxiliary phase detector
NR	12	Reference divider ratio
NA	12	Auxiliary divider ratio
PA	1	Auxiliary prescaler mode: PA = “0”: divide by 4 PA = “1”: divide by 1
*Not including reset cycles and Fractional-N effects.		

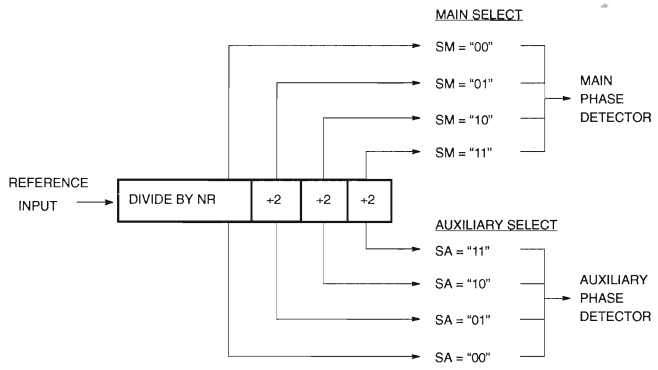


Figure 5. Reference Divider

Table 2. Prescaler Ratio

The total division ratio from prescaler to the phase detector may be expressed as:	
if PR = “01”	N = (NM1 + 2) x 64 + NM2 x 65 N’ = (NM1 + 1) x 64 + (NM2 + 1) x 65 (*)
if PR = “10”	N = (NM1 + 2) x 64 + NM2 x 65 + (NM3 + 1) x 72 N’ = (NM1 + 1) x 64 + (NM2 + 1) x 65 + (NM3 + 1) x 72 (*)
(*) When the fractional accumulator overflows the prescaler ratio = 65 (64 + 1) and the total division ratio N’ = N + 1	

Table 3. PR Modulus

PR	Modulus Prescaler	Bit Capacity		
		NM1	NM2	NM3
01	2	12	8	–
10	3	12	4	4

When the serial input A word is loaded, the output circuits are in the "speed-up mode" as long as the STROBE is H, else the "normal mode" is active. In the "normal mode" the current output PHP is:

$$I_{PHP\_N} = I_{PHP} + I_{PHP\_comp}$$

where:

$$|I_{PHP}| = \frac{CN \cdot I_{RN}}{32} \quad \text{:charge pump current}$$

$$|I_{PHP\_comp}| = FRD \cdot \frac{I_{RF}}{128} \quad \text{:fractional comp. current}$$

The current in PHI is zero in "normal mode".

In "speed-up mode" the current in output PHP is:

$$I_{PHP\_S} = I_{PHP} + I_{PHP\_comp}$$

$$|I_{PHP}| = \left(\frac{CN \cdot I_{RN}}{32}\right)(2^{CL+1} + 1)$$

$$|I_{PHP\_comp}| = \left(\frac{F_{RD} \cdot I_{RF}}{128}\right)(2^{CL+1} + 1)$$

In "speed-up mode" the current in output PHI is:

$$I_{PHI\_S} = I_{PHI} + I_{PHI\_comp}$$

where:

$$|I_{PHI}| = \left(\frac{I_{RN}CN}{32}\right)(2^{CL+1})\ CK$$

$$|I_{PHI\_comp}| = \left(\frac{I_{RF}F_{RD}}{128}\right)(2^{CL+1})\ CK$$

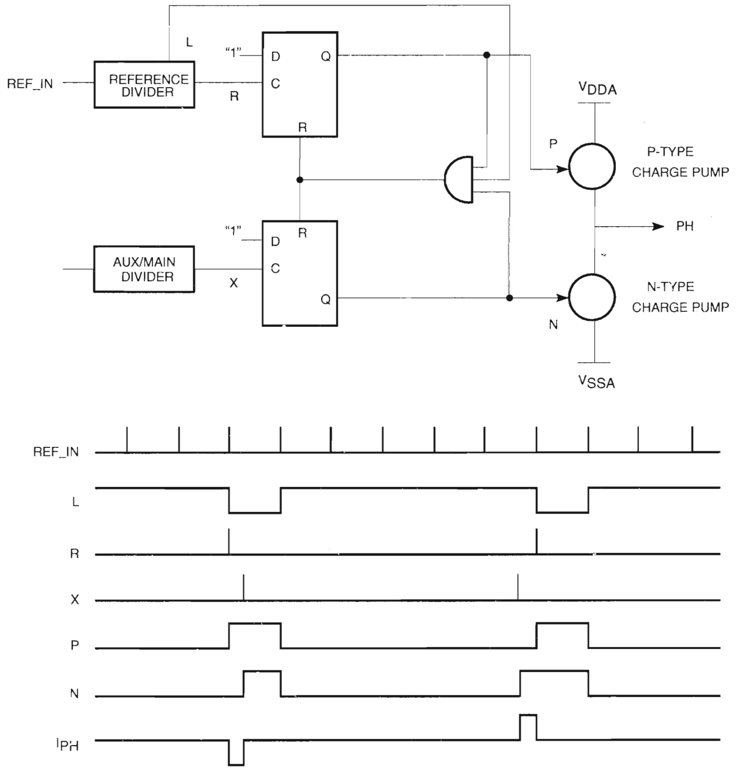


Figure 6. Phase Detector Structure with Timing

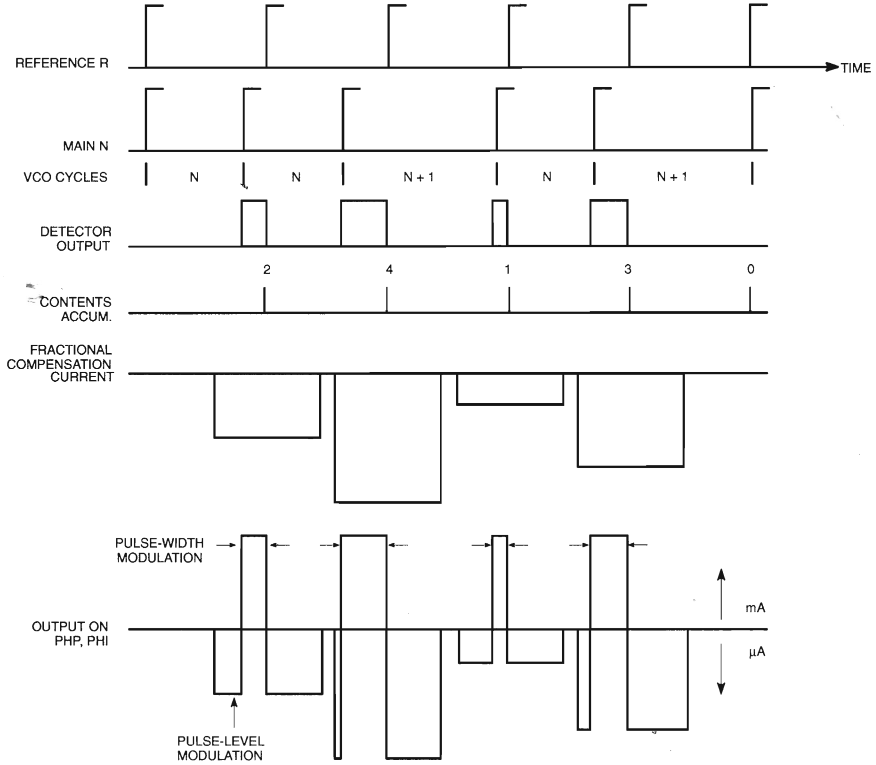


Figure 7. Waveforms for NF = 2, Fraction = 0.4

Lock Detect

The output LOCK is H when the auxiliary phase detector AND the main phase detector indicates a lock condition. The lock condition is defined as a phase difference of less than +1 cycle on the reference input REF_IN. The lock condition is also fulfilled when the relative counter is disabled (EM = “0” or respectively EA = “0”) for the main, respectively auxiliary counter.

Test Modes

The lock output is selectable as f_{REF}, f_{AUX}, f_{MAIN} and lock. Bits T1 and T0 of the E word control the selection (see Figures 4 and 8).

If T1 = T0 = Low, or if the E-word is not sent, the lock output is configured as the normal lock output described in the Lock Detect section.

If T1 = Low and T0 = High, the lock output is configured as f_{REF}. The signal is the buffered output of the reference divider NR and the 3-bit binary counter SM. The f_{REF} signal appears as normally low and pulses high whenever the divider reaches terminal count from the value programmed into the NR and SM registers. The f_{REF} signal can be used to verify the divide ratio of the Reference divider.

If T1 = High and T0 = Low, the lock output is configured as f_{AUX}. The signal is normally high and pulses low whenever the divider reaches terminal count from the value programmed into the NA and PA registers. The f_{AUX} signal can be used to verify the divide ratio of the Auxiliary divider.

If T1 = High and T0 = High, the lock output is configured as f_{MAIN}. The signal is the buffered output of the MAIN divider. The f_{MAIN} signal appears as normally high and pulses low whenever the divider reaches terminal count from the value programmed into the NM1, NM2 or NM3 registers. The f_{MAIN} signal can be used to verify the divide ratio of the MAIN divider and the prescaler.

Test Pin

The Test pin, Pin 19, is a buffered logic input which is exclusively ORed with the output of the prescaler. The output of the XOR gate is the input to the MAIN divider. The Test pin must be connected to V_{DD} during normal operation as a synthesizer. This pin can be used as an input for verifying the divide ratio of the MAIN divider; while in this condition the input to the prescaler, RF_{IN}, may be connected to V_{CCP} through a 10kΩ resistor in order to place prescaler output into a known state.

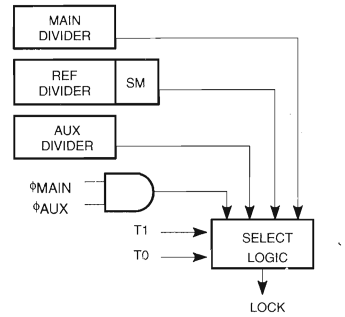
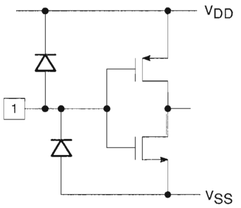
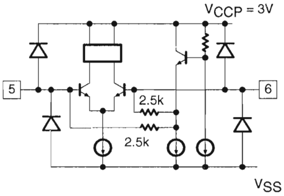
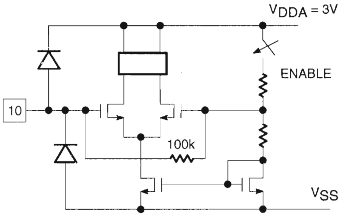
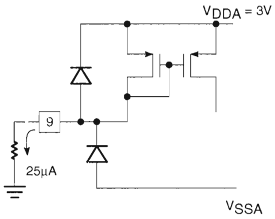
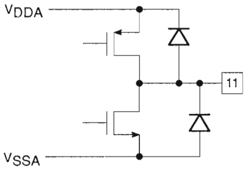
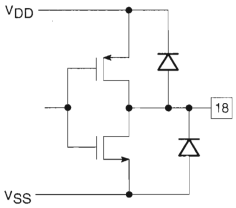


Figure 8. Test Mode Diagram

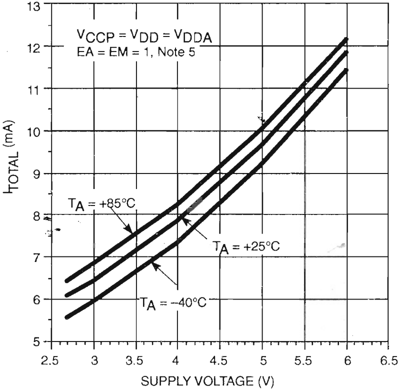
PIN FUNCTIONS

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	CLOCK	—	
2	DATA	—	
3	STROBE	—	
19	TEST	—	
5	RF_{IN}	2.1	
6	$\overline{RF_{IN}}$	2.1	
8	REF_{IN}	1.8	
10	AUX_{IN}	1.8	

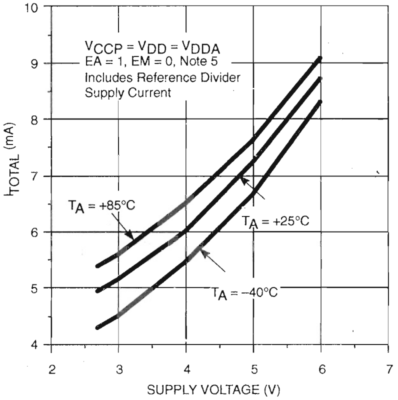
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
9	RA	1.35	
16	RN	1.35	
17	RF	1.35	
11	PHA	—	
13	PHI	—	
14	PHP	—	
18	LOCK	—	

TYPICAL PERFORMANCE CHARACTERISTICS

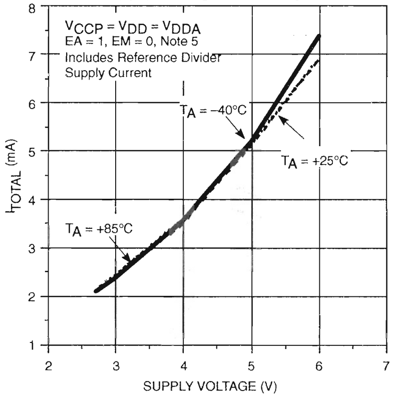
Operational Supply Current vs Supply Voltage and Temperature



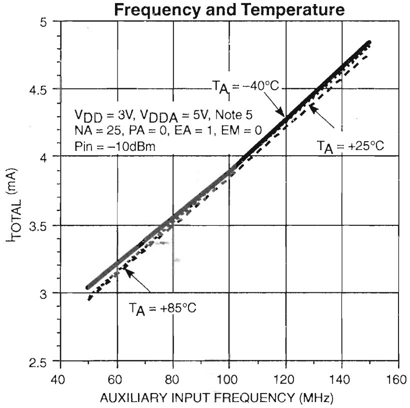
Main Operational Supply Current vs Supply Voltage and Temperature



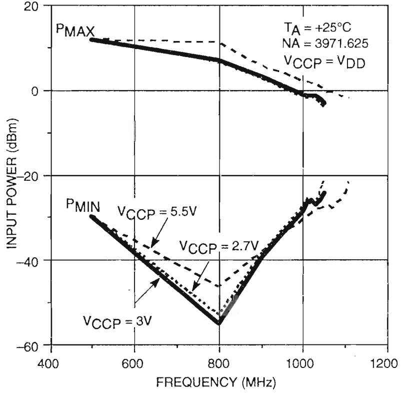
Auxiliary Operational Supply Current vs Supply Voltage and Temperature



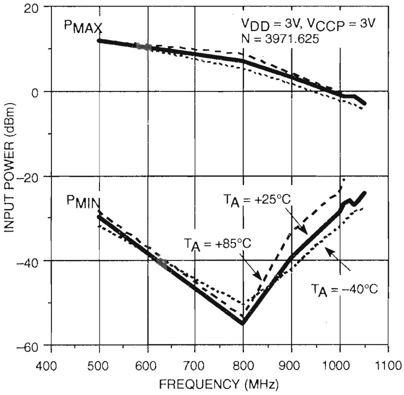
Auxiliary Operational Supply Current vs Frequency and Temperature



Main Divider Input Power vs Frequency and Supply

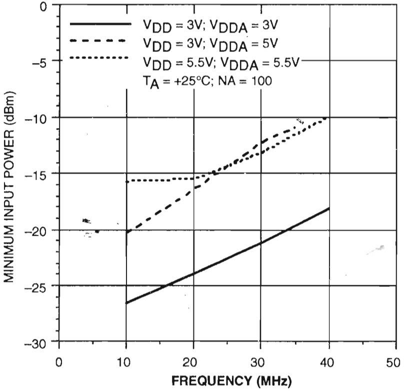


Main Divider Input Power vs Frequency and Temperature

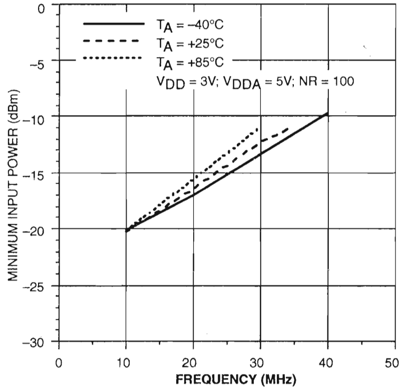


TYPICAL PERFORMANCE CHARACTERISTICS

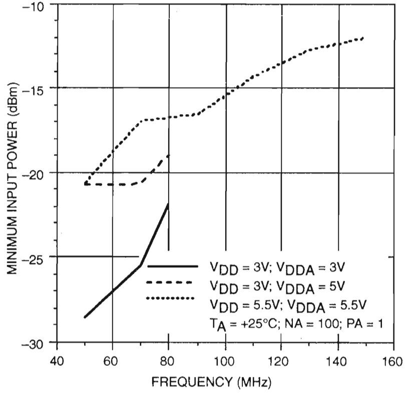
Reference Divider Minimum Input power vs Frequency and Supply



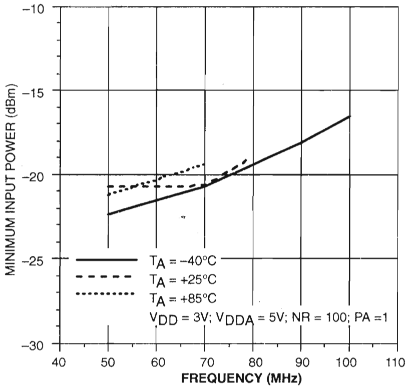
Reference Divider Minimum Input power vs Frequency and Temperature



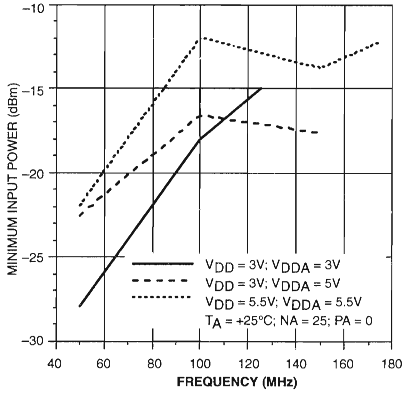
Auxiliary Divider Minimum Input power vs Frequency and Supply



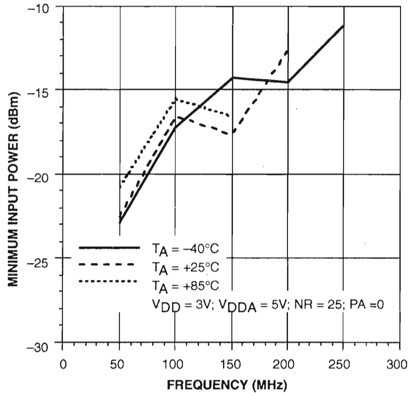
Auxiliary Divider Minimum Input power vs Frequency and Temperature

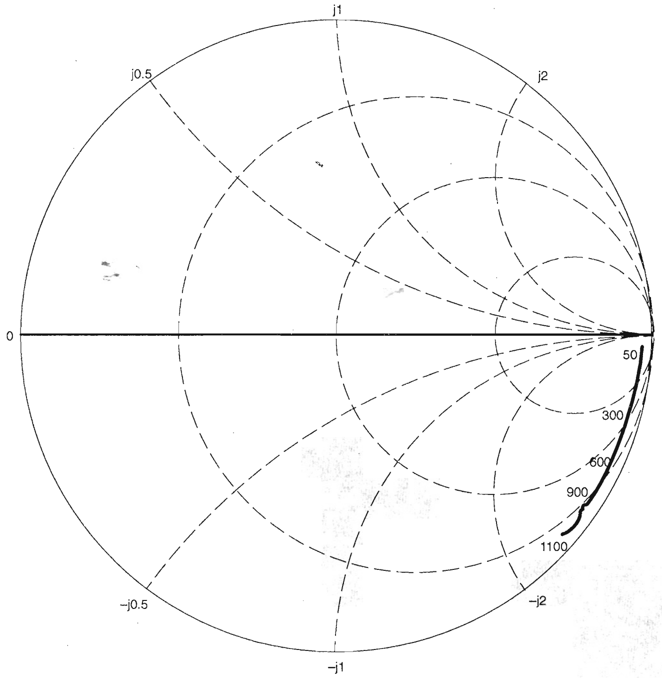


Auxiliary Divider Minimum Input power vs Frequency and Supply



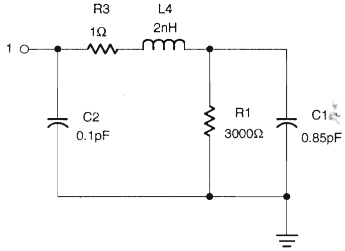
Auxiliary Divider Minimum Input power vs Frequency and Temperature



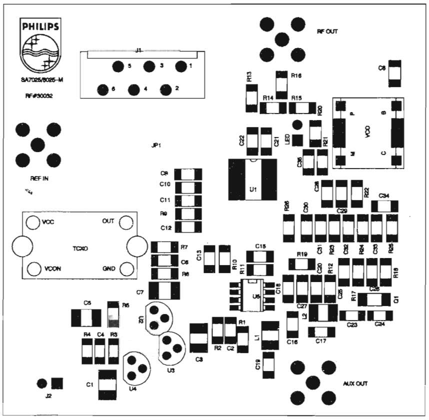


Typical RF_{IN} Input Impedance

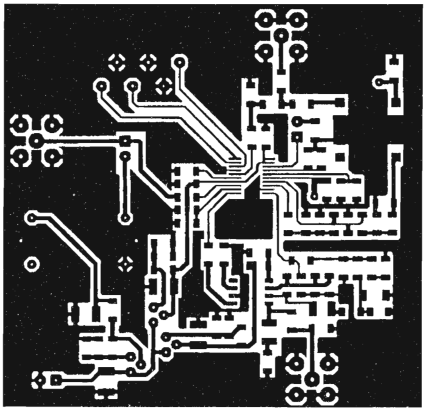
$V_{CCP} = V_{DD} = 3V$
$T_A = 25°C$



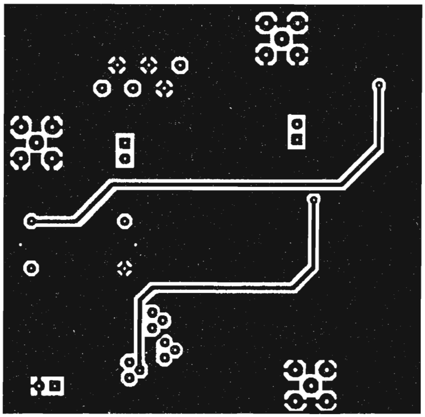
Equivalent Input Impedance



TOP SILK SCREEN



TOP VIEW



BOTTOM VIEW

Figure 9. SA7025DK Demoboard Layout (NOT ACTUAL SIZE)

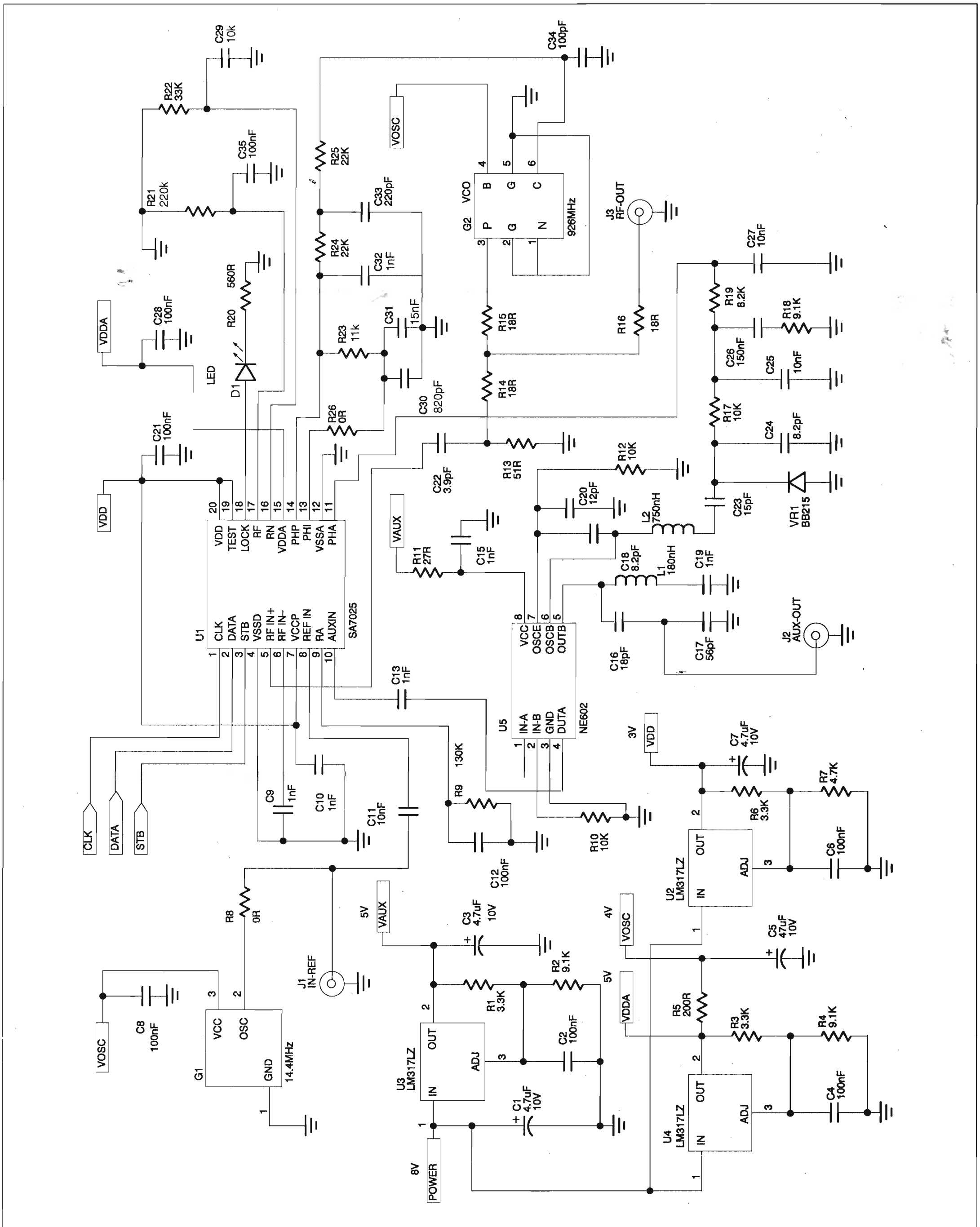


Figure 10. SA7025DK Application Circuit

Low-voltage 2GHz fractional-N synthesizer SA8025

DESCRIPTION

The SA8025 is a monolithic low power, high performance dual frequency synthesizer fabricated in QUBiC BiCMOS technology. Featuring Fractional-N division with selectable modulo 5 or 8 implemented in the Main synthesizer to allow the phase detector comparison frequency to be five or eight times the channel spacing. This feature reduces the overall division ratio yielding a lower noise floor and faster channel switching. The phase detectors and charge pumps are designed to achieve phase detector comparison frequencies up to 5MHz. A four modulus prescaler (divide by 64/65/68/73) is integrated on chip with a maximum input frequency of 1.8GHz at 3V. Programming and channel selection are realized by a high speed 3-wire serial interface. A 1GHz version (SA7025DK) is also available with the same pinout.

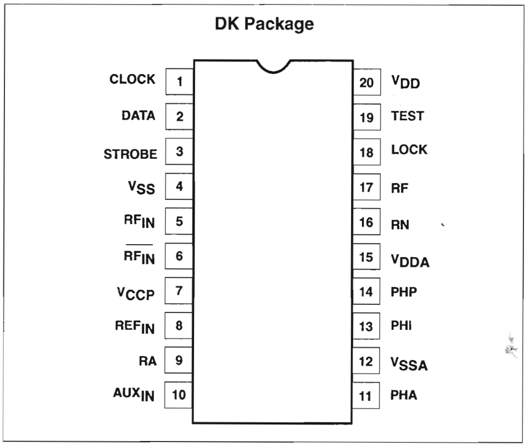
FEATURES

- Operation up to 1.8GHz at 3V
- Fast locking by "Fractional-N" divider
- Auxiliary synthesizer
- Digital phase comparator with proportional and integral charge pump output
- High speed serial input
- Low power consumption
- Programmable charge pump currents
- Supply voltage range 2.7 to 5.5V
- Excellent input sensitivity: $V_{RF\_IN} = -20dBm$

APPLICATIONS

- PHP (Personal Handy Phone)
- PDC (Personal Digital Cellular)
- PCS (Personal Communication Service)
- Portable communication systems

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (SSOP)	–40 to +85°C	SA8025DK	1563–

ABSOLUTE MAXIMUM RATINGS

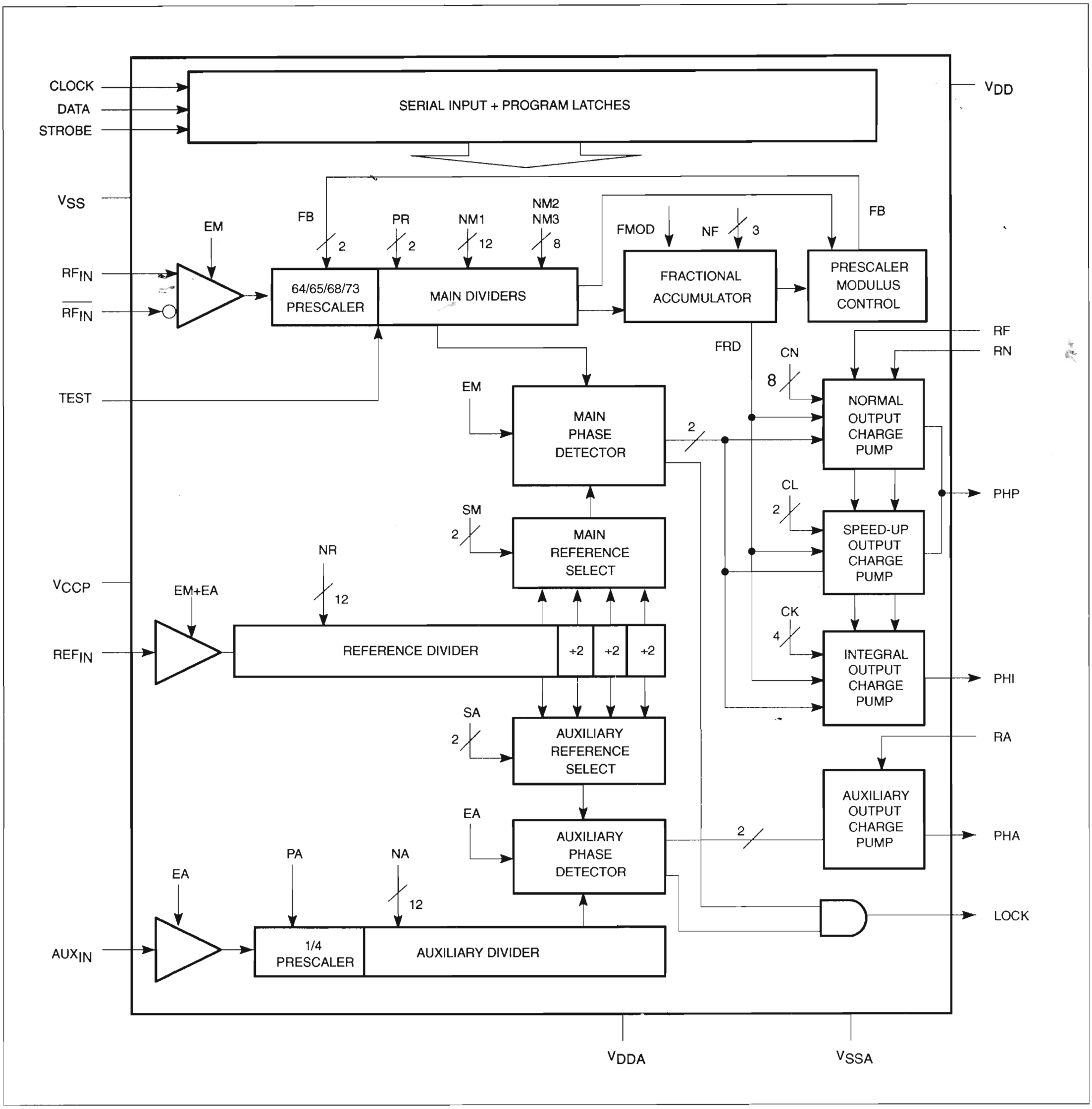
SYMBOL	PARAMETER	RATING	UNITS
V	Supply voltage, V_{DD}, V_{DDA}, V_{CCP}	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{DD} + 0.3)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C

NOTE: Thermal impedance (θ_{JA}) = 117°C/W.

PIN DESCRIPTIONS

Symbol	Pin	Description
CLOCK	1	Serial clock input
DATA	2	Serial data input
STROBE	3	Serial strobe input
V_{SS}	4	Digital ground
RF_{IN}	5	Prescaler positive input
$\overline{RF_{IN}}$	6	Prescaler negative input
V_{CCP}	7	Prescaler positive supply voltage. This pin supplies power to the prescaler and RF input buffer
REF_{IN}	8	Reference divider input
RA	9	Auxiliary current setting; resistor to V_{SSA}
AUX_{IN}	10	Auxiliary divider input
PHA	11	Auxiliary phase detector output
V_{SSA}	12	Analog ground
PHI	13	Integral phase detector output
PHP	14	Proportional phase detector output
V_{DDA}	15	Analog supply voltage. This pin supplies power to the charge pumps, Auxiliary prescaler, Auxiliary and Reference buffers.
RN	16	Main current setting; resistor to V_{SSA}
RF	17	Fractional compensation current setting; resistor to V_{SSA}
LOCK	18	Lock detector output
TEST	19	Test pin; connect to V_{DD}
V_{DD}	20	Digital supply voltage. This pin supplies power to the CMOS digital part of the device

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{CCP} = 3V$; $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
$I_{STANDBY}$	Standby supply currents	$V_{RA} = V_{RF} = V_{RN} = V_{DDA}$, EM = EA = 0		100		µA
I_{AUX}	Operational supply currents[5]	EM = 0, EA = 1		2.7		mA
I_{MAIN}	Operational supply currents[5]	EM = 1, EA = 0		9.6		mA
I_{TOTAL}	Operational supply currents[5]	EM = EA = 1		11		mA
Digital inputs CLK, DATA, STROBE						
V_{IH}	High level input voltage range		$0.7xV_{DD}$		V_{DD}	V
V_{IL}	Low level input voltage range		0		$0.3xV_{DD}$	V
Digital outputs LOCK						
V_{OL}	Output voltage LOW	$I_O = 2mA$			0.4	V
V_{OH}	Output voltage HIGH	$I_O = -2mA$	$V_{DD}-0.4$			V
Charge pump PHA						
$\lvert I_{PHA} \rvert$	Output current PHA	$I_{RA} = -62.5µA$; $V_{PHA} = V_{DDA}/2$[13]	400	500	600	µA
		$I_{RA} = -25µA$; $V_{PHA} = V_{DDA}/2$	160	200	240	
$\frac{\Delta I_{PHP\_A}}{\lvert I_{PHP\_A} \rvert}$	Relative output current variation PHA	$I_{RA} = -62.5µA$[2, 13]		2	6	%
ΔI_{PHA_M}	Output current matching	$I_{RA} = -62.5µA$; $V_{PHA} = V_{DDA}/2$[12, 13]			±50	µA
Charge pump PHP, normal mode[1, 4, 6] $V_{RF} = V_{DDA}$						
$\lvert I_{PHP\_N} \rvert$	Output current PHP	$I_{RN} = -62.5µA$; $V_{PHP} = V_{DDA}/2$[13]	440	550	660	µA
		$I_{RN} = -25µA$; $V_{PHP} = V_{DDA}/2$	175	220	265	
$\frac{\Delta I_{PHP\_N}}{I_{PHP\_N}}$	Relative output current variation PHP	$I_{RN} = -62.5µA$[2, 13]		2	6	%
$\Delta I_{PHP\_N\_M}$	Output current matching	$I_{RN} = -62.5µA$;$V_{PHP} = V_{DDA}/2$[12, 13]			±50	µA
Charge pump PHP, speed-up mode [1, 4, 7] $V_{RF} = V_{DDA}$						
$\lvert I_{PHP\_S} \rvert$	Output current PHP	$I_{RN} = -62.5µA$; $V_{PHP} = V_{DDA}/2$[13]	2.20	2.75	3.30	mA
		$I_{RN} = -25µA$; $V_{PHP} = V_{DDA}/2$	0.85	1.1	1.35	
$\frac{\Delta I_{PHP\_S}}{I_{PHP\_S}}$	Relative output current variation PHP	$I_{RN} = -62.5µA$[2, 13]		2	6	%
$\Delta I_{PHP\_S\_M}$	Output current matching	$I_{RM} = -62.5µA$;$V_{PHP} = V_{DDA}/2$[12, 13]			±250	µA
Charge pump PHI, speed-up mode [1, 4, 8] $V_{RF} = V_{DDA}$						
$\lvert I_{PHI} \rvert$	Output current PHI	$I_{RN} = -62.5µA$; $V_{PHI} = V_{DDA}/2$[13]	4.4	5.5	6.6	mA
		$I_{RN} = -25µA$; $V_{PHI} = V_{DDA}/2$	1.75	2.2	2.65	
$\frac{\Delta I_{PHI}}{I_{PHI}}$	Relative output current variation PHI	$I_{RN} = -62.5µA$[2, 13]		2	8	%
ΔI_{PHI_M}	Output current matching	$I_{RN} = -62.5µA$; $V_{PHI} = V_{DDA}/2$[12, 13]			±500	µA
Fractional compensation PHP, normal mode [1, 9] $V_{RN} = V_{DDA}$, $V_{PHP} = V_{DDA}/2$						
$I_{PHP\_F\_N}$	Fractional compensation output current PHP vs F_{RD}[3]	$I_{RF} = -62.5µA$;F_{RD} = 1 to 7[13]	–675	–500	–325	nA
		$I_{RF} = -25µA$;F_{RD} = 1 to 7	–270	–200	–130	
Fractional compensation PHP, speed up mode [1, 10] $V_{PHP} = V_{DDA}$, $V_{RN} = V_{DDA}$						
$I_{PHP\_F\_S}$	Fractional compensation output current PHP vs F_{RD}[3]	$I_{RF} = -62.5µA$;F_{RD} = 1 to 7[13]	–3.35	–2.5	–1.65	µA
		$I_{RF} = -25µA$;F_{RD} = 1 to 7	–1.35	–1.0	–0.65	
Fractional compensation PHI, speed up mode [1, 11] $V_{PHP} = V_{DDA}/2$, $V_{RN} = V_{DDA}$						
I_{PHI_F}	Fractional compensation output current PHI vs F_{RD}[3]	$I_{RF} = -62.5µA$;F_{RD} = 1 to 7[13]	–5.4	–4.0	–2.6	µA
		$I_{RF} = -25µA$;F_{RD} = 1 to 7	–2.15	–1.6	–1.05	

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Charge pump leakage currents, charge pump not active						
I_{PHP_L}	Output leakage current PHP; normal mode[1]	V_{PHP} = 0.7 to V_{DDA} – 0.8		0.1	10	nA
I_{PHI_L}	Output leakage current PHI; normal mode[1]	V_{PHI} = 0.7 to V_{DDA} – 0.8		0.1	10	nA
I_{PHA_L}	Output leakage current PHA	V_{PHA} = 0.7 to V_{DDA} – 0.8		0.1	10	nA

AC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{CCP} = 3V$; $T_A = 25°C$; unless otherwise specified. Test Circuit, Figure 2. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Main divider						
f_{RF_IN}	Input signal frequency	Pin = -10dBm, Direct coupled input[14]	0	1.8		GHz
		Pin = -10dBm, 1000pF input coupling		1.8		
V_{RF_IN}	Input sensitivity	f_{IN} = 1700MHz	–20		0	dBm
Reference divider						
f_{REF_IN}	Input signal frequency		0		20	MHz
		$4.5V \leq V_{DDA} \leq 5.5V$	0		30	
V_{REF_IN}	Input signal range, AC coupled		300			mV_{P-P}
Z_{REF_IN}	Reference divider input impedance[15]			100		kΩ
					3	pF
Auxiliary divider						
f_{AUX_IN}	Input signal frequency		0		50	MHz
	PA = "0", prescaler enabled	$4.5V \leq V_{DDA} \leq 5.5V$	0		150	
	Input signal frequency		0		30	
	PA = "1", prescaler disabled	$4.5V \leq V_{DDA} \leq 5.5V$	0		40	
V_{AUX_IN}	Input signal range, AC coupled		200			mV_{P-P}
Z_{AUX_IN}	Auxiliary divider input impedance[15]			100		kΩ
					3	pF
Serial interface[15]						
f_{CLOCK}	Clock frequency				10	MHz
t_{SU}	Set-up time: DATA to CLOCK, CLOCK to STROBE		30			ns
t_H	Hold time; CLOCK to DATA		30			ns
t_W	Pulse width; CLOCK		30			ns
	Pulse width; STROBE	B, C, D, E words	30			
t_{SW}	Pulse width; STROBE	A word, PR = '01'	$\frac{1}{f_{VCO}} \cdot (NM2 \cdot 65) + t_W$			ns
		A word, PR = '10'	$\frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65) + (NM3 + 1) \cdot 68] + t_W$			
		A word, PR = '11'	$\frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65 + (NM3 + 1) \cdot 68 + (NM4 + 1) \cdot 73)] + t_W$			
		A word, PR = '00'	$\frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65) + (NM4 + 1) \cdot 73] + t_W$			

NOTES:

1. When a serial input "A" word is programmed, the main charge pumps on PHP and PHI are in the "speed up mode" as long as STROBE = H. When this is not the case, the main charge pumps are in the "normal mode".
2. The relative output current variation is defined thus:
   $$\frac{\Delta I_{OUT}}{I_{OUT}} = 2 \cdot \frac{(I_2 - I_1)}{|(I_2 + I_1)|}$$ with $V_1 = 0.7V$, $V_2 = V_{DDA} - 0.8V$ (see Figure 1).
3. F_{RD} is the value of the 3 bit fractional accumulator.
4. Monotonicity is guaranteed with $C_N = 0$ to 255.
5. Power supply current measured with $f_{RF\_IN} = 1667.4MHz$, NM1 = 0, NM2 = 1, NM3 = 1, NM4 = 4, FMOD = 8, N = 694 6/8, main phase detector frequency = 2.4MHz, $f_{REF\_IN} = 19.2MHz$, NR = 8, SM = 1, $f_{AUX\_IN} = 150MHz$, NA = 125, SA = 1, PA = 0, auxiliary phase detector frequency = 300kHz, IRN = IRA = IRF = 25μA, CN = 160, CL = 0, CK = 0, lock condition, normal mode, $V_{CCP} = V_{DD} = V_{DDA} = 3V$. Operational supply current = $I_{DDA} + I_{DD} + I_{CCP}$.
6. Specification condition: CN = 255
7. Specification conditions:
   1) CN = 255; CL = 1, or
   2) CN = 75; CL = 3
8. Typical output current $| I_{PHI} | = -I_{RN}$ x CN x $2^{(CL+1)}$ x CK/32:
   1) CN = 160; CL = 3; CK = 1, or
   2) CN = 160; CL = 2; CK = 2, or
   3) CN = 160; CL = 1; CK = 4, or
   4) CN = 160; CL = 0; CK = 8
9. Specification condition: $F_{RD} = 1$ to 7.
10. Specification conditions: $F_{RD} = 1$ to 7; CL = 1.
11. Specification conditions:
    1) $F_{RD} = 1$ to 7; CL = 1; CK = 2, or
    2) $F_{RD} = 1$ to 7; CL = 2; CK = 1.
12. The output current matching is measured when both (positive current and negative current) sections of the output charge pumps are on.
13. Limited analog supply voltage range 4.5 to 5.5V.
14. For $f_{IN} < 50MHz$, minimum input slew rate of 32V/μs is required.
15. Guaranteed by design.

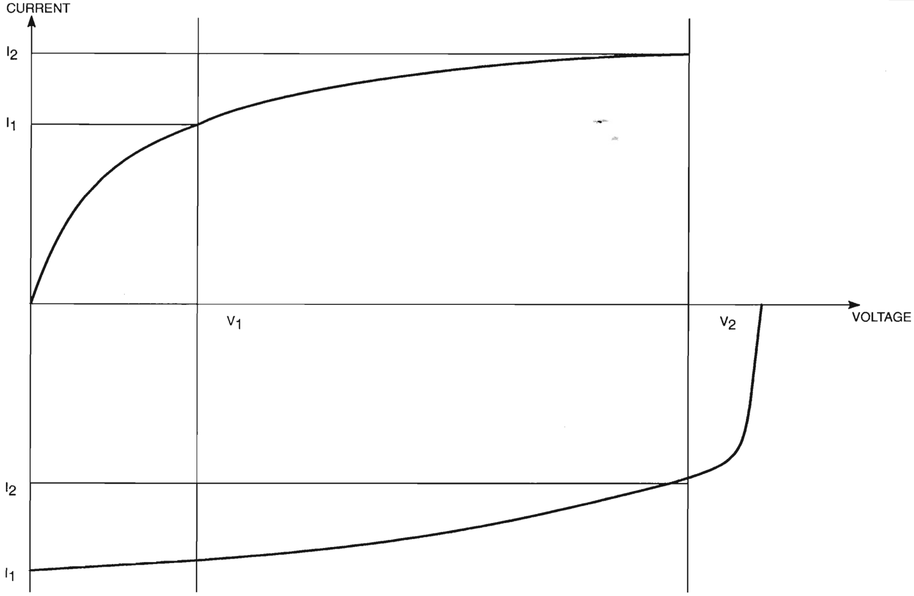


Figure 1. Relative Output Current Variation

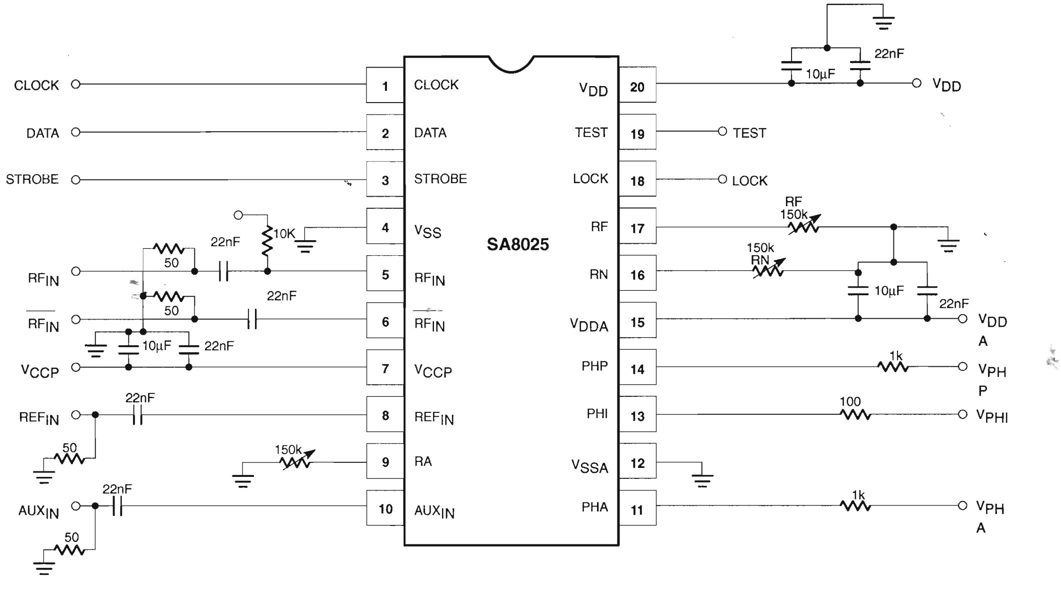


Figure 2. Test Circuit

AC TIMING CHARACTERISTICS

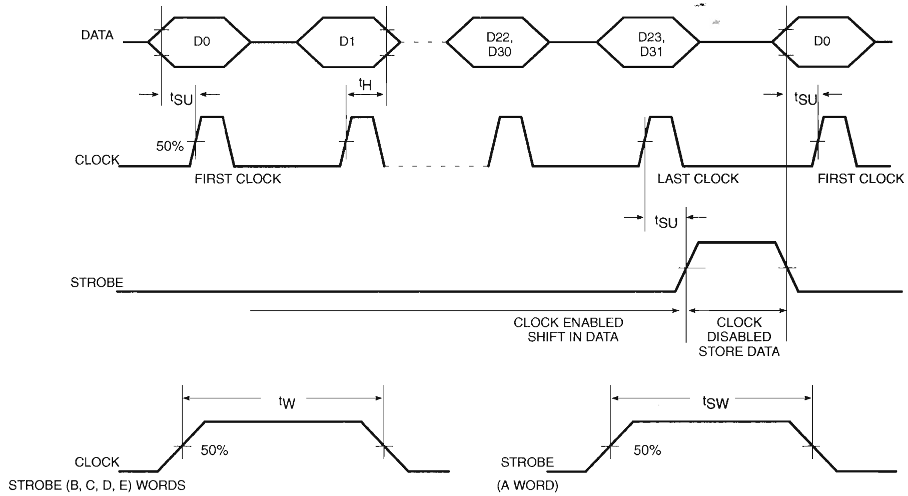


Figure 3. Serial Input Timing Sequence

FUNCTIONAL DESCRIPTION

Serial Input Programming

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program all counter ratios, DACs, selection and enable bits. The programming data is structured into 24 or 32 bit words; each word includes 1 or 4 address bits. Figure 3 shows the timing diagram of the serial input. When the STROBE = L, the clock driver is enabled and on the positive edges of the CLOCK the signal on DATA input is clocked into a shift register. When the STROBE = H, the clock is disabled and the data in the shift register remains stable. Depending on the 1 or 4 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 4 words must be sent: D, C, B and A. Figure 4 and Table 1 shows the format and the contents of each word. The E word is for testing purposes only. The E (test) word is reset when programming the D word. The data for CN and PR is stored by the B word in temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the A word into the work registers which avoids false temporary main divider input. CN is only loaded from the temporary registers when a short 24 bit A0 word is used. CN will be directly loaded by programming a long 32 bit A1 word. The flag LONG in the D word determines whether A0 (LONG = “0”) or A1 (LONG = “1”) format is applicable. The A word contains new data for the main divider.

Main Divider Synchronization

The A word is loaded only when a main divider synchronization signal is also active in order to avoid phase jumps when reprogramming the main divider. The synchronization signal is generated by the main divider. The signal is active while the NM1 divider is counting down from the programmed value. The new A word will be loaded after the NM1 divider has reached its terminal count; also, at this time a main divider output pulse will be sent to the main phase detector. The loading of the A word is disabled while the other dividers are counting up to their programmed values. Therefore, the new A word will be correctly loaded provided that the STROBE signal has been at an active high value for at least a minimum number of VCO input cycles at RF_{IN} or $\overline{RF_{IN}}$.

For PR = ‘01’

$$t\_strobe\_min = \frac{1}{f_{VCO}}(NM2 \cdot 65) + t_W$$

For PR = ‘10’

$$t\_strobe\_min = \frac{1}{f_{VCO}}[NM2 \cdot 65 + (NM3 + 1) \cdot 68] + t_W$$

For PR = ‘11’

$$t\_strobe\_min = \frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65 + (NM3 + 1) \\ 68 + (NM4 + 1) \cdot 73)] + t_W$$

For PR = ‘00’

$$t\_strobe\_min = \frac{1}{f_{VCO}} \cdot [(NM2 \cdot 65) + (NM4 + 1) \cdot 73] + t_W$$

Programming the A word means also that the main charge pumps on output PHP and PHI are set into the speed-up mode as long as the STROBE is H.

Auxiliary Divider

The input signal on AUX_IN is amplified to logic level by a single-ended CMOS input buffer, which accepts low level AC coupled input signals. This input stage is enabled if the serial control bit EA = “1”. Disabling means that all currents in the input stage are switched off. A fixed divide by 4 is enabled if PA = “0”. This divider has been optimized to accept a high frequency input signal. If PA = “1”, this divider is disabled and the input signal is fed directly to the second stage, which is a 12-bit programmable divider with standard input frequency (40MHz). The division ratio can be expressed as:

if PA = “0”: N = 4 x NA
if PA = “1”: N = NA; with NA = 4 to 4095

Reference Divider

The input signal on REF_IN is amplified to logic level by a single-ended CMOS input buffer, which accepts low level AC coupled input signals. This input stage is enabled by the OR function of the serial input bits EA and EM. Disabling means that all currents in the input stage are switched off. The reference divider consists of a programmable divider by NR (NR = 4 to 4095) followed by a three bit binary counter. The 2 bit SM register (see Figure 5) determines which of the 4 output pulses is selected as the main phase detector input. The 2 bit SA register determines the selection of the auxiliary phase detector signal.

Main Divider

The differential inputs are amplified (to internal ECL logic levels) and provide excellent sensitivity (–20dBm at 1.7GHz) making the prescaler ideally suited to directly interface to a VCO as integrated on the Philips front-end devices including RF gain stage, VCO and mixer. The internal four modulus prescaler feedback loop FB controls the selection of the divide by ratios 64/65/68/73, and reduces the minimum system division ratio below the typical value required by standard dual modulus (64/65) devices.

This input stage is enabled when serial control bit EM = “1”. Disabling means that all currents in the prescaler are switched off.

The main divider is built up by a 12 bit counter plus a sign bit. Depending on the serial input values NM1, NM2, NM3, NM4 and the prescaler select PR, the counter will select a prescaler ratio during a number of input cycles according to Table 2 and Table 3.

The loading of the work registers NM1, NM2, NM3, NM4 and PR is synchronized with the state of the main counter, to avoid extra phase disturbance when switching over to another main divider ratio as explained in the Serial Input Programming section.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented with NF. The accumulator works modulo Q. Q is preset by the serial control bit FMOD to 8 when FMOD = “1”. Each time the accumulator overflows, the feedback to the prescaler will select one cycle using prescaler ratio R2 instead of R1.

As shown above, this will increase the overall division ratio by 1 if R2 = R1 + 1. The mean division ratio over Q main divider will then be

$$NQ = N + \frac{NF}{Q}$$

Programming a fraction means the prescaler with main divider will divide by N or N + 1. The output of the main divider will be modulated with a fractional phase ripple. This phase ripple is proportional to the contents of the fractional accumulator FRD, which is used for fractional current compensation.

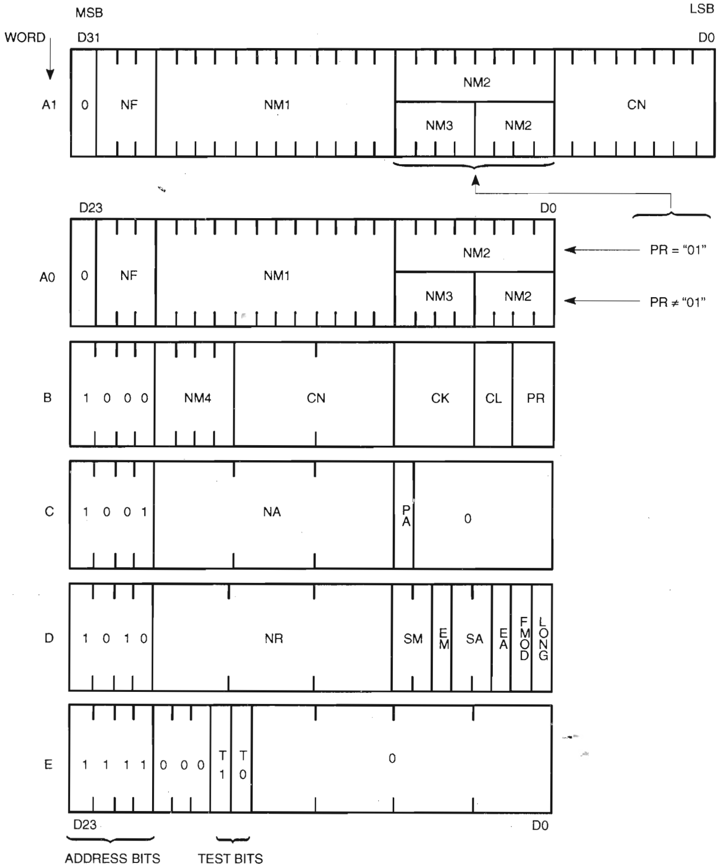


Figure 4. Serial Input Word Format

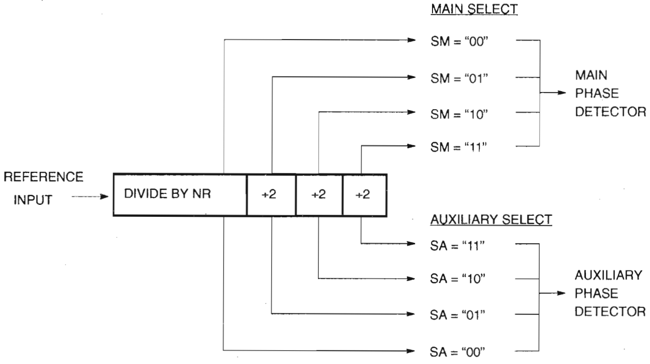


Figure 5. Reference Divider

Table 1. Function Table

Symbol	Bits	Function
NM1	12	Number of main divider cycles when prescaler modulus = 64*
NM2	8 if PR = "01" 4 if PR = "10"	Number of main divider cycles when prescaler modulus = 65*
NM3	4 if PR = "10"	Number of main divider cycles when prescaler modulus = 68*
NM4	4 if PR = "11" or "00"	Number of main divider cycles when prescaler modulus = 73*
PR	2	Prescaler type in use PR = "01": modulus 2 prescaler (64/65) PR = "10": modulus 3 prescaler (64/65/68) PR = "11": modulus 4 prescaler (64/65/68/73) PR = "00": modulus 3 prescaler (64/65/73)
NF	3	Fractional-N increment
FMOD	1	Fractional-N modulus selection flag "1": modulo 8 "0": modulo 5
LONG	1	A word format selection flag "0": 24 bit A0 format "1": 32 bit A1 format
CN	8	Binary current setting factor for main charge pumps
CL	2	Binary acceleration factor for proportional charge pump current
CK	4	Binary acceleration factor for integral charge pump current
EM	1	Main divider enable flag
EA	1	Auxiliary divider enable flag
SM	2	Reference select for main phase detector
SA	2	Reference select for auxiliary phase detector
NR	12	Reference divider ratio
NA	12	Auxiliary divider ratio
PA	1	Auxiliary prescaler mode: PA = "0": divide by 4 PA = "1": divide by 1

*Not including reset cycles and Fractional-N effects.

Table 2. Prescaler Ratio

The total division ratio from prescaler to the phase detector may be expressed as:

if PR = "01"	N = (NM1 + 2) x 64 + NM2 x 65 N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 (*)
if PR = "10"	N = (NM1 + 2) x 64 + NM2 x 65 + (NM3 + 1) x 68 N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 + (NM3 + 1) x 68 (*)
if PR = "11"	N = (NM1 + 2) x 64 + NM2 x 65 + (NM3 + 1) x 68 + (NM4 + 1) x 73 N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 + (NM3 + 1) x 68 + (NM4 + 1) x 73 (*)
if PR = "00"	N = (NM1 + 2) x 64 + NM2 x 65 + (NM4 + 1) x 73 N' = (NM1 + 1) x 64 + (NM2 + 1) x 65 + (NM4 + 1) x 73 (*)

(*) When the fractional accumulator overflows the prescaler ratio = 65 (64 + 1) and the total division ratio N' = N + 1

Table 3. PR Modulus

PR	Modulus Prescaler	Bit Capacity			
		NM1	NM2	NM3	NM4
01	2	12	8	–	–
10	3	12	4	4	–
11	4	12	4	4	4
00	3	12	4	–	4

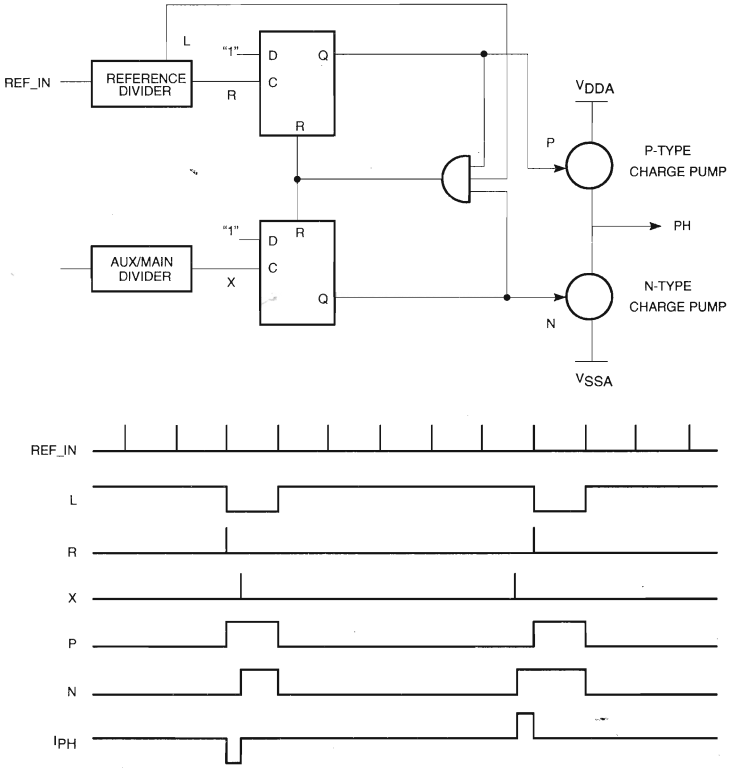


Figure 6. Phase Detector Structure with Timing

Phase Detectors

The auxiliary and main phase detectors are a two D-type flip-flop phase and frequency detector shown in Figure 6. The flip-flops are set by the negative edges of output signals of the dividers. The rising edge of the signal, L, will reset the flip-flops after both flip-flops have been set. Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or deadband around zero phase error. The flip-flops drive on-chip charge pumps. A source current from the charge pump indicates the VCO frequency will be increased; a sink current indicates the VCO frequency will be decreased.

Current Settings

The SA8025 has 3 current setting pins: RA, RN and RF. The active charge pump currents and the fractional compensation currents are linearly dependent on the current connected between the current setting pin and V_{SS}. The typical value R (current setting resistor) can be calculated with the formula:

$$R = \frac{V_{DDA} - 0.9 - 150\sqrt{I_R}}{I_R}$$

The current can be set to zero by connecting the corresponding pin to V_{DDA}.

Auxiliary Output Charge Pumps

The auxiliary charge pumps on pin PHA are driven by the auxiliary phase detector and the current value is determined by the external resistor RA at pin RA. The active charge pump current is typically:

$$|I_{PHA}| = 8 \cdot I_{RA}$$

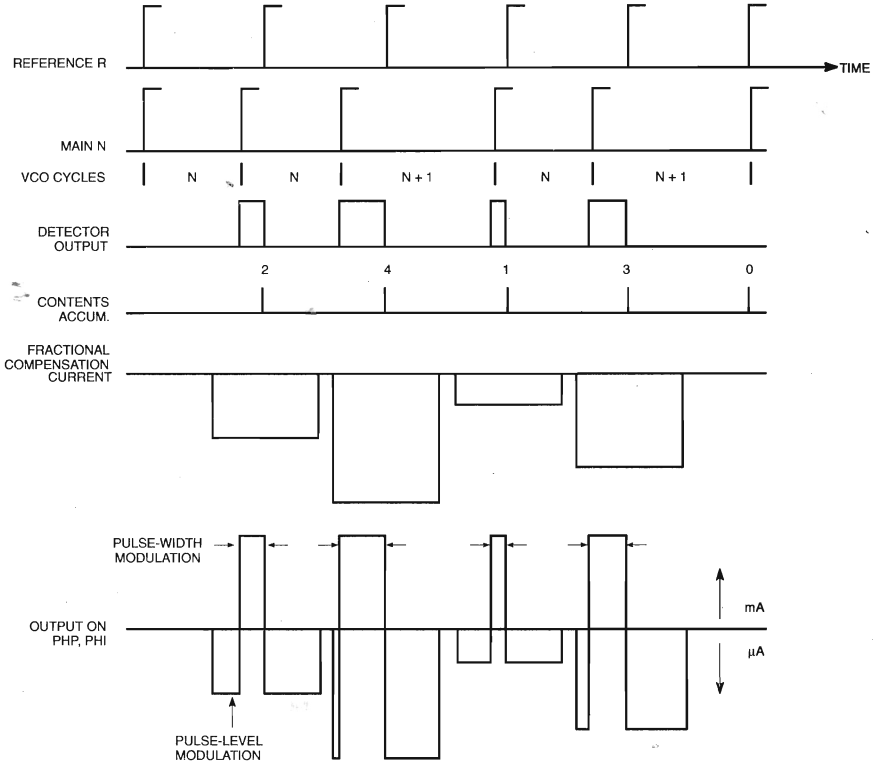


Figure 7. Waveforms for NF = 2, Fraction = 0.4

Main Output Charge Pumps and Fractional Compensation Currents

The main charge pumps on pin PHP and PHI are driven by the main phase detector and the current value is determined by the current at pin RN and via a number of DACs which are driven by registers of the serial input. The fractional compensation current is determined by the current at pin RF, the contents of the fractional accumulator FRD and a number of DACs driven by registers from the serial input. The timing for the fractional compensation is derived from the reference divider. The current is on during 1 input reference cycle before and 1 cycle after the output signal to the phase comparator. Figure 7 shows the waveforms for a typical case.

When the serial input A word is loaded, the output circuits are in the "speed-up mode" as long as the STROBE is H, else the "normal mode" is active. In the "normal mode" the current output PHP is:

$$I_{PHP\_N} = I_{PHP} + I_{PHP\_comp}$$

where:

$$|I_{PHP}| = \frac{CN \cdot I_{RN}}{32} \quad \text{:charge pump current}$$

$$|I_{PHP\_comp}| = FRD \cdot \frac{I_{RF}}{128} \quad \text{:fractional comp. current}$$

The current in PHI is zero in "normal mode".

In "speed-up mode" the current in output PHP is:

$$I_{PHP\_S} = I_{PHP} + I_{PHP\_comp}$$

$$|I_{PHP}| = \left(\frac{CN \cdot I_{RN}}{32}\right)(2^{CL+1} + 1)$$

$$|I_{PHP\_comp}| = \left(\frac{FRD \cdot I_{RF}}{128}\right)(2^{CL+1} + 1)$$

In "speed-up mode" the current in output PHI is:

$$I_{PHI\_S} = I_{PHI} + I_{PHI\_comp}$$

where:

$$|I_{PHI}| = \left(\frac{CN \cdot I_{RN}}{32}\right)(2^{CL+1})\ CK$$

$$|I_{PHI\_comp}| = \left(\frac{FRD \cdot I_{RN}}{128}\right)(2^{CL+1})\ CK$$

Lock Detect

The output LOCK is H when the auxiliary phase detector AND the main phase detector indicates a lock condition. The lock condition is defined as a phase difference of less than +1 cycle on the reference input REF_IN. The lock condition is also fulfilled when the relative counter is disabled (EM = “0” or respectively EA = “0”) for the main, respectively auxiliary counter.

Test Modes

The lock output is selectable as f_{REF}, f_{AUX}, f_{MAIN} and lock. Bits T1 and T0 of the E word control the selection (see Figures 4 and 8).

If T1 = T0 = Low, or if the E-word is not sent, the lock output is configured as the normal lock output described in the Lock Detect section.

If T1 = Low and T0 = High, the lock output is configured as f_{REF}. The signal is the buffered output of the reference divider NR and the 3-bit binary counter SM. The f_{REF} signal appears as normally low and pulses high whenever the divider reaches terminal count from the value programmed into the NR and SM registers. The f_{REF} signal can be used to verify the divide ratio of the Reference divider.

If T1 = High and T0 = Low, the lock output is configured as f_{AUX}. The signal is normally high and pulses low whenever the divider reaches terminal count from the value programmed into the NA and PA registers. The f_{AUX} signal can be used to verify the divide ratio of the Auxiliary divider.

If T1 = High and T0 = High, the lock output is configured as f_{MAIN}. The signal is the buffered output of the MAIN divider. The f_{MAIN} signal appears as normally high and pulses low whenever the divider reaches terminal count from the value programmed into the NM1, NM2, NM3 or NM4 registers. The f_{MAIN} signal can be used to verify the divide ratio of the MAIN divider and the prescaler.

Test Pin

The Test pin, Pin 19, is a buffered logic input which is exclusively ORed with the output of the prescaler. The output of the XOR gate is the input to the MAIN divider. The Test pin must be connected to V_{DD} during normal operation as a synthesizer. This pin can be used as an input for verifying the divide ratio of the MAIN divider; while in this condition the input to the prescaler, RF_{IN}, may be connected to V_{CCP} through a 10kΩ resistor in order to place prescaler output into a known state.

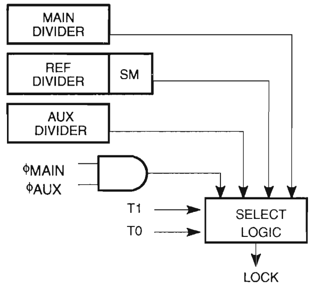
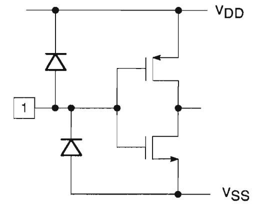
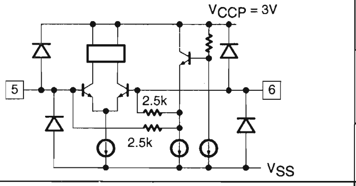
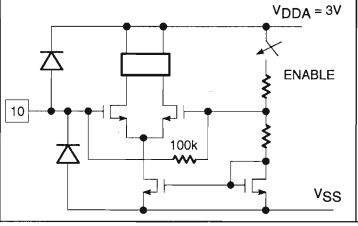
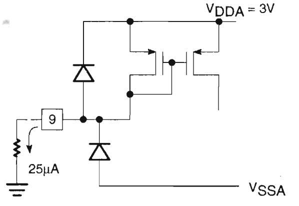
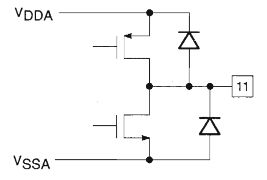
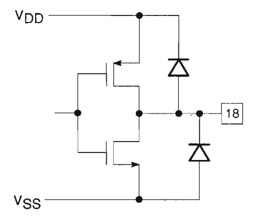


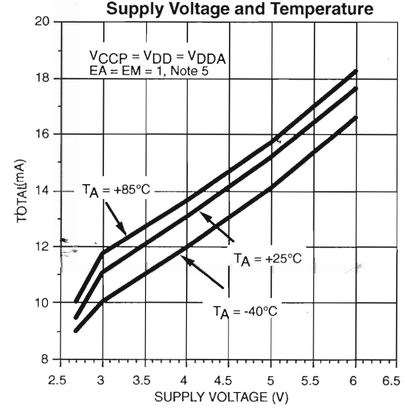
Figure 8. Test Mode Diagram

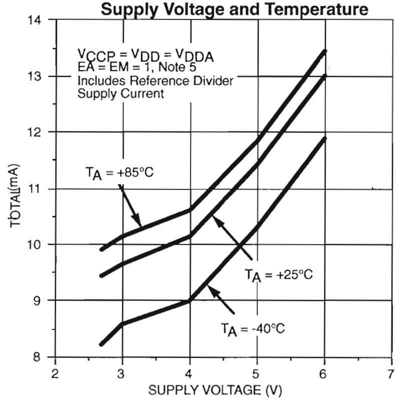
PIN FUNCTIONS

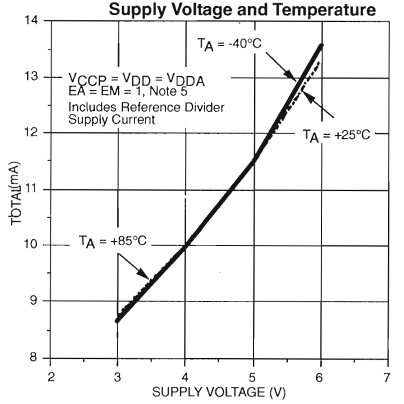
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	CLOCK	—	
2	DATA	—	
3	STROBE	—	
19	TEST	—	
5	RF_{IN}	2.1	
6	$\overline{RF_{IN}}$	2.1	
8	REF_{IN}	1.8	
10	AUX_{IN}	1.8	

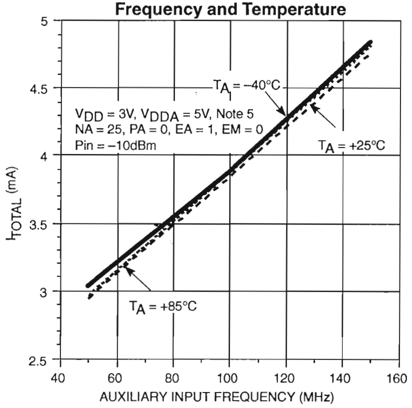
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
9	RA	1.35	
16	RN	1.35	
17	RF	1.35	
11	PHA	—	
13	PHI	—	
14	PHP	—	
18	LOCK	—	

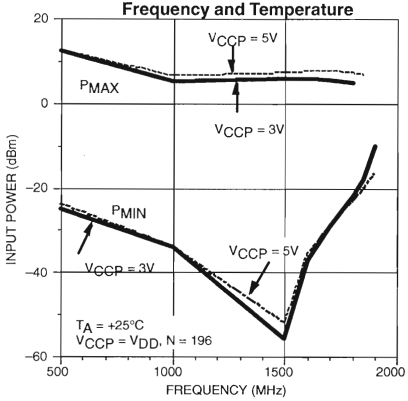
TYPICAL PERFORMANCE CHARACTERISTICS

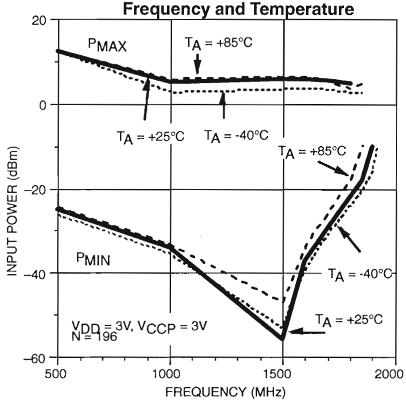

Operational Supply Current vs Supply Voltage and Temperature


Main Operational Supply Current vs Supply Voltage and Temperature


Auxiliary Operational Supply Current vs Supply Voltage and Temperature

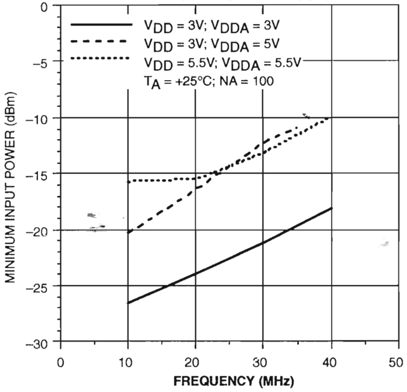

Auxiliary Operational Supply Current vs Frequency and Temperature


Main Divider Input Power vs Frequency and Temperature

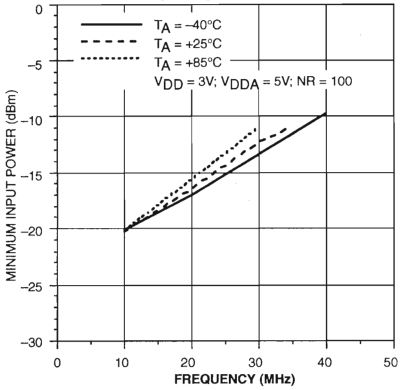

Main Divider Input Power vs Frequency and Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

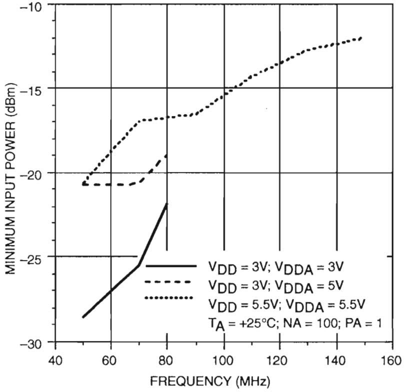
Reference Divider Minimum Input power vs Frequency and Supply



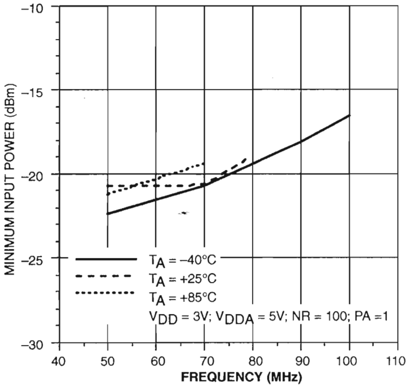
Reference Divider Minimum Input power vs Frequency and Temperature



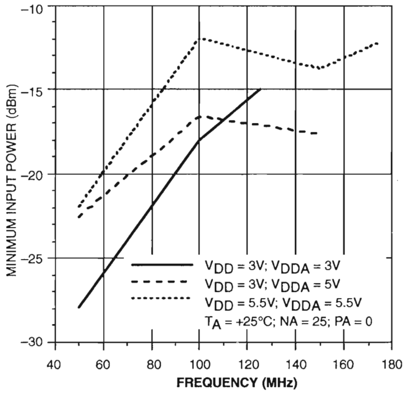
Auxiliary Divider Minimum Input power vs Frequency and Supply



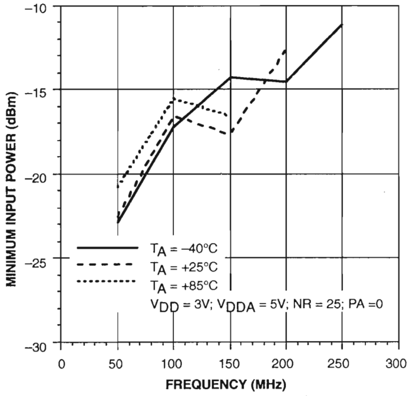
Auxiliary Divider Minimum Input power vs Frequency and Temperature

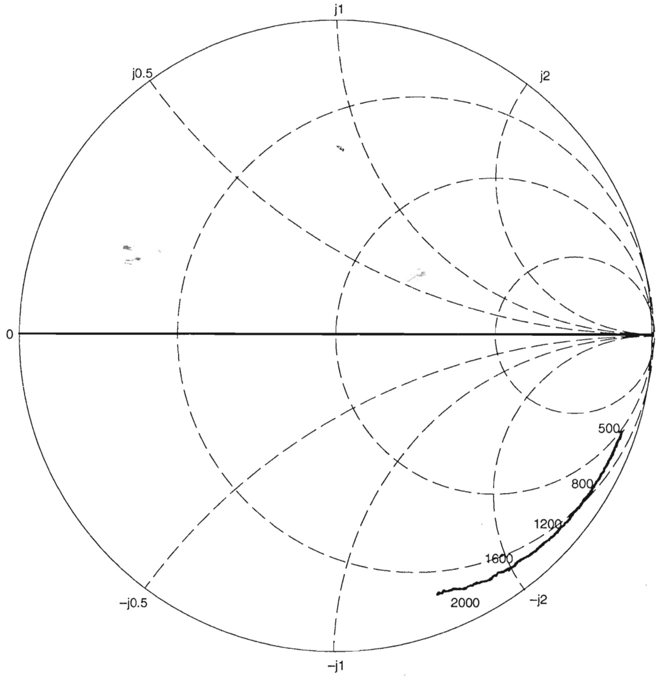


Auxiliary Divider Minimum Input power vs Frequency and Supply

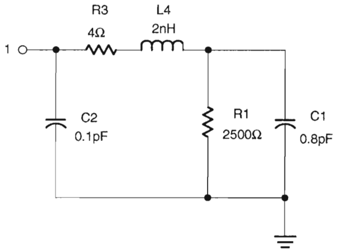


Auxiliary Divider Minimum Input power vs Frequency and Temperature



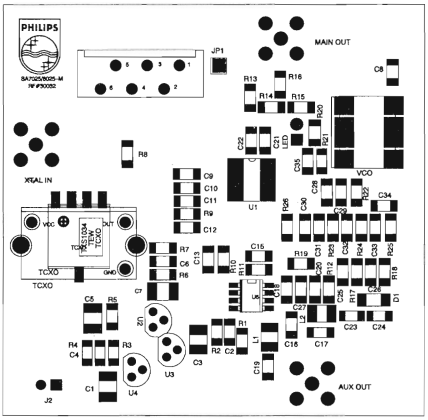


$V_{CCP} = V_{DD} = 3V$
$T_A = 25°C$

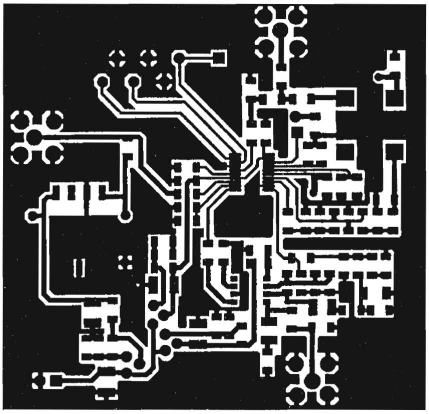


Equivalent Input Impedance

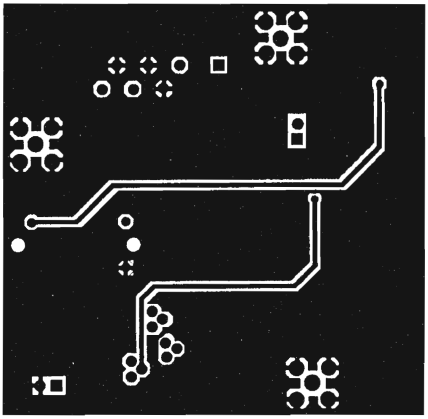
Typical RF_{IN} Input Impedance



TOP SILK SCREEN



TOP VIEW



BOTTOM VIEW

Figure 9. SA8025DK Demoboard Layout (NOT ACTUAL SIZE)

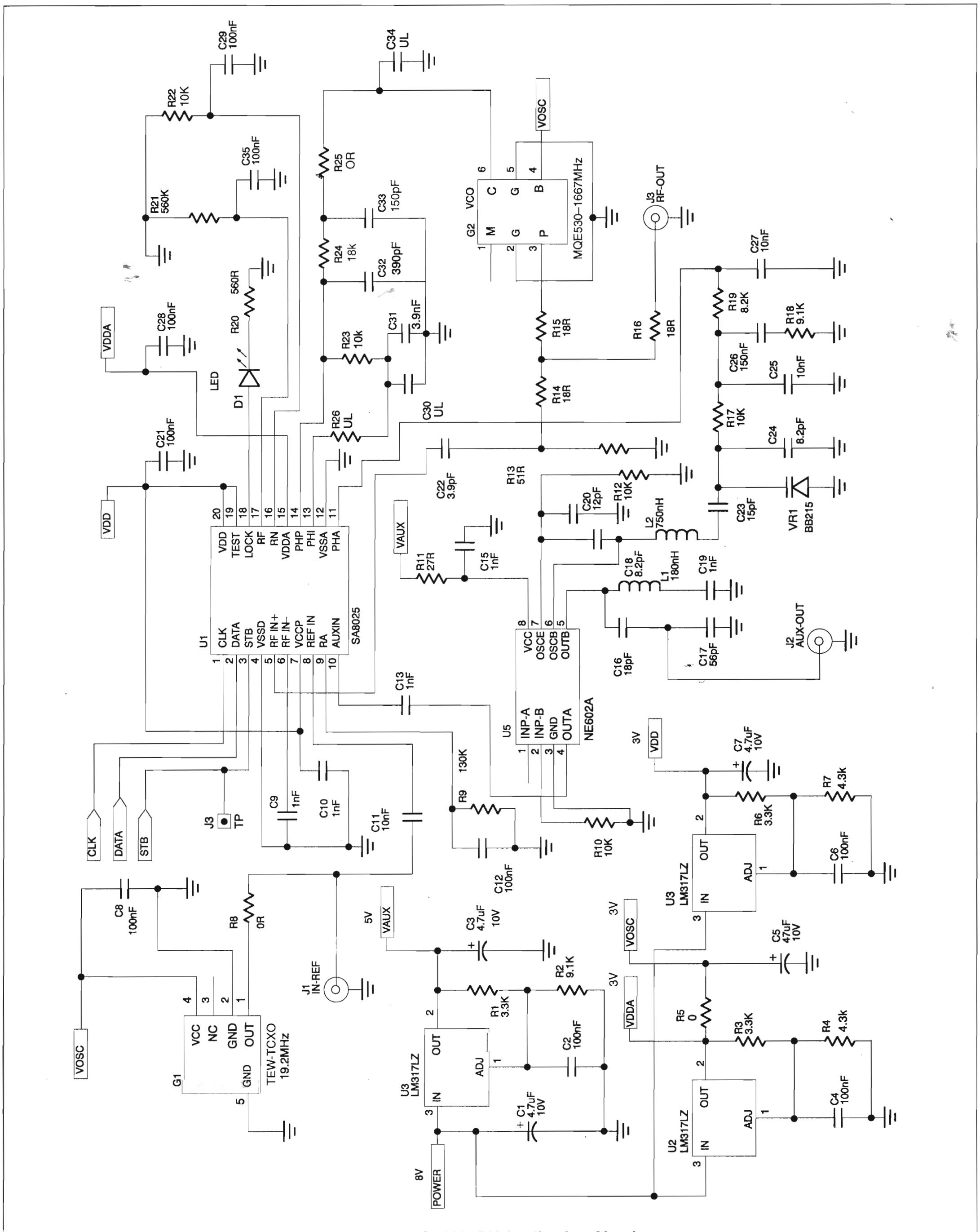


Figure 10. SA8025DK Application Circuit

SA8025 Fractional-N synthesizer for 2GHz band applications AN1891

Author: Wing S. Djen

INTRODUCTION

The SA8025 is a 3V, 1.8GHz, SSOP 20-pin packaged fractional-N phase locked-loop (PLL) frequency synthesizer. It is targeted for systems like the Japan Personal Handy Phone System (PHS, formerly PHP) which demands fast switching time and good noise performance. Built on the QUBiC BiCMOS process, it has phase detectors with maximum frequency of 5MHz and an auxiliary synthesizer that can operate up to 150MHz. This design was based on the UMA1005 (all CMOS), an earlier version fractional-N synthesizer which requires an external prescaler for 1 and 2GHz applications. There is also a 1GHz version fractional-N PLL frequency synthesizer, the SA7025, available for systems operating under 1GHz. One should expect the performance of the SA8025 and SA7025 to be comparable to the UMA1005 with an extra prescaler. This application note will serve as a supplement to the application note for the UMA1005 (Report No: SCO/AN92002) or as a stand-alone document specifically for the SA8025.

OVERVIEW OF THE FRACTIONAL-N FREQUENCY SYNTHESIZER

Figure 1 shows the basic building blocks of a PLL frequency synthesizer. It consists of a programmable reference divider, phase detector and programmable RF divider (prescaler and main divider). The low-pass filter and voltage-controlled oscillator (VCO) are external to provide design flexibility. The loop has a self-correction mechanism which forces comparison frequency $f_{COMP} = f_{COMP'}$. Since $f_{COMP} = f_{REF}/M$ and $f_{COMP}' = f_{VCO}/N$, the desired frequency becomes $f_{VCO} = (f_{REF}/M)N$. M (reference divider) is fixed for generating f_{COMP}. By incrementing or decrementing the value of N, different frequencies can be synthesized.

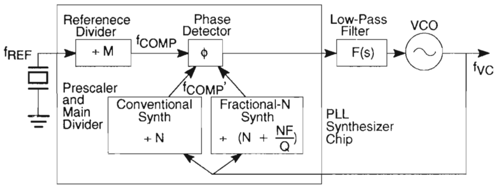


Figure 1. PLL Synthesizer

For conventional synthesizers, the phase detector comparison frequency must be equal to the channel spacing (frequency resolution) because the main divider (N) can only increment and decrement in integer steps. However, the main divider of the fractional-N synthesizer is capable of generating steps to be a fraction of the comparison frequency. Now the total divider ratio consists of an integer part (N) and a fractional part (NF/Q). The numerator (NF) and the denominator (Q, either 5 or 8) of a fraction are controlled through software programming.

Referring to Figure 2, to synthesize channels 1680MHz, 1680.3MHz and 1680.6MHz with channel spacing of 300kHz, the values have to be 5600MHz, 5601MHz and 5602MHz, respectively. The channel spacing of a fractional-N synthesizer is a fraction of the comparison frequency. When using the SA8025, the comparison frequency is increased to either 1.5MHz (mod 5) or 2.4MHz (mod 8), yielding a smaller N value of 1120 (mod 5) or 700 (mod 8) to synthesize 1680MHz.

To synthesize 1680, 1680.3, 1680.6MHz with channel spacing = 300kHz

Conventional syn. $f_{VCO} = f_{COMP}$ (N)	SA8025 (mod 5) $f_{VCO} = f_{COMP}$ (N + NF/5)	SA8025 (mod 8) $f_{VCO} = f_{COMP}$ (N + NF/8)
1680 = 0.3 (5600)	1680 = 1.5 (1120 + 0/5)	1680 = 2.4 (700 + 0/8)
1680.3 = 0.3 (5601)	1680.3 = 1.5 (1120 + 1/5)	1680.3 = 2.4 (700 + 1/8)
1680.6 = 0.3 (5602)	1680.6 = 1.5 (1120 + 2/5)	1680.6 = 2.4 (700 + 2/8)
f_{COMP} $= f_{CH}$ = 0.3MHz	f_{COMP} $= 5 \times f_{CH}$ = 1.5MHz	f_{COMP} $= 8 \times f_{CH}$ = 2.4MHz

Figure 2. What Is Fractional-N?

The advantage of fractional-N synthesizers is two-fold. Since the close-in noise floor is directly related to total divide ratio (N), reducing N five or eight times theoretically implies a close-in noise floor improvement of 14dB (20log(5)) or 18dB (20log(8)), respectively. At the same time, the comparison breakthrough will be 5 or 8 times further away than it would be if a conventional synthesizer were used. This allows a wider loop filter to be used, thus achieving a faster switching time. Faster switching is also achieved due to the higher number of comparison cycles.

DESIGNING WITH THE SA8025

Reference Signal and Divider

Since the synthesized signal is derived from the reference signal, using a clean crystal with an appropriate level is crucial. The reference signal should be AC coupled and deliver between 300 and $600mV_{P-P}$ to Pin 8 for the input buffer to convert it into a CMOS compatible level. The maximum crystal frequency the part can handle is determined by both analog and digital supplies because the input buffer and the reference divider are powered by V_{DDA} and V_{DD}, respectively. For a $V_{DD} = V_{DDA} = 3V$ configuration, the maximum crystal frequency allowed is 20MHz. When $V_{DD} = 3V$ and $V_{DDA} = 5V$, this frequency becomes 30MHz.

Phase Detector and Charge Pumps

The main and auxiliary phase detectors (see Figure 3) detect both the phase and frequency difference between the divided-down VCO and reference signals. If the main/aux leads the reference, there will be a pulse coming out of the phase detector which turns on the N-type charge pump and sinks current from the low-pass filter. On the other hand, if the main/aux lags the reference, the P-type charge pump will be activated and more current will be delivered to the low-pass filter.

Due to the internal delays of CMOS devices, the phase comparator needs a minimum phase difference, backlash time, to generate an output pulse. This backlash time will introduce a dead-zone around zero phase difference where a small phase error cannot be detected. The way the SA8025 eliminates this problem is by having a minimum on-time of $1/f_{REF}$ for the P pump (sourcing) and N pump (sinking) when the loop is in lock condition, which is shown in Figure 4. Since the charge pump on-time is determined by the crystal reference frequency (f_{REF}), the higher the frequency, the better will be the close-in noise performance. Typically, there will be 3dB close-in noise improvement for a 50% increase in reference frequency (e.g., from 9.6 to 14.4MHz).

Since the phase detector detects phase from -2π to 2π, its gain (K_{ϕ}) equals the charge pump output current (I_{CP}) divided by 2π with units of A/rad.

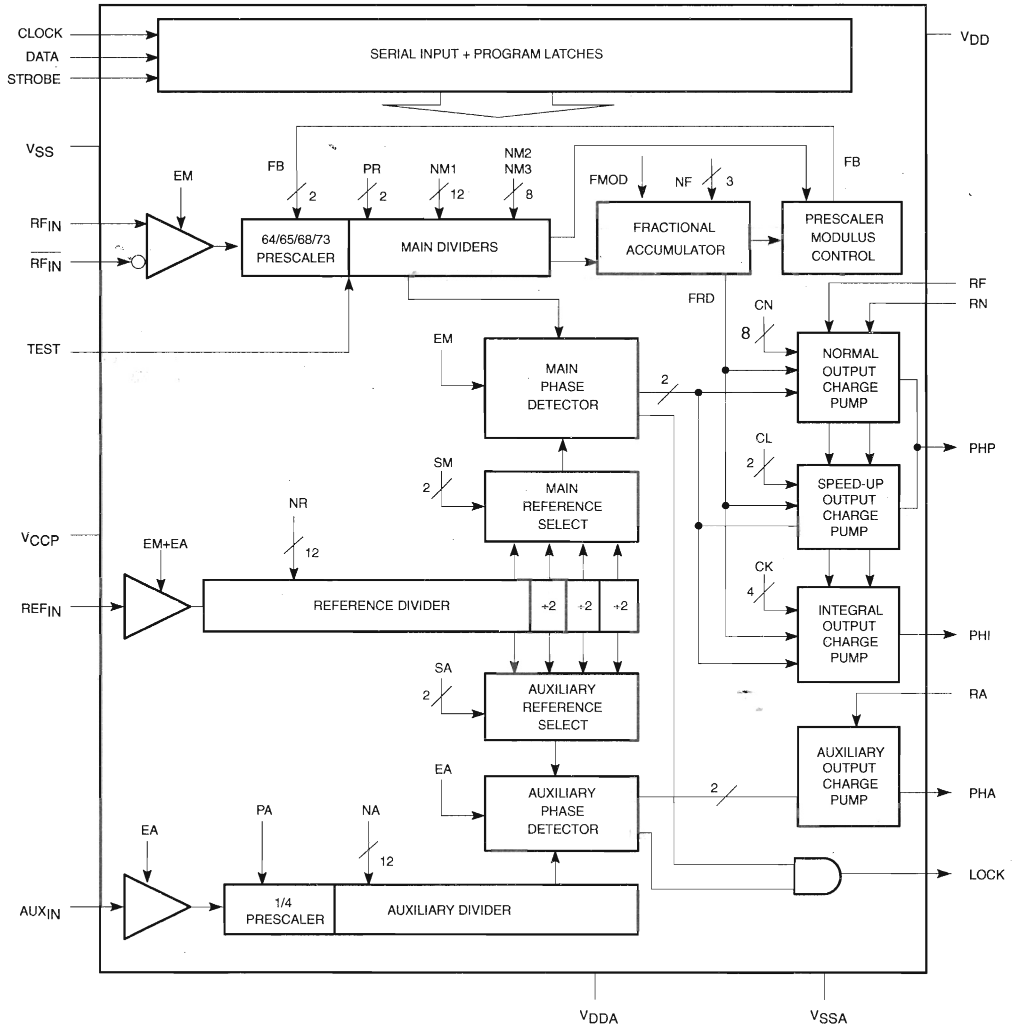


Figure 3. Block Diagram of the SA8025

The charge pump output current, I_{CP} (A), is determined by the external resistor RN and the internal registers CN, CK and CL values. The I_{CP} for normal mode operation (PHP pump only) is:

$$I_{CP} = \frac{CN \cdot I_{RN}}{32} \qquad \text{(EQ. 1)}$$

where $$RN = \frac{V_{DDA} - 0.9 - 150(I_{RN})^{0.5}}{I_{RN}} \qquad \text{(EQ. 2)}$$

Figure 5 shows a graphical representation of Eq. 2. The curves are valid for both main and aux synthesizers. Notice that in normal mode, currents due to the CK and CL values are negligible and only the PHP pump is activated. When the part is in speed-up, both charge pumps are on and the I_{CP} for PHP is:

$$I_{CP} = \frac{CN \cdot I_{RN}}{32}\left(2^{CL+1} + 1\right) \qquad \text{(EQ. 3)}$$

I_{CP} for PHI is:

$$I_{CP} = \frac{CN \cdot I_{RN}}{32}\left(2^{CL+1}\right) CK \qquad \text{(EQ. 4)}$$

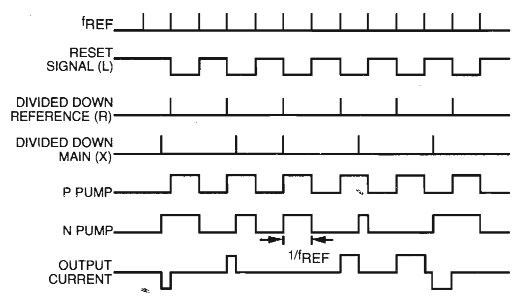


Figure 4. Phase Detector Timing Diagram

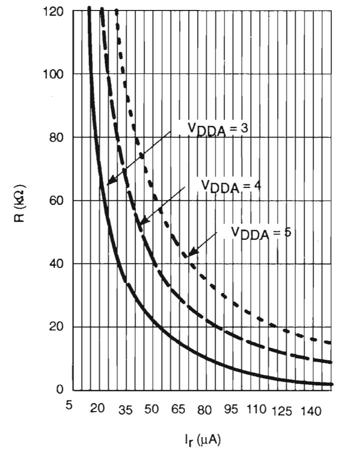


Figure 5. RN(RA) vs. $I_{RN}(I_{RA})$ for Different V_{DDA}

From Eq. 3 notice that in speed-up mode, the PHP output current will be at least 3 times higher than the normal mode current even though CL=0. Speed-up mode stays active as long as the STROBE signal is high after an A word is sent.

Bypass capacitors (100nF) should be used for RN, RF and RA pins to prevent high frequency noise being coupled into the pins causing modulation of the VCO.

Main Divider

The total divide ratio, N, is determined by the combination of the main divider ratio (NM1, NM2, NM3, NM4) and the prescaler values. The part is internally controlled to produce division ratios of N or N+1 when a fractional function is used. The minimum divide ratio, N', which guarantees that all the channels above this ratio can be synthesized consecutively (no blind channels) is different for each prescaler ratio. Since the fractional-N synthesizer increases the comparison frequency, lower N values can be used. To accomplish this, the SA8025 uses a 4 modulus (64/65/68/73) prescaler that lowers the minimum divide ratio to 933.

When programming a total divide ratio (N) which has no components of NM3 or NM4, simply treat them as "don't cares". Using divide ratios below the minimum divide ratio (N') to synthesize channels is possible, but it requires trial and error. For instance, in the Japan Personal Handy Phone System (PHS), the VCO is running at 1646.7 to 1670.1MHz (248.45MHz first IF). Using a modulus 8 fraction with 300kHz channel spacing, the required N value is between 686 and 695, which is less than the N' of the 4 modulus prescaler. Calculation showed that only N = 695 is not obtainable using the 4 modulus prescaler, but it can be obtained using the 64/65/73 prescaler. The B word must be sent to change the prescaler ratio.

Table 1.

Prescaler Ratio	PR Bits	N'	Total Divide Ratio, N
64/65	01	4032	N = (NM1 + 2) × 64 + NM2 × 65
64/65/68	10	1348	N = (NM1 + 2) × 64 + NM2 × 65 + (NM3 + 1) × 68
64/65/68/73	11	933	N = (NM1 + 2) × 64 + NM2 × 65 + (NM3 + 1) × 68 + (NM4 + 1) × 73
64/65/73	00	1096	N = (NM1 + 2) × 64 + NM2 × 65 + (NM4 + 1) × 73

Determining the Programming Values for NM1, NM2, NM3 and NM4

For the 2-modulus prescaler (64/65), NM1 and NM2 can be determined by:

$$NM2 = 64 \cdot FRAC\left(\frac{N}{64}\right) \qquad (EQ. 5)$$

$$NM1 = INT\left(\frac{N}{64}\right) - NM2 - 2 \qquad (EQ. 6)$$

where FRAC (...) and INT (...) takes the fractional integer part of the argument.

For the 3-modulus prescaler, NM1, NM2 and NM3 (NM4 when PR = 00) can be determined by:

$$K1 = INT\left(\frac{N-R}{64}\right) - 3, \quad K2 = FRAC\left(\frac{N-R}{64}\right) \cdot 64 \qquad (EQ. 7)$$

$$NM3 = INT\left(\frac{K2}{R}\right) \qquad (EQ. 8)$$

$$NM2 = FRAC\left(\frac{K2}{R}\right) \cdot R \qquad (EQ. 9)$$

$$NM1 = K1 - NM2 - NM3 \qquad (EQ. 10)$$

where R = 4 for 64/65/68 prescaler, R = 9 for 64/65/73 prescaler.

For the 4-modulus prescaler (64/65/68/73), we first arbitrarily choose NM4 (smaller values are preferable) and then use the following formulas to calculate NM1, NM2 and NM3:

$$K1 = INT\left(\frac{N-13}{64}\right) - 4, \quad K2 = FRAC\left(\frac{N-13}{64}\right) \cdot 64 \qquad (EQ. 11)$$

$$NM3 = INT\left(\frac{K2 - 9 \cdot NM4}{4}\right) \qquad (EQ. 12)$$

$$NM2 = FRAC\left(\frac{K2 - 9 \cdot NM4}{4}\right) \cdot 4 \qquad (EQ. 13)$$

$$NM1 = K1 - NM2 - NM3 - NM4 \qquad (EQ. 14)$$

Notice that the formulas shown above will give only one set of NM1, NM2, NM3 and NM4 that generates the desired N value. Generating continuous N below 933 (4 modulus) is still possible if all four modulus options are used. It was found that the part can generate N continuously from 702. The program "8025NMIN.EXE", provided with the "UMAWINE.EXE" for controlling the SA8025 demoboard, calculates all the N values that the part can generate. Users should run the program to find out the right NM1, NM2, NM3 and NM4 if N value of less than 702 is needed. This program will give only one possible combination of NM1 to NM4 for each N.

```
      program sa8025
     ┌──────────────────────────────────────────────────────┐
      Philips Semiconductors, Sunnyvale, CA
      Author: Wing S. Djen
      Date: 5/9/94
      Purpose: To find the minimum divide ratio on the SA8025
     └──────────────────────────────────────────────────────┘
      integer i, n1, n2, n3, n4, mod2, mod3a, mod3b, mod4,
      +            delta1, delta2, delta3, delta4,
      +            temp2, temp3a, temp3b, temp4
      +            lown, highn

      write(*,*) 'Enter the lowest N value→'
      read(*,*) lown
      write(*,*) 'Enter the highest N value→'
      read(*,*) highn
      do 10 i=lown, highn
      do 10 n1=0,10
      do 10 n2=0,10
      do 10 n3=0,10
      do 10 n4=0,10
         mod2 = (n1+2)*64 + n2*65
         mod3a = (n1+2)*64 + n2*65 + (n3+1)*68
         mod3b = (n1+2)*64 + n2*65 + (n4+1)*73
         mod4 = (n1+2)*64 + n2*65 + (n3 + 1)*68 + (n4+1)*73
        delta1 = i-mod2
        delta2 = i-mod3a
        delta3 = i-mod3b
        delta4 = i-mod4
        if (delta1.eq.0) then
          if (temp2.eq.mod2) goto 1
          write(*,5) mod2, n1, n2
 5        format(' PR="01"  N=',i5,3x,'NM1',i2,3x,
      +              'NM2=',i2)
          temp2=mod2
          endif
 1        if (delta2.eq.0) then
          if (temp3a.eq.mod3a) goto 2
          write(*,6) mod3a, n1, n2, n3
 6        format(' PR="10"  N=',i5,3x,'NM1',i2,3x,
      +              'NM2=',i2,3x,'NM3=',i2)
          temp3a=mod3a
          endif
 2        if (delta3.eq.0) then
          if (temp3b.eq.mod3b) goto 3
          write(*,7) mod3b, n1, n2, n4
 7        format(' PR="00"  N=',i5,3x,'NM1',i2,3x,
      +              'NM2=',i2,3x,'NM4=',i2)
          temp3b=mod3b
          endif
 3        if (delta4.eq.0) then
          if (temp4.eq.mod4) goto 10
          write(*,8) mod4, n1, n2, n3, n4
 8        format(' PR="11"  N=',i5,3x,'NM1',i2,3x,
      +              'NM2=',i2,3x,'NM3=',i2,3x,'NM4=',i2)
          temp4=mod4
          endif
 10       continue
          end
```

The following is a sample output of the "8025NMIN.EXE" program. It shows the divide ratios that cover the PHS band.

```
PR="01"   N=128   NM1=0   NM2=0
PR="01"   N=192   NM1=1   NM2=0
PR="01"   N=193   NM1=0   NM2=1
   :        :       :       :
   :        :       :       :
PR="11"   N=679   NM1=0   NM2=1   NM3=4   NM4=1
PR="00"   N=679   NM1=1   NM2=3   NM4=3
PR="00"   N=680   NM1=0   NM2=4   NM4=3
PR="11"   N=680   NM1=1   NM2=1   NM3=2   NM4=2
PR="11"   N=681   NM1=0   NM2=2   NM3=2   NM4=2
PR="11"   N=682   NM1=0   NM2=0   NM3=5   NM4=1
PR="11"   N=683   NM1=0   NM2=3   NM3=0   NM4=3
PR="11"   N=684   NM1=0   NM2=1   NM3=3   NM4=2
PR="11"   N=685   NM1=1   NM2=1   NM3=1   NM4=3
PR="00"   N=685   NM1=3   NM2=0   NM4=4
PR="11"   N=686   NM1=0   NM2=2   NM3=1   NM4=3
PR="00"   N=686   NM1=2   NM2=1   NM4=4
PR="11"   N=687   NM1=0   NM2=0   NM3=4   NM4=2
PR="00"   N=687   NM1=1   NM2=2   NM4=4
PR="00"   N=688   NM1=0   NM2=3   NM4=4
PR="11"   N=688   NM1=1   NM2=0   NM3=2   NM4=3
PR="11"   N=689   NM1=0   NM2=1   NM3=2   NM4=3
PR="11"   N=690   NM1=1   NM2=1   NM3=0   NM4=4
PR="11"   N=691   NM1=0   NM2=2   NM3=0   NM4=4
PR="11"   N=692   NM1=0   NM2=0   NM3=3   NM4=3
PR="11"   N=693   NM1=1   NM2=0   NM3=1   NM4=4
PR="11"   N=694   NM1=0   NM2=1   NM3=1   NM4=4
PR="00"   N=694   NM1=2   NM2=0   NM4=5
PR="00"   N=695   NM1=1   NM2=1   NM4=5
PR="00"   N=696   NM1=0   NM2=2   NM4=5
PR="11"   N=697   NM1=0   NM2=0   NM3=2   NM4=4
PR="11"   N=698   NM1=1   NM2=0   NM3=0   NM4=5
PR="11"   N=699   NM1=0   NM2=1   NM3=0   NM4=5
PR="11"   N=702   NM1=0   NM2=0   NM3=1   NM4=5
```

RF Inputs

The RF inputs were designed to be used differentially for better noise rejection. However, the part can also be driven single-endedly with $RF_{IN}+$ or $RF_{IN}-$ pin terminated by a 1nF capacitor. The matching network between VCO and RF input was intended for matching both the VCO and the Main Out on the demoboard to 50Ω (see Figure 6).

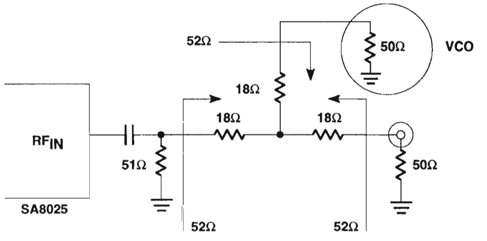


Figure 6. Matching Network for the RF_{IN} Pin

Lock Detect

The LOCK pin is selectable by software to be either the lock detect indicator, output of the main divider, output of the reference divider, or output of the auxiliary divider. Programming details can be found in the data sheet. The pin voltage will go to V_{DD} once the lock condition has been satisfied. Upon power up, the part is in an unknown state and the LOCK pin may go high. It will be functional only after the part is programmed.

Auxiliary Synthesizer

The auxiliary synthesizer does not have fractional-N capability. Therefore, its close-in phase noise and comparison breakthrough performance is comparable to that of a conventional synthesizer. However, this type of performance is not necessary for creating an offset frequency for a Frequency Division Duplex (FDD) system or the 2nd LO in a dual-conversion receiver. Also, an FM signal (e.g., GFSK or analog FM) can be obtained by directly frequency modulating the auxiliary VCO in a PLL structure. The auxiliary phase detector has the same bandwidth (5MHz) as the main phase detector. Current setting for the charge pump (I_{RA}) can be calculated using Eq. 2 and Figure 5. The charge pump output current (I_{CP}) becomes

$$I_{CP} = 8 \cdot I_{RA} \qquad \text{(EQ. 15)}$$

Fractional Spurs and Compensation

The total divide ratio of the SA8025 is constantly changing between N and N + 1 to achieve fractional-N capability. This effect introduces an instantaneous phase error at the output of the phase detector in lock condition, which will cause the VCO to generate unwanted spurs at the fractions ($f_{VCO} \pm NF/Q$) of the comparison frequency (f_{COMP}). The SA8025 has internal circuitry which generates appropriate amounts of current to compensate for the phase error for different NF.

Due to the difference in processing technology, fractional compensation current on the SA8025 will not follow the UMA1005. Experimental results show that the resistor RF has to be between 200 and 600 kΩ for optimum fractional spur suppression. It is recommended to adjust the CN value for the high, the middle and the low channel to minimize the fractional spurs. Then linear interpolation technique can be applied to calculate all the CN values for the rest of the channels. A long "A" word (A1) needs to be sent to change the channel and set the CN value at the same time.

PCB Layout

Since careful PCB layout has a great impact on the performance of the synthesizer, users should pay special attention to the rules in building RF circuits. Here are some tips for the synthesizer board layout:

- Follow the layout in this document or on the demoboard.
- It is important that VCO ground is large in size and coupled immediately to the grounded side of the PCB. Make sure that there is a clean path for the VCO ground to get to the system ground (power supply ground).
- To avoid interference, the lead between the VCO output and the RF input should be kept as short as possible. A 50Ω termination resistor should be placed close to the RF input.
- Digital ground (V_{SS}) and analog ground (V_{SSA}) must be separated on the component side of the board. They have to be large in size on the PCB and coupled immediately to the grounded side of the PCB. Designers should refer to the latter part of this application note for the recommended PCB layout.
- Power supply bypass capacitors (100nF) for all devices should be located close to the devices with short leads.
- V_{SSA} should be separated from the ground of other devices such as VCO and mixer chip (NE602).

LOOP FILTER DESIGN

This section presents the procedure for designing the loop filter. Due to the sampling nature of the phase detector and the delay introduced in frequency dividers, complicated mathematical analysis is required for deriving the loop design formulas. However, to give designers a convenient tool for quick design, a simple design procedure based on linear control theory is given below. The detailed derivation is included in the Appendix.

Figure 7a shows a simple 1 pole + 1 zero passive low-pass filter which is commonly used with the PLL synthesizer whose phase detector output is current. This filter has a pole at 0Hz and a zero at ($1/2\pi\ R_1\ C_1$)Hz. Together with the pole introduced by the VCO, this filter will give a 2nd order type 2 (2 poles at 0Hz) PLL loop, which our design procedure is based upon. The inclusion of C_2, R_2 and C_3 (see Figure 7b) effectively introduces two more poles located far away from the zero. This will provide more attenuation, if necessary, on the spurious sidebands without affecting the 2nd order nature of the loop.

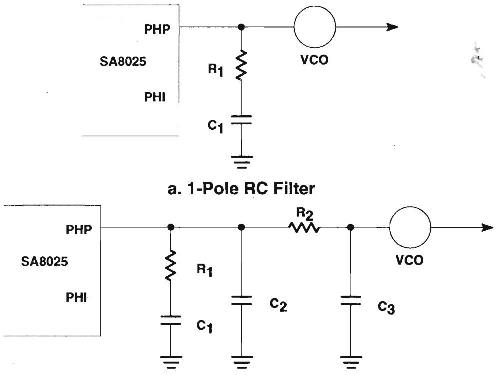


Figure 7. RC Filter Configurations

Definition of the PLL parameters:

δ: final frequency resolution after settling

$$\delta = \frac{\text{frequency error after settling}}{\text{switching step}} \qquad \text{(EQ. 16)}$$

t_{SW}: switching time (sec)

f_N: natural frequency of the 2nd order system (Hz), $\omega_N = 2\pi f_N$ (rad/s)

N: total divide ratio

ξ: damping factor of the second order system. Typ. value is 0.707

K_{VCO}: VCO gain (Hz/V) or 2π × VCO gain (rad/V)

K_ϕ: phase detector gain = $I_{CP}/2\pi$ (A/rad)

Normal Mode Design

The set of formulas (see Appendix) presented here is valid for normal mode operation in which only charge pump PHP is connected to the low-pass filter. This assumes the STROBE length is short enough so that speed-up due to STROBE high is minimum in the switching process. Designers should use the normal mode design approach as a starting point and go on to the adaptive mode design if desired PLL performance cannot be met using this configuration.

$$\omega_N = \frac{-\ln(\delta \cdot \xi)}{\xi \cdot t_{SW}} \qquad \text{(EQ. 17)}$$

$$C_1 = \frac{K_\phi \cdot K_{VCO}}{N\ \omega_N^{\,2}} \qquad \text{(EQ. 18)}$$

$$R_1 = 2 \cdot \xi \left(\frac{N}{K_\phi \cdot K_{VCO} \cdot C_1}\right)^{0.5} \qquad \text{(EQ. 19)}$$

$$C_2 \le \frac{C_1}{10} \qquad \text{(EQ. 20)}$$

$$\omega = \frac{1}{C_3 \cdot R_2} \quad \omega \text{ should be at least 10 times larger than } \omega_n \qquad \text{(EQ. 21)}$$

NOTE: The unit of the factor $K_\phi \times K_{VCO}$ is unity when all the variables are expressed in radians. Therefore, designers can simply multiply the charge pump output current (I_{CP}) with the VCO gain in Hz/V to obtain this factor.

Adaptive Mode Design

The adaptive mode allows designers to take advantage of having one filter with two different loop filter responses. When the synthesizer is switching from channel to channel, a wider filter bandwidth (speed-up) is desired. Once the loop is locked at the correct frequency, a narrower filter is required to achieve lower noise. This mode can be realized by connecting the PHI charge pump to the integrating capacitor C1 (see Figure 8), controlling the width of the STROBE (amount of time for speed-up), and programming the CK and CL registers. Due to this configuration, the zero of the filter gets multiplied by $[2^{CL+1}(CK + 1) + 1] / [1 + 2^{CL+1}]$ times, which makes the loop more stable in speed-up mode. One drawback of this design is that switching from speed-up to normal current will cause a difference in the final phase error due to different current gain, which results in frequency instability or a "glitch" in the frequency domain. Because of this effect, the actual switching time will be longer than what the speed-up loop is designed for, since the loop has to re-settle again due to the glitch. Experimental trial of the width of the STROBE can help alleviate this problem.

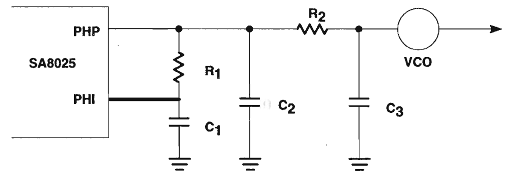


Figure 8. Adaptive Filter

Definition:

ξ_S: speed-up mode damping ratio

ξ_N: normal mode damping ratio

ω_{NS}: speed-up mode natural frequency

ω_{NN}: normal mode natural frequency

Design Steps:

1. Calculate ω_{NS} to meet the system switching time requirement using Eq. 17.
2. Decide how many times ω_{NN} is smaller than ω_{NS}. 5 times will be a good number.
3. Calculate filter component values using Eq. 17 to Eq. 20.
4. Calculate CL and CK values according to

$$CL = 3.32 \log_{10}\left(\frac{\xi_s \cdot \omega_{NS}}{\xi_N \cdot \omega_{NN}} - 1\right) - 1 \qquad \text{(EQ. 22)}$$

$$CK = \left[\frac{\left(\frac{\omega_{NS}}{\omega_{NN}}\right)^2 - 1}{\left(\frac{\xi_S \cdot \omega_{NS}}{\xi_N \cdot \omega_{NN}} - 1\right)}\right] - 1 \qquad \text{(EQ. 23)}$$

The above procedure ensures the loop bandwidth in speed-up mode is 5 times greater than that in normal mode while maintaining the required stability of the loop.

DESIGN EXAMPLE

This section shows a design example using the SA8025 for the Personal Handy Phone System (PHS), where the device is used in the normal mode (only PHP charge pump is active). The system parameters are as follows:

VCO frequency (f_{VCO}) = 1646.7 to 1670.1MHz

Channel spacing (f_{CH}) = 300kHz

Comparison frequency (f_{COMP}) = 8 × 300kHz = 2.4MHz

Switching time (t_{SW}) = 500µs

Switching step = 25MHz

Frequency error = within 1kHz

VCO gain (K_{VCO}) = 15MHz/V

Reference Crystal (f_{REF}) = 19.2MHz

Determine total divide ratio N

To synthesize channels from 1646 to 1670MHz with f_{COMP} = 2.4MHz, N should be between 686 and 695. For the same loop components, larger N yields smaller natural frequency (f_N). So, jumping from high-end to low-end (larger N) is slower than from low-end to high-end (smaller N). To ensure the same switching time from either direction, we use N = 695 for the worst case.

Determine ω_N

Using Eq. 16

$$\delta = \frac{1000}{25e6} = 0.04e\text{-}3$$

Pick ξ = 0.707 and use t_{SW} = 400µs for safety.
Using Eq. 17

$$\omega_N = \frac{-\ln\,(0.04e\text{-}3 \cdot 0.707)}{0.707 \cdot 400e\text{-}6} = 37{,}035$$

Determine R_N and I_{CP}

Pick RN = 10kΩ and CN = 100. Referring to Figure 5, I_{RN} becomes 80µA when V_{DDA} = 3V.
Using Eq. 1

$$I_{CP} = 100\left(\frac{80e\text{-}6}{32}\right) = 250\mu A$$

Determine R_1, C_1 and C_2

Using Eq. 18 with 2π's from K_{VCO} (rad/V) and K_ϕ (A/rad) cancel out

$$C_1 = 15e6\left(\frac{250e\text{-}6}{695 \cdot 37{,}035^2}\right) = 3.93nF$$

Using Eq. 19

$$R_1 = 2 \cdot 0.707 \cdot \left(\frac{695}{15e6 \cdot 250e\text{-}6 \cdot 3.9e\text{-}9}\right)^{0.5} = 9.7k\Omega$$

Using Eq. 20

$$C_2 = \frac{3.93e\text{-}9}{10} = 390pF$$

Determine R_2 and C_3

R_2 and C_3 can help attenuate the unwanted fractional spurs at 300kHz offset.

Using Eq. 21

$$\omega = \frac{1}{R_2 \cdot C_3} \geq 10\omega_N$$

Pick R_2 = 18kΩ, then C_3 = 150pF.

Fractional spurs compensation, if necessary

With f_{COMP} = 300kHz, there would be some spurs located at 300kHz or multiples of 300kHz when NF not equal to 0. For this particular design, we are able to use a fixed CN value (100) to achieve spurs suppression of at least -64dBc for spurs located at 300kHz carrier offset. Spurs located at other frequencies are not present.

Design results

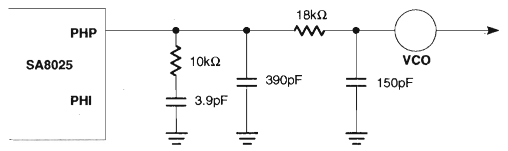


Figure 9. Main Loop Filter

Component values used on the demoboard:
C31 = 3.9pF
R23 = 10kΩ
C32 = 390pF
R24 = 18kΩ
C33 = 150pF
R21 = 560kΩ (RF)
R22 = 10kΩ (RN)

Software setting:
CN = 100
STROBE = 190µs

MEASUREMENT RESULTS

The major performance parameters for a PLL synthesizer are close-in phase noise, spurious sidebands and switching time. This section presents the measurement results obtained from the design made in the section on LOOP FILTER DESIGN.

Close-In Phase Noise

The close-in phase noise level directly correlates with the residual FM and integrated jitter performance, two integrated noise parameters. It is measured within the loop bandwidth (the peak of the "hump" around the carrier) at a specified carrier frequency offset, e.g., 1kHz, and it is expressed in -dBc/Hz. Figure 10 displays the result of such a measurement. The carrier is located at 1668.3MHz (NF = 1) and the span is 10kHz. The resolution bandwidth (measurement bandwidth) is 100Hz. Therefore, the close-in phase noise at 1kHz offset is:

$$= -58.2\text{dBc} - 10 \log (100)$$

$$= -78.2\text{dBc/Hz}$$

Spurious Performance

Figures 11 and 14 show the spurious performance of the highest and the lowest bands of interest with NF = 1 and 7, which are the worst case for fractional spurs. Other spurs within the band are totally compensated.

Switching Time

The switching time (see Figures 15 and 16) was measured using the HP 53310A Modulation Domain Analyzer (MDA) with option 031. Under the TRIGGER Menu of the MDA, "Triggered", "Ext Edge" and "Arm Only" were selected. The instrument was setup to accept an external trigger, which was the STROBE signal used for programming the synthesizer. This signal was connected to the Ext Arm input while the VCO signal was fed into the Channel C. The MDA would display the frequency versus time variation of the VCO signal upon the arrival of the STROBE signal. This design achieved a switching time of 400µs to within 1kHz of the final frequency for a 21.6MHz jump between 1646.7 and 1668.3MHz in either direction. The STROBE width used in this experiment was 190µs.

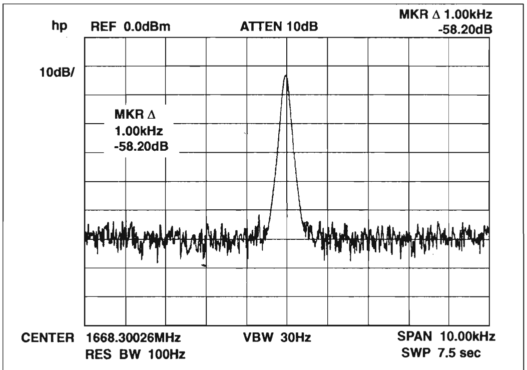


Figure 10. Close-In Phase Noise at 1668.3MHz

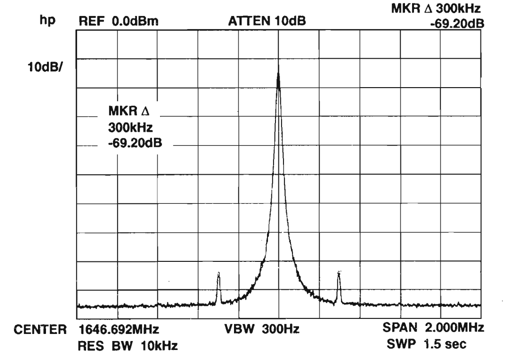


Figure 11. Fractional Spurs (f_{VCO} = 1646.7MHz, NF = 1)

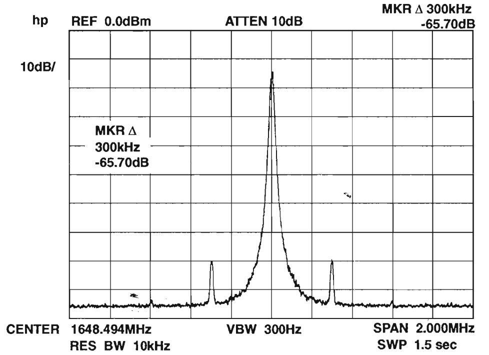


Figure 12. Fractional Spurs (f_{VCO} = 1648.5MHz, NF = 7)

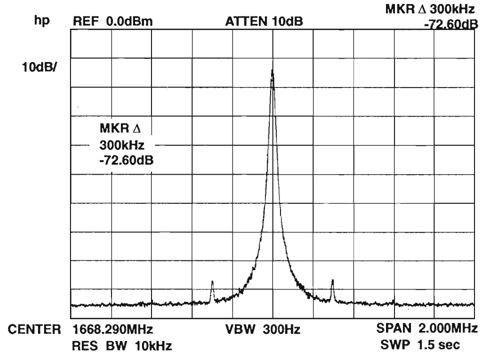


Figure 13. Fractional Spurs (f_{VCO} = 1668.3MHz, NF = 1)

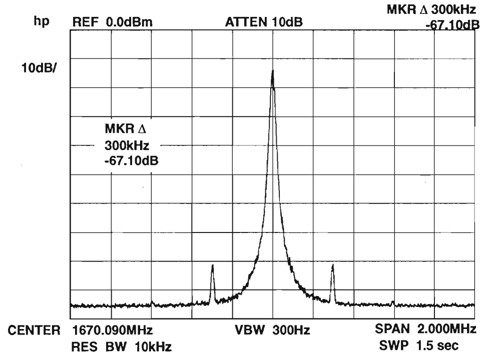


Figure 14. Fractional Spurs (f_{VCO} = 1670.1MHz, NF = 7)

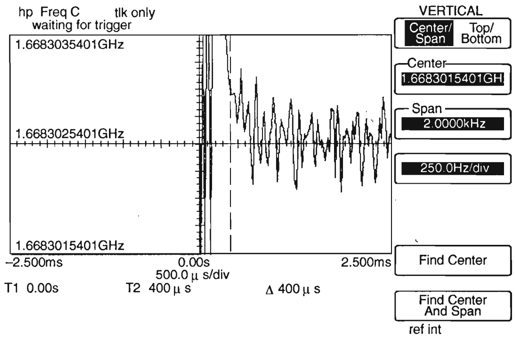


Figure 15. Switching Time (1668.3 to 1646.7MHz Step to Within 1kHz)

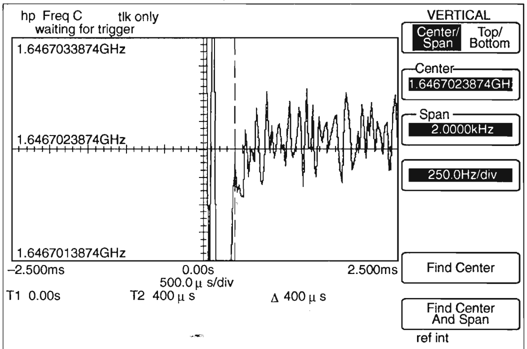


Figure 16. Switching Time (1646.7 to 1668.3MHz Step to Within 1kHz)

MODULO 4 DESIGN

Previous sections showed a design using a 4 modulus prescaler (64/65/68/73) to synthesize total divide ratios (N) from 686 to 694. This requires sending both B and A words since NM4 is stored in B word. In some designs, users may prefer to send only one word for channel switching due to hardware limitation. We could have used modulo 5 (FMOD = 5) to make N five times higher and used a triple modulus prescaler (64/65/68 or 64/65/73). In some situations this is impossible since the comparison frequency has to be an integer factor of the crystal reference. For instance, if f_{REF} is 19.2MHz and f_{CH} is 300kHz, f_{COMP} becomes 1.5MHz, which is not an integer factor of 19.2MHz. To get around this problem, a modulo 4 design must be used.

Figure 17 shows the concept of a modulo 4 design. In the mod 4 case, f_{COMP} is four times the channel spacing, f_{CH}. Instead of programming NF to one through seven, even numbers are used.

To synthesize 1656.3, 1656.6, 1656.9, 1657.2MHz with channel spacing = 300kHz using mod 8 and mod 4.

SA8025 (mod 8)	**SA8025 (mod 4)**
$f_{VCO} = f_{COMP}$ (N+NF/8)	$f_{VCO} = f_{COMP}$ (N+NF/8)
1656.3 = 2.4 (690 + 1/8)	1656.3 = 1.2 (1380 + 2/8)
1656.6 = 2.4 (690 + 2/8)	1656.6 = 1.2 (1380 + 4/8)
1656.9 = 2.4 (690 + 3/8)	1656.9 = 1.2 (1380 + 6/8)
1657.2 = 2.4 (690 + 4/8)	1657.2 = 1.2 (1381 + 0/8)
f_{COMP} $= 8 \times f_{CH}$ = 2.4MHz	f_{COMP} $= 4 \times f_{CH}$ = 1.2MHz

Figure 17.

To achieve the same loop response with the mod 8 design, the same loop filter with twice the charge pump current can be used. This can be derived from Eq. 18. When N is doubled, K_ϕ (two times more current) has to be doubled as well to maintain the same natural frequency which determines the switching time and residual FM. In this case, we use CN = 200 for the mod 4 design.

The only penalty of this method is that theoretical close-in phase noise performance is affected. Since N is twice as much, the close-in noise floor should be 20log(2) = 6dB higher. However, minor degradation for using mod 4 was measured in the laboratory. This could be due to the fact that the comparison cycles are fewer with mod 4, which makes the charge pump ON time less, thus producing less noise. In addition, higher charge pump current improves the phase noise.

MOD 4 DESIGN MEASUREMENT RESULTS

Figures 18 to 22 show the measurement results for the mod 4 design. The close-in phase noise level is shown to be -77.1dBc/Hz at 1kHz carrier offset with a measurement bandwidth of 100Hz. Spurious sidebands (see Figures 19 and 20), which are caused by fractional jitter, are -67dB down from carrier for the high band and -68dB down for the low band. Switching time (see Figures 21 and 22) is exactly the same as the mod 8 design (400μs) because the loop natural frequency is the same for both cases.

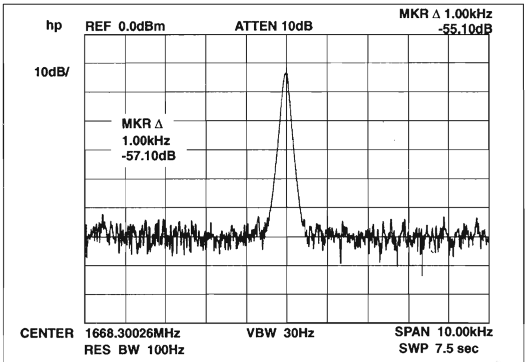


Figure 18. Close-In Phase Noise at 1668.3MHz

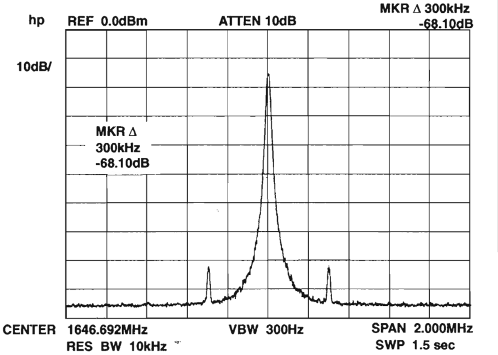


Figure 19. Fractional Spurs (f_{VCO} = 1646.7MHz, NF = 2)

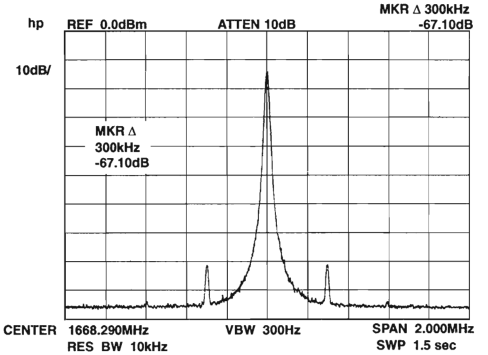


Figure 20. Fractional Spurs (f_{VCO} = 1668.3MHz, NF = 2)

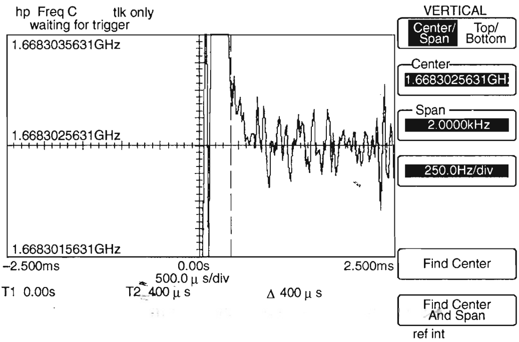


Figure 21. Switching Time (1668.3 to 1646.7MHz Step to Within 1kHz)

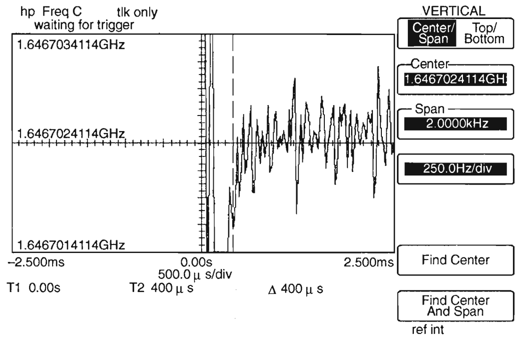


Figure 22. Switching Time (1646.7 to 1668.3MHz Step to Within 1kHz)

FREQUENTLY ASKED QUESTIONS

Q. The part is powered-up and programmed. The VCO is still free-running. What's wrong?

A. Three things to check for if the PLL does not lock:

1. Make sure the correct data have been transmitted to the CLK, DATA and STROBE pins
2. Make sure a reference signal with correct frequency and amplitude are present at the REF_{IN} pin.
3. Make sure that the prescaler value is chosen correctly. The SA8025 has two 3 modulus prescalers and uses different programming bits.
4. Be aware of cold solder joints. Pay special attention to the loop filter section and the connection from the VCO to the RF_{IN} pin.

Q. The synthesizer locks up, but it locks at a wrong frequency. Why?

A. Check the NM1, NM2, NM3 and NM4 bits. Make sure they are correctly programmed.

Q. I see spurs sitting at the comparison frequency offset and they don't change with the filter bandwidth. How can I get rid of them?

A. These spurs may be caused by improper grounding of the VCO and the filter section. Make sure they all have short and clean paths going back to the supply ground. Also, clean the filter section to avoid leakage.

Q. I see some spurs which are neither fractional nor comparison spurs. What are they?

A. Since the VCO is a very sensitive device, it can be influenced by many noise sources. Common ones are:

1. Computer monitor. The sweeping frequency of the screen will modulate the VCO and create spurious sidebands at 30 to 40kHz carrier offset.
2. Free-running auxiliary VCO. Even though the EA bit is disabled, if the auxiliary VCO is still ON, it will modulate the main VCO and cause spurs.
3. Fluorescent lamp.

Q. How can the residual FM be improved?

A. Three things can be done to improve residual FM:

1. Use a narrower loop filter.
2. Use a higher crystal reference frequency. This will reduce the charge pumps ON time and make the charge pumps generate less noise.
3. Use higher charge pump output current. This will increase the signal to noise ratio at the charge pump, which makes the circuit less noisy.

Q. When I FM modulate the AUX synthesizer, I see modulation on the MAIN carrier as well. Is that normal?

A. Yes, that is normal. The amount of interference between the AUX and the MAIN has to be verified experimentally.

Q. If I double the phase detector gain (twice the current), what should be done to keep the switching time the same?

A. Referring to Eq. 18 and Eq. 19, the value of C_1 should be doubled and R_1 should be halved if you want to maintain the same natural frequency of the loop when the detector gain (K_ϕ) is twice what it was before.

Q. When I use the 3 modulus prescaler (PR = 10), what should the values for NM4 be?

A. Simply treat them as "don't cares".

Q. What is the phase detector gain? Is it charge pump output current divided by 2π or just the charge pump output current, itself?

A. The phase detector gain (K_ϕ) is equal to the charge pump output current (I_{CP}) divided by 2π since the phase detector covers 2π range. However, when we use the design formulas shown in the "Loop Filter Design" section, K_ϕ can be replaced directly by I_{CP} because the 2π factor will be cancelled out by the 2π from the VCO gain, K_{VCO}.

Q. What should I do with the RA and PHA pins when the auxiliary synthesizer is not used?

A. When the auxiliary synthesizer is not used, leave PHA open, connect AUX_{IN} to ground, connect RA to V_{DDA} or leave it open and program EA bit to zero.

Q. Variations on the RF pins input impedance for different prescaler value can cause VCO pulling. Does that happen to the SA8025?

A. The RF input to the prescaler is well buffered, and the input impedance should always stay the same.

Q. Can the clock signal be disconnected after the A word is sent?
A. Yes, the clock signal can be disabled after the A word is sent and enabled again for sending new words to the part.

Q. Can I drive the part with a +5dBm RF signal even though the spec is 0dBm max?
A. Users should refer to the graphs put in the latter part of the data sheet for minimum and maximum input power. The device should be able to handle +5dBm at 1800MHz, but this is not guaranteed in the data sheet.

Q. I am doing open-loop modulation on the main synthesizer. How do I put the charge pump to high impedance state to allow modulation?
A. Program CN register to zero. This will set the charge pump to a high output impedance state so that FM modulation can be done.

Q. Is the demoboard layout good for any applications? If not, what should I do?
A. The demoboard layout included in this document was optimized only for this particular design. Designers should consult the PCB layout hints in the "PCB Layout" section of this application note when laying out circuit boards for other applications.

Q. I am using the S8025 for PHS system and seeing different amplitudes on the fractional spurs from part to part. However, this variation does not appear to affect my RX/TX performance. Is this a safe assumption?
A. Yes, because the SA8025 is targeted for the PHS system and any spurs that only fall in the adjacent channels (at 300kHz carrier offset) are acceptable for the PHS.

REFERENCES

"Digital PLL Frequency Synthesizers", Ulrich L. Rohde, Prentice Hall, 1983.

"Designer Guide to Frequency Synthesis Using the UMA1005", Application Note, Report No: SCO/AN92002.

"Modem Control Systems", Richard C. Dorf, Addison Wesley, 1989.

APPENDIX

Derivation of the 2nd order PLL design formula:

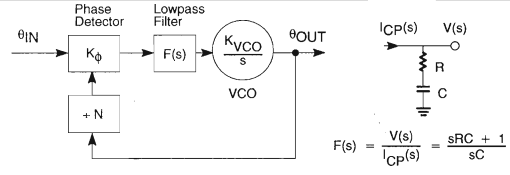


Figure 23. PLL Block Diagram

The transfer function of the loop low-pass filter is represented by:

$$F(s) = \frac{sRC + 1}{sC} \qquad \text{(EQ. 24)}$$

The low-pass filter has a pole at 0Hz (set denominator to zero) and a zero at $1/2\pi RC$ Hz (set numerator to 0).

Referring to Figure 23, the open-loop response of the system (multiplication of the Forward Gain and Feedback Gain) becomes:

$$G(s)H(s) = \frac{K_\phi \cdot K_{VCO}}{Ns}\left(\frac{sRC + 1}{sC}\right) \qquad \text{(EQ. 25)}$$

Phase Margin (ϕ_{PM}) is defined as the difference between -180° and the phase at the point where the open-loop response has unity gain. A stable system must have a ϕ_{PM} greater than 0°. Eq. 25 shows that there are two poles sitting at 0Hz, one from the filter and one from the VCO, which causes -180° phase shift. In order to have a stable system, a zero has to be added to the filter so that ϕ_{PM} will be greater than zero. ϕ_{PM} is related to the damping factor, ξ, with $\xi = 0.01 \times \phi_{PM}$.

To find the characteristic equation (CE) of the system, we equate 1 + G(s)H(s) to zero. Therefore,

$$1 + \frac{K_\phi \cdot K_{VCO}\,(sRC + 1)}{s^2NC} = 0 \qquad \text{(EQ. 26)}$$

The CE becomes

$$s^2 + \frac{K_\phi \cdot K_{VCO} \cdot R}{N}\,s + \frac{K_\phi \cdot K_{VCO}}{NC} \qquad \text{(EQ. 27)}$$

Compare Eq. 27 with the standard 2nd order CE ($s^2 + 2\zeta\omega_N s + \omega_N^2$), we have

$$\omega_N^{\,2} = \frac{K_\phi \cdot K_{VCO}}{NC} \quad \Rightarrow \quad C = \frac{K_\phi \cdot K_{VCO}}{N\,\omega_N^{\,2}} \qquad \text{(EQ. 28)}$$

$$2\xi\omega_N^{\,2} = \frac{K_\phi \cdot K_{VCO} \cdot R}{N} \Rightarrow R = 2 \cdot \xi\left(\frac{N}{K_\phi \cdot K_{VCO} \cdot C}\right)^{0.5} \qquad \text{(EQ. 29}$$

which are the design used in "Loop Filter Design" section.

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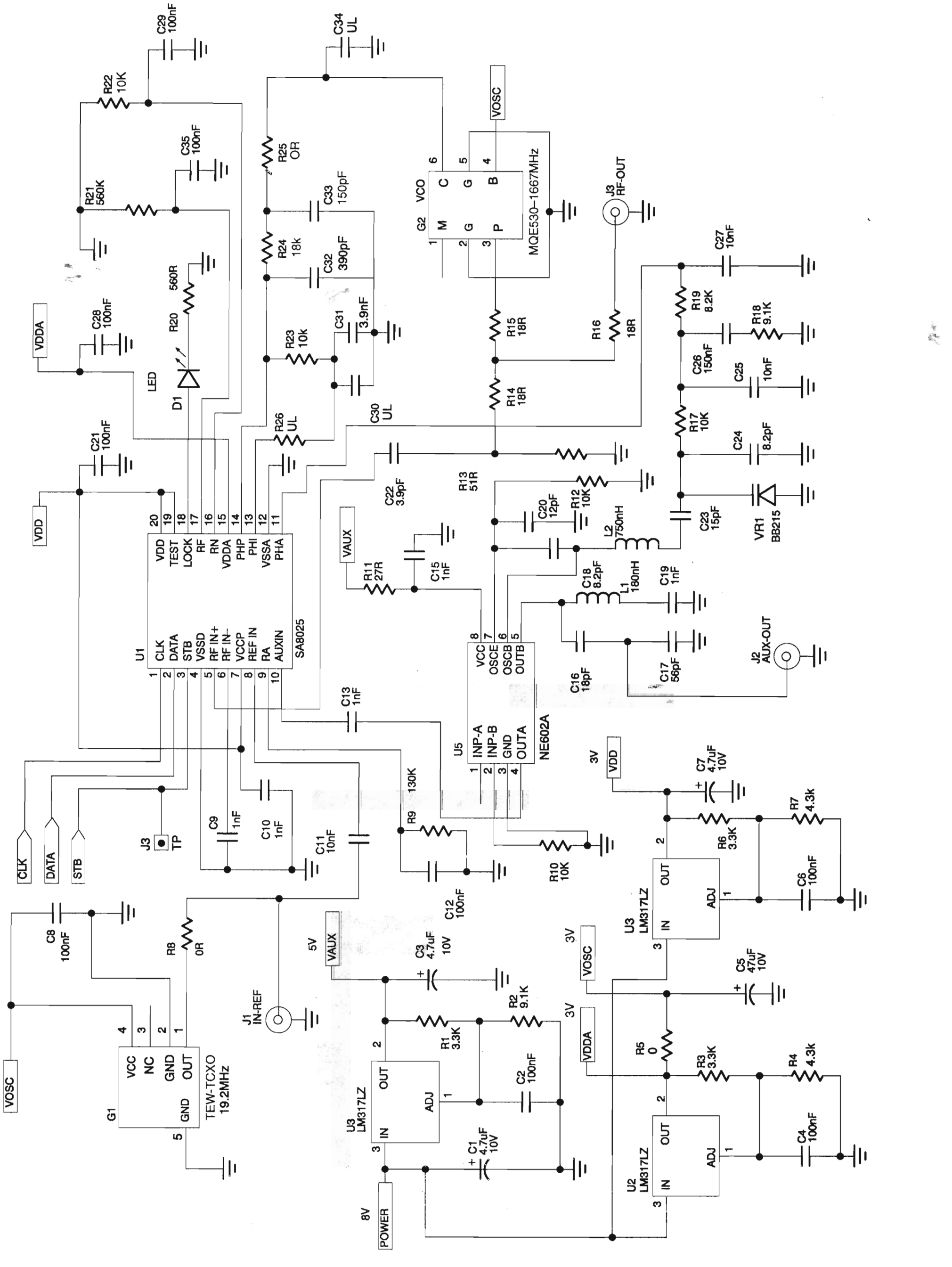
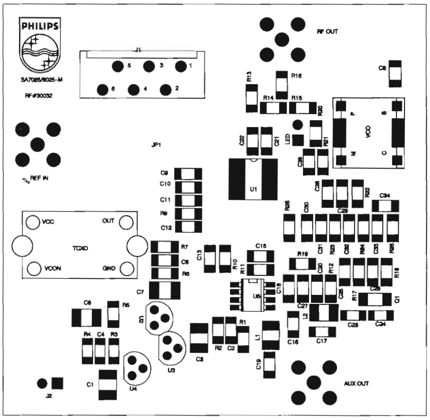
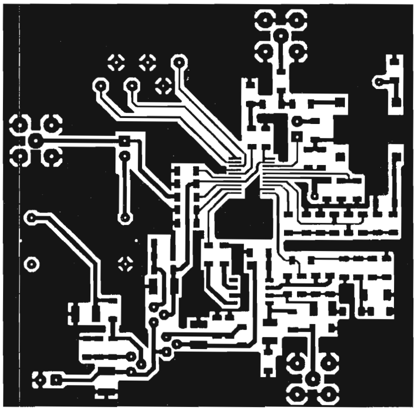


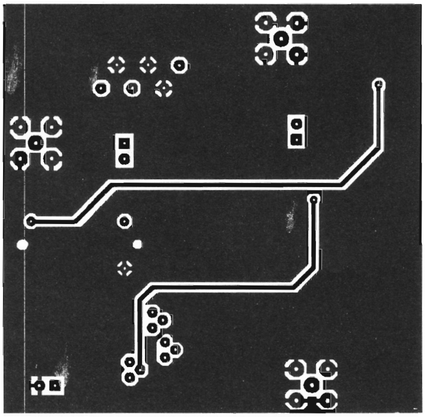
Figure 24. SA8025DK Application Circuit



TOP SILK SCREEN



TOP VIEW



BOTTOM VIEW

Figure 25. SA8025DK Demoboard Layout (NOT ACTUAL SIZE)

Table 2. Customer Application Component List for SA8025DK

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	3.9pF	50V	C22	Cap. cer. 1206 NPO ±0.5pF	Garrett	Rohm	MCH315A3R9CK
2	8.2pF	50V	C24, C18	Cap. cer. 1206 NPO ±0.5pF	Garrett	Rohm	MCH315A8R2CK
1	12pF	50V	C20	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A120JK
1	15pF	50V	C23	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A150JK
1	18pF	50V	C16	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A180JK
1	56pF	50V	C17	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A560JK
1	150pF	50V	C33	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A151JK
1	390pF	50V	C32	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A391JK
5	1000pF	50V	C9, C10, C13, C15, C19	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315A102JP
1	3900pF	50V	C31	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C392KK
3	0.01μF	50V	C11, C25, C27	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C103KK
9	0.1μF	50V	C2, C4, C6, C8, C12, C21, C28, C29, C35	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C104KP
1	0.15μF	16V	C26	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C154KP
4	4.7μF	10V	C1, C3, C5, C7	Tant. chip cap. A 3216 ±10%	Garrett	Philips	49MC475B010KOAS
Surface Mount Resistors							
3	0Ω		R5, R8, R25	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW000E
3	18Ω		R14, R15, R16	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW180E
1	27Ω		R11	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW270E
1	51Ω		R13	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW510E
1	560Ω		R20	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW561E
3	3.3kΩ		R1, R3, R6	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW332E
2	4.3kΩ		R5, R8, R25	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW432E
1	8.2kΩ		R19	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW822E
2	9.1kΩ		R2, R18	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW912E
5	10kΩ		R10, R12, R17, R22, R23	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW103E
1	18kΩ		R24	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW183E
1	130kΩ		R9	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW134E
1	560kΩ		R21	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW564E
Surface Mount Diodes							
1			VR1 (Varactor)	Variable capacitance SMD diode	Digikey	Philips	BB215
1			D1	SM Led	Digikey		
Surface Mount Inductors							
1	0.18μH		L1	Inductor SM Mold/WW A	Garrett	J.W. Miller	PM20-R18M
1	0.75μH		L2	Inductor SM Mold/WW A	Garrett	J.W. Miller	PM20-R68M
Voltage Regulators							
3			U1, U2, U3	Voltage regulator	Digikey		LM317LZ
TCXO							
1	19.2MHz		G1	Temp. controlled crystal osc.	TEW	TEW	TXS1034N-19.2MHz
VCO							
1	1667MHz		G2	Voltage controlled osc.	Murata	Murata Erie	MQE530-1667
Surface Mount Integrated Circuits							
1			U4	1MHz Fractional-N Synthesizer	Philips	Philips	SA8025DK
1			U5	Double Balanced Mixer Oscillator	Philips	Philips	NE/SA602A
Miscellaneous							
3			SMA1, SMA2, SMA3	SMA right angle jack receptacle	Newark	EF Johnson	142-0701-301
1			J1	Male 6-pins connector	STOCKO	STOCKO	MKS1956-6-0-606
1			J2	Male 2-pins connector	STOCKO	STOCKO	MKS1851-6-0-202
1			JP1	Test point	Digikey	3M	929647-36
1				Printed circuit board	Philips	Philips	SA7025/8025-M
75 Total Parts							

CMOS frequency synthesizer TDD1742T

GENERAL DESCRIPTION

The TDD1742T is a low power, high-performance frequency synthesizer in local oxidation CMOS (LOCMOS) technology. The device is designed for use in channelized VHF/UHF applications especially portable and mobile radios.

The circuit incorporates many of the features of the HEF4750V (frequency synthesizer) and HEF4751 (universal divider), including a high-gain phase comparator together with an on-chip sample-and-hold capacitor and phase modulator.

A multiplexed or bus-structured programming sequence allows interface to a microcontroller or external memory (ROM/PROM); power is applied to the memory only when it is required for programming via additional on-chip circuitry.

Operation is possible with a minimum supply voltage of 7 V and a maximum input frequency of 8,5 MHz.

Encapsulation in a 28-lead mini-pack enables the construction of small, low power consumption synthesizers with low noise performance and high side-band attenuation.

Features

- On-chip sample-and-hold capacitor
- Low power consumption
- High-gain phase comparator with low levels of noise and spurious outputs
- Auxiliary digital phase comparator for fast locking
- On-chip phase modulator
- Simple interfacing to external memory
- Microcontroller compatible
- Power-on reset circuitry

QUICK REFERENCE DATA

Supply voltage ranges			
pin 14	$V_{DD1} = V_{14-6}$		7 to 10 V
pin 8	$V_{DD2} = V_{8-6}$		4,5 to 5 V
pin 1	$V_{DD3} = V_{1-6}$		7 to 10 V
Supply current (at T_{amb} = 25 °C; $V_{DD1} = V_{DD3}$ = 7,4 V; V_{DD2} = 5 V)			
pin 14 (phase modulator OFF)	$I_{DD1} = I_{14}$	max.	1,5 mA
pin 8	$I_{DD2} = I_8$	max.	100 μA

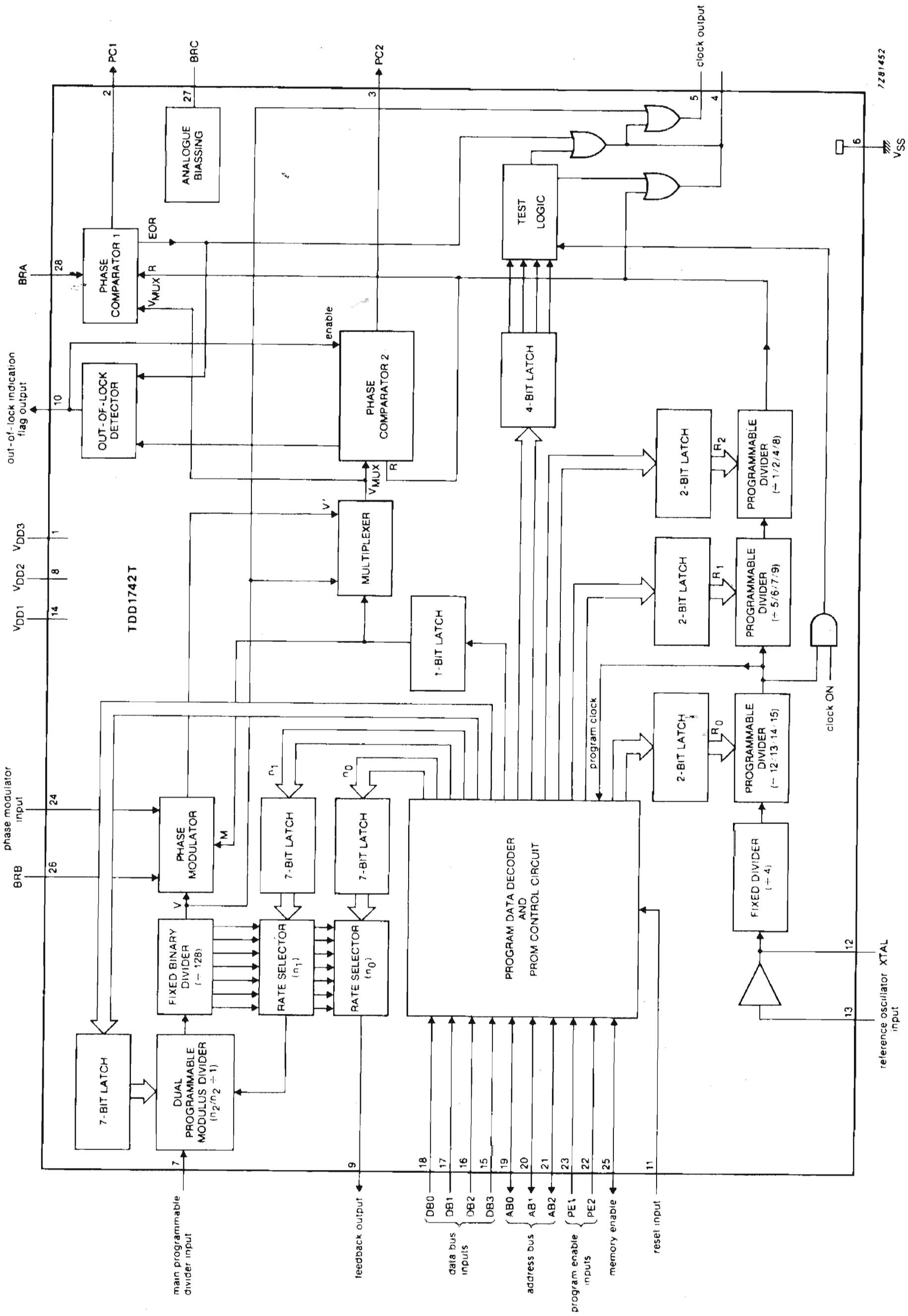


Fig. 1 Block diagram.

PINNING

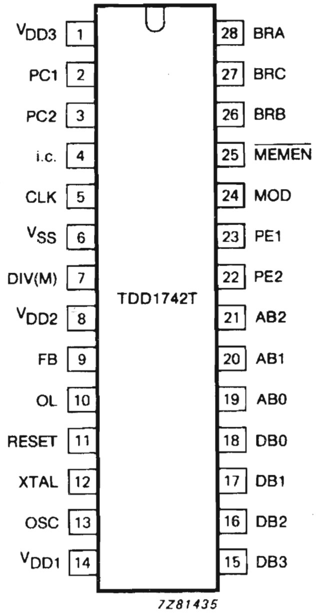


Fig. 2 Pinning diagram.

Pin functions

pin no.	mnemonic	description
1	V_{DD3}	**Power Supply 3:** analogue supply voltage (7 to 10 V).
2	PC1	**Phase Comparator 1:** high-gain analogue phase comparator output which is used when the system is in-lock to give low levels of noise and spurious outputs.
3	PC2	**Phase Comparator 2:** low-gain digital phase comparator 3-state output which enables the achievement of fast lock times when the system is initially out-of-lock. Phase comparator 2 is inhibited when the phase is within the locking range of phase comparator 1.
4	i.c.	**internally connected** (must be left floating).
5	CLK	**Clock:** clock output.
6	V_{SS}	**Ground:** circuit earth potential.
7	DIV(M)	**Divider:** input to the main programmable divider (8,5 MHz max.), usually from prescaler.
8	V_{DD2}	**Power Supply 2:** supply voltage for TTL-compatible stages (+ 5 V ± 10%).
9	FB	**Feedback:** feedback output to control the modulus of the external prescaler.
10	OL	**Out-of-lock:** out-of-lock indication flag output. This output is HIGH when phase comparator 2 is in operation (when the system is out-of-lock).
11	RESET	**Power-on-Reset:** Following power up an initial pulse is applied to this input pin to set the internal counters.

Pin functions (continued)

pin no.	mnemonic	description
12	XTAL	**Crystal:** output to external crystal to form the oscillator circuit in combination with the OSC input. Alternatively this pin may be used as a buffer output.
13	OSC	**Oscillator:** input to reference oscillator which together with the XTAL output and an external crystal is used to generate the reference frequency. Alternatively to OSC input may be used as a buffer amplifier for an external reference oscillator.
14	V_{DD1}	**Power Supply 1:** digital supply voltage (7 to 10 V).
15-18	DB3-DB0	**Data Bus:** Data Bus inputs (TTL compatible).
19-21	AB0-AB2	**Address Bus:** TTL compatible bidirectional address bus. Provides address output to an external memory or input from microcontroller. The outputs are 3-state with internal pull-downs.
22	PE2	**Program Enable 2:** TTL compatible inputs to initiate the programming cycle or strobe the internal data latches.
23	PE1	**Program Enable 1:**
24	MOD	**Modulator:** high impedance linear phase modulator input, which applies a voltage controlled delay to the programmable divider output to the phase comparator.
25	$\overline{\text{MEMEN}}$	**Memory Enable:** mode control and memory enable bidirectional pin. If pin 25 is LOW at general reset the TDD1742T is set to the microcontroller mode; if pin 25 is HIGH at general reset the TDD1742T is set to the memory mode and the ROM/PROM is enabled.
26	BRB	**Bias Resistor B:** current mirror which acts as gain control for the phase modulator.
27	BRC	**Bias Resistor C:** current mirror pin which provides analogue biassing.
28	BRA	**Bias Resistor A:** current mirror pin which acts as gain control for phase comparator 1.

FUNCTIONAL DESCRIPTION

Reference oscillator chain

The reference oscillator chain comprises a crystal oscillator and dividers to give the required frequency to drive the phase comparators.
The oscillator stage is a single inverter connected between pin 12 (XTAL) and pin 13 (OSC). Satisfactory operation is achieved with crystals up to 9 MHz. Alternatively, the OSC input may be used as a buffer amplifier for an external reference oscillator.
The reference divider chain comprises a fixed divide by 4-stage followed by three cascaded programmable dividers of ratios ÷ 12/13/14/15, ÷ 5/6/7/9 and ÷ 1/2/4/8. The output of the last stage is applied as one input (R) to the two phase comparators. Thus a number of division ratios between 240 and 4320 are possible which provides all the required VHF and UHF channel spacings with reference crystals in a 1 to 9 MHz range.

Main programmable divider

The main programmable divider is a rate feedback binary divider. As shown in figure 1 it comprises a fixed 7-bit binary divider (÷ 128) and two rate selectors (n_1 and n_0). One rate selector controls a 7-bit fully programmable dual modulus divider ($\div\ n_2/n_2 + 1$) and the other controls the external dual modulus prescaler ($\div\ A/A + 1$).

The overall division rate (N) is given by:

$$N = (128\, n_2 + n_1)\, A + n_0$$

Where:

$$0 \leqslant n_0 \leqslant 127$$
$$0 \leqslant n_1 \leqslant 127$$
$$1 \leqslant n_2 \leqslant 127.$$

The output from the programmable divider is fed to the phase comparators via the phase modulator and the multiplexer. The phase modulator is bypassed if not selected.

Phase comparison

The TDD1742T contains 2 phase comparators which act in close co-operation. Phase comparator 1 is the main comparator. It is designed to have a high-gain analogue output, 4500 volts/cycle at 10 kHz (typ.). This enables a low noise performance to be achieved. However, the output of phase comparator 1 will saturate at high or low levels for very small phase excursions.
Phase comparator 2 is an auxiliary comparator with a wide range, which enables faster lock times to be achieved than otherwise would be possible. This digital phase comparator has a linear ± 2 π radians phase range, which corresponds to a gain of $\frac{V_{DD}}{2}$ volts/cycle.

To avoid degrading the noise performance of the system by the relatively low gain of phase comparator 2, once a small phase error has been achieved an internal switch disconnects phase comparator 2, leaving only phase comparator 1 connected. Thus the low noise properties of phase comparator 1 are obtained once phase-lock has been achieved.

FUNCTIONAL DESCRIPTION (continued)

Phase comparator 1 (see Fig. 3)

Phase comparator 1 is comprised of a linear ramp generator and a sample and hold circuit.

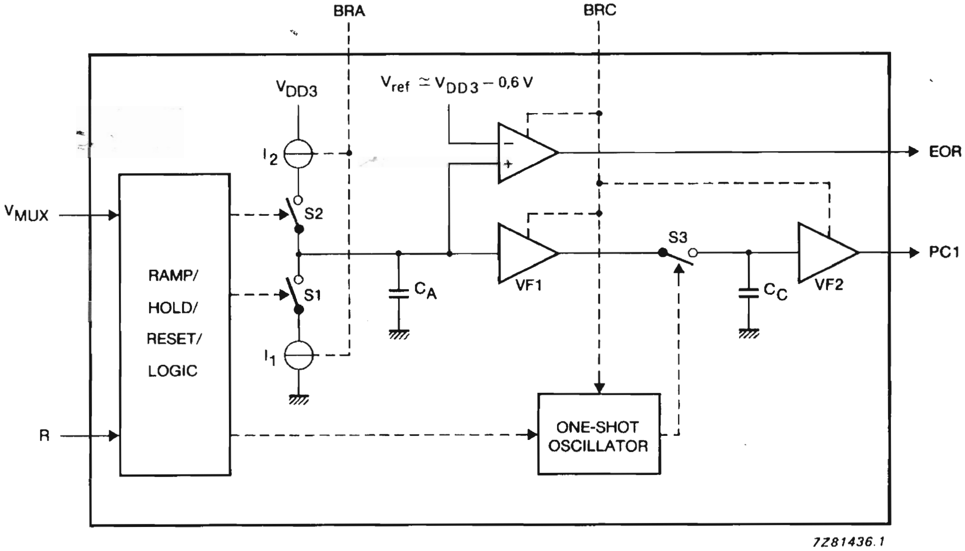


Fig. 3 Simplified block diagram of phase comparator 1.

A negative-going transition at the V_{MUX} input causes the hold capacitor C_A to be discharged via switch S1 and constant current source I_1.
A positive-going transition at the V_{MUX} input causes the hold capacitor C_A to be charged via switch S2 and constant current source I_2, which produces a linear ramp.
A negative-going transition at the R input terminates the linear ramp.
Capacitor C_A holds the voltage that the ramp has attained, and is buffered by the voltage follower VF1. After the output of VF1 is stable (2 μs), the sample switch S3 is closed for approximately 1 μs by the one-shot oscillator. This enables the capacitor C_C to charge to the voltage level of VF1 and in turn buffered by voltage follower VF2 made available at output PC1.
The construction and small duty cycle of the sample switch S3 provides a low hold step, resulting in a minimum side-band level.
If the linear ramp terminates before a negative-going transition at the R input is present, an end of ramp (EOR) signal is produced, generating in turn an out-of-lock (OL) signal. OL enables phase comparator 2 via the out-of-lock detector.

These actions are illustrated in the waveforms of Fig. 4 and Fig. 5.

The gain of phase comparator 1 as measured at PC1 is given by:

$$\text{PC gain} \simeq \frac{446\ I_{BRA}}{F_R}$$

Where:

I_{BRA} is in μA
F_R is the phase comparator reference frequency in kHz

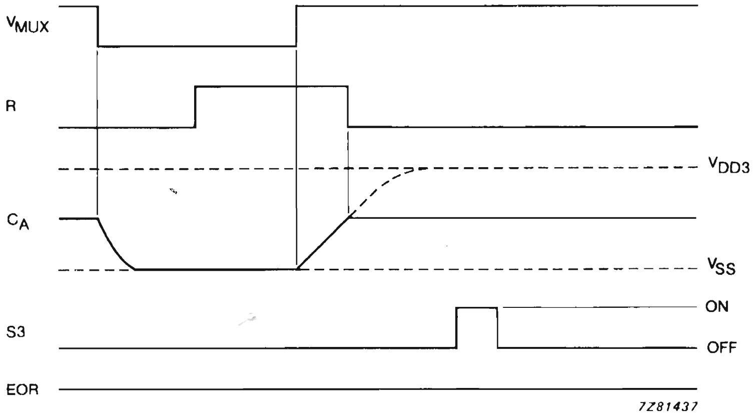


Fig. 4 Waveforms of phase comparator 1; in-lock condition.

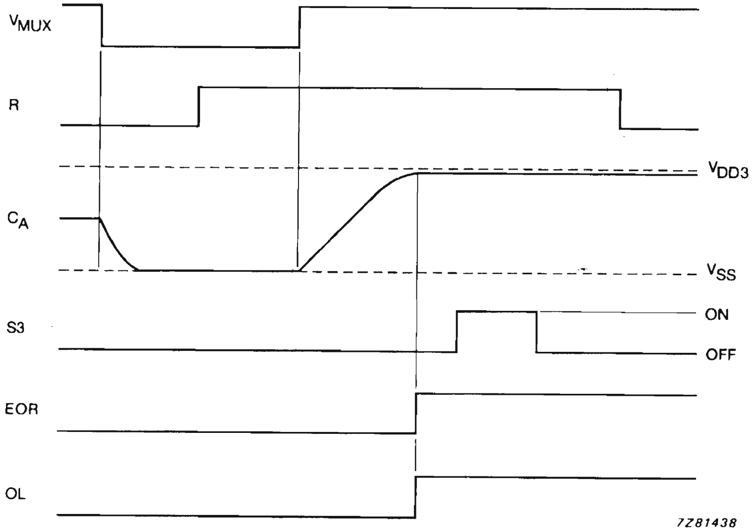


Fig. 5 Waveforms of phase comparator 1; out-of-lock condition.

When V_{MUX} leads R the output signal at pin 2 (PC1) is proportional to the phase difference (in-lock condition) or HIGH (out-of-lock condition).
When R leads V_{MUX} the output signal at pin 2 (PC1) remains LOW.

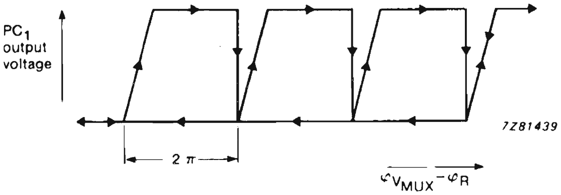


Fig. 6 Phase characteristic of output PC1.

FUNCTIONAL DESCRIPTION (continued)

Phase comparator 2 (see Fig. 7)

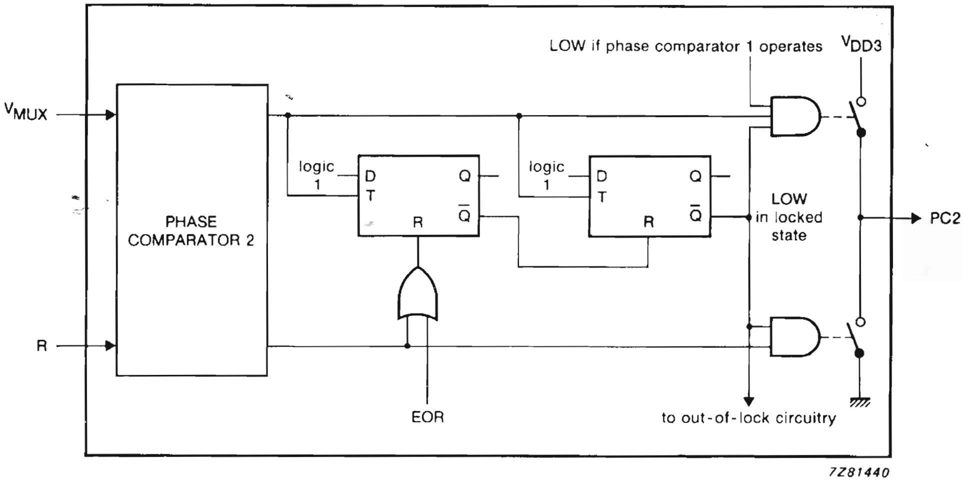


Fig. 7 Simplified block diagram of phase comparator 2.

The digital phase comparator (PC2) has three stable states:

- Reset
- V_{MUX} leads R
- R leads V_{MUX}

Table 1 Phase comparator 2: stable states and corresponding output levels

state	V_{MUX} leads R	R leads V_{MUX}
reset	0	0
V_{MUX} leads R	1	0
R leads V_{MUX}	0	1

Transition from one state to another takes place on command of either an active V_{MUX}-edge or an active R-edge as shown in Fig. 8.

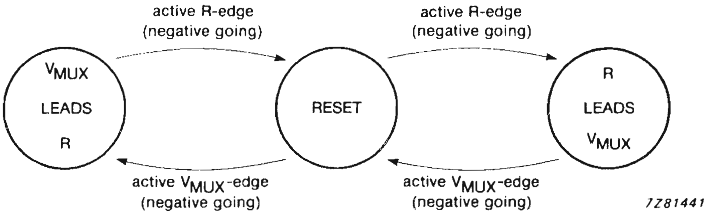

active R-edge (negative going)
active R-edge (negative going)
V_{MUX} LEADS R
RESET
R LEADS V_{MUX}
active V_{MUX}-edge (negative going)
active V_{MUX}-edge (negative going)
7Z81441

Fig. 8 Transition of state; phase comparator 2.

The output of phase comparator 2 produces positive or negative going pulses with variable width, dependent on the phase relationship of R and V_{MUX}.
The average output voltage is a linear function of the phase difference. Output at pin 3 (PC2) remains in the high impedance OFF-state in the region in which phase comparator 1 operates

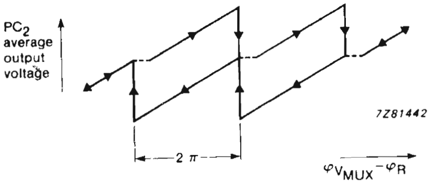


Fig. 9 Phase characteristic of output PC2.

To reach the reset state of phase comparator 2 it is necessary to apply:

- $2V_{MUX}$ + R*
  or
- 2R + V_{MUX}

Thus to achieve the R leads V_{MUX} state 2R must be applied; to achieve the V_{MUX1} leads R state $2V_{MUX}$ must be applied.

Out-of-lock function

There are several situations when the system goes from the locked to the out-of-lock state (OL output goes HIGH):

- V_{MUX} leads R, however out of the range of phase comparator 1
- R leads V_{MUX}
- R-pulse is missing
- V_{MUX}-pulse is missing

In the first three situations the locked state can be reset by applying two successive cycles within the range of phase comparator 1.
In the fourth situation the locked state can be reset by applying a V_{MUX} pulse followed by two successive cycles within the range of phase comparator 1.

Phase modulator (see Fig. 10)

The linear phase modulator applies a voltage controlled delay to the signal from the programmable divider to the phase comparator input. The gain of the phase modulator is adjustable via an external bias resistor (BRB) which is connected between pin 26 and ground.
The time delay introduced into the V path to the phase modulator is:

$$\frac{909}{I_{BRB}} \text{ ns/volt of input applied to pin 24 (MOD)}$$

When a positive-going transition appears at the V-input, the D type flip-flop produces a HIGH V′ level and causes capacitor C_B to produce a positive-going ramp via switch S1 and constant current source I_1 starting at the V_{SS} potential. When the ramp has reached a value equal to the modulation input voltage (at MOD), the comparator resets the D type flip-flop, which terminates the V pulse. C_B now discharges to V_{SS} via switch S1 and constant current source I_2 and the circuit returns to the start position. Because the trailing edge of the V′ pulse is the active edge for the phase comparators, a linear phase modulation is achieved. The associated waveforms are shown in Fig. 11. The phase modulator can be switched OFF, via the programming logic, to avoid superfluous dissipation. To achieve, this the M signal must be programmed to logic 0. The V pulse will then be connected via switch S2 to V_{MUX}.

* This means apply two successive active V_{MUX} edges followed by one active R edge.

FUNCTIONAL DESCRIPTION (continued)

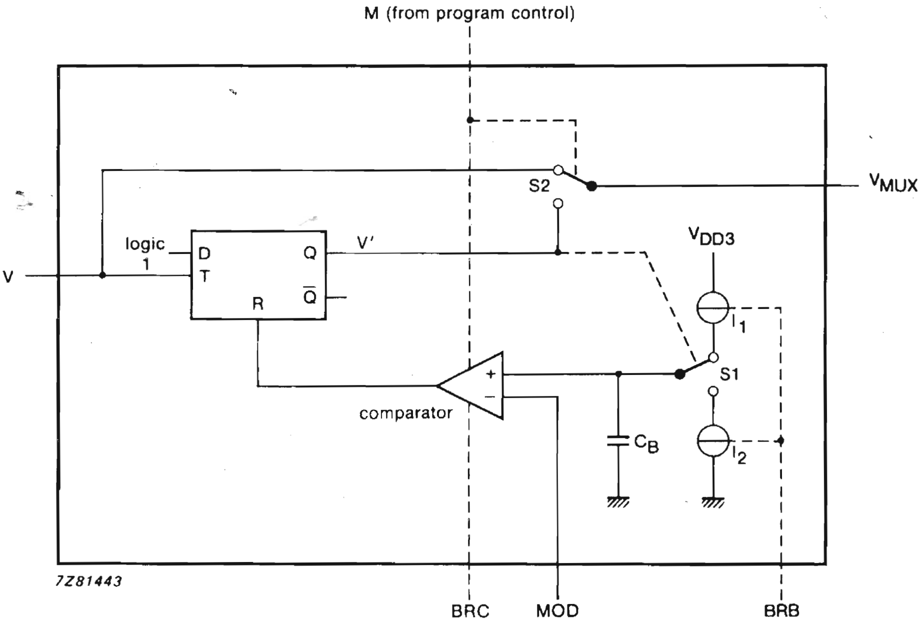


Fig. 10 Simplified block diagram of the phase modulator.

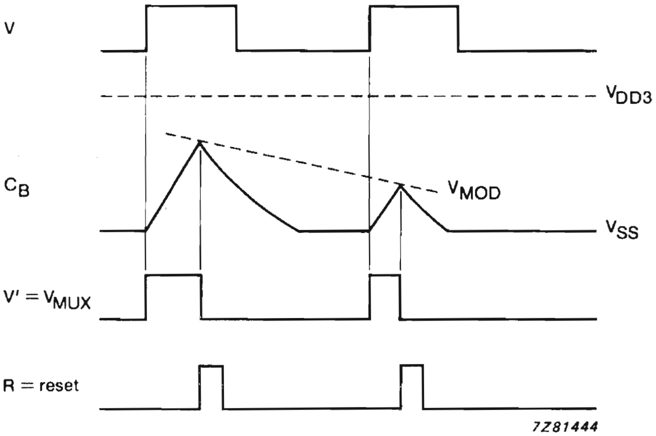


Fig. 11 Phase modulator waveforms; M = 1.

Program control

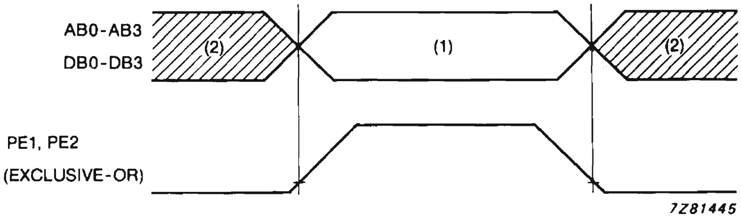
A multiplexed or bus structured sequence allows the TDD1742T to be interfaced to a microcontroller or a PROM.
The device is fully programmable in terms of:

- 6 bits to define the reference divider ratio
- 21 bits to define the main divider ratio
- 1 bit to switch the modulator
- 4 bits to determine the test status

Thus the TDD1742T is programmed with a total of 32 bits which are organized as eight 4-bit words.
The address bus is 3 bits wide and the data bus is 4 bits wide. Both buses are TTL compatible.
The data words are described in detail in Tables 3 to 7.

Microcontroller mode

If pin 25 ($\overline{\text{MEMEN}}$) is LOW at general reset, the device is set to the micro-controller mode. In this mode a 7-bit word, comprised of 3 address bits (AB0 to AB2) and 4 data bits (DB0 to DB3), may be strobed into the TDD1742T when the program enable pins PE1 and PE2 are set to opposite state (EXCLUSIVE -OR condition; see Fig. 12 and Table 2). One frame of 8 words is necessary to completely program the TDD1742T. Incoming data is not clocked into the internal counter latches until after the receipt of data corresponding to address 111. Upon subsequent reprogramming it is not necessary to change all eight words but a reprogramming sequence must always finish with the data corresponding to address 111.



(1) Address and data valid.
(2) Address and data not valid.

Fig. 12 Waveforms for program enable function; microcontroller mode.

Table 2 Truth table for program enable function; microcontroller mode

PE1	PE2	load
0	0	NO
1	0	YES
0	1	YES
1	1	NO

Program control (continued)

Memory mode (PROM)

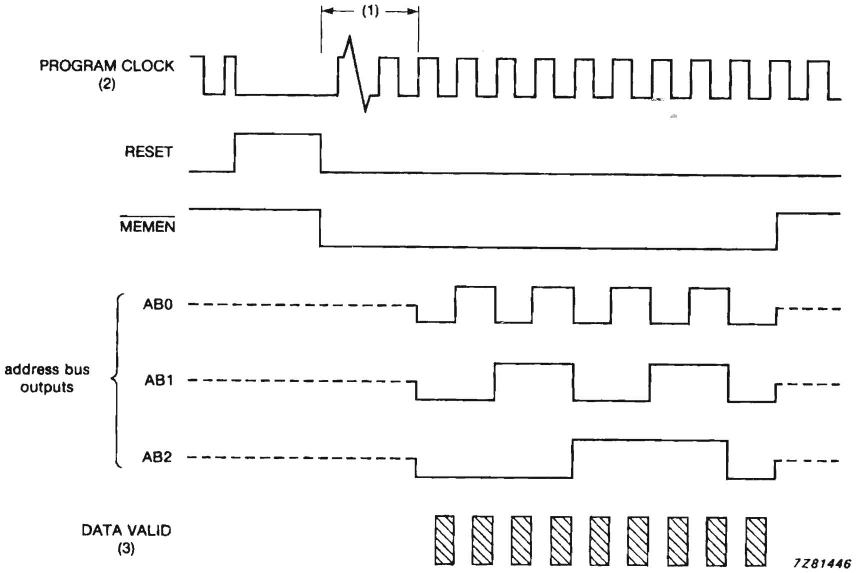
If pin 25 ($\overline{\text{MEMEN}}$) is HIGH at general reset, TDD1742T is set to the memory mode and a programming cycle is initiated. Subsequent reprogramming is performed by applying a pulse to program enable PE1 (pin 23) or PE2 (pin 22). If PE1 is LOW, programming will occur on the LOW-to-HIGH transition of PE2. If PE1 is HIGH, programming will occur on the HIGH-to-LOW transition of PE2. PE1 and PE2 are interchangeable. Reprogramming will also occur by applying a pulse to RESET (pin 11).

At the start of a programming sequence pin 25 goes LOW and may be used to apply power to the memory via an external driver. After a settling time the address bus outputs 000 followed by the remaining seven addresses. During the second half of each address period data, from the memory is latched into the TDD1742T so that the access time of the PROM is not critical.

Note

The program clock is derived from the reference divider chain and its frequency equals $f_{OSC}/4R_0$.

After the full 32 bits have been read the address returns to address 000 before going 3-state. This step transfers data from the internal data latches to the appropriate divider latches. Pin 25 now returns to a high impedance state and power is removed from the memory. Fig. 13 shows the timing for a reset initiated programming sequence; the timing is similar for program enable initiated sequence.



(1) Delay time for PROM settling.
(2) The program clock is derived from the reference divider chain.
(3) Data is valid during the shaded period.

Fig. 13 Timing diagram for TDD1742T PROM control.

Data memory maps

Table 3 Bit programming of the eight 4-bit words

address			data			
AB2	AB1	AB0	DB3	DB2	DB1	DB0
0	0	0	see Table 4			
0	0	1	$n_0 3$	$n_0 2$	$n_0 1$	$n_0 0$
0	1	0	$R_0 0$	$n_0 6$	$n_0 5$	$n_0 4$
0	1	1	$n_1 3$	$n_1 2$	$n_1 1$	$n_1 0$
1	0	0	$R_0 1$	$n_1 6$	$n_1 5$	$n_1 4$
1	0	1	$n_2 3$	$n_2 2$	$n_2 1$	$n_2 0$
1	1	0	M	$n_2 6$	$n_2 5$	$n_2 4$
1	1	1	$R_2 1$	$R_2 0$	$R_1 1$	$R_1 0$

In Table 3

n_0, n_1 and n_2 comprises the main programmable divider.

$n_0 0$ is the LSB of n_0, $n_0 6$ the MSB and so forth.

If M is 1 the modular is ON.

Table 4 Memory map for address 000

DB3	DB2	DB1	DB0	program clock to output CLK	mode
0	0	X	X	yes	idle
0	1	0	0	no	idle
all other combinations				not defined	not defined

Where

X = don't care.

For optimum performance (minimum crosstalk) 0100 should be programmed into address 000.

Memory maps (continued)

Table 5 Reference divider control; part 1

R_01	R_00	division ratio
0	0	12
0	1	13
1	0	14
1	1	15

In Table 5:

R_00 and R_01 control the ÷ 12/13/14/15 portion of the reference divider.

Table 6 Reference divider control; part 2

R_11	R_10	division ratio
0	0	9
0	1	5
1	0	6
1	1	7

In Table 6:

R_10 and R_11 control the ÷ 5/6/7/9 portion of the reference divider.

Table 7 Reference divider control; part 3

R_21	R_20	division ratio
0	0	1
0	1	2
1	0	4
1	1	8

In Table 7:

R_20 and R_21 control the ÷ 1/2/4/8 portion of the reference divider.

Current biassing

Current biassing is provided by 3 external bias resistors A, B and C.

Bias Resistor A: is connected between pin 28 (BRA) and ground. The value of the resistor must be such that $I_{BRA} = 20\ \mu A$, which acts as gain control for analogue phase comparator 1.
Bias Resistor B: is connected between pin 26 (BRB) and ground. The value of the resistor must be such that $I_{BRB} = 3$ to $25\ \mu A$, which acts as gain control for the phase modulator.
Bias Resistor C: is connected between pin 27 (BRC) and ground. The value of the resistor must be such that $I_{BRC} = 5$ to $30\ \mu A$, which provides biassing for the remainder of the analogue circuitry.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges				
pin 14	V_{DD1}		−0,5 to + 15	V
pin 8	V_{DD2}		−0,5 to + 15	V
pin 1	V_{DD3}		−0,5 to + 15	V
Voltage on any input	V_I		−0,5 to V_{DD1}+ 0,5	V
Relative supply voltage	V_{DD2}-V_{DD1}	max.	0,5	V
Relative supply voltage	V_{DD3}-V_{DD1}	max.	0,5	V
D.C. current into any input or output	± I	max.	10	mA
Power dissipation per package for T_{amb} = 0 to + 85 °C	P_{tot}	max.	400	mW
Power dissipation per output for T_{amb} = 0 to + 85 °C	P_O	max.	100	mW
Storage temperature range	T_{stg}		−65 to 150	°C
Operating ambient temperature range	T_{amb}		−40 to 85	°C

D.C. CHARACTERISTICS

$V_{DD1} = V_{DD3} = 7{,}4$ V; $V_{DD2} = 5$ V; $V_{SS} = 0$ V; $T_{amb} = 25$ °C unless otherwise specified; for definitions see note 1.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage					
pin 14	V_{DD1}	7	–	10	V
pin 8	V_{DD2}	4,5	–	5	V
pin 1	V_{DD3}	7	–	10	V
Supply current					
pin 14 (phase modulator OFF)	I_{DD1}	–	–	1,5	mA
pin 8	I_{DD2}	–	–	100	μA
pin 1 (phase modulator OFF)	I_{DD3}	–	–	1,5	mA
Input leakage current (notes 2 and 3)					
logic inputs, MOD	$\pm I_{LI}$	–	–	300	nA
Output leakage current (notes 2 and 3) at ½ V_{DD}					
PC2 high impedance OFF state	$\pm I_{LO}$	–	–	50	nA
$\overline{\text{MEMEN}}$ high impedance state	$\pm I_{LO}$	–	–	1,6	μA
I/O current					
AB0 to AB2 high impedance state	$I_{I/O}$	5	–	30	μA
Logic input voltage LOW					
CMOS inputs; CMOS I/Os	V_{IL}	–	–	$0{,}3V_{DD1}$	V
TTL inputs; TTL I/Os	V_{IL}	–	–	0,8	V
Logic input voltage HIGH					
CMOS inputs; CMOS I/Os	V_{IH}	$0{,}7V_{DD1}$	–	–	V
TTL inputs; TTL I/Os	V_{IH}	2	–	–	V
Logic output voltage LOW (note 2)					
at $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	50	mV
Logic output voltage HIGH (note 2)					
at $\lvert I_O \rvert < 1$ μA	V_{OH}	V_{DD1}-50	–	–	mV

parameter	symbol	min.	typ.	max.	unit
Logic output voltage LOW (note 2)					
$\overline{\text{MEMEN}}$ at I_{OL} = 4 mA	V_{OL}	–	–	1	V
PC2 at I_{OL} = 1,5 mA	V_{OL}	–	–	0,5	V
CLK; OL at I_{OL} = 1 mA	V_{OL}	–	–	0,5	V
XTAL at I_{OL} = 3 mA	V_{OL}	–	–	0,5	V
FB at I_{OL} = 1 mA	V_{OL}	–	–	0,5	V
AB0; AB1; AB2 at I_{OL} = 0,2 mA	V_{OL}	–	–	0,4	V
Logic output voltage HIGH (notes 2 and 3)					
PC2 at $-I_{OH}$ = 1,5 mA	V_{OH}	$V_{DD1}-0,5$	–	–	V
CLK; OL at $-I_{OH}$ = 1 mA	V_{OH}	$V_{DD1}-0,5$	–	–	V
XTAL at $-I_{OH}$ = 3 mA	V_{OH}	$V_{DD1}-1$	–	–	V
FB at $-I_{OH}$ = 1 mA	V_{OH}	$V_{DD2}-1$	–	–	V
AB0; AB1 at I_{OH} = 0,2 mA	V_{OH}	2,4	–	–	V
AB2 at I_{OH} = 0,8 mA	V_{OH}	2,4	–	–	V
Output PC1					
sink current (notes 2, 3 and Fig. 15)	I_O	1	–	–	mA
source current (notes 2, 3 and Fig. 16)	$-I_O$	1	–	–	mA
Internal resistance of phase comparator 1 (notes 2 and 3) locked state |output swing| < 200 mV specified output range: 0,5 V_{DD} –0,5 V to 0,5 V_{DD} + 0,5 V	R_i	–	2,0	–	Ω

A.C. CHARACTERISTICS

A dynamic specification is given for the circuit, built-up with external components as shown in Fig. 14, under the following conditions; for definitions see note 1; V_{DD} = 7,4 ± 0,4 V; T_{amb} = 25 °C; input transition times ⩽ 40 ns; $C_A = C_B = C_C$ = 10 nF; R_A chosen so that I_{RA} = 20 µA ± 1 µA; R_B chosen so that I_{RB} = 3 to 25 µA; R_C chosen so that I_{RC} = 5 to 30 µA; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Main programmable divider (DIV(M); pin 7)					
input frequency all divider ratios (square wave input)	$f_{DIV(M)}$	8,5	–	–	MHz
Reference divider					
input frequency all divider ratios (square wave input)	$f_{DIV(R)}$	9	–	–	MHz
Oscillator frequency (OSC; pin 13)	f_{OSC}	9	12	–	MHz
Input capacitance					
DIV(M); OSC	C_I	–	–	3	pF
DB0 to DB3; PE1; PE2; AB0 to AB2	C_I	–	–	5	pF
Propagation delay (see Fig. 17)					
Feedback output to external prescaler					
DIV(M) → FB at C_L = 10 pF					
HIGH to LOW*	t_{PHL}	–	35	70	ns
LOW to HIGH*	t_{PLH}	–	35	70	ns
Average power supply current (notes 3 and 4)					
in-lock state	I_{DD1}	–	2	–	mA
	I_{DD2}	–	0,15	–	mA
	I_{DD3}	–	0,45	–	mA

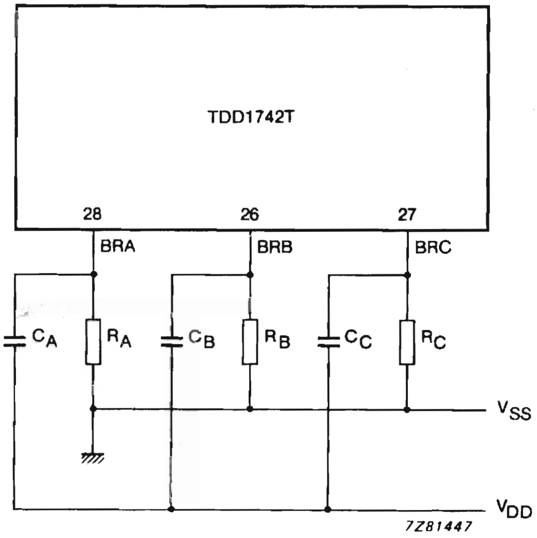


Fig. 14 Test circuit for measuring a.c. characteristics.

Notes to the characteristics

1. Definitions:
   R_A = external biassing resistor between pins BRA and V_{SS}.
   R_B = external biassing resistor between pins BRB and V_{SS}.
   R_C = external biassing resistor between pins BRC and V_{SS}.
   C_A = decoupling capacitor between pins BRA and V_{DD}.
   C_B = decoupling capacitor between pins BRB and V_{DD}.
   C_C = decoupling capacitor between pins BRC and V_{DD}.
   CMOS logic inputs: RESET, OSC.
   CMOS logic outputs: PC2, CLK, OL, XTAL.
   CMOS logic I/O: $\overline{\text{MEMEN}}$.
   TTL logic inputs: DB0 to DB3, PE2, PE1.
   TTL logic output: FB.
   TTL logic I/O: AB0 to AB2.
   Analogue inputs: DIV(M), MOD.
   Analogue output: PC1.
   Analogue biassing pins: BRA, BRB, BRC.
2. All logic inputs at V_{SS} or V_{DD}.
3. R_A connected; its value chosen such that $I_{BRA} = 20\ \mu A$.
   R_B connected; its value chosen such that $I_{BRB} = 20\ \mu A$.
   R_C connected; its value chosen such that $I_{BRC} = 20\ \mu A$.
4. Average power supply current measured at:
   f_{OSC} = 5 MHz, external clock, divider ratio 420;
   $f_{DIV(M)}$ = 2 MHz, divider ratio 168.

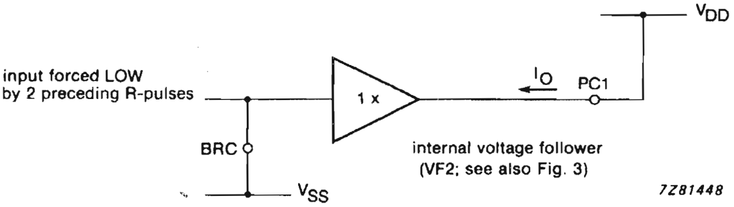


Fig. 15 Equivalent circuit for output PC1 sink current.

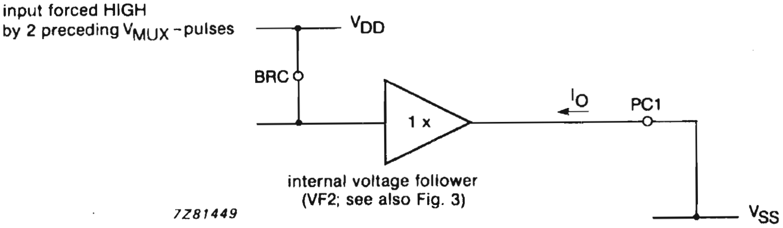


Fig. 16 Equivalent circuit for output PC1 source current.

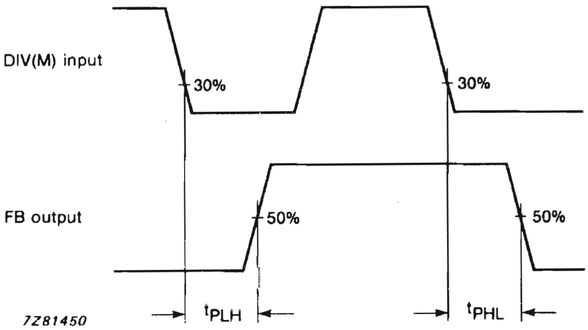


Fig. 17 Waveforms showing propagation delay; DIV (M) → FB.

APPLICATION INFORMATION

Fig. 18 shows a typical application circuit using the TDD1742T in the memory mode with the following design parameters:

Frequency range	150 to 155 MHz
VCO sensitivity	1 MHz/V
Reference frequency	12,5 kHz
Prescaler	÷ 80/81
Reference crystal frequency	5,25 MHz
Reference divider chain	÷ 15; ÷ 7; ÷ 1
Total division ratio	12000 to 12400
Loop bandwidth	300 Hz

APPLICATION INFORMATION (continued)

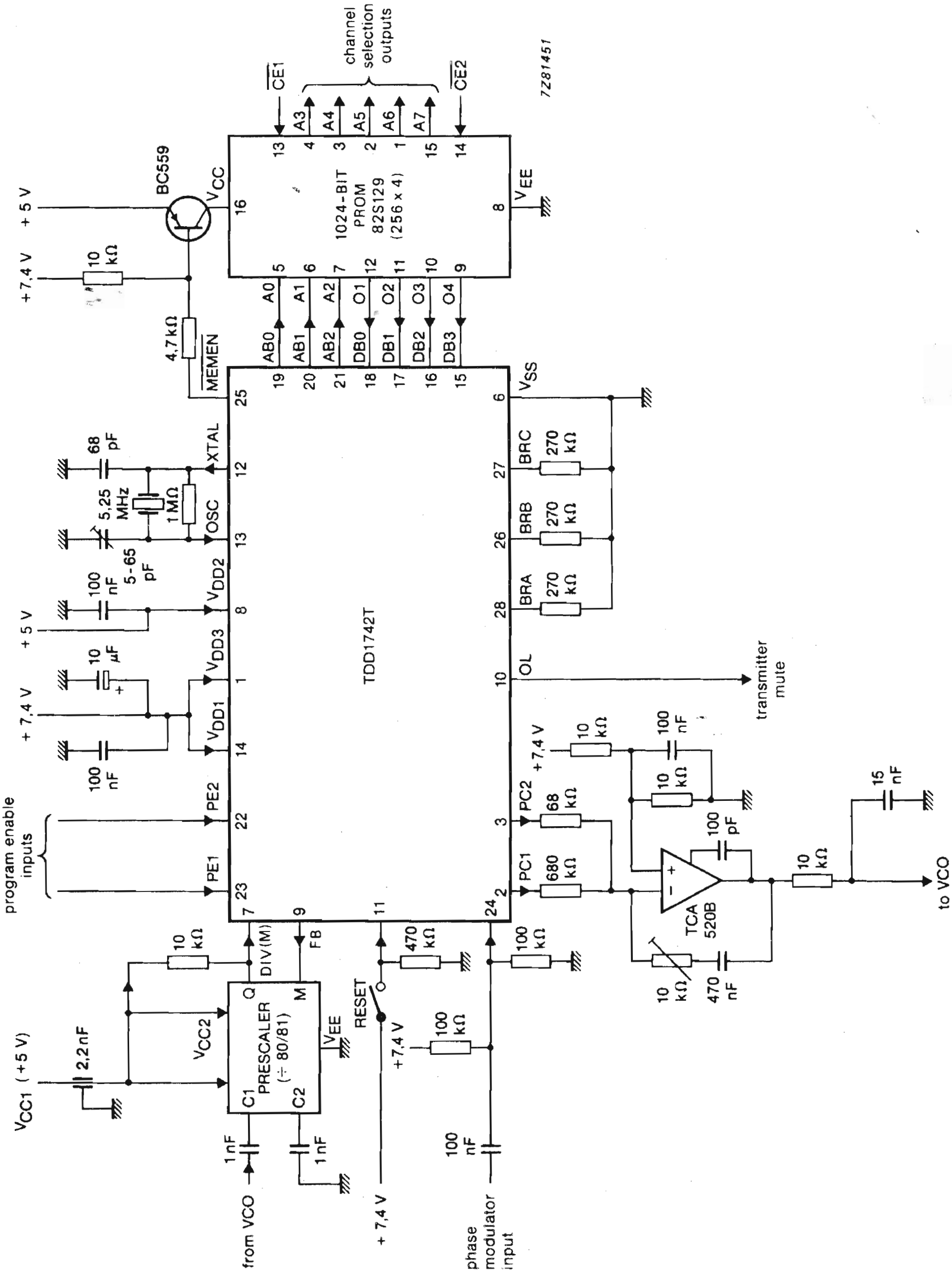


Fig. 18 Typical application circuit using the TDD1742T in memory mode.

Radio tuning PLL frequency synthesizer TSA6057/T

GENERAL DESCRIPTION

The TSA6057/6057T is a bipolar single chip frequency synthesizer manufactured in SUBILO-N technology (components laterally separated by oxide). It performs all the tuning functions of a PLL radio tuning system. The IC is designed for application in all types of radio receivers.

Features

- On-chip AM and FM prescalers with high input sensitivity
- On-chip high performance one input (two output) tuning voltage amplifier for the AM and FM loop filters
- On-chip 2-level current amplifier (charge pump) to adjust the loop gain
- Only one reference oscillator (4 MHz) for both AM and FM
- High speed tuning due to a powerful digital memory phase detector
- 40 kHz output reference frequency for co-operation with the FM/IF system and microcomputer-based tuning interface IC (TEA6100)
- Oscillator frequency ranges of: 512 kHz to 30 MHz and 30 MHz to 150 MHz
- Three selectable reference frequencies of 1 kHz, 10 kHz or 25 kHz for both tuning ranges
- Serial 2-wire I²C-bus interface to a microcomputer and one programmable address input
- Software controlled bandswitch output

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
pin 3		$V_{CC1} = V_{3\text{-}4}$	4.5	5.0	5.5	V
pin 16		$V_{CC2} = V_{16\text{-}4}$	V_{CC1}	8.5	12	V
Supply current	no outputs loaded					
pin 3		I_3	12	20	28	mA
pin 16		I_{16}	0.7	1.0	1.3	mA
Max. input frequency on AM_I		f_{iAM}	30	–	–	MHz
Min. input frequency on AM_I		f_{iAM}	–	–	0.512	MHz
Max. input frequency on FM_I		f_{iFM}	150	–	–	MHz
Min. input frequency on FM_I		f_{iFM}	–	–	30	MHz
Input voltage on AM_I (RMS value)	$V_{iFM} = 0$ V	$V_{iAM(rms)}$	30	–	500	mV
Input voltage on FM_I (RMS value)	$V_{iAM} = 0$ V	$V_{iFM(rms)}$	20	–	300	mV
Total power dissipation		P_{tot}	–	0.14	–	W
Operating ambient temperature range		T_{amb}	–30	–	+ 85	°C

PACKAGE OUTLINES

TSA6057: 16-lead DIL; plastic (SOT38).
TSA6057T: 16-lead minipack; plastic (SO16L; SOT162A).

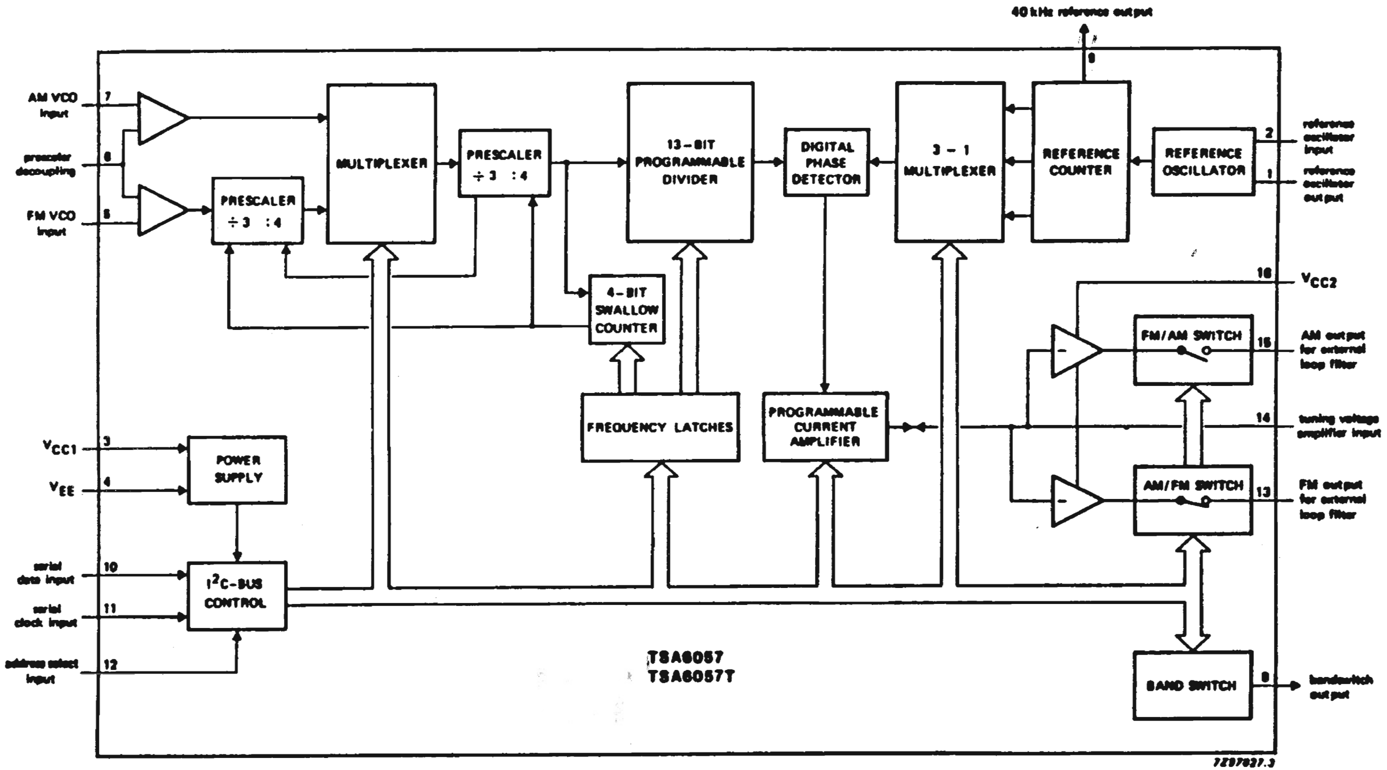


Fig.1 Block diagram.

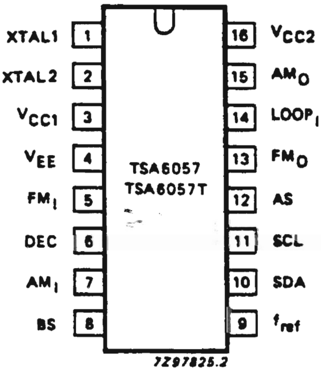


Fig.2 Pinning diagram.

PINNING

1	XTAL1	reference oscillator output	
2	XTAL2	reference oscillator input	
3	V_{CC1}	positive supply voltage	
4	V_{EE}	ground	
5	FM_I	FM VCO input	
6	DEC	prescaler decoupling	
7	AM_I	AM VCO input	
8	BS	bandswitch output	
9	f_{ref}	40 kHz reference output	
10	SDA	serial data input	I^2C-bus
11	SCL	serial clock input	
12	AS	address select input	
13	FM_O	FM output for external loop filter	
14	$LOOP_I$	tuning voltage amplifier input	
15	AM_O	AM output for external loop filter	
16	V_{CC2}	positive supply voltage	

FUNCTIONAL DESCRIPTION

The TSA6057/6057T contains the following parts and facilities:

- Separate input amplifiers for the AM and FM VCO-signals.
- A prescaler with the divisors 3:4 on AM and 15:16 on FM, a multiplexer to select AM or FM and a 4-bit programmable swallow counter.
- A 13-bit programmable counter.
- A digital memory phase detector.
- A reference frequency channel comprised of a 4 MHz crystal oscillator followed by a reference counter. The reference frequency can be 1 kHz, 10 kHz or 25 kHz and is applied to the digital memory phase detector. The reference counter also outputs a 40 kHz reference frequency to pin 9 for co-operation with the FM/IF system and microcomputer-based tuning interface IC (TEA6100).
- A programmable current amplifier (charge pump) which consists of a 5 μA and a 450 μA current source. This allows adjustment of loop gain, thus providing high current-high speed tuning and low current-stable tuning.
- A one input – two output tuning voltage amplifier. One output is connected to the external AM loop filter and the other output to the external FM loop filter. Under software control, the AM output is switched to a high impedance state by the FM/AM switch in the FM position and the FM output is switched to a high impedance state by the AM/FM switch in the AM position. The outputs can deliver a tuning voltage of up to 10.5 V.
- An I^2C-bus interface with data latches and control logic. The I^2C-bus is intended for communication between microcontrollers and different ICs or modules. Detailed information on the I^2C-bus specification is available on request.
- A software-controlled bandswitch output.

FUNCTIONAL DESCRIPTION (continued)

Controls

The TSA6057/6057T is controlled via the 2-wire I²C-bus. For programming there is one module address, a logic 0 R/W bit, a subaddress byte and four data bytes. The subaddress determines which one of the four data bytes is transmitted first. The module address contains a programmable address bit (D1) which with address select input AS (pin 12) makes it possible to operate two TSA6057s in one system.

The auto increment facility of the I²C-bus allows programming of the TSA6057/6057T within one transmission (address + subaddress + 4 data bytes).

- The TSA6057/6057T can also be partially programmed. Transmission must then be ended by a stop condition.

The bit organization of the 4 data bytes is shown in Fig.3 and are described in sections (a) to (f).

(a) The bits S0 to S16 (DB0: D7-D1; DB1: D7-D0; DB2: D1-D0) together with bit FM/AM (DB2: D5) are used to set the divisor of the input frequency at inputs $\mathrm{AM_I}$ (pin 7) or $\mathrm{FM_I}$ (pin 5). If the system is in lock the following is valid:

FM/$\overline{\mathrm{AM}}$	input frequency (f_i)	input
0	$(S0 \times 2^0 + S1 \times 2^1 \ldots\ldots + S13 \times 2^{13} + S14 \times 2^{14}) \times f_{ref}$	$\mathrm{AM_I}$
1	$(S0 \times 2^0 + S1 \times 2^1 \ldots\ldots + S15 \times 2^{15} + S16 \times 2^{16}) \times f_{ref}$	$\mathrm{FM_I}$

Where

The minimum dividing ratio for AM mode is $2^6 = 64$
The minimum dividing ratio for FM mode is $2^8 = 256$

(b) The bit CP is used to control the charge pump current (DB0: D0).

CP	current
0	low
1	high

(c) The bits REF1 and REF2 are used to set the reference frequency applied to the phase detector (DB2: D7-D6).

REF1	REF2	frequency (kHz)
0	0	1
0	1	10
1	0	25
1	1	none

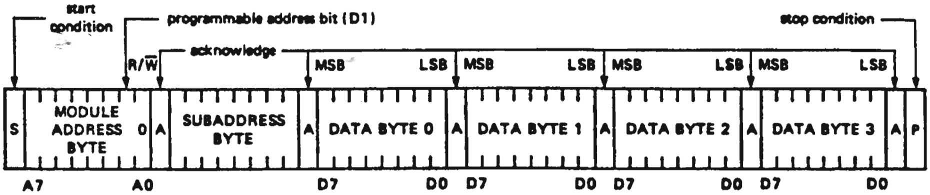
(d) The bit $\overline{\mathrm{FM}}$/AM OPAMP controls the switch AM/FM; FM/AM in the tuning voltage amplifier output circuitry (DB2: D4).

$\overline{\mathrm{FM}}$/AM OPAMP	switch FM/AM	switch AM/FM
1	closed	open
0	open	closed

(e) The bit BS controls the open collector bandswitch output (DB2: D2).

BS	bandswitch output
1	sink current
0	floating

(f) The data byte DB3 must be set to 0 . . . . . .0. It is also used for test purposes.



	MSB							LSB
MODULE ADDRESS	1	1	0	0	0	1	0/1	0
	A7							A0
SUBADDRESS	0	0	0	0	0	0	0/1	0/1
DATA BYTE 0 (DB0)	S6	S5	S4	S3	S2	S1	S0	CP
	D7							D0
DATA BYTE 1 (DB1)	S14	S13	S12	S11	S10	S9	S8	S7
	D7							D0
DATA BYTE 2 (DB2)	REF1	REF2	FM/$\overline{AM}$	$\overline{FM}$/AM OPAMP	NOT USED	BS	S16	S15
	D7							D0
DATA BYTE 3 (DB3)	T1	T2	T3	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED
	D7							D0

Examples using auto-increment facility

S	ADDRESS	A	SUBADDRESS 02	A	DB2	A	DB3	A	P					
S	ADDRESS	A	SUBADDRESS 00	A	DB0	A	DB1	A	P					
S	ADDRESS	A	SUBADDRESS 03	A	DB3	A	DB0	A	DB1	A	DB2	A	P	

7Z97826.2

Fig.3 Bit organization.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 3)	$V_{CC1} = V_{3\text{-}4}$	−0.3	5.5	V
Supply voltage (pin 16)	$V_{CC2} = V_{16\text{-}4}$	V_{CC1}	12.5	V
Total power dissipation	P_{tot}	−	0.85	W
Operating ambient temperature	T_{amb}	−30	+85	°C
Storage temperature range	T_{stg}	−65	+150	°C

CHARACTERISTICS

$V_{CC1} = 5$ V; $V_{CC2} = 8.5$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		V_{CC1}	4.5	5.0	5.5	V
Supply voltage (pin 16)		V_{CC2}	V_{CC1}	8.5	12	V
Supply current	no outputs loaded					
pin 3		I_{CC1}	12	20	28	mA
pin 16		I_{CC2}	0.7	1.0	1.3	mA
I^2C-bus inputs (SDA; SCL)						
Input voltage HIGH		V_{IH}	3.0	−	5.0	V
Input voltage LOW		V_{IL}	−0.3	−	1.5	V
Input current HIGH		I_{IH}	−	−	10	μA
Input current LOW		I_{IL}	−	−	10	μA
SDA output	open collector					
Output voltage LOW	$I_{OL} = 3.0$ mA	V_{OL}	−	−	0.4	V
AS input						
Input voltage HIGH		V_{IH}	3.0	−	5.0	V
Input voltage LOW		V_{IL}	−0.3	−	1.0	V
Input current HIGH		I_{IH}	−	−	10	μA
Input current LOW		I_{IL}	−	−	10	μA
RF input (AM; FM)						
Max. input frequency on AM_I		f_{iAM}	30	−	−	MHz
Min. input frequency on AM_I		f_{iAM}	−	−	0.512	MHz
Max. input frequency on FM_I		f_{iFM}	150	−	−	MHz
Min. input frequency on FM_I		f_{iFM}	−	−	30	MHz
Input voltage on AM_I (RMS value)	$V_{iFM} = 0$ V measured in Fig.4	$V_{iAM(rms)}$	30	−	500	mV
Input impedance AM_I						
resistance		R_{AM}	−	5.9	−	kΩ
capacitance		C_{AM}	−	2	−	pF

parameter	conditions	symbol	min.	typ.	max.	unit
RF input (continued)						
Input voltage on FM_I (RMS value)	V_{iAM} = 0 V measured in Fig.4	$V_{iFM(rms)}$	20	–	300	mV
Input impedance FM_I						
resistance		R_{FM}	–	3.6	–	kΩ
capacitance		C_{FM}	–	2	–	pF
Oscillator (XTAL1; XTAL2)						
Crystal resonance resistance (4 MHz)	see Fig.5	R_{XTAL}	–	–	150	Ω
Programmable charge pump						
Output current to loop filter						
bit CP = logic 0		I_{chp}	3	5	7	µA
bit CP = logic 1		I_{chp}	400	500	600	µA
Ripple rejection	f_{ripple} = 100 Hz					
20 log $\Delta V_{CC1}/\Delta V_O$		RR	40	50	–	dB
20 log $\Delta V_{CC2}/\Delta V_O$		RR	40	50	–	dB
Bandswitch output (pin 8)						
Output voltage HIGH		V_{OH}	–	–	12	V
Output voltage LOW	I_{OL} = 3 mA	V_{OL}	–	–	0.8	V
Output leakage current	V_{OH} = 12 V	I_{LO}	–	–	10	µA
Reference frequency output (pin 9)						
Output frequency	4 MHz crystal	f_{ref}	–	40	–	kHz
Output voltage HIGH	I_{source} = 5 µA	V_{OH}	1.2	1.4	1.7	V
Output voltage LOW		V_{OL}	–	0.1	0.2	V
Tuning voltage amplifier outputs						
AM output (pin 15)						
max. output voltage	I_{source} = 0.5 mA	$V_{O(max)}$	V_{CC2} −1.5	–	–	V
min. output voltage	I_{sink} = 1 mA	$V_{O(min)}$	–	–	0.8	V
max. output source current		I_{source}	0.5	–	–	mA
max. output sink current		I_{sink}	1.0	–	–	mA
FM output (pin 13)						
max. output voltage	I_{source} = 0.5 mA	$V_{O(max)}$	V_{CC2} −1.5	–	–	V
min. output voltage	I_{sink} = 1 mA	$V_{O(min)}$	–	–	0.8	V
max. output source current		I_{source}	0.5	–	–	mA
max. output sink current		I_{sink}	1.0	–	–	mA
Impedance of switched off output		$Z_{O(off)}$	5	–	–	MΩ
Input bias current (absolute value)		I_{bias}	–	1	5	nA

SENSITIVITY MEASUREMENT

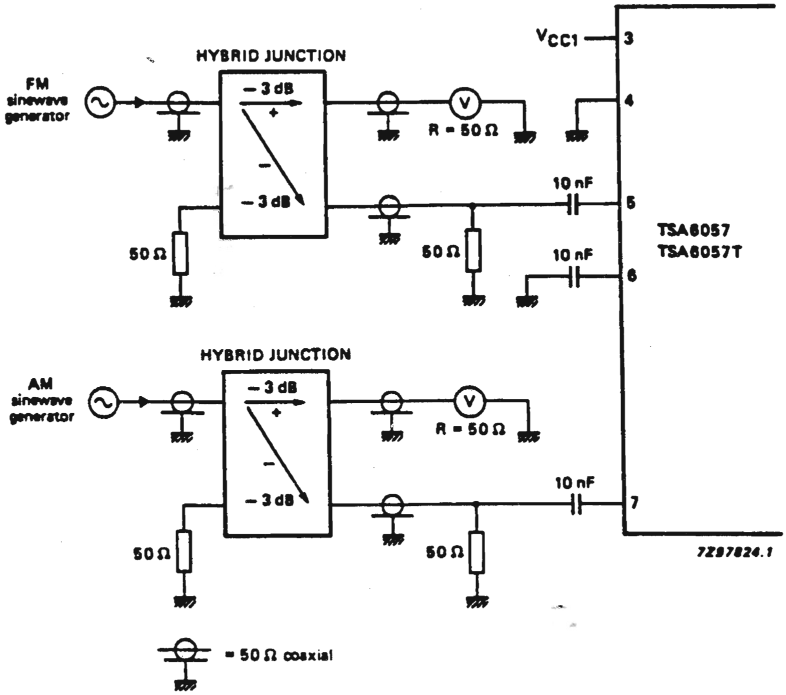


Fig.4 Prescaler input sensitivity.

APPLICATION INFORMATION

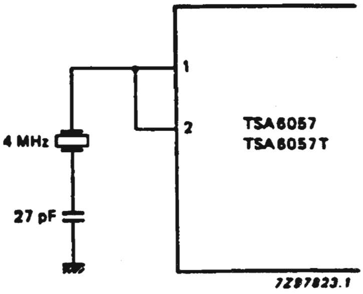


Fig.5 Crystal connection (4 MHz).

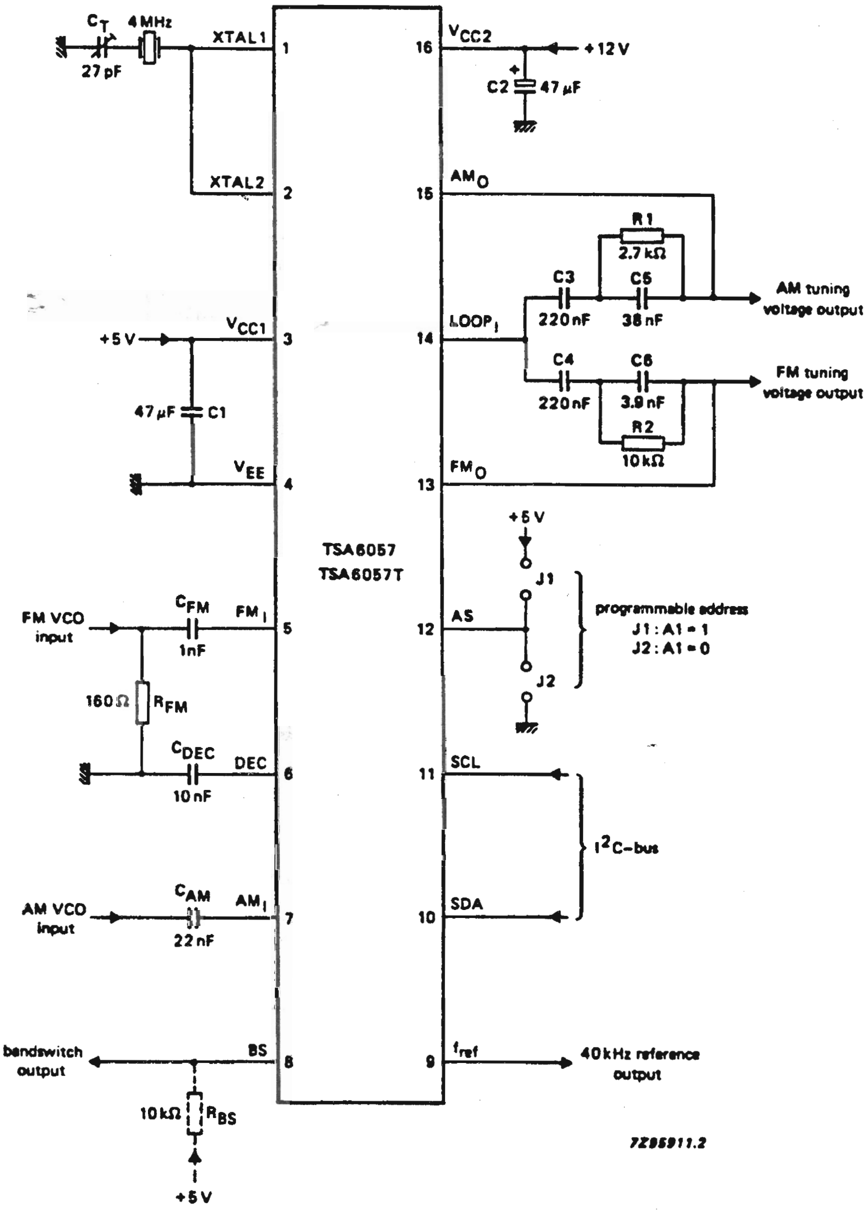


Fig.6 Application diagram

1.3GHz bi-directional I^2C bus controlled synthesizer TSA5511

FEATURES

- Complete 1.3 GHz single chip system
- Low power 5 V, 35 mA
- I^2C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- Address selection for Picture-In-Picture (PIP), DBS tuner
- Analog-to-digital converter
- 8 bus controlled ports (5 for TSA5511T), 4 open collector outputs (bi-directional)
- Power-down flag

APPLICATIONS

- TV tuners
- VCR Tuners

DESCRIPTION

The TSA5511 is a single chip PLL frequency synthesizer designed for TV tuning systems. Control data is entered via the I^2C-bus; five serial bytes are required to address the device, select the oscillator frequency, programme the eight output ports and set the charge-pump current. Four of these ports can also be used as input ports (three general purpose I/O ports, one ADC). Digital information concerning those ports can be read out of the TSA5511 on the SDA line (one status byte) during a READ operation. A flag is set when the loop is "in-lock" and is read during a READ operation. The device has one fixed I^2C-bus address and 3 programmable addresses, programmed by applying a specific voltage on Port 3. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	–	5	–	V
I_{CC}	supply current	–	35	–	mA
Δf	frequency range	64	–	1300	MHz
V_I	input voltage level				
	80 MHz to 150 MHz	12	–	300	mV
	150 MHz to 1 GHz	9	–	300	mV
	1 GHz to 1.3 GHz	40	–	300	mV
f_{XTAL}	crystal oscillator	3.2	4	4.48	MHz
I_O	open–collector output current	10	–	–	mA
I_O	current–limited output current	–	1	–	mA
T_{amb}	operating ambient temperature range	–10	–	80	°C
T_{stg}	storage temperature range (IC)	–40	–	150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA5511	18	DIL	plastic	SOT102
TSA5511T	16	SO	plastic	SOT109
TSA5511AT	20	SO	plastic	SOT163

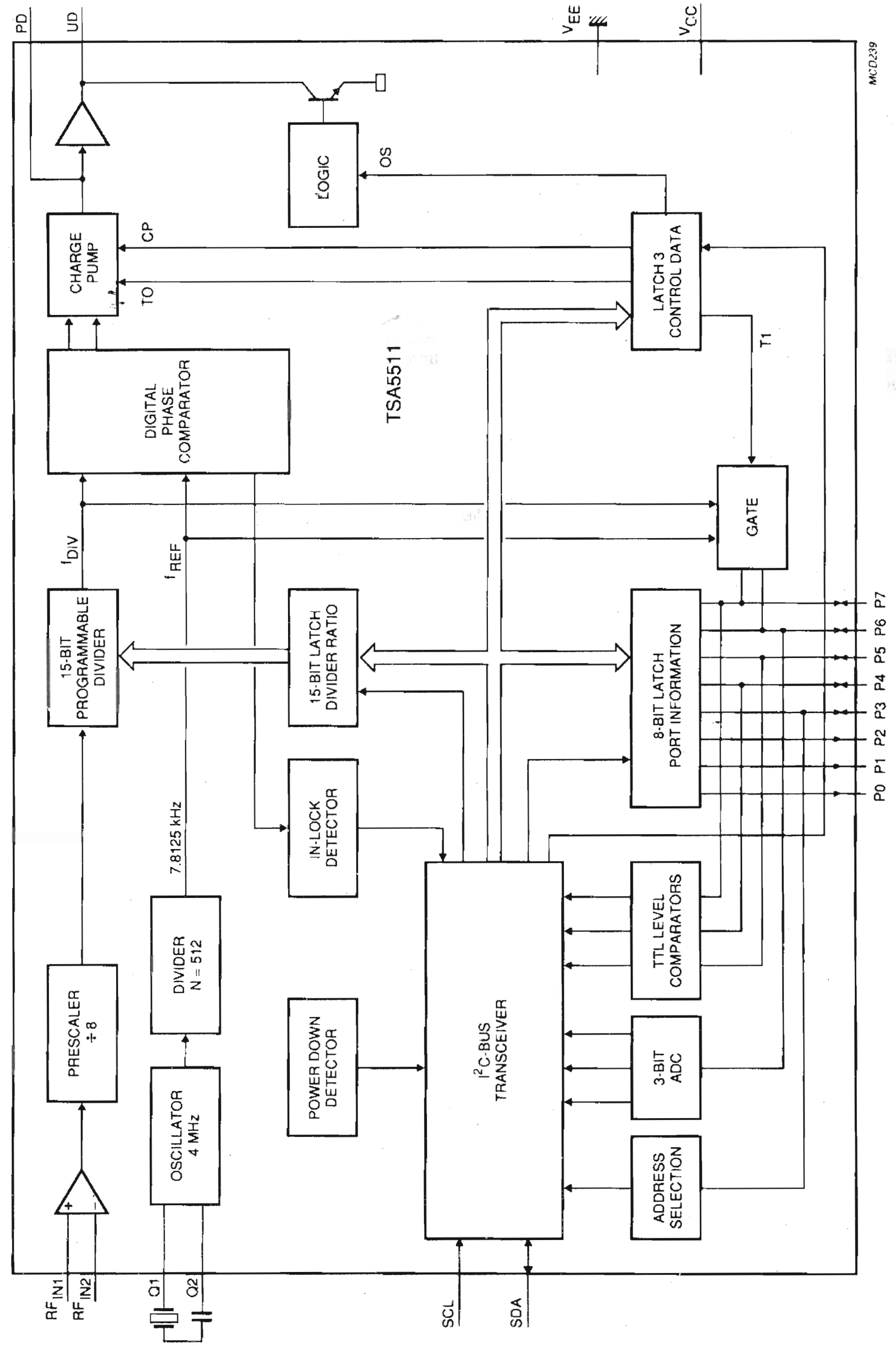


Fig.1 Block diagram.

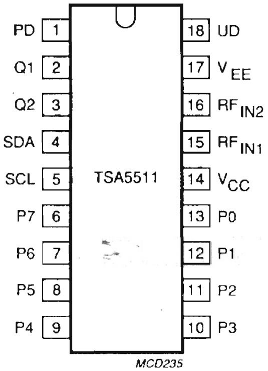


Fig.2 Pin configuration (SOT102).

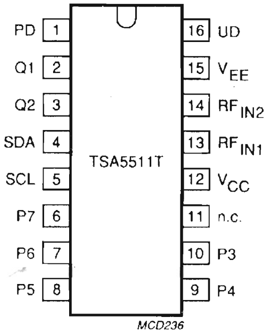


Fig.3 Pin configuration (SOT109).

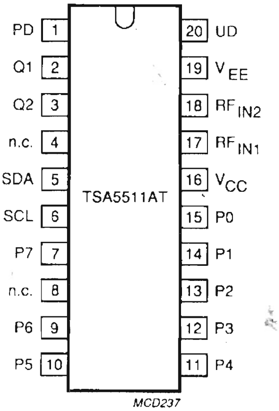


Fig.4 Pin configuration (SOT163).

PINNING

SYMBOL	PIN DIL 18	PIN SO16	PIN SO20	DESCRIPTION
PD	1	1	1	charge-pump output
Q1	2	2	2	crystal oscillator input 1
Q2	3	3	3	crystal oscillator input 2
n.c.			4	not connected
SDA	4	4	5	serial data input/output
SCL	5	5	6	serial clock input
P7	6	6	7	port output/input (general purpose)
n.c.			8	not connected
P6	7	7	9	port output/input for general purpose ADC
P5	8	8	10	port output/input (general purpose)
P4	9	9	11	port output/input (general purpose)
P3	10	10	12	port output/input for address selection
P2	11		13	port output
n.c.		11		not connected
P1	12		14	port output
P0	13		15	port output
V$_{CC}$	14	12	16	voltage supply
RF$_{IN1}$	15	13	17	UHF/VHF signal input 1
RF$_{IN2}$	16	14	18	UHF/VHF signal input 2 (decoupled)
V$_{EE}$	17	15	19	GND
UD	18	16	20	drive output

FUNCTIONAL DESCRIPTION

The TSA5511 is controlled via the two-wire I^{2}C-bus. For programming, there is one module address (7 bits) and the R/$\overline{W}$ bit for selecting READ or WRITE mode.

WRITE mode : R/$\overline{W}$ = 0 (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are needed to fully program the TSA5511. The bus transceiver has an auto-increment facility which permits the programming of the TSA5511 within one single transmission (address + 4 data bytes).

The TSA5511 can also be partially programmed on the condition that the first data byte following the address is byte 2 or byte 4. The meaning of the bits in the data bytes is given in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge pump and port information (first bit = 1) will follow. Until an I^{2}C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning or AFC purpose. At power-on the ports are set to the high impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz crystal oscillator by 512. Because the input of UHF/VHF signal is first divided by 8 the step size is 62.5 kHz. A 3.2 MHz crystal can offer step sizes of 50 kHz.

Table 1 Write data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	byte 1
Programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
Programmable divider	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
Charge-pump and test bits	1	CP	T1	T0	1	1	1	OS	A	byte 4
Output ports control bits	P7	P6	P5	P4	P3	P2*	P1*	P0*	A	byte 5

note

* not valid for TSA5511T.

MA1, MA0 programmable address bits (see Table 4)

A acknowledge bit

$N = N14 \times 2^{14} + N13 \times 2^{13} + \ldots + N1 \times 2^{1} + N0$

CP charge-pump current

CP = 0 50 μA

CP = 1 220 μA

P3 to P0 = 1 limited-current output is active

P7 to P4 = 1 open-collector output is active

P7 to P0 = 0 output are in high impedance state

T1 = 1 P6 = f_{ref}, P7 = f_{DIV}

T0 = 1 3-state charge-pump

OS = 1 operational amplifier output is switched off (varicap drive disable)

FUNCTIONAL DESCRIPTION (continued)

READ mode : R/$\overline{W}$ = 1 (see Table 2)

Data can be read out of the TSA5511 by setting the R/$\overline{W}$ bit to 1. After the slave address has been recognized, the TSA5511 generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a high position of the SCL clock signal.

A second data byte can be read out of the TSA5511 if the processor generates an acknowledge on the SDA line. End of transmission will occur if no acknowledge from the processor occurs.

The TSA5511 will then release the data line to allow the processor to generate a STOP condition.

When ports P3 to P7 are used as inputs, they must be programmed in their high-impedance state.

The POR flag (power-on-reset) is set to 1 when V_{CC} goes below 3 V and at power-on. It is reset when an end of data is detected by the TSA5511 (end of a READ sequence).

Control of the loop is made possible with the in-lock flag FL which indicates (FL = 1) when the loop is phase-locked. The bits I2, I1 and I0 represent the status of the I/O ports P7, P5 and P4 respectively. A logic 0 indicates a LOW level and a logic 1 a HIGH level (TTL levels).

A built-in 5-level ADC is available on I/O port P6. This converter can be used to feed AFC information to the controller from the IF section of the television as illustrated in the typical application circuit in Fig. 5. The relationship between bits A2, A1 and A0 and the input voltage on port P6 is given in Table 3.

Table 2 Read data format

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	1	A	byte 1
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	–	byte 2

POR	power-on-reset flag. (POR = 1 on power-on)
FL	in-lock flag (FL = 1 when the loop is phase-locked)
I2, I1, I0	digital information for I/O ports P7, P5 and P4 respectively
A2, A1, A0	digital outputs of the 5-level ADC. Accuracy is 1/2 LSB (see Table 3)

MSB is transmitted first.

Address selection

The module address contains programmable address bits (MA1 and MA0) which together with the I/O port P3 offers the possibility of having several synthesizers (up to 3) in one system.

The relationship between MA1 and MA0 and the input voltage I/O port P3 is given in Table 4.

Table 3 A/D converter levels

Voltage applied on the port P6	A2	A1	A0
0.6 V_{CC} to 13.5 V	1	0	0
0.45 V_{CC} to 0.6 V_{CC}	0	1	1
0.3 V_{CC} to 0.45 V_{CC}	0	1	0
0.15 V_{CC} to 0.3 V_{CC}	0	0	1
0 to 0.15 V	0	0	0

Table 4 Address selection

MA1	MA0	Voltage applied on port P3
0	0	0 to 0.1 V_{CC}
0	1	always valid
1	0	0.4 to 0.6 V_{CC}
1	1	0.9 V_{CC} to 13.5 V

LIMITING VALUES

In accordance with Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.3	6	V
V_1	charge-pump output voltage	–0.3	V_{CC}	V
V_2	crystal (Q1) input voltage	–0.3	V_{CC}	V
V_4	serial data input/output	–0.3	6	V
V_5	serial clock input	–0.3	6	V
V_{6-13}	P7 to P1 I/O voltage	–0.3	+16	V
V_{15}	prescaler input	–0.3	V_{CC}	V
V_{18}	drive output voltage	–0.3	V_{CC}	V
I_6	P7 to P0 output current (open collector)	–1	15	mA
I_4	SDA output current (open collector)	–1	5	mA
T_{stg}	storage temperature range (IC)	–40	+150	°C
T_j	maximum junction temperature		150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air (DIL18)	-	80	K/W
	from junction to ambient in free air (SO16)	-	110	K/W
	from junction to ambient in free air (SO20)	-	80	K/W

CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified
All pin numbers refer to DIL 18 version

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Functional range						
V_{CC}	supply voltage range		4.5	–	5.5	V
T_{amb}	operating ambient temperature range		−10	–	80	°C
f_{CLK}	clock input frequency		64	–	1300	MHz
N	divider		256	–	32767	
I_{CC}	supply current		25	35	50	mA
f_{XTAL}	crystal oscillator		3.2	4	4.48	MHz
Z_I	input impedance (pin 2)		−480	−400	−320	Ω
	input level	V_{CC} = 4.5 V to 5.5 V; T_{amb} = −10 to 80 °C; see typical sensitivity curve in Fig. 6				
	f = 80 to 150 MHz		12/−25	–	300/2.6	mV/dBm
	f = 150 to 1000 MHz		9/−28	–	300/2.6	mV/dBm
	f = 1000 to 1300 MHz		40/−15	–	300/2.6	mV/dBm
R_I	prescaler input resistance see SMITH chart in Fig. 7		–	50	–	Ω
C_I	input capacitance		–	2	–	pF
Output ports (current-limited) P0-P3						
I_{LO}	leakage current	V_{13} = 13.5 V	–	–	10	µA
I_{sink}	output sink current	V_{13} = 12 V	0.7	1.0	1.5	mA
Output ports (open collector) P4-P7 (see note 1)						
I_{LO}	leakage current	V_9 = 13.5 V	–	–	10	µA
V_{OL}	output voltage LOW	I_9 = 10 mA; note 2	–	–	0.7	V
Input P3						
I_{OH}	input current HIGH	V_{OH} = 13.5 V	–	–	10	µA
I_{OL}	input current LOW	V_{OL} = 0 V	−10	–	–	µA
Input ports P4-5, P7						
V_{IL}	input voltage LOW		–	–	0.8	V
V_{IH}	input voltage HIGH		2.7	–	–	V
I_{IH}	input current HIGH	V_6 = 13.5 V	–	–	10	µA
I_{IL}	input current LOW	V_6 = 0 V	−10	–	–	µA
Input port P6						
I_{IH}	input current HIGH	V_7 = 13.5 V	–	–	10	µA
I_{IL}	input current LOW	V_7 = 0 V	−10	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCL and SDA inputs						
V_{IH}	input voltage HIGH		3.0	–	5.5	V
V_{IL}	input voltage LOW		–	–	1.5	V
I_{IH}	input current HIGH	$V_5 = 5$ V, $V_{CC} = 0$ V; $V_5 = 5$ V, $V_{CC} = 5$ V	– –	– –	10 10	µA µA
I_{IL}	input current LOW	$V_5 = 0$ V, $V_{CC} = 0$ V; $V_5 = 0$ V, $V_{CC} = 5$ V	−10 −10	– –	– –	µA µA
Output SDA (open collector)						
I_{LO}	leakage current	$V_4 = 5.5$ V	–	–	10	µA
V_4	output voltage	$I_4 = 3$ mA	–	–	0.4	V
Charge-pump output PD						
I_{IH}	input current HIGH (absolute value)	CP = 1	90	220	300	µA
I_{IL}	input current LOW (absolute value)	CP = 0	22	50	75	µA
V_O	output voltage	in-lock	1.5	–	2.5	V
I_{1Leak}	off-state leakage current	T0 = 1	−5	–	5	nA
Operational amplifier output UD (test mode : T0 = 1)						
V_{18}	output voltage	$V_{IL} = 0$ V	–	–	100	mV
V_{18}	output voltage when switched-off	OS = 1; $V_{IL} = 2$ V	–	–	200	mV
G	operational amplifier current gain; $I_{18}/(I_1 - I_{1leak})$	OS = 0; $V_{1L} = 2$ V; $I_{18} = 10$ µA	2000	–	–	

Notes to the characteristics

1. When a port is active, the collector voltage must not exceed 6 V.
2. Measured with a single open-collector port active.

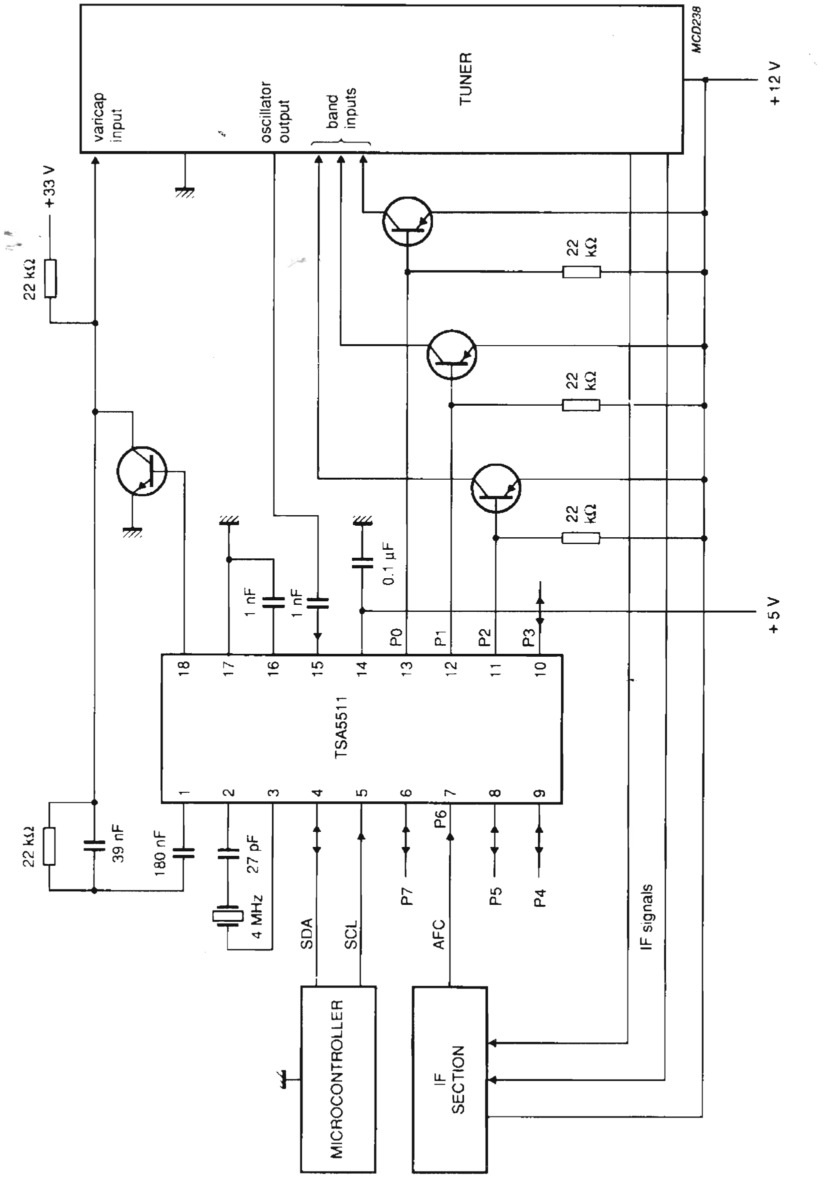


Fig.5 Typical application (DIL18).

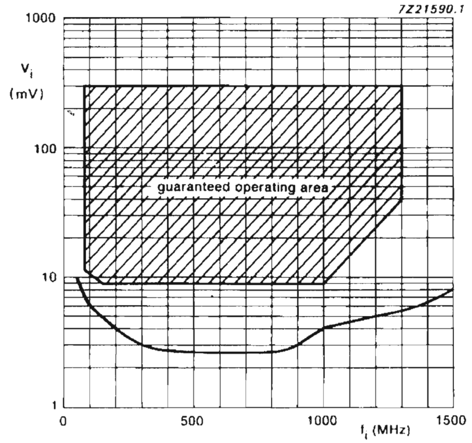


Fig.6 Prescaler typical input sensitivity curve; V_{CC} = 4.5 to 5.5 V; T_{amb} = –10 to +80 °C.

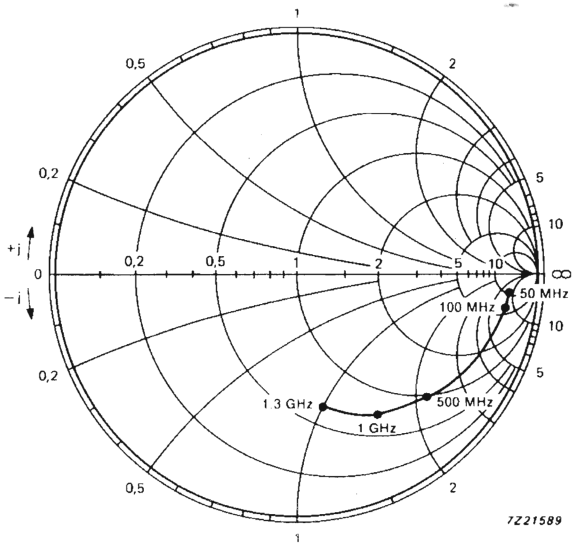


Fig.7 Prescaler Smith chart of typical input impedance; V_{CC} = 5 V; reference value = 50 Ω.

FLOCK FLAG DEFINITION (FL)

When the FL flag is 1, the maximum frequency deviation (Δf) from stable frequency can be expressed as follows:

$$\Delta f = \pm (K_{VCO} / K_O) \times I_{CP} \times (C1 + C2)/(C1 \times C2)$$

where:

K_{VCO} = oscillator slope (Hz/V)

I_{CP} = charge-pump current (A)

K_O = 4 x 10E6

C1 and C2 = loop filter capacitors

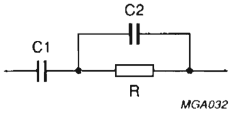


Fig.8 Loop filter.

FLOCK FLAG APPLICATION

- K_{VCO} = 16 MHz/V (UHF band)
- I_{CP} = 220 μA
- C1 = 180 nF
- C2 = 39 nF
- Δf = ± 27.5 kHz.

Table 5 Flock flag settings

	MIN.	MAX.	UNIT
Time span between actual phase lock and FL-flag setting	1024	1152	μs
Time span between the loop losing lock and FL-flag resetting	0	128	μs

Purchase of Philips I^{2}C components conveys a license under the Philips' I^{2}C patent to use the components in the I^{2}C system provided the system conforms to the I^{2}C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

Dual low-power frequency synthesizer UMA1005T

FEATURES

- Fast locking by 'Fractional-N' divider
- Auxiliary synthesizer
- Digital phase comparator with proportional and integral charge pump output
- High-speed serial input
- Low-power consumption
- Programmable charge pump currents
- Supply voltage range 2.9 to 5.5 V.

APPLICATIONS

- Mobile telephony
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1005T is a low-power, high-performance dual frequency synthesizer fabricated in CMOS technology. Fractional-N division with selectable modulo 5 or 8 is implemented in the main synthesizer.

The detectors and charge pumps are designated to achieve 10 to 5000 kHz channel spacing using fractional-N decreases the channel spacing by a factor 5 or 8. Together with an external standard 2, 3 or 4 ratio prescaler the main synthesizer can operate in the GHz frequency range.

Channel selection and programming is realized by a high-speed 3-wire serial interface.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1005T	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

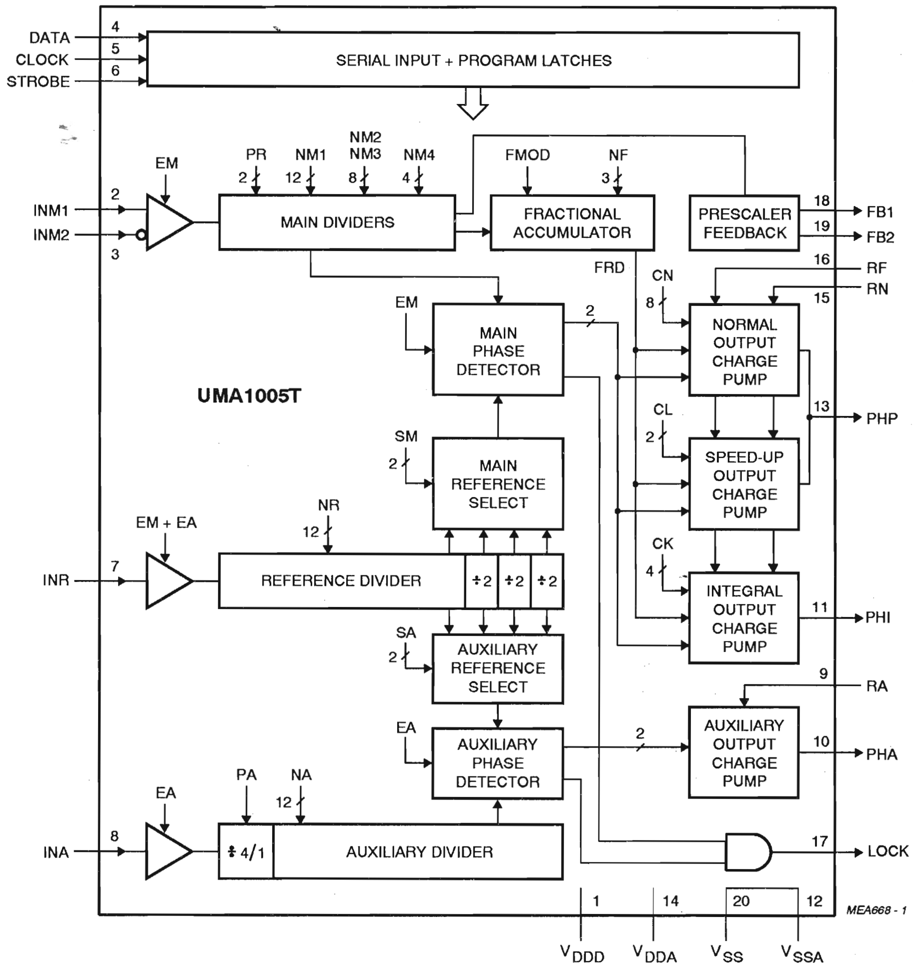


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DDD}	1	digital supply voltage
INM1	2	main divider positive input; rising edge active
INM2	3	main divider negative input; falling edge active
DATA	4	serial data input line
CLOCK	5	serial clock input line
STROBE	6	serial strobe input line
INR	7	reference divider input line; rising edge active
INA	8	auxiliary divider input line; rising edge active
RA	9	auxiliary current setting; resistor to V_{SS}
PHA	10	auxiliary phase detector output
PHI	11	integral phase detector output
V_{SSA}	12	analog ground; internally connected to V_{SS}
PHP	13	proportional phase detector output
V_{DDA}	14	analog supply voltage
RN	15	main current setting input; resistor to V_{SS}
RF	16	fractional compensation current setting input; resistor to V_{SS}
LOCK	17	lock detector output
FB1	18	feedback output 1 for prescaler modulus control
FB2	19	feedback output 2 for prescaler modulus control
V_{SS}	20	common ground connection

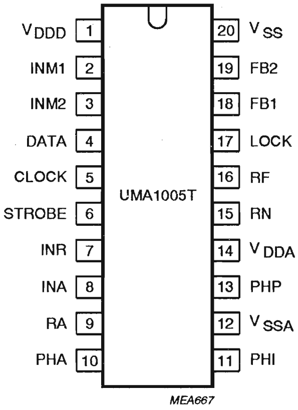


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Serial programming input

The serial input is a 3-wire input (CLOCK, STROBE and DATA) to program all counter ratios, DACs, selection and enable bits. The programming data is structured into 24 or 32-bit words. Each word includes 1 or 4 address bits. Figure 3 shows the timing diagram of the serial input. When the STROBE = LOW, the clock driver is enabled and on the positive edges of the CLOCK the signal on the DATA input is clocked into a shift register. When the STROBE = HIGH, the clock is disabled and the data in the shift register remains stable. Depending on the 1 or 4 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 4 words must be sent:

1. D word.
2. C word.
3. B word.
4. A word.

Figure 4 shows the format and the contents of each word. The E word is for testing purposes only. The E (test) word is reset when programming the D word. The data for NM4, CN and PR is stored by the B word temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the A word into the work registers which avoids false temporary main divider input. CN is only loaded from the temporary registers when a short 24-bit A0 word is used. CN will be directly loaded by programming a long 32-bit A1 word. The flag LONG in the D word determines whether A0 (LONG = 0) or A1 (LONG = 1) format is applicable.

The A word contains new data for the main divider. The A word is loaded only when a main divider synchronization signal is also active, to avoid phase jumps when reprogramming the main divider. The synchronization signal is generated by the main divider. It disables the loading of the A word each main divider cycle during maximum 300 main divider input cycles. To make sure that the A word will be correctly loaded the STROBE signal must be HIGH for at least 300 main divider input cycles. Programming the A word also means that the main charge pumps on outputs PHP and PHI are set into the speed-up mode as long as the STROBE remains HIGH.

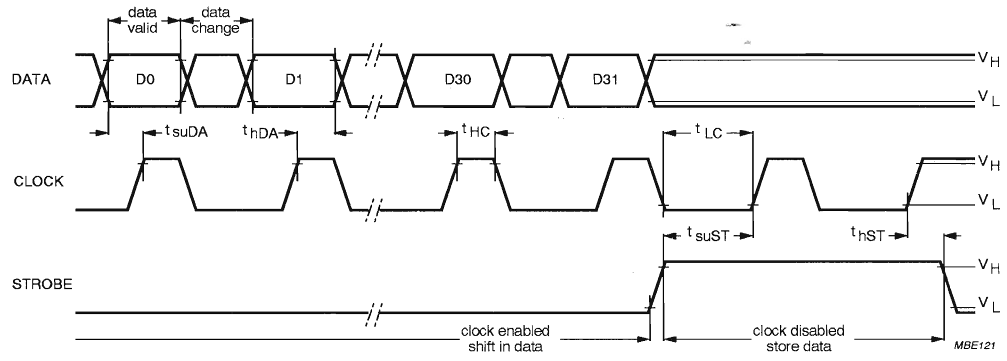


Fig.3 Serial input timing sequence.

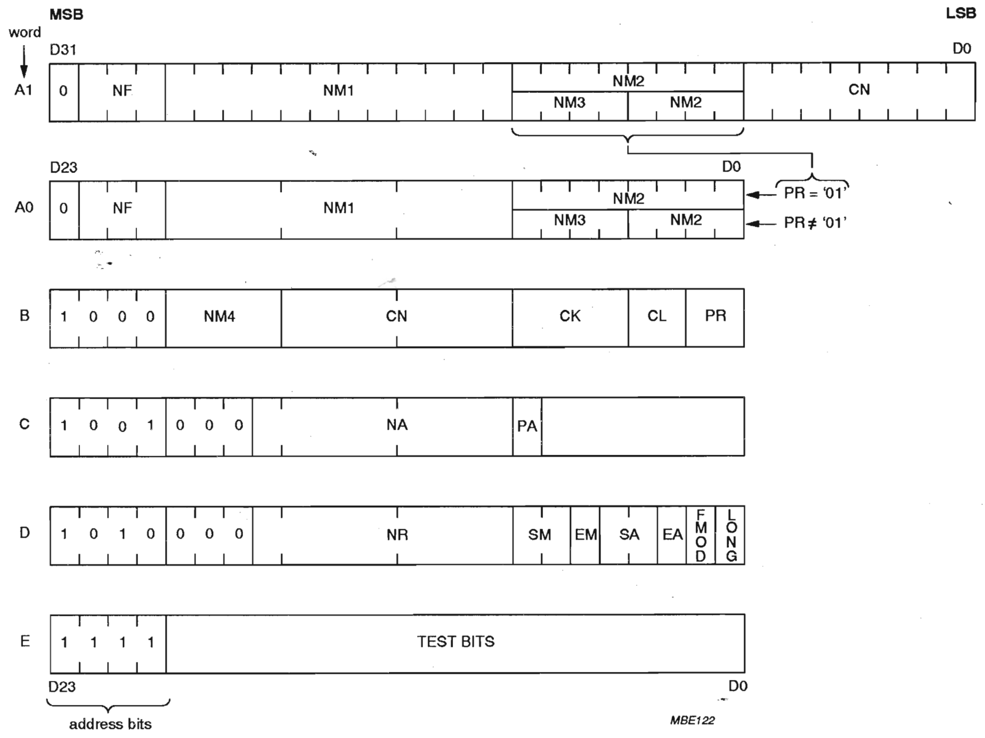


Fig.4 Serial input word format.

Table 1 Description of symbols used in Fig.4

SYMBOL	BITS(1)	FUNCTION
NM1	12	number of main divider cycles when prescaler is programmed in ratio R1 (FB1 = 1; FB2 = 0); note 2
NM2	8 if PR = 01 4 if PR ≠ 01	number of main divider cycles when prescaler is programmed in ratio R2 (FB1 = 0; FB2 = 0); note 2
NM3	4 if PR = 1X	number of main divider cycles when prescaler is programmed in ratio R3 (FB1 = 0; FB2 = 1); note 2
NM4	4 if PR = 11 or 00	number of main divider cycles when prescaler is programmed in ratio R4 (FB1 = 1; FB2 = 1); note 2
PR	2	prescaler type in use: PR = 01; modulus 2 prescaler PR = 10; modulus 3 prescaler PR = 11; modulus 4 prescaler PR = 00; modulus 4 prescaler (inhibit ratio 3)
NF	3	fractional-N increment
FMOD	1	fraction-N modulus selection flag: 1 = modulo 8 0 = modulo 5
LONG	1	A word format selection flag: 0 = 24-bit A0 format 1 = 32-bit A1 format
CN	8	binary current setting factor for main charge pumps
CL	2	binary acceleration factor for proportional charge pump current
CK	4	binary acceleration factor for integral charge pump current
EM	1	main divider enable flag
EA	1	auxiliary divider enable flag
SM	2	reference select for main phase detector
SA	2	reference select for auxiliary phase detector
NR	9	reference divider ratio
NA	9	auxiliary divider ratio
PA	1	auxiliary prescaler mode: PA = 0; divide-by-4 PA = 1; divide-by-1

Notes

1. X = don't care.
2. Not including reset cycles and fractional-N effects.

Auxiliary variable divider

The input signal on INA is amplified to a logic level by a single ended input buffer, which accepts LOW level AC coupled input signals. This input stage is enabled if the serial control bit EA = 1. Disabling means that all currents in the input stage are switched off. A fixed divide by 4 is enabled if PA = 0. This divider has been optimized to accept a high-frequency (90 MHz at a supply voltage range of 4.75 to 5.5 V) input signal. If PA = 1 this divider is disabled and the input signal is fed directly to the second stage, which is a 9-bit programmable divider with standard input frequency (30 MHz). The division ratio can be expressed as:

If PA = 0; N = 4 × NA.

If PA = 1; N = NA; with NA = 4 to 511.

Reference variable divider (Fig.5)

The input signal on INR is amplified to a logic level by a single ended input buffer, which accepts LOW level AC coupled input signals. This input stage is enabled by the OR function of the serial input bits EA and EM. Disabling means that all currents in the input stage are switched off. The reference divider consists of a programmable divider by NR (NR = 4 to 511) followed by a 3-bit binary counter. The 2-bit SM determines which of the 4 output pulses is selected as main phase detector input. The 2-bit SA determines the selection of the auxiliary phase detector signal. To obtain the best time spacing for the main and auxiliary reference signals, the opposite output will be used for the auxiliary phase detector, reducing the possibility of unwanted interactions. For this reason the programmable divider produces a symmetric output pulse for even ratios and a 1 input cycle asymmetric pulse for odd ratios.

Main variable divider

The input signals on INM1 and INM2 are amplified to a logic level by a balanced input comparator giving a common mode rejection. This input stage is enabled when serial control bit EM = 1. Disabling means that all currents in the comparator are switched off. The main divider is built-up by a 12-bit counter plus a sign bit. Depending on the serial input values of NM1, NM2, NM3, NM4 and the prescaler select PR, the counter will select a prescaler ratio during a number of input cycles in accordance with the information in Table 2.

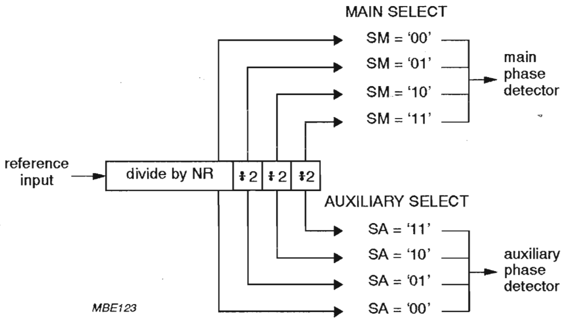


Fig.5 Reference variable divider.

Table 2 Selection of prescaler ratio

COUNTER STATUS	FB1	FB2	PRESCALER RATIO(1)
(–NM1 – 1) to 0	1	0	R1
(–NM1 – 1) to –1	1	0	R1(2)
1 to NM2	0	0	R2
0 to NM2	0	0	R2(2)
0 to NM3	0	1	R3; if PR = 1X
0 to NM4	1	1	R4; if PR = 11 or 00

Notes

1. X = don't care.
2. When the fractional accumulator overflows.

The total division ratio from prescaler to the phase detector expressions are given in Table 3.

Table 3 Total division from prescaler to phase detector expressions

CONDITION	EXPRESSION
PR = 01	N = (NM1 + 2) × R1 + NM2 × R2
	N′ = (NM1 + 1) × R1 + (NM2 + 1) × R2; note 1
PR = 10	N = (NM1 + 2) × R1 + NM2 × R2 + (NM3 + 1) × R3
	N′ = (NM1 + 1) × R1 + (NM2 + 1) × R2 + (NM3 + 1) × R3; note 1
PR = 11	N = (NM1 + 2) × R1 + NM2 × R2 + (NM3 + 1) × R3 + (NM4 + 1) × R4
	N′ = (NM1 + 1) × R1 + (NM2 + 1) × R2 + (NM3 + 1) × R3 + (NM4 + 1) × R4; note 1
PR = 00	N = (NM1 + 2) × R1 + NM2 × R2 + (NM4 + 1) × R4
	N′ = (NM1 + 1) × R1 + (NM2 + 1) × R2 + (NM4 + 1) × R4; note 1

Note

1. When the fractional accumulator overflows.

When the prescaler ratio is R2 = R1 + 1 the total division ratio N′ = N + 1.

Table 4 Modulus prescaler

PR	MODULUS PRESCALER	BIT CAPACITY			
		NM1	NM2	NM3	NM4
00	4	12	4	–	4
01	2	12	8	–	–
10	3	12	4	4	–
11	4	12	4	4	4

The loading of the work registers NM1, NM2, NM3, NM4 and PR is synchronized with the state of the main counter, to avoid extra phase disturbance when switching over to another main divider ratio as is explained in Section "Serial programming input".

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also the fractional accumulator is incremented with NF. The accumulator works modulo Q. Q is preset by the serial control bit FMOD to 8 when FMOD = 1. Each time the accumulator overflows, the feedback to the prescaler will select one cycle using prescaler ratio R2 instead of R1.

As shown above, this will increase the overall division ratio by 1 if R2 = R1 + 1. The mean division ratio over Q main divider cycles will then be: $NQ = N + \frac{NF}{Q}$

Programming a fraction means the prescaler with main divider will divide by N or N + 1.

The output of the main divider will be modulated with a fractional phase ripple. This phase ripple is proportional to the contents of the fractional accumulator FRD, which is used for fractional current compensation.

Phase detectors (Fig.6)

The auxiliary and main phase detectors are a 2 D-type flip-flop phase and frequency detector. The flip-flops are set by the negative edges of output signals of the dividers. The reset inputs are activated when both flip-flops have been set and when the reset enable signal is active (LOW). Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or dead band around zero phase error. The flip-flops drive on-chip charge pumps. A pull-up current from the charge pump indicates that the VCO frequency shall be increased while a pull-down pulse indicates that the VCO frequency shall be decreased.

Current settings

The UMA1005T has 3 current setting pins RA, RN and RF. The active charge pump currents and the fractional compensation currents are linearly dependent on the current in the current setting pins. This current I_R can be set by an external resistor to be connected between the current setting pin (pin 9) and V_{SS}. The typical value for R (current setting resistor) can be calculated with the equation:

$$R = \frac{(V_{DDA} - 0.5) - 237\sqrt{I_R}}{I_R}$$

The current can be set to zero by connecting the corresponding pin to V_{DDA}.

Auxiliary output charge pumps

The auxiliary charge pumps on pin PHA are driven by the auxiliary phase detector and the current value is determined by the external resistor (R_{ext}) at pin RA. The active charge pump current is typically: $|I_{PHA}| = 8 \times I_{RA}$.

Main output charge pumps and fractional compensation currents

The main charge pumps on pins PHP and PHI are driven by the main phase detector and the current value is determined by the current at pin RN and via a number of DACs which are driven by registers of the serial input. The fractional compensation current is determined by the current at pin RF, the contents of the fractional accumulator FRD and a number of DACs driven by registers from the serial input. The timing for the fractional compensation is derived from the reference divider. The current is on during 1 input reference cycle before and 1 cycle after the output signal to the phase comparator. Figure 7 shows the waveforms for a typical case.

When the serial input A word is loaded, the output circuits are in the 'speed-up mode' as long as the STROBE is HIGH, else the 'normal mode' is active.

NORMAL MODE

In the 'normal mode' the current output at PHP is: $I_{PHP(N)} = I_{pump10} + I_{comp10}$.

Where:

$$|I_{pump10}| = \frac{CN \times I_{RN}}{29}$$; charge pump current.

$$I_{comp10} = \frac{FRD \times I_{RF}}{128}$$; fractional compensation current.

In 'normal mode' the current at output PHI is zero.

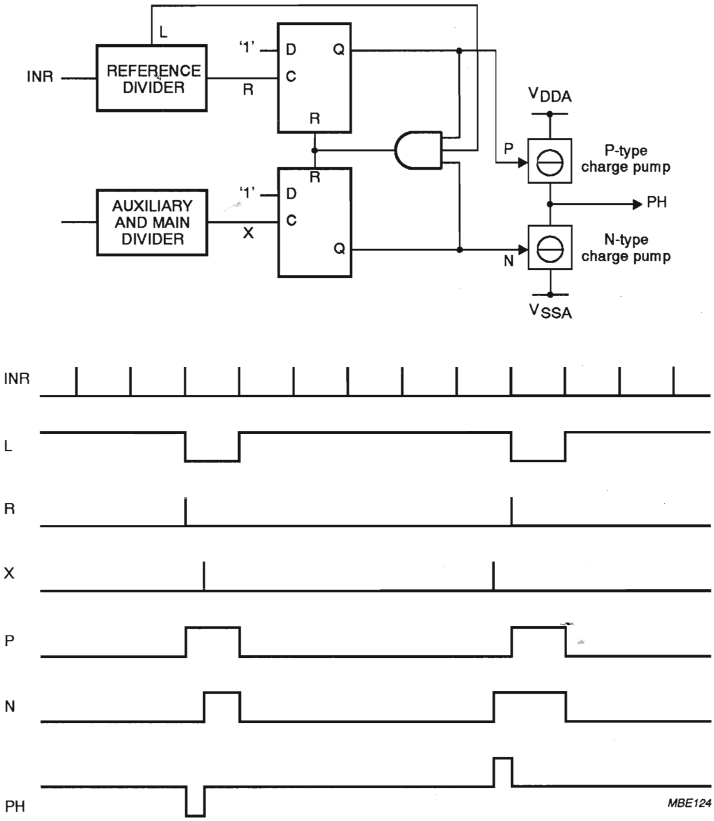


Fig.6 Phase detector structure with timing.

SPEED-UP MODE

In ‘speed-up mode’ the current in output PHP is:
$I_{PHP(S)} = I_{PHP(N)} + I_{pump11} + I_{comp11}$.

Where:

$I_{pump11} = I_{pump10} \times 2^{(CL+1)}$; charge pump current.

$I_{comp11} = I_{comp10} \times 2^{(CL+1)}$; fractional compensation current.

In ‘speed-up mode’ the current in output PHI is:
$I_{PHI(S)} = I_{pump21} + I_{comp21}$.

Where:

$I_{pump21} = I_{pump11} \times CK$; charge pump current.

$I_{comp21} = I_{comp11} \times CK$; fractional compensation current.

Figure 7 shows that for a proper fractional compensation the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output. This means that the current setting on the inputs RN and RF must have following ratio: $\frac{I_{RN}}{I_{RF}} = \frac{29 \times Q \times f_{VCO}}{64 \times CN \times f_{i(max)2}}$.

Where:

Q = fractional-N modulus.

$f_{VCO} = f_{i(max)1} \times N$; input frequency of the prescaler.

$f_{i(max)1}$ = maximum input frequency of the main divider (pins INM1 and INM2).

$f_{i(max)2}$ = maximum input frequency of the reference divider (pin INR).

Lock detect

The output LOCK is HIGH when the auxiliary phase detector and the main phase detector indicate a lock condition. The lock condition is defined as a phase difference of less than ±1 cycle on the reference input INR. The lock condition is also fulfilled when the relative counter is disabled (EM = 0 or EA = 0 respectively) for the main or auxiliary counter respectively.

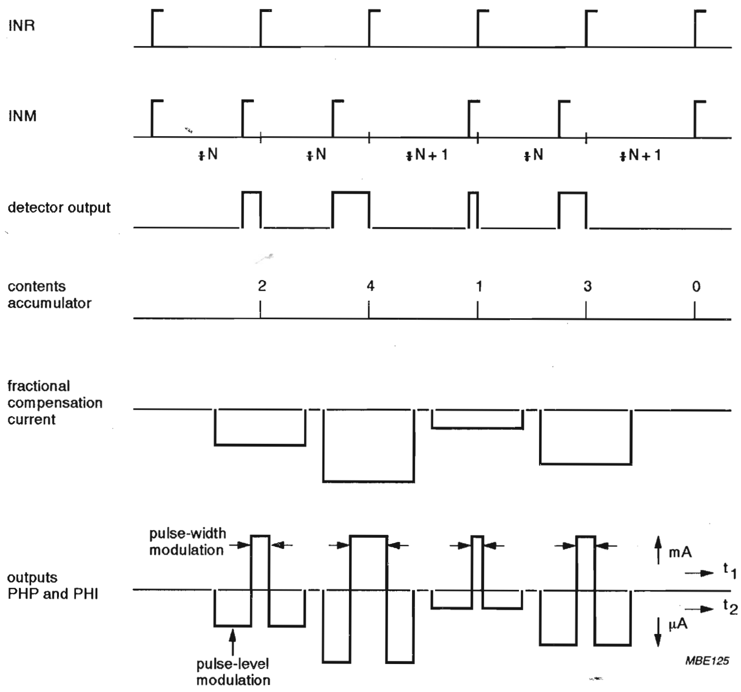


Fig.7 Waveforms for NF = 2 and fraction = 0.4.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	−0.5	6.5	V
V_{DDA}	analog supply voltage	−0.5	6.5	V
V_I	voltage on any input	−0.5	V_{DD} + 0.5	V
I_n	DC current into any input or output	−10	+10	mA
P_{tot}	total power dissipation	−	25	mW
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−40	+70	°C

DC CHARACTERISTICS

$V_{DDD} = V_{DDA} = 2.9$ to 5.5 V; $T_{amb} = -40$ to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$I_{DDD(stb)}$	digital standby supply current	EM = EA = 0; inputs on V_{DD} or 0	−	−	5	µA
I_{DDD}	operating digital supply current	note 1	−	−	5	mA
$I_{DDA(stb)}$	analog standby supply current	$V_{RA} = V_{DDA}$; $V_{RF} = V_{DDA}$; $V_{RN} = V_{DDA}$	−	−	10	µA
I_{DDA}	operating analog supply current	note 1	−	−	0.6	mA
Digital inputs CLK, DATA and STROBE						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	V_{DD}	V
V_{IL}	LOW level input voltage		0	−	$0.3V_{DD}$	V
Digital outputs FB1, FB2 and LOCK						
V_{OL}	LOW level output voltage	I_O = 2 mA; note 2	−	−	0.4	V
V_{OH}	HIGH level output voltage	I_O = −2 mA; note 2	V_{DD} − 0.4	−	−	V
Charge pump PHA						
$\lvert I_{PHA}\rvert$	output current	I_{RA} = −62.5 µA; $V_{PHA} = \frac{1}{2}V_{DD}$; note 2	400	500	600	µA
		I_{RA} = −25 µA; $V_{PHA} = \frac{1}{2}V_{DD}$	160	200	240	µA
$\frac{\Delta I_{PHA}}{\lvert I_{PHA}\rvert}$	relative output current variation	I_{RA} = −62.5 µA; notes 2 and 3	−	2	6	%
$\Delta I_{PHA\,M}$	output current matching	I_{RA} = −62.5 µA; $V_{PHA} = \frac{1}{2}V_{DD}$; notes 2 and 4	−	−	±50	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Charge pump PHP; normal mode (notes 5, 6 and 7); $\mathbf{V_{RF} = V_{DD}}$						
$\lvert I_{PHP(N)} \rvert$	output current	$I_{RN} = -62.5$ μA; $V_{PHP} = \frac{1}{2}V_{DD}$; note 2	440	550	660	μA
		$I_{RN} = -25$ μA; $V_{PHP} = \frac{1}{2}V_{DD}$	175	220	265	μA
$\Delta I_{PHP(N)}$	relative output current variation	$I_{RN} = -62.5$ μA; note 3	–	2	6	%
$\Delta I_{PHP(N\ M)}$	output current matching	$I_{RN} = -62.5$ μA; $V_{PHP} = \frac{1}{2}V_{DD}$; notes 2 and 4	–	–	±50	μA
Charge pump PHP; speed-up mode (notes 5, 6 and 8); $\mathbf{V_{RF} = V_{DD}}$						
$\lvert I_{PHP(S)} \rvert$	output current	$I_{RN} = -62.5$ μA; $V_{PHP} = \frac{1}{2}V_{DD}$; note 2	2.20	2.75	3.30	mA
		$I_{RN} = -25$ μA; $V_{PHP} = \frac{1}{2}V_{DD}$	0.85	1.1	1.35	mA
$\Delta I_{PHP(S)}$	relative output current variation	$I_{RN} = -62.5$ μA; notes 2 and 3	–	2	6	%
$\Delta I_{PHP(S\ M)}$	output current matching	$I_{RN} = -62.5$ μA; $V_{PHP} = \frac{1}{2}V_{DD}$; notes 2 and 4	–	–	±250	μA
Charge pump PHI; speed-up mode (notes 5, 6 and 9); $\mathbf{V_{RF} = V_{DD}}$						
$\lvert I_{PHI(S)} \rvert$	output current	$I_{RN} = -62.5$ μA; $V_{PHI} = \frac{1}{2}V_{DD}$; note 2	4.4	5.5	6.6	mA
		$I_{RN} = -25$ μA; $V_{PHI} = \frac{1}{2}V_{DD}$	1.75	2.2	2.65	mA
$\Delta I_{PHI(S)}$	relative output current variation	$I_{RN} = -62.5$ μA; notes 2 and 3	–	2	8	%
$\Delta I_{PHI(S\ M)}$	output current matching	$I_{RN} = -62.5$ μA; $V_{PHI} = \frac{1}{2}V_{DD}$; notes 2 and 4	–	–	±500	μA
Fractional compensation PHP; normal mode (notes 5, 10 and 11); $\mathbf{V_{RN} = V_{DD}}$; $\mathbf{V_{PHP} = \frac{1}{2}V_{DD}}$						
$I_{PHP(F\ N)}$	fractional compensation output current PHP as a function of FRD	$I_{RF} = -62.5$ μA; FRD = 1 to 7; notes 2 and 12	−675	−500	−325	nA
		$I_{RF} = -25$ μA; FRD = 1 to 7; note 12	−270	−200	−130	nA
Fractional compensation PHP; speed-up mode (notes 5, 11 and 13); $\mathbf{V_{RN} = V_{DD}}$; $\mathbf{V_{PHP} = \frac{1}{2}V_{DD}}$						
$I_{PHP(F\ S)}$	fractional compensation output current PHP as a function of FRD	$I_{RN} = -62.5$ μA; FRD = 1 to 7; notes 2 and 12	−3.35	−2.50	−1.65	μA
		$I_{RN} = -25$ μA; FRD = 1 to 7; note 12	−1.35	−1.00	−0.65	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fractional compensation PHI; speed-up mode (notes 5, 11 and 14); $\mathbf{V_{RN} = V_{DD}}$; $\mathbf{V_{PHP} = \frac{1}{2}V_{DD}}$						
$I_{PHI(F)}$	fractional compensation output current PHI as a function of FRD	I_{RN} = −62.5 μA; FRD = 1 to 7; notes 2 and 12	−5.4	−4.0	−2.6	μA
		I_{RN} = −25 μA; FRD = 1 to 7; note 12	−2.15	−1.60	−1.05	μA
Charge pump leakage currents; charge pump not active						
$I_{PHP(LO)}$	output leakage current PHP	normal mode; V_{PHP} = 0.7 to V_{DDA} − 0.8 V note 5	−	10	750	nA
$I_{PHI(LO)}$	output leakage current PHI	normal mode; V_{PHI} = 0.7 to V_{DDA} − 0.8 V note 5	−	10	100	nA
$I_{PHA(LO)}$	output leakage current PHA	V_{PHA} = 0.7 to V_{DDA} − 0.8 V	−	10	750	nA

Notes

1. Operational conditions:
   a) Main and auxiliary divider enabled (EM = EA = 1).
   b) NA = 125.
   c) NR = 125.
   d) NM1 = 60.
   e) NM2 = 63.
   f) $f_{i(max)1} = f_{i(max)2}$ = 15 MHz.
   g) $f_{i(max)3}$ = 60 MHz.
   h) Lock condition.
   i) Normal mode; note 5
   j) $I_{RN} = I_{RF} = I_{RA}$ = 25 μA.
   k) CN = 255.
   l) PA = 0.
2. Limited supply voltage range 4.5 to 5.5 V.
3. The relative output current variation is defined as:

   $$\frac{\Delta I_O}{I_O} = 2 \times \frac{I_2 - I_1}{|I_2 + I_1|}$$; with V_1 = 0.7 V; $V_2 = V_{DD}$ − 0.8 V (see Fig.8).
4. The output current matching is measured when both (positive and negative current) sections of the output charge pumps are on.
5. When a serial ‘A’ word is programmed, the main charge pumps on PHP and PHI are in the ‘speed-up mode’ as long as STROBE = HIGH, otherwise the main charge pumps are in the ‘normal mode’.
6. Monotonicity is guaranteed with CN = 0 to 255.
7. Typical output current: $|I_{PHP(N)}| = -I_{RN} \times \frac{CN}{29}$; specification condition: CN = 255.

8. Typical output current: $\left|I_{PHP(S)}\right| = -I_{RN} \times CN \times \frac{2^{(CL+1)} + 1}{29}$; specification conditions:
   - a) CN = 255; CL = 1 or,
   - b) CN = 75; CL = 3.
9. Typical output current: $\left|I_{PHI}\right| = -I_{RN} \times CN \times 2^{(CL+1)} \times \frac{CK}{29}$; specification conditions:
   - a) CN = 160; CL = 3; CK = 1 or,
   - b) CN = 160; CL = 2; CK = 2 or,
   - c) CN = 160; CL = 1; CK = 4 or,
   - d) CN = 160; CL = 0; CK = 8.
10. Typical fractional compensation output current: $I_{PHP(F\,N)} = I_{RF} \times \frac{FRD}{128}$; specification condition: FRD = 1 to 7.
11. The compensation current specified does not include the leakage current of this output.
12. FRD is the value of the 3-bit fractional accumulator.
13. Typical fractional compensation output current: $I_{PHP(F\,S)} = I_{RF} \times FRD \times \frac{2^{(CL+1)} + 1}{128}$; specification conditions: FRD = 1 to 7; CL = 1.
14. Typical fractional compensation output current: $I_{PHI(F)} = I_{RF} \times FRD \times 2^{(CL+1)} \times \frac{CK}{128}$; specification conditions:
   - a) FRD = 1 to 7; CL = 1; CK = 2 or,
   - b) FRD = 1 to 7; CL = 2; CK = 1.

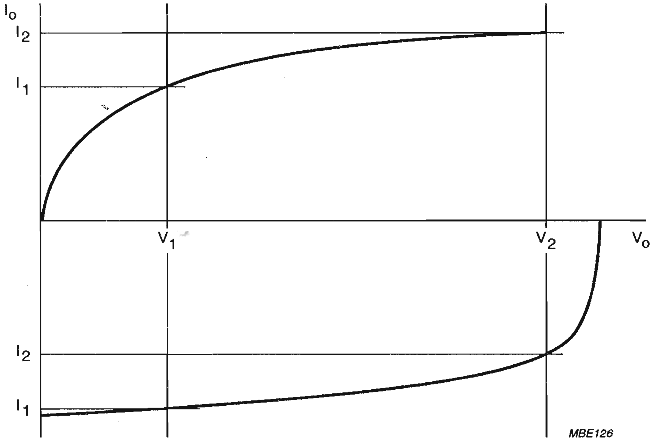


Fig.8 Relative output current variation.

AC CHARACTERISTICS

$V_{DDD} = V_{DDA} = 2.9$ to 5.5 V; $T_{amb} = -40$ to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Main divider (inputs INM1 and INM2)						
$f_{i(max)1}$	maximum input frequency		10	–	–	MHz
		note 1	30	–	–	MHz
$\Delta V_{INM(p-p)}$	differential input signal amplitude $V_{INM1} - V_{INM2}$ (peak-to-peak value)		600	–	–	mV
V_{CM}	common mode range for V_{INM1} and V_{INM2}		1	–	$V_{DD} - 1$	V
t_{pd}	propagation delay time from I_{NM1} and I_{NM2} to FB1 and FB2		–	–	60	ns
		note 1	–	18	30	ns
msr	mark-to-space ratio for differential input signals		35 : 65	–	65 : 35	
$Z_{i(min)}$	minimum input impedance	resistive; note 2	5	–	–	kΩ
		capacitive; note 2	–	–	5	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference divider (input INR)						
$f_{i(max)2}$	maximum input frequency		15	–	–	MHz
		note 1	30	–	–	MHz
$V_{i(p-p)}$	input signal amplitude AC coupled (peak-to-peak value)		300	–	–	mV
$Z_{i(min)}$	minimum input impedance	resistive; note 2	5	–	–	kΩ
		capacitive; note 2	–	–	5	pF
Auxiliary divider (input INA)						
$f_{i(max)3}$	maximum input frequency	prescaler enabled; PA = 0	35	–	–	MHz
		prescaler enabled; PA = 0; note 1	90	–	–	MHz
		prescaler disabled; PA = 1	15	–	–	MHz
		prescaler disabled; PA = 1; note 1	30	–	–	MHz
$V_{i(p-p)}$	input signal amplitude AC coupled (peak-to-peak value)		300	–	–	mV
$Z_{i(min)}$	minimum input impedance	resistive; note 2	5	–	–	kΩ
		capacitive; note 2	–	–	5	pF
Serial interface (inputs DATA, CLOCK and STROBE); see Fig.3						
f_{clk}	clock frequency		–	–	10	MHz
t_{HC}	clock HIGH time		30	–	–	ns
t_{LC}	clock LOW time		30	–	–	ns
t_{suDA}	DATA set-up time		30	–	–	ns
t_{hDA}	DATA hold time		30	–	–	ns
t_{suST}	STROBE set-up time		30	–	–	ns
t_{hST}	STROBE hold time		30	–	–	ns

Notes

1. Limited supply voltage range 4.5 to 5.5 V.
2. Periodically sampled; not 100% tested.

Low-power frequency synthesizer for mobile radio communications

UMA1014

FEATURES

- Single chip synthesizer; compatible with Philips cellular radio chipset
- Fully programmable RF divider
- I²C interface for two-line serial bus
- On-chip crystal oscillator/TCXO buffer from 3 to 16 MHz
- 16 reference division ratios allowing 5 to 100 kHz channel spacing
- 1/8 crystal frequency output
- On-chip out-of-lock indication
- Two extra VCO control outputs
- Latched synthesizer alarm output
- Status register including out-of-lock indication and power failure
- Power-down mode.

APPLICATIONS

- Cellular mobile radio (NMT, AMPS, TACS)
- Private mobile radio (PMR)
- Cordless telephones

GENERAL DESCRIPTION

The UMA1014 is a low-power universal synthesizer which has been designed for use in channelized radio communication. The IC is manufactured in bipolar technology and is designed to operate at 5 to 100 kHz channel spacing with an RF input from 50 to 1100 MHz. The channel is programmed via a standard I²C-bus. A low-power sensitive RF divider is incorporated together with a dead-zone eliminated, 3-state phase comparator. The low-noise charge pump delivers 1 mA or 1/2 mA output current to enable a better compromise between fast switching and loop bandwidth. A power-down circuit enables the synthesizer to be set to idle mode.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{CP}	supply voltage range	4.5	5.0	5.5	V
$I_{CC} + I_{CP}$	supply current	–	13	–	mA
I_{CCpd}	I_{CC} in power-down	–	2.5	–	mA
f_{ref}	phase comparator reference frequency	5	–	100	kHz
f_{RF}	RF input frequency	50	–	1100	MHz
T_{amb}	operating ambient temperature range	–40	–	85	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UMA1014T	16	SO16	plastic	SOT109A

Low-power frequency synthesizer for mobile radio communications

UMA1014

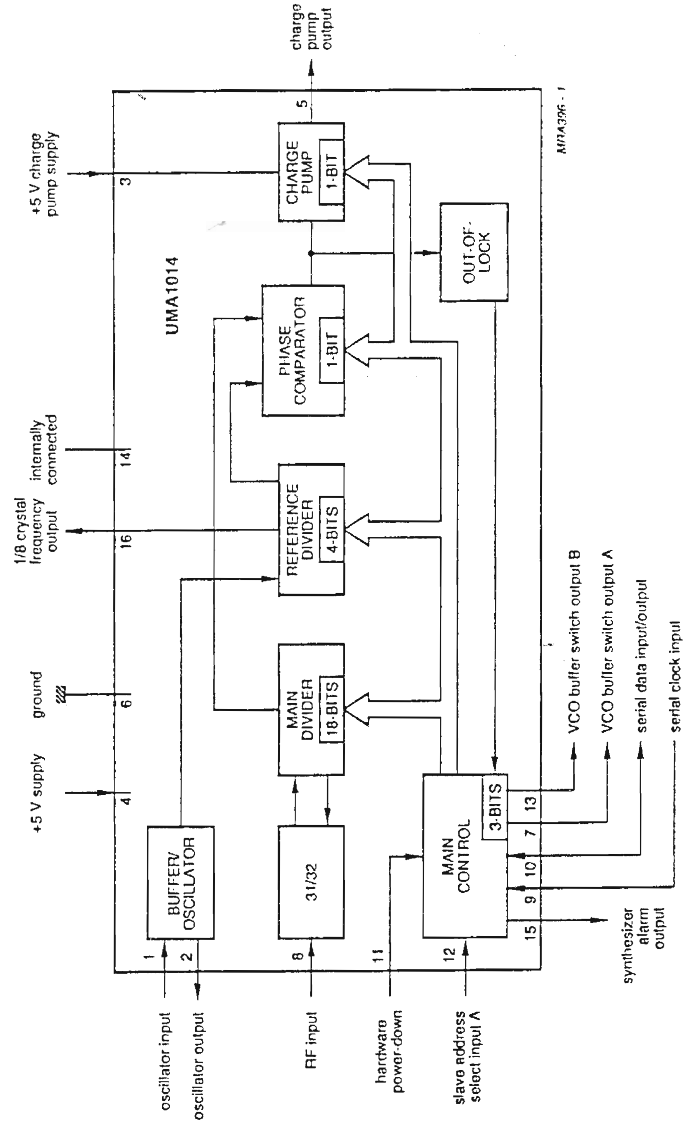


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCIN	1	oscillator or TCXO input
OSCOUT	2	oscillator output
V_{CP}	3	5 V charge pump supply
V_{CC}	4	5 V supply
PCD	5	charge pump output
GND	6	ground
VCOA	7	VCO buffer switch output A (including out-of-lock)
RF	8	RF input
SCL	9	serial clock input
SDA	10	serial data input/output
$\overline{\text{HPD}}$	11	hardware power-down (active LOW)
SAA	12	slave address select input A
VCOB	13	VCO buffer switch output B
i.c.	14	internally connected
SYA	15	synthesizer alarm output
FX8	16	1/8 crystal frequency output

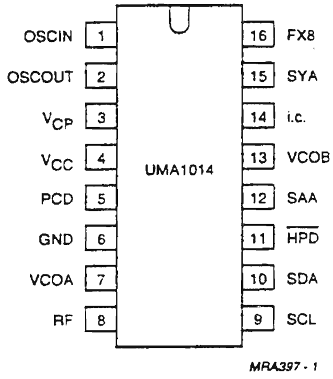


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The UMA1014 is a low-power frequency synthesizer for radio communication which operates in the 50 to 1100 MHz range. The device includes an oscillator/buffer circuit, a reference divider, an RF divider, a 3-state phase comparator, a charge pump and a main control circuit to transfer the serial data into the four internal 8-bit registers. The V_{CC} supply feeds the logic part, the V_{CP} supply feeds the charge-pump only. Both supplies are +5 V (±10%). The power-down facility puts the synthesizer in the idle mode (all current supplies are switched off except in the control part). This allows any I^{2}C transfer and all information in the registers is retained thus enabling fast power-up.

Main divider

The main divider is a pulse swallow type counter which is fully programmable. After a sensitive input amplifier (50 mV, −13 dBm), the RF signal is applied to a 31/32 duo-modulus counter. The output is then used as the clock for the 5-bit swallow counter R = (MD4 to MD0) and the 13-bit main counter N = (MD17 to MD5). The ratio is transferred via the I^{2}C-bus to the registers B, C and D, and then buffered in an 18-bit latch. The ratio in the divider chain is updated with the new information when the least significant bit is received (i.e. D0). This update is synchronized to the output of the divider in order to limit the phase error during small jumps of the synthesized frequency.

The main divider can be programmed to any value between 2048 and 262143 (i.e. $2^{18} - 1$). If ratio X, below 2048, is sent to the divider, the ratio (X + 2048) will be programmed. When it is required to switch between adjacent channels it is possible to program register D only, thus allowing shorter I^{2}C programming time.

Oscillator

The oscillator is a common collector Colpitts type with external capacitive feedback. The oscillator has very small temperature drift and high voltage supply rejection. A TCXO or other type of clock can be used to drive the oscillator by connecting the source (preferably AC-coupled) to pin 1 and leaving pin 2 open-circuit. The oscillator acts as a buffer in this mode and requires no additional external components. The signal from the clock source should have a minimum space width of 31 ns.

Reference divider

The reference divider is semi-programmable with 16 division ratios which can be selected via the I^{2}C-bus. The programming uses four bits of the register A (A3 to A0) as listed in Table 2. These ratios allow the use of a large number of crystal frequencies from 3 MHz up to 16 MHz. All main channel spacings can be obtained with a single crystal/TXCO frequency of 9.6 MHz.

Phase comparator

A diagram of the phase comparator and charge pump is illustrated in Fig.3.

The phase comparator is both a phase and frequency detector. The detector comprises dual flip-flops together with logic circuitry to eliminate the dead-zone. When a phase error is detected the UP or DOWN signal goes HIGH. This switches on the corresponding current generator which produces a source or sink current for the loop filter. When no phase error is detected PCD goes high impedance. The final tuning voltage for the VCO is provided by the loop filter. The charge pump current is programmable via the I^{2}C-bus. When IPCD (bit 5) is set to logic 1 the charge pump delivers 1 mA; when IPCD is set to logic 0 the charge pump delivers 0.5 mA.

The phase comparator has a phase inverter logic input (PHI). This allows the use of inverted or non-inverted loop filter configurations. It is thus possible to use a passive loop filter which offers higher performances without an operational amplifier. The function of the phase comparator is given in Table 3 and a typical transfer curve is illustrated in Fig.4.

Out-of-lock detector

An out-of-lock detector using the UP and DOWN signals from the phase comparator is included on-chip. The pin VCOA is an open collector output which is forced LOW during an out-of-lock condition. The same information is also available via the I^{2}C-bus in the status register (bit OOL). When the phase error (measured at the phase comparator) is greater than approximately 200 ns, an out-of-lock condition is immediately flagged. The flag is only released after 6 reference cycles when the phase error is less than 200 ns.

Table 1 Division ratio in the main divider

MAIN COUNTER: N									SWALLOW COUNTER: R		
MD17	MD16	MD15	...	MD8	MD7	...	MD5	MD4	...	MD0
B1	B0	C7	...	C0	D7	...	D5	D4	...	D0
MSB										LSB

Table 2 Reference divider programming

A3(RD3)	A2(RD2)	A1(RD1)	A0(RD0)	REFERENCE DIVISION RATIO	CHANNEL SPACING FOR 9.6 MHz AT OSCIN
0	0	0	0	128	75 kHz
0	0	0	1	160	60 kHz
0	0	1	0	192	50 kHz
0	0	1	1	240	40 kHz
0	1	0	0	256	37.5 kHz
0	1	0	1	320	30 kHz
0	1	1	0	384	25 kHz
0	1	1	1	480	20 kHz
1	0	0	0	512	18.75 kHz
1	0	0	1	640	15 kHz
1	0	1	0	768	12.5 kHz
1	0	1	1	960	10 kHz
1	1	0	0	1024	9.375 kHz
1	1	0	1	1280	7.5 kHz
1	1	1	0	1536	6.25 kHz
1	1	1	1	1920	5 kHz

Table 3 Operation of the phase comparator

	PHI = 0 (PASSIVE LOOP FILTER)			PHI = 1 (ACTIVE LOOP FILTER)		
	$f_{ref} < f_{var}$	$f_{ref} > f_{var}$	$f_{ref} = f_{var}$	$f_{ref} < f_{var}$	$f_{ref} > f_{var}$	$f_{ref} = f_{var}$
UP	0	1	0	1	0	0
DOWN	1	0	0	0	1	0
I_{pod}	−1 mA	1 mA	< ±5 nA	1 mA	−1 mA	< ±5 nA

MAIN CONTROL

The control part consists mainly of the I²C-bus control interface and a set of four registers A, B, C and D. The serial input data (SDA) is converted into 8-bit parallel words and stored in the appropriate registers. The data transmission to the synthesizer is executed in the burst mode with the following format:

//slave addr./subaddr./data1/data2/.../datan// ; n up to 4

Data byte 1 is written in the register indicated by the subaddress. An auto-increment circuit, if enabled (AVI = 1), then provides the correct addressing for the ensuing data bytes. Since the length of the data burst is not fixed, it is possible to program only one register or the whole set. The registers are structured in such a way so that the burst, for normal operation, is kept as short as possible. The bits that are only programmed during the set-up (reference division ratio, power-down, phase inversion and current on PCD) are stored in registers A and B.

In the slave address six bits are fixed, the remaining two bits depend on the application.

Table 4 Slave address

1	1	0	0	0	1	$\overline{SAA}$	R/$\overline{W}$

SAA is the slave address. When SAA goes HIGH then $\overline{SAA}$ = 0, when SAA goes LOW then $\overline{SAA}$ = 1. This allows the use of two UMA1014s on the same bus but using a different address. R/$\overline{W}$ should be set to logic 0 when writing to the synthesizer or set to logic 1 when reading the status register.

The subaddress includes the register pointer, and sets the two flags related to the auto-increment (AVI) and the alarm disable (DI)

Table 5 Subaddress

X	X	X	DI	AVI	X	SB1	SB0

Where:

X = not used

DI (Disable Interrupt):
DI = 1 disables the alarm on SYA
DI = 0 enables the alarm.

AVI (Auto Value Increment):
AVI = 1 enables the automatic increment
AVI = 0 disables the auto-increment.

SB1/SB0 are the pointers of the register where DATA1 will be written (see Table 6).

When the auto-increment is disabled (AVI = 0), the subaddress pointer will maintain the same value during the I²C-bus transfer. All the data bytes will then be written consecutively in the register pointed by the subaddress.

Table 6 Pointer of the registers

SB1	SB0	REGISTER POINTED
0	0	A
0	1	B
1	0	C
1	1	D

Status register and synthesizer alarm

When an out-of-lock condition or a power dip occurs, SYA, which is an open collector output, is forced LOW and latched. The pin SYA will be released after the status register is read via the I²C-bus.

The status register contains the following information:

Table 7 Status register

0	0	0	OOL	0	LOOL	LPD	DI

Where:

OOL = momentary out-of-lock
LOOL = latched out-of-lock
LPD = latched power dip
DI = disable interrupt (of the last write cycle)

The I²C-bus protocol to read this internal register is a single byte without subaddressing:

//slave address (R/$\overline{W}$ = 1)/status register (read)//

Table 8 Bit allocation

REGISTER	POINTER	BIT ALLOCATION								PRESET
		7	6	5	4	3	2	1	0	
A	00	PD	X	IPCD	X	RD3	RD2	RD1	RD0	00001110
B	01	1	0	1	PHI	VCOB	VCOA	MD17	MD16	10100101
C	10	MD15	MD14	MD13	MD12	MD11	MD10	MD9	MD8	00111000
D	11	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	10000000

Where X = not used

Table 9 Register allocation

REGISTER NAME	BIT NAME	FUNCTION		PRESET VALUE
A	PD	power down	PD = 0 normal operation	0
	IPCD	programmable charge pump current	IPCD = 1 = 1 mA; IPCD = 0 = 0.5 mA	0
	RD3...RD0	reference ratio	see Table 2	1110; r = 1536
B	PHI	phase inverter	PHI = 0 passive loop filter	0
	VCOA	VCO switch A	set pin 7	1
	VCOB	VCO switch B	set pin 13	0
	MD17, MD16	bits 17 and 16	MSB of main divider ratio	01
C	MD15 to MD8	bits 15 to 8	main divider ratio	00111000
D	MD7 to MD0	bits 7 to 0	main divider ratio	10000000; r = 80000

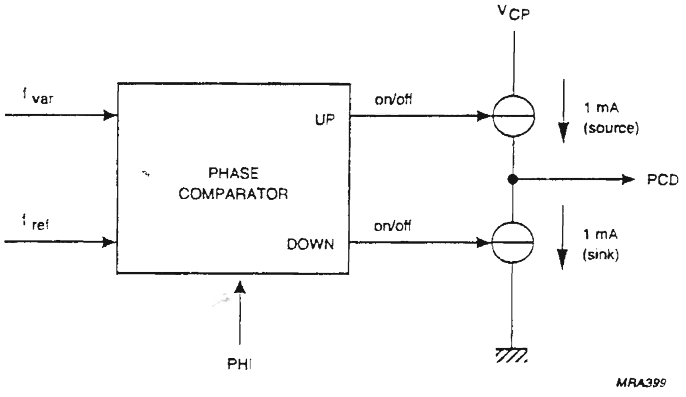


Fig.3 Phase comparator block diagram.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage range	−0.3	7.0	V
V_I	voltage range to ground (all pins)	0	V_{CC}	V
T_{stg}	IC storage temperature range	−55	+125	°C
T_{amb}	operating ambient temperature range	−40	+85	°C

HANDLING

Every pin referenced to ground withstands ESD (HMB) tests in accordance with MIL-STD-883C method 3015 class 2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling Integrated Circuits.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

CHARACTERISTICS

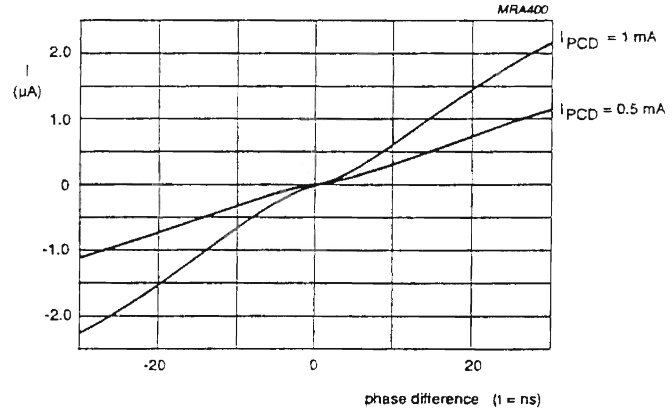
T_{amb} = 25 °C; V_{CC} = 4.5 to 5.5 V; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins V_{CC} and V_{CP})						
V_{CC}	supply voltage range		4.5	–	5.5	V
I_{CC}	supply current		–	11.5	13.5	mA
I_{CCpd}	supply current	power-down	–	2.5	3.3	mA
V_{CP}	charge pump supply voltage		4.5	–	5.5	V
I_{CP}	charge pump supply current	IPCD = 0.5 mA	–	1.4	1.8	mA
I_{CPpd}	charge pump supply current	power-down	–	0.01	–	mA
RF dividers (pin RF)						
f_{RF}	frequency range		50	–	1100	MHz
$V_{RF(rms)}$	input voltage level (RMS value)	50 to 100 MHz	150	–	200	mV
		100 to 1100 MHz	50	–	150	mV
R_I	input resistance	at 1 GHz	–	200	–	Ω
		at 100 MHz	–	600	–	Ω
C_I	input capacitance	note 1	–	2.0	–	pF
R_{RF}	division ratios		2048	–	262143	–
Oscillator and reference divider (pins OSCIN and OSCOUT)						
f_{OSC}	oscillator frequency range		3	–	16	MHz
$V_{OSC(RMS)}$	input level sine wave (RMS value)		0.15	–	V_{CC}/2.8	V
$V_{OSC(p-p)}$	input level square wave (peak-to-peak value)		0.45	–	V_{CC}	V
$t_{OSC\ mk}$	input mark width	see Fig.8	10	–	–	ns
$t_{OSC\ sp}$	input space width		31	–	–	ns
Z_{OSC}	output impedance at pin OSCOUT		–	–	2	kΩ
R_{ref}	reference division ratio	see Table 1	128	–	1920	
1/8 crystal frequency (open collector output) (pin FX8)						
I_{OL}	LOW level output current	$V_{OL} \geq 0.6$ V	1.0	–	–	mA
Phase comparator (pin PCD)						
f_{PCD}	frequency range		5	–	100	kHz
I_{PCD}	output current	V_{PCD} = 2.5 V				
		bit IPCD = 1	0.9	1.2	1.4	mA
		bit IPCD = 0	0.45	0.6	0.75	mA
I_{PCDl}	output leakage current		−5	±1	+5	nA
V_{PCD}	output voltage		0.4	–	V_{CP}−0.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial clock and serial data input (pins SCL and SDA)						
f_{CLK}	clock frequency		0	–	100	kHz
V_{IH}	HIGH level input voltage		3	–	–	V
V_{IL}	LOW level input voltage		–	–	1.5	V
I_{IH}	HIGH level input current		–	3	10	µA
I_{IL}	LOW level input current		−10	−5	–	µA
C_I	input capacitance		–	–	10	pF
I_{sink}	SDA sink current	$V_{OL} = 0.4$ V	3	–	–	mA
Slave address select input (pin SAA) and Hardware power-down input (pin HPDN)						
V_{IH}	HIGH level input voltage		3	–	–	V
V_{IL}	LOW level input voltage		–	–	0.4	V
I_{IH}	HIGH level input current		–	–	0.1	µA
I_{IL}	LOW level input current		−10	–	–	µA
VCO output switches (pins VCOA and VCOB) and synthesizer alarm (pin SYA); note 2						
I_{OL}	LOW level sink current	$V_{OL} \geq 0.4$ V	400	–	–	µA

Notes to the characteristics

1. C_I is in parallel with R_I
2. Pin VCOA is forced to logic 0 during out-of-lock condition



The current I_{PCD} is averaged over a reference period of 24 µs.

Fig.4 Gain of phase detector and charge pump.

Low-power frequency synthesizer for mobile radio communications

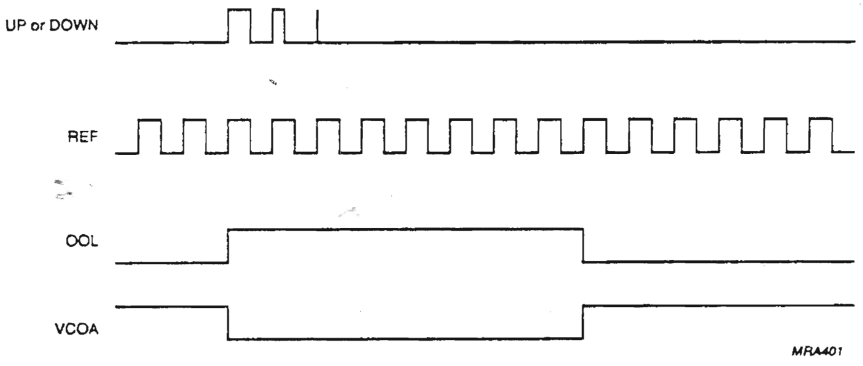


Fig.5 Out-of-lock function.

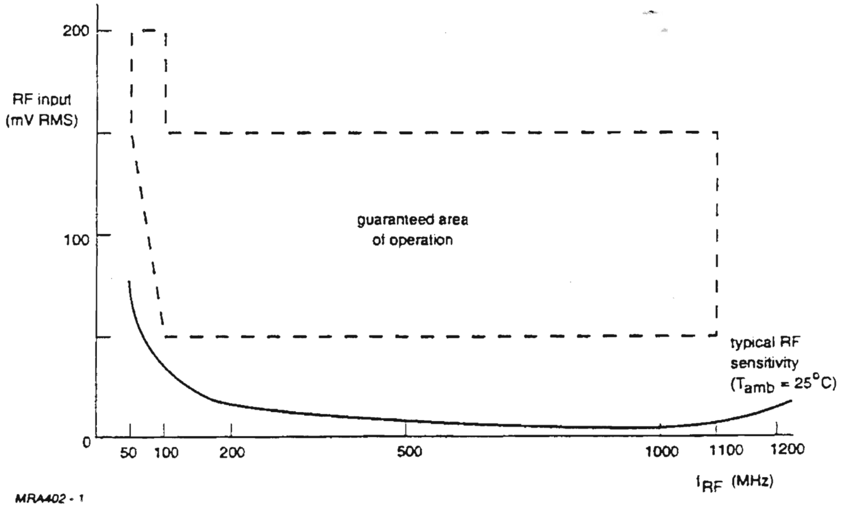


Fig.6 RF input high frequency sensitivity.

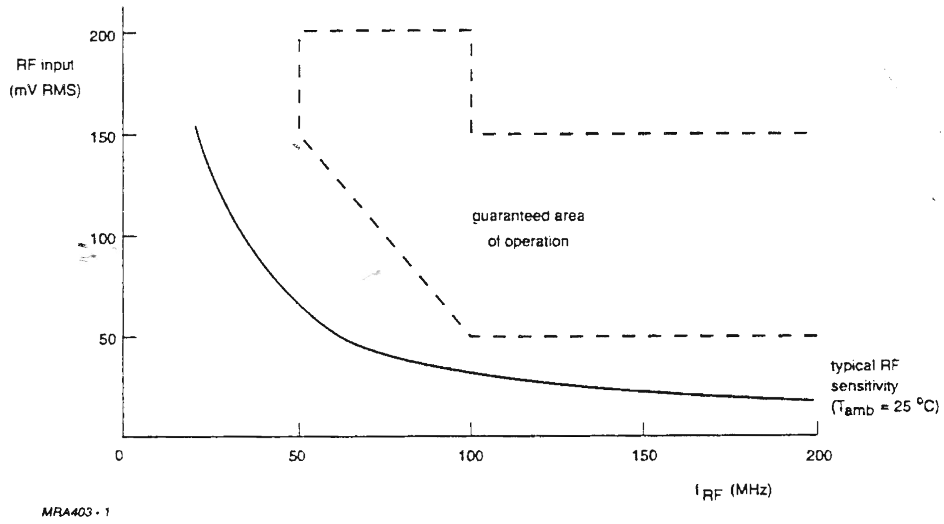


Fig.7 RF input low frequency sensitivity.

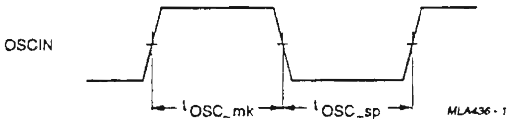
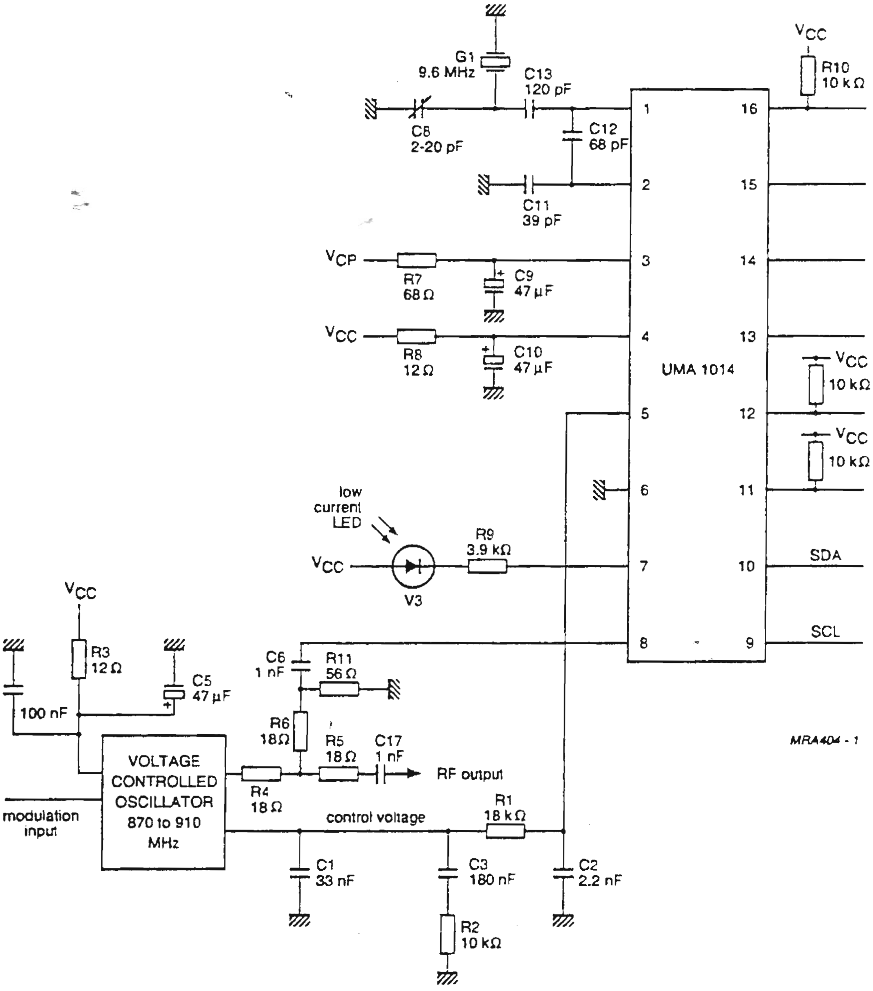


Fig.8 Oscillator input timing.



ETACS application for:

V_{CO} sensitivity = 11 MHz/V.

Channel spacing = 12.5 kHz.

Fig.9 Typical cellular mobile radio application.

Application report for the UMA1014T frequency synthesizer

SCO/AN91004

1. INTRODUCTION

This application note is intended as a guide to designing a phase locked loop based on the Philips UMA1014T frequency synthesizer integrated circuit. The UMA1014T is a low power single chip solution to frequency synthesis in the range 100 MHz to 1100 MHz and is primarily intended for use in analogue cellular radio applications.

The device comprises of the following functional blocks:

- RF dual-modulus prescaler.
- RF programmable divider.
- Reference oscillator.
- Reference programmable divider.
- Digital phase comparator.
- In-lock detection circuitry.
- I^{2}C serial programming interface.

In addition, the device features a power down mode for battery conservation and a XTAL/8 output for use with the Philips cellular radio chipset. The only major external component required is a voltage controlled oscillator (VCO).

This application report presents a design for a frequency synthesizer based on the UMA1014T suitable for the local oscillator for analogue cellular radio applications in the 900 MHz band. A PCB layout is suggested. For detailed device specifications of the UMA1014T refer to the data sheet (Reference 1).

2. FUNCTIONAL DESCRIPTION OF THE UMA1014T

The main functions are illustrated in a Phase Lock Loop (PLL) block diagram (Fig 1). A temperature controlled crystal oscillator (TCXO) provides a reference frequency to the PLL. A phase comparator uses a charge pump to send correction current pulses to a low pass filter. The filter integrates the pulses giving a voltage which controls a VCO. VCO and TCXO o/ps are divided down to a common comparison frequency to control the phase comparator. When the VCO o/p is on frequency the current pulses need only be large enough to cancel leakage currents thus maintaining the required voltage on the VCO.

2.1 Main Divider Chain

The UMA1014T contains a fully programmable main divider chain with an on-chip RF prescaler. The range of the main divider is from 2048 to 262143, thus permitting all useful phase detector comparison frequencies over the full range of input frequencies.

2.2 Reference Divider Chain

Since current analogue systems have only a few different channel spacings, and in any system there is a restricted choice of reference crystal frequencies, the UMA1014T implements a reference divider with limited programmability. A total of 16 different division ratios can be selected which enables all the required phase detector comparison frequencies to be generated. These ratios are 128, 160, 192, 240, 256, 320, 384, 480, 512, 640, 768, 960, 1024, 1280, 1536 and 1920.

In addition, there is one eighth of the crystal frequency available on an output for use with the Philips cellular radio chipset. This chipset uses a 1.2 MHz clock for the analogue and digital baseband circuits which is provided by the frequency synthesizer; the synthesizer thus requires the use of a 9.6 MHz crystal in this application.

2.3 Phase Detector

There are three requirements for the phase detector; firstly it should cover the full 360 degree phase range, secondly it should have good noise performance, and thirdly it should have good comparison frequency suppression. In order to meet these requirements, the use of a high gain digital phase comparator is beneficial. The comparator covers the complete phase range while introducing little noise owing to the high proportion of time that is spent in a high impedance state. Good reference rejection is achieved due to low leakage currents.

2.3.1 Digital Phase Comparator

The Digital Phase Comparator (PCD) has three states, sinking current, sourcing current and a high impedance tristate. The design is based on D type flip-flops and responds to the full 360 degree range of phase inputs. The D type flip-flops control two current sources arranged in a push pull configuration. PCD delivers a constant current while the main and reference dividers are out of phase, either sinking or sourcing (Fig 2). The current IPCD is programmed via the I^{2}C interface to be either 1 mA or 0.5 mA. The phase comparator gain is hence:

$$PCD\,gain = \frac{IPCD}{2 \times \pi}\ A/rad \qquad (1)$$

The phase comparator circuit incorporates a delay which eliminates a dead band that would otherwise be present in digital phase comparators. Dead bands are due to the finite time the current sources take to switch on. The design of the UMA1014T takes this into account by introducing the delay into the D type reset line. This gives the current sources enough time to respond. Both current sources are switched on for the duration of the delay thus cancelling each other at PCD.

3. INTERFACING TO THE UMA1014T

The UMA1014T provides two way communication to a controller, power down facility, programmable o/p ports, oscillator circuitry and PLL control. The UMA1014T is designed to have the minimum of external components to enable low cost, compact and reliable circuits.

3.1 Programming the UMA1014T

The UMA1014T is programmed via the Philips Standard I^{2}C bus. To program information into the device registers, it is necessary to transmit first the device address, then the sub-address, and finally the data bytes for the register(s) (Reference 2). To read the status register, it is only necessary to transmit the address before reading back the value of the status register. When writing to the UMA1014T the sub-address allows writing to any single register, or a burst mode where all registers can be written in one I^{2}C transfer. The formats are thus:

Write to one register:

```
START - address - sub-address - data - STOP
           |           |
           |           |____contains register number to be accessed
           |
           |____R/WN (read/write not) bit set to 0 (write)
```

Write to several registers:

```
START - address - sub-address - data 1 - ... - data n - STOP
           |           |
           |           |____ contains first register number to be
           |                 accessed in the sequence and auto-
           |                 increment enabled
           |
           |____R/WN bit set to 0 (write)
```

Read from status register:

```
START - address - status - STOP
           |
           |____R/WN bit set to 1 (read)
```

The address byte, in addition to containing the R/WN bit as shown above, has one bit that reflects the inverse of the SAA pin logic level. This allows the addressing of up to two synthesizer circuits on the same I^{2}C bus.

The format for the address bus is as follows:

```
1   1   0   0   1   SAA   0    R/WN
|                    |          |
|                    |          |____0 (write), 1 (read)
|                    |
|                    |____opposite logic level to that of SAA pin
|
|____MSB  of device address, transmitted first after START condition
```

The sub-address has the following format: (X means not used)

```
X   X   X  DI  AVI  X   SB1   SB0
           |    |        |      |
           |    |        |______|____register pointer
           |    |
           |    |____auto-increment - 0 (disable), 1 (enable)
           |
           |____SYA interrupt - 1 (disable), 0 (enable)
```

Data is formatted as a series of registers as follows:

Reg/ister	SB 0/1	Bit Allocation								Preset
		7	6	5	4	3	2	1	0	
A	00	PD	0	IPCD	X	RD3	RD2	RD1	RD0	00001110
B	01	1	0	1	PHI	VCOB	VCOA	MD17	MD16	10101001
C	10	MD15	MD14	MD13	MD12	MD11	MD10	MD9	MD8	00111000
D	11	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	10000000

Register map bit polarities:

	0	1
PD	Normal operation	Power down
IPCD	Current in PCD = 0.5 mA	PCD = 1 mA
RD3..0	Reference divider ratio MSB = RD3	
PHI	Passive loop (no inversion)	Active loop (Phase inversion)
VCOA	Set pin 7 low	Set pin 7 high
VCOB	Set pin 13 low	Set pin 13 high
MD17..0	Main divider ratio MSB = MD17	

RD3..RD0 reference divider programming:

RD3	RD2	RD1	RD0	Reference Division Ratio
0	0	0	0	128
0	0	0	1	160
0	0	1	0	192
0	0	1	1	240
0	1	0	0	256
0	1	0	1	320
0	1	1	0	384
0	1	1	1	480
1	0	0	0	512
1	0	0	1	640
1	0	1	0	768
1	0	1	1	960
1	1	0	0	1024
1	1	0	1	1280
1	1	1	0	1536
1	1	1	1	1920

MD17..MD0 main divider value 2048 to 262143 (hex $800 to $3ffff).

3.2 Hardware Control Inputs and Outputs

There are a number of status and control signals generated by the UMA1014T and also a hardware control input.

3.2.1 HPD Input

This input is used to disable the divider chains in order to save power when the synthesizer is not required to be operational. The power down state can be activated either by taking this pin low or by setting the power down bit in the I^{2}C register to a '1'. The input has an internal pull-up resistor so that normal operation will be obtained if the pin is left open circuit.

The power down state does not have any effect on the I^{2}C circuitry, so that the device may still be addressed, and new information programmed into the registers even in the power down mode.

3.2.2 FX8 Output

This is an open collector output of one eighth of the crystal or TCXO input frequency. It is required for use with the Philips cellular radio chipset for AMPS and TACS systems; in this application the synthesizer should be used with a 9.6 MHz TCXO. The recommended pull-up load is 27 k Ohm.

3.2.3 SYA (Synthesizer Alarm) Output

This is an open collector output which is normally held high by an external 27 k Ohm load. Under error conditions, the synthesizer latches SYA low. The error conditions that set SYA low are a power dip or an out-of-lock condition. A power dip occurs when VCC supply falls below about 3.5 V. SYA is reset again by reading the status register, which contains the relevant alarm information. The SYA output can also be enabled and disabled via I^{2}C as required.

The typical use of SYA would be to interrupt a microcontroller to warn of the error condition. As the output is open collector, it is possible to connect more than one device together directly; in this case the microcontroller would poll the relevant devices to locate the source of the error condition.

3.2.4 VCO0 and VCO1 Outputs

These are open collector outputs and are intended for enabling the power supply to VCOs or buffer stages so that these parts of the set can be powered down when not required to be operational. The outputs are controlled via I^{2}C. In addition, the VCO0 output is forced low during an out-of-lock condition; this output could therefore be used to disable the transmitter when this condition occurs to prevent causing interference. In this case, there may well be other parts of the circuitry also controlling the transmitter in the same way; as the VCO0 and VCO1 lines are open collector, they may be directly connected to other such controlling signals.

The VCO1 output is not affected by the hardware power down input or power down via I^{2}C. The VCO0 output will of course be forced low due to the out-of-lock condition resulting from a power down.

3.3 Crystal Oscillator

For analogue cellular radio applications, the UMA1014T will almost certainly be used with an external oscillator in order to provide the stability necessary to ensure operation within the specification. However, in case some other applications do not require such accuracy, provision has been made to form a crystal oscillator using the OSCIN and OSCOUT inputs (pins 1 and 2 respectively). The oscillator circuit should be of the Colpitts type and requires the addition of four capacitors to function. This is shown in Fig 3, with capacitor values suitable for operation at 9.6 MHz.

The internal biasing provides possible operation over the range 3 MHz to 16 MHz with the addition of a suitable crystal. It may be necessary to adjust the values of the capacitors slightly to guarantee oscillation under all conditions for frequencies significantly different to 9.6 MHz.

The crystal used in this circuit is parallel resonant, fundamental mode, with a load capacitance of 30 pF which is approximately the series combination of the three fixed capacitors in parallel with the trimmer capacitor.

3.4 External Oscillator

When using an external oscillator such as a TCXO module, the output from the oscillator should be connected directly to the OSCin pin (pin 1). The OSCout pin (pin 2) should either be left open circuit, or could be used as a buffered version of the signal applied to OSCin.

3.5 RF Connection to Main Divider

The output from the VCO needs to be split between the synthesizer RF o/p and the UMA1014T main divider input. A matched splitter is used as shown in Fig 4. Ideally, the splitter should provide maximum isolation to the VCO to prevent pulling or modulation due to changes in the load impedance at the RF o/p and main divider input. The amount of isolation is limited by the required RF output power and the main divider input sensitivity. Emphasis is placed on the importance of providing sufficient isolation between the VCO and the main divider to keep spurious modulations at a minimum level.

3.6 Loop Filter Design

The correct design of the loop filter is of considerable importance to the optimum performance of the synthesizer. The filter should be designed so as to achieve the required compromise between noise performance and switching time. The actual circuit will therefore depend on the particular application. A procedure has been established to ensure quick and simple loop filter design. The method, based on first order approximations, provides a working solution without a need for computer simulation and modelling.

Design Procedure

For typical applications a passive loop is used thus removing the need for an operational amplifier. The following design is based on a second order low pass filter (Reference 3). Then, for applications requiring further reference breakthrough rejection, a third order is incorporated. The third order loop filter is used for circuits and measurements in this report.

Loop parameters are first chosen, these are:

Radio frequency	RF
Comparison frequency	CF
Switching time	St
Minimum modulating frequency	MF
VCO gain rad/Volt	Ko
Phase comparator gain Amps/rad	Kd
Phase margin	ϕ

Determine the loop bandwidth Fn from

$$\frac{3}{switching\ time} = Fn \qquad (2)$$

Determine main divider ratio N from N = RF / CF (3)
Determine angular velocity wn rads / s from wn = 2 x π x Fn

The loop filter circuit (Fig 5) has three time constants, these are:

- T1 = C3 x R2 (4)
- T2 = R2 x C1 x C3 / (C3 + C4) (5)
- T3 = C2 x R1 (6)

The second order loop is designed by omitting R1 and C2 (T3) and uses the equations below:

$$T2 = \frac{\frac{1}{COS\,\phi} - Tan\,\phi}{wn} \qquad (7)$$

$$T1 = 1 / (wn^2 \times T2) \qquad (8)$$

$$C3 + C1 = K \sqrt{\frac{1 + (wn \times T1)^2}{1 + (wn \times T2)^2}} \qquad (9)$$

$$where\ K = \frac{Kd\ x\ Ko}{N\ x\ wn^2} \tag{10}$$

$$C1 = \frac{T2\ x\ (C3 + C1)}{T1} \tag{11}$$

$$C3 = (C3 + C1) - C1 \tag{12}$$

$$R2 = T1\ /\ C3 \tag{13}$$

Measuring the reference spurs and comparing with a particular specification establishes if a third order is necessary.

If a further 'A' dB of breakthrough suppression is needed to meet specification, then T3 is included to make a third order filter. Note 'A' should not be so large that T3 x 10 > T1. A good starting value for 'A' is 20 dB.

$$T3 = \sqrt{\left(\frac{10^{(A/20)} - 1}{(2\ x\ \Pi\ x\ Fc)^2} \right)} \tag{14}$$

T2 determines the loop stability and remains the same as for 2nd order loop.

A calculated value of closed loop bandwidth wnc is used. This is usually slightly less than wn so the switching time will be slightly longer than originally specified.

$$wnc = \frac{(T2 + T3)}{T2^2}\ x\ tan\ \phi\ x \left(\sqrt{1 + \frac{4\ x\ T2^2}{(2\ x\ tan\ \phi\ x\ (T2 + T3))^2}} - 1 \right) \tag{15}$$

$$T1 = \frac{1}{wnc^2\ x\ (T2 + T3)} \tag{16}$$

$$C3 + C1 = K \sqrt{\frac{1 + (wnc\ x\ T1)^2}{(1 - wnc^2\ x\ T2\ x\ T3)^2 + \frac{T3 + T2}{T1}}} \tag{17}$$

$$where\ K = \frac{Ko\ x\ Kd}{N\ x\ wnc^2} \tag{18}$$

$$C1 = \frac{(C3 + C1)\ x\ T2}{T1} \tag{19}$$

$$C3 = (C3 + C1) - C1 \tag{20}$$

$$C2 = C1\ /\ 16 \tag{21}$$

$$R2 = T1\ /\ C3 \tag{22}$$

$$R1 = T3\ /\ C2 \tag{23}$$

For a successful filter it is important that C3 $>>$ C1 and C1 $>>$ C2.

3.6.1 Worked Example

As an example the design of the third order loop filter for the UMA1014T under the following conditions is shown below. This design on the PCAL1143-1 board suitable for ETACS transmit application. Switching time is set sightly shorter than expected to compensate for the reduction in the final loop bandwidth Fnc.

VCO frequency = 888 MHz
VCO gain Ko = 13 MHz / V
Channel spacing = 25 kHz (with half channel offset)
Reference oscillator = 9.6 MHz
Switching time = 12 ms (for a requirement < 14 ms)
Min mod frequency = 300 Hz
Phase margin(degrees) = 45
Additional reference
Rejection A = 20 dB

In this example the phase comparator gain Kd chosen is 1 mA / cycle as opposed to 0.5 mA / cycle. In open environments a loop based on this is less susceptible to interference as capacitor values are higher. A comparison frequency of 12.5 kHz is chosen to allow for the half channel offset specified in ETACS.

The first order loop bandwidth Fn:

$$\frac{3}{12 x 10^{3}} = 250\,Hz \quad wn = 2 x \pi x Fn = 1570\ rads/s \qquad Use\ (2)$$

The main divider ratio N:

$$\frac{888 x 10^{6}}{12.5 x 10^{3}} = 71040 \qquad Use\ (3)$$

$$T2 = \frac{\frac{1}{cos\ 45} - tan\ 45}{1570} = 2.64 x 10^{-4} \qquad Use\ (7)$$

$$T3 = \sqrt{\left(\frac{10^{20/20} - 1}{(2 x \pi x 12500)^{2}}\right)} = 3.82 x 10^{-5} \qquad Use\ (14)$$

$$wnc = \frac{(2.64 x 10^{-4} + 3.82 x 10^{-5}) x\ tan\ 45}{(2.64 x 10^{-4})^{2}} x$$

$$\left(\sqrt{1 + \frac{4 x (2.64 x 10^{-4})^{2}}{(2 x\ tan\ 45 x (2.64 x 10^{-4} + 3.82 x 10^{-5}))^{2}}} - 1\right) = 1421 \qquad Use\ (15)$$

$$T1\ \frac{1}{1421^{2} x (2.64 x 10^{-4} + 3.82 x 10^{-5})} = 1.64 x 10^{-3} \qquad (Use\ (16)$$

$$K = \frac{13 \times 10^{6} \times 10^{-3}}{71040 \times 1421^{2}} = 9.04 \times 10^{-8} \qquad \text{Use } (18)$$

$$C1 + C3 = K\sqrt{\frac{1 + (1421 \times 1.64 \times 10^{-3})^{2}}{(1 - 1421^{2} \times 2.64 \times 10^{-4} \times 3.82^{-5})^{2} + \dfrac{3.82 \times 10^{-5} + 2.64^{-4}}{1.64 \times 10^{-3}}}}$$

$$= 2.14 \times 10^{-7} \qquad \text{Use } (17)$$

$$C1 = \frac{2.14 \times 10^{-7} \times 2.64 \times 10^{-4}}{1.64 \times 10^{-3}} = 3.45 \times 10^{-8} \qquad \text{Use } (19)$$

$$C3 = 2.14 \times 10^{-7} - 3.45 \times 10^{-8} = 1.8 \times 10^{-7} \qquad \text{Use } (20)$$

$$C2 = 3.45 \times 10^{-8}/16 = 2.15 \times 10^{-9} \qquad \text{Use } (21)$$

$$R2 = 1.64 \times 10^{-3}/1.8 \times 10^{-7} = 9111 \qquad \text{Use } (22)$$

$$R1 = 3.82 \times 10^{-5} / 2.15 \times 10^{-9} = 17767 \qquad \text{Use } (23)$$

Check C2 << C1 << C3.

Values chosen for filter components are:

C1 = 33	nF	R1 = 18	k Ohms
C2 = 2.2	nF	R2 = 10	k Ohms
C3 = 180	nF		

3.7 PCB Layout Considerations

The circuit of the UMA1014T demonstration board (PCAL1143-1) is shown in Fig 6, with the layout shown in Fig 7. This PCB has a solid ground plane on one side (apart from isolated pads for non-grounded connections to leaded components). In addition, there are areas of ground plane on the surface mount side of the board to ensure satisfactory grounding of important components. There are a good number of plated-through holes connecting the two layers of ground plane. Normal RF design practices should of course be taken into account when laying out the circuit.

There are a number of particular points that should be borne in mind when considering the circuit and layout.

- The non-surface mount side of the board (if a 2 sided board is used) should be virtually solid ground plane to give good RF performance.
- The 5 V digital supply (VCC) should be well decoupled as close to the pin as possible, preferably with a large value capacitor (eg: 47 uF) and in series with a small value resistor (eg: 12 Ohms) from the 5 V line.
- The 5 V charge pump supply (VCP) should be decoupled separately from VCC but in a similar manner. Routing the 5 V supply under the IC is to be avoided.
- Incorporating a ground plane on the surface mount side of the PCB underneath the synthesizer helps isolate digital noise from the charge pump parts. This ground plane should be well connected with vias to the full ground plane.

4. TYPICAL PERFORMANCE

This section describes the typical performance obtainable with the UMA1014T with the circuit shown in Fig 6 and parameters listed in 3.6.1. The relevant performance criteria for a synthesizer are usually:

Close-in phase noise (ie: noise within the loop bandwidth).

Noise floor at an offset from the carrier.

Comparison breakthrough components.

Switching time.

It should be noted of course that these criteria can be traded off against each other to some extent to tailor the overall performance, and that the performance described here is only one compromise between the various criteria. In general, the choice of a low loop bandwidth will improve the comparison frequency breakthrough and will filter out more of the close-in phase noise, but will result in a longer switching time. The use of a higher order filter can improve comparison frequency breakthrough with little effect on the noise or switching time. The noise floor at offsets significantly higher than the loop bandwidth are determined completely by the VCO itself.

Plots of the close-in spectrum (span of 2 kHz) and also a span of 50 kHz are shown in Figs 8 and 9 respectively for a carrier frequency of 888 MHz and a comparison frequency of 12.5 kHz. From Fig 8 we can see from the noise plateau that the loop bandwidth is around 270 Hz, and Fig 9 shows the spectrum analyser noise floor at offsets greater than about 15 kHz from the carrier with the first and second comparison frequency breakthrough component being visible at 12.5 kHz and 25 kHz from the carrier respectively.

Figure 10 shows switching waveforms for a frequency jump of 10 MHz. The top trace (labelled CH1) is the I^2C transfer to the UMA1014T; the second (CH2) is the VCO control line. The third trace (CH3) is the VCOA output showing the out-of-lock condition. The fourth trace (CH4) is the RF output of the VCO mixed down to 0 Hz with a signal generator at the destination frequency. The VCO output is coupled to the mixer via an amplifier with 17 dB gain followed by a 10 dB attenuator. This is to provide isolation to the VCO from the mixer.

The mixer output trace shows that the switching time is 13 m seconds, which is a little longer than the VCO control line trace appears to show. This is because observation of the VCO control line is not accurate due to the very high VCO gain (13 MHz / V).

From Fig 10, we can see that the VCO control line has a single overshoot during switching; this shows that the loop is properly damped, so the phase margin is correct.

To summarise the performance of the circuit in Fig 6:

loop bandwidth	270 Hz
close-in noise	- 55 dBc / Hz at 200 Hz from carrier
VCO noise floor	- 113 dBc / Hz at 25 kHz from carrier
residual fm	< 18 Hz rms, CCITT weighted
comparison frequency breakthrough	- 65 dBc at 12.5 kHz - 82 dBc at 25 kHz
typical switching time	< 13 m seconds for 10 MHz jump to within 1 kHz of the destination frequency

5. CONCLUSIONS

Information regarding the use of the UMA1014T in a frequency synthesizer application has been presented. A methodology for determining the loop filter components has been described since the switching and noise performance of the complete circuit depends on a good filter design. The layout of the PCAL1143-1 demonstration board has been shown as an example PCB layout.

6. REFERENCES

1. UMA1014T, Initial Specification Data Sheet, September 1990.

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3. Ulriche, L Rhode;
Digital PLL Frequency Synthesizers Theory and Design.
28/3/91.

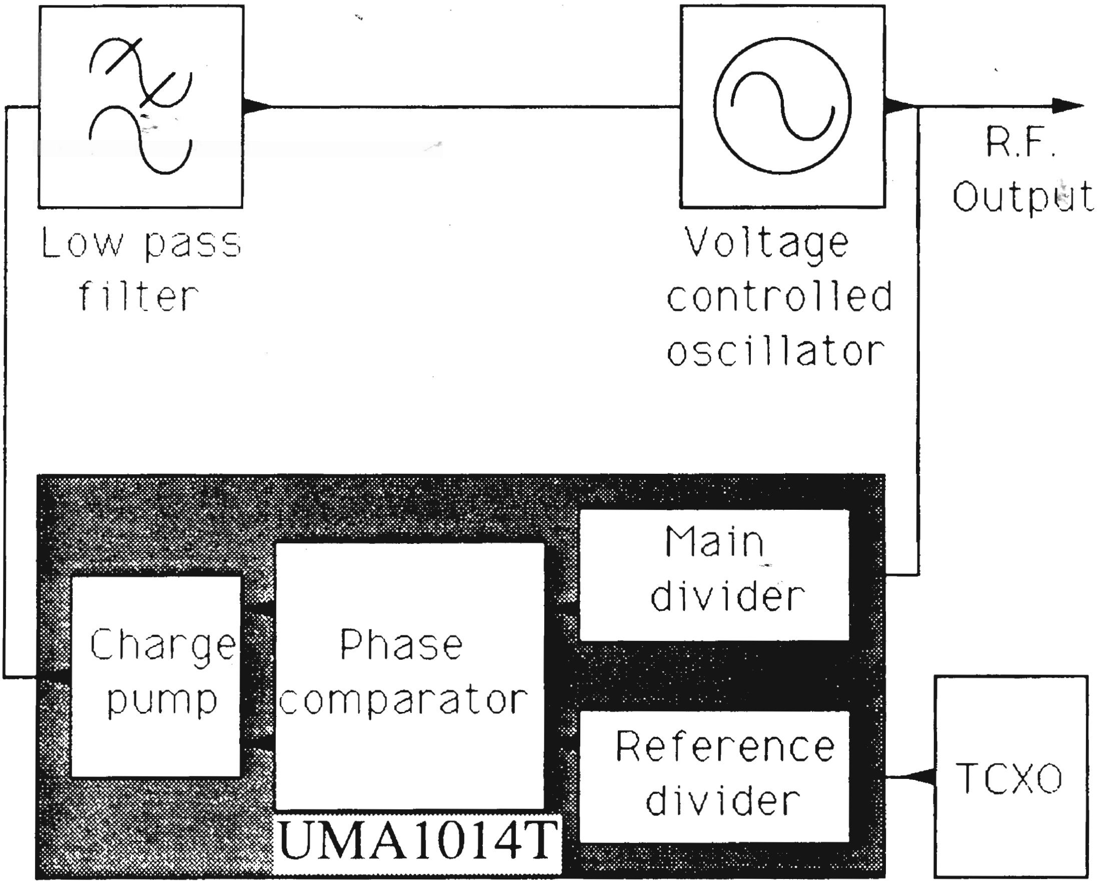

Fig 1 PLL Circuit Block Diagram

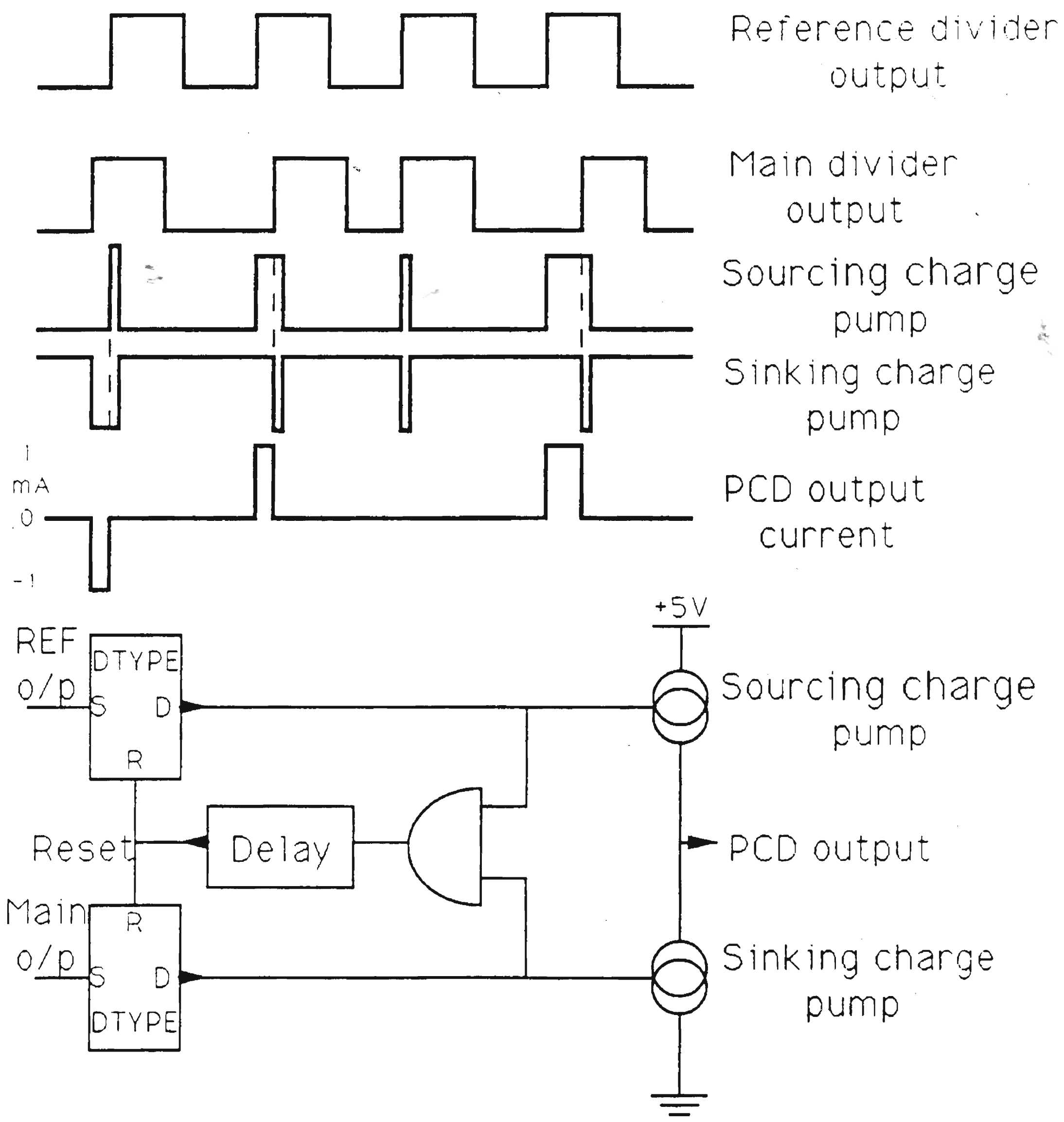

Fig 2 Digital Phase Comparator Operation

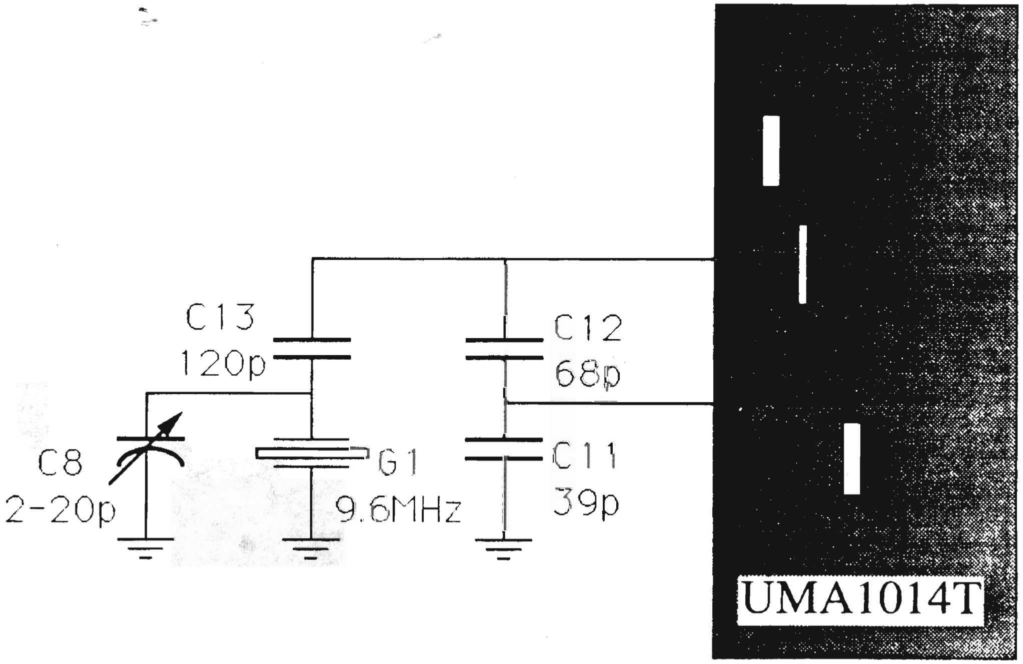

Fig 3 Crystal Oscillator Circuit Diagram

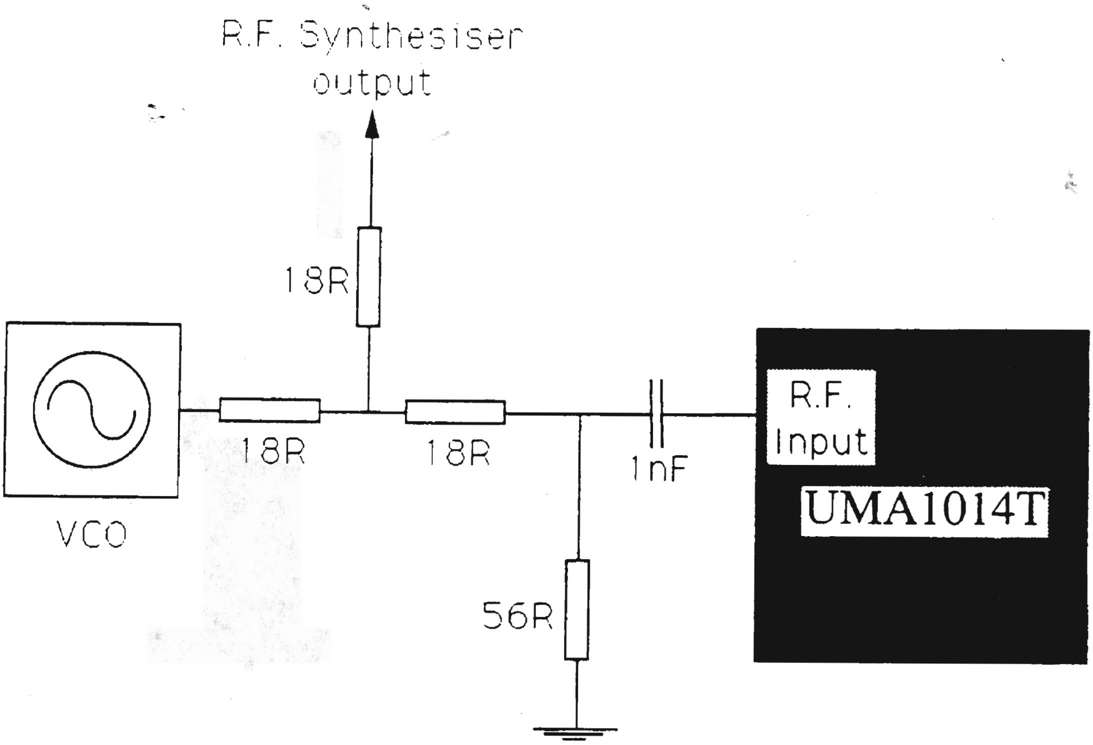

Fig 4 RF Power Splitter Circuit Diagram

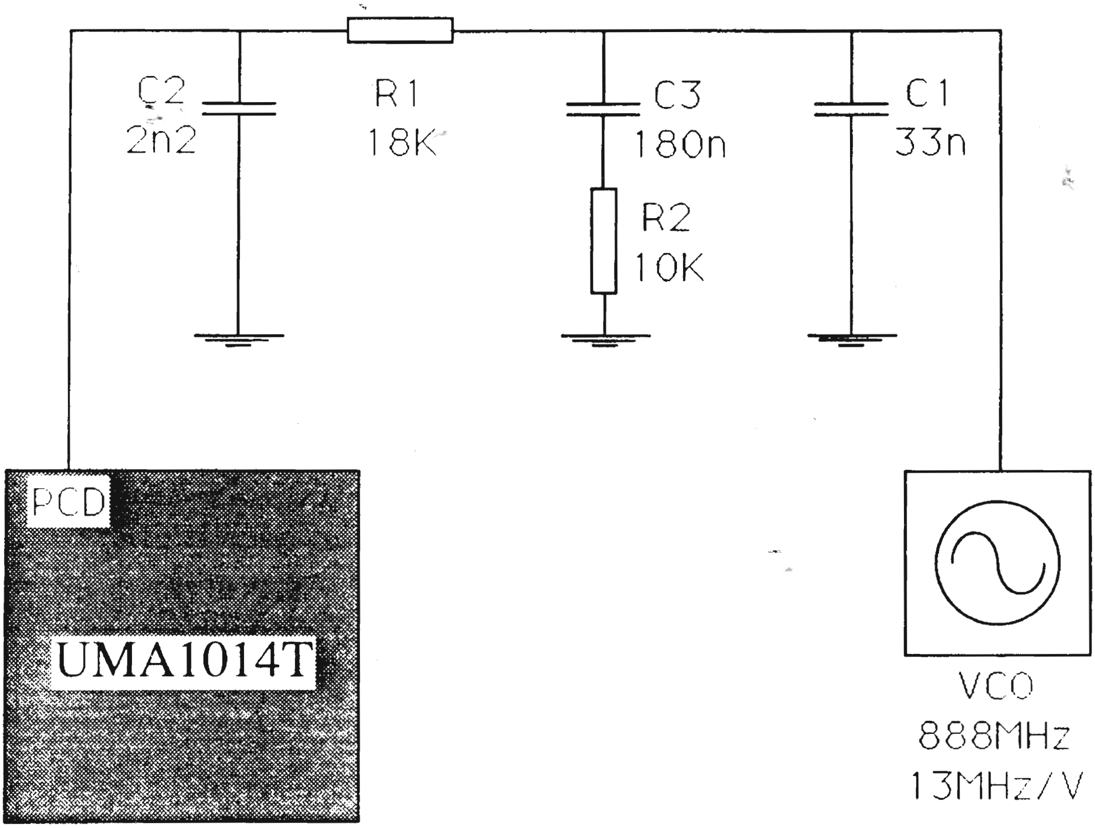

Fig 5 Loop Filter Circuit Diagram

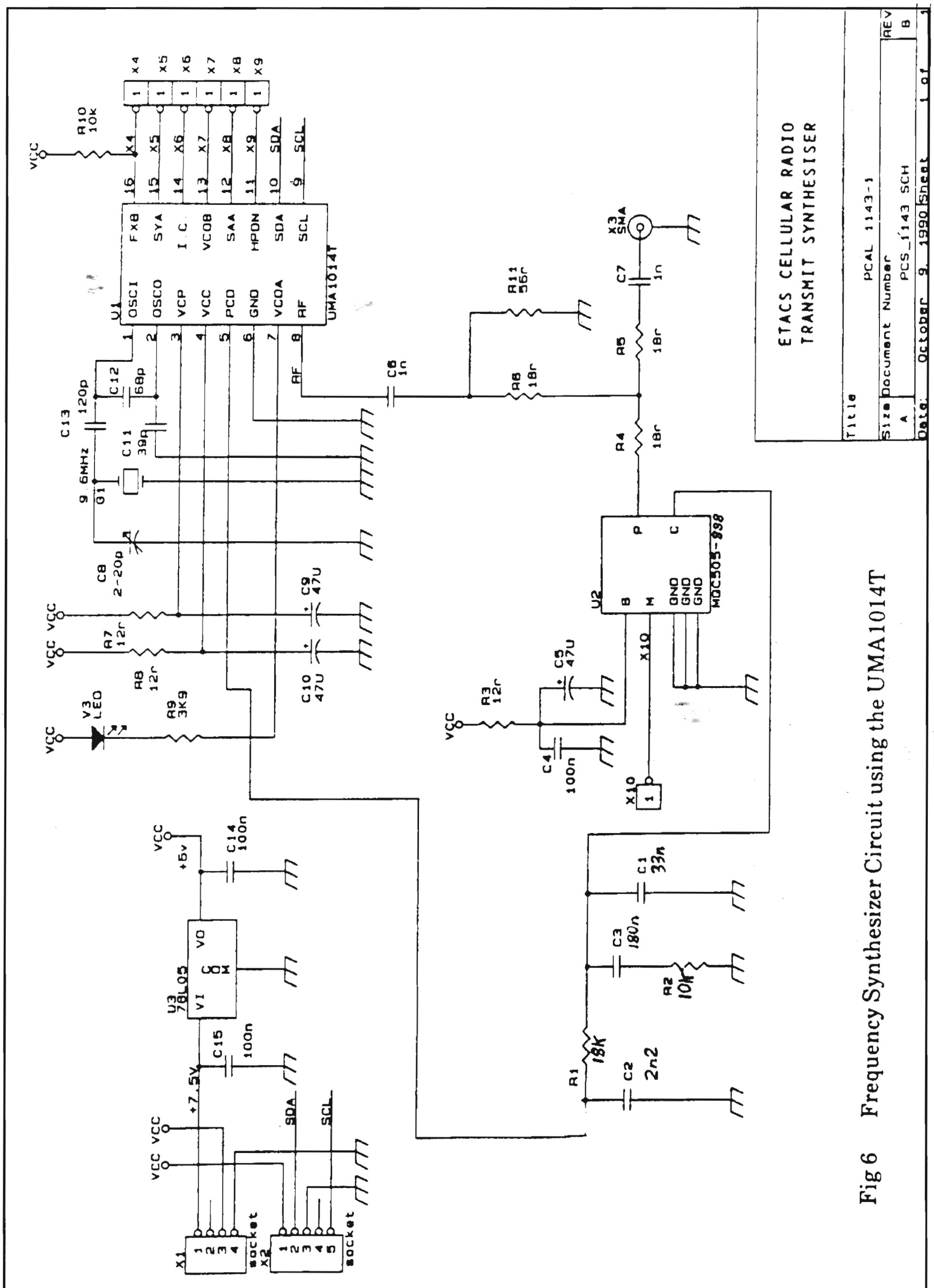

Fig 6 Frequency Synthesizer Circuit using the UMA1014T

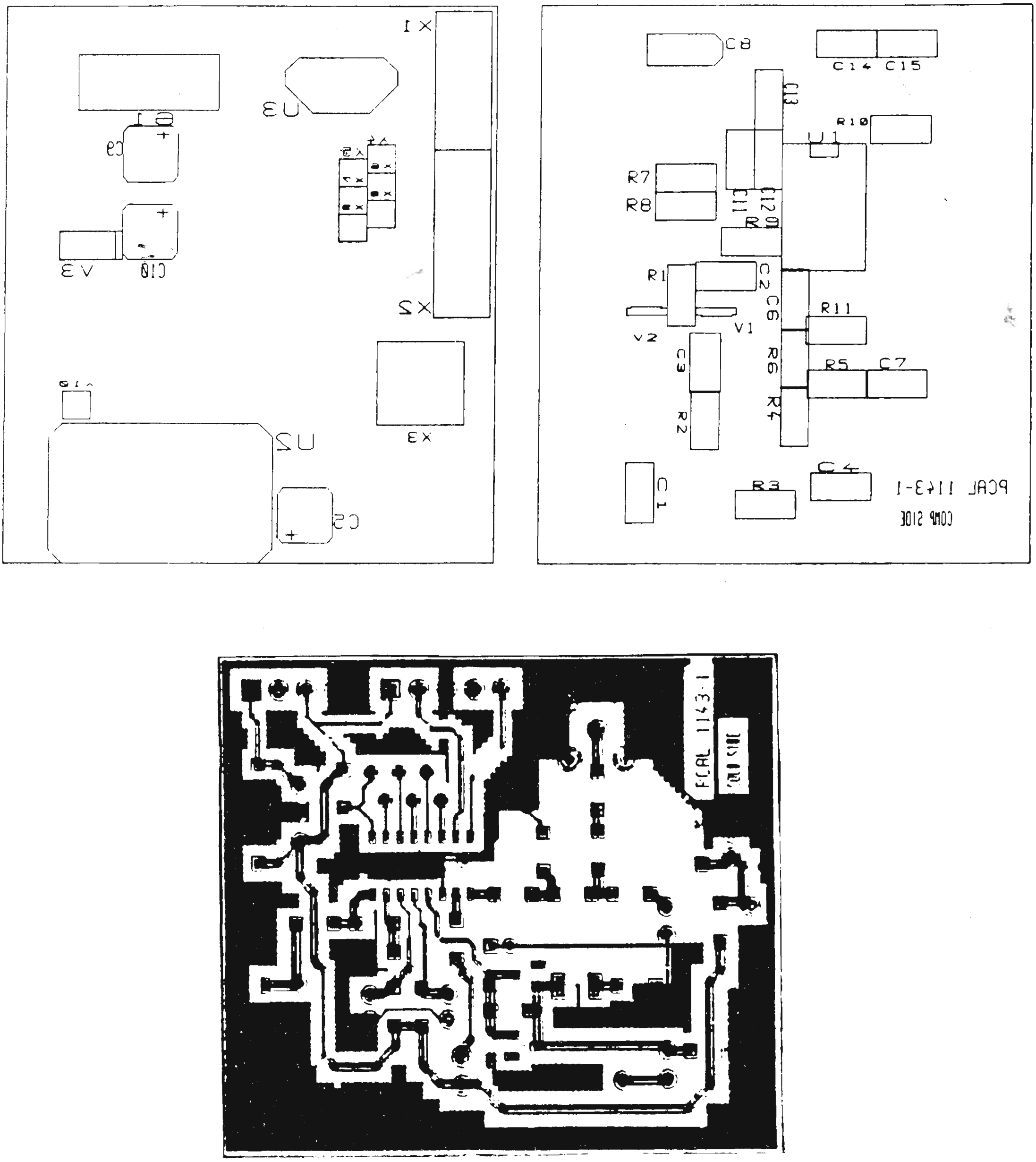

Fig 7 Board Layout for UMA1014T Frequency Synthesizer

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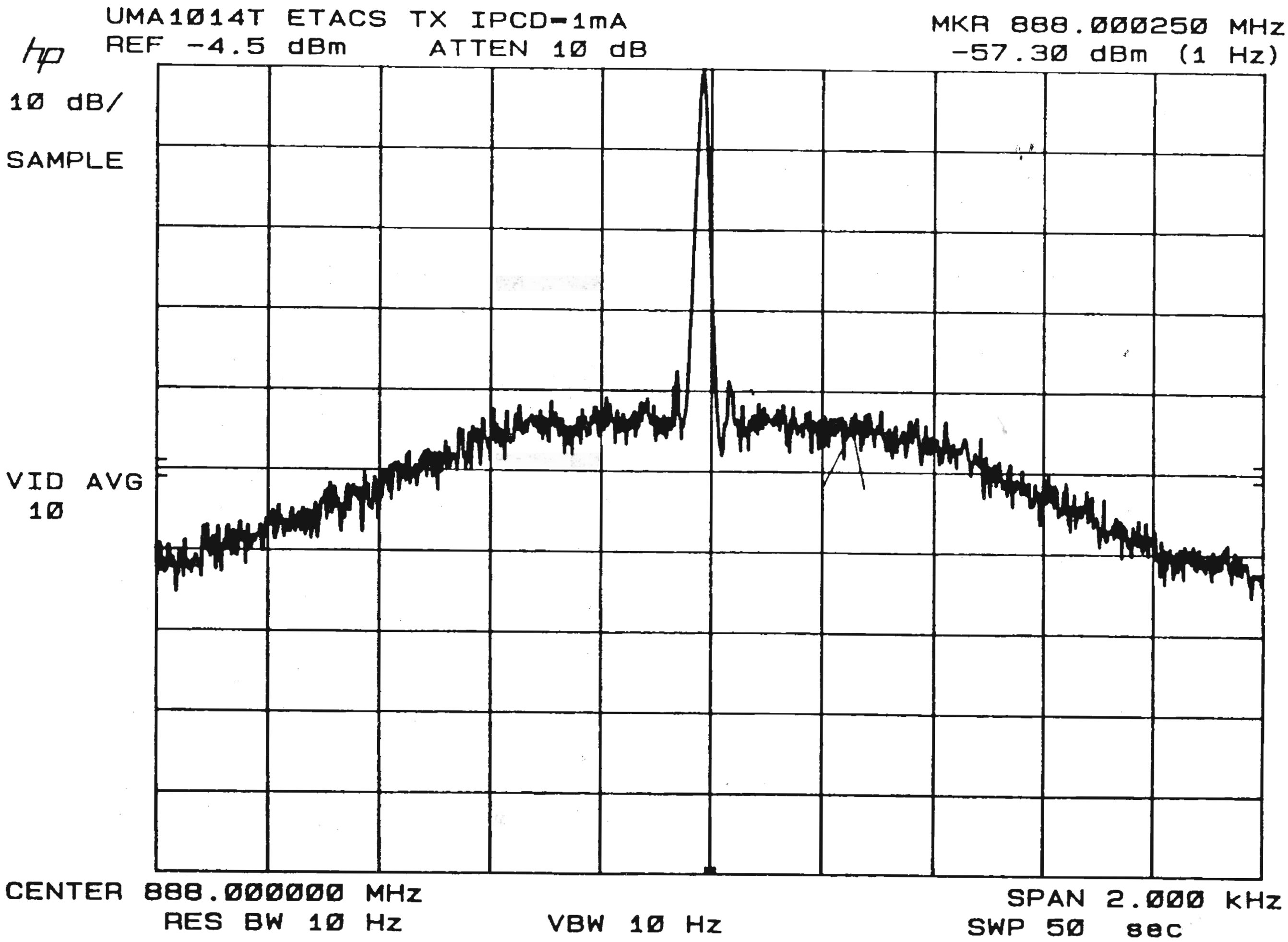


Fig 8 Typical Carrier Spectrum - 2 kHz Span

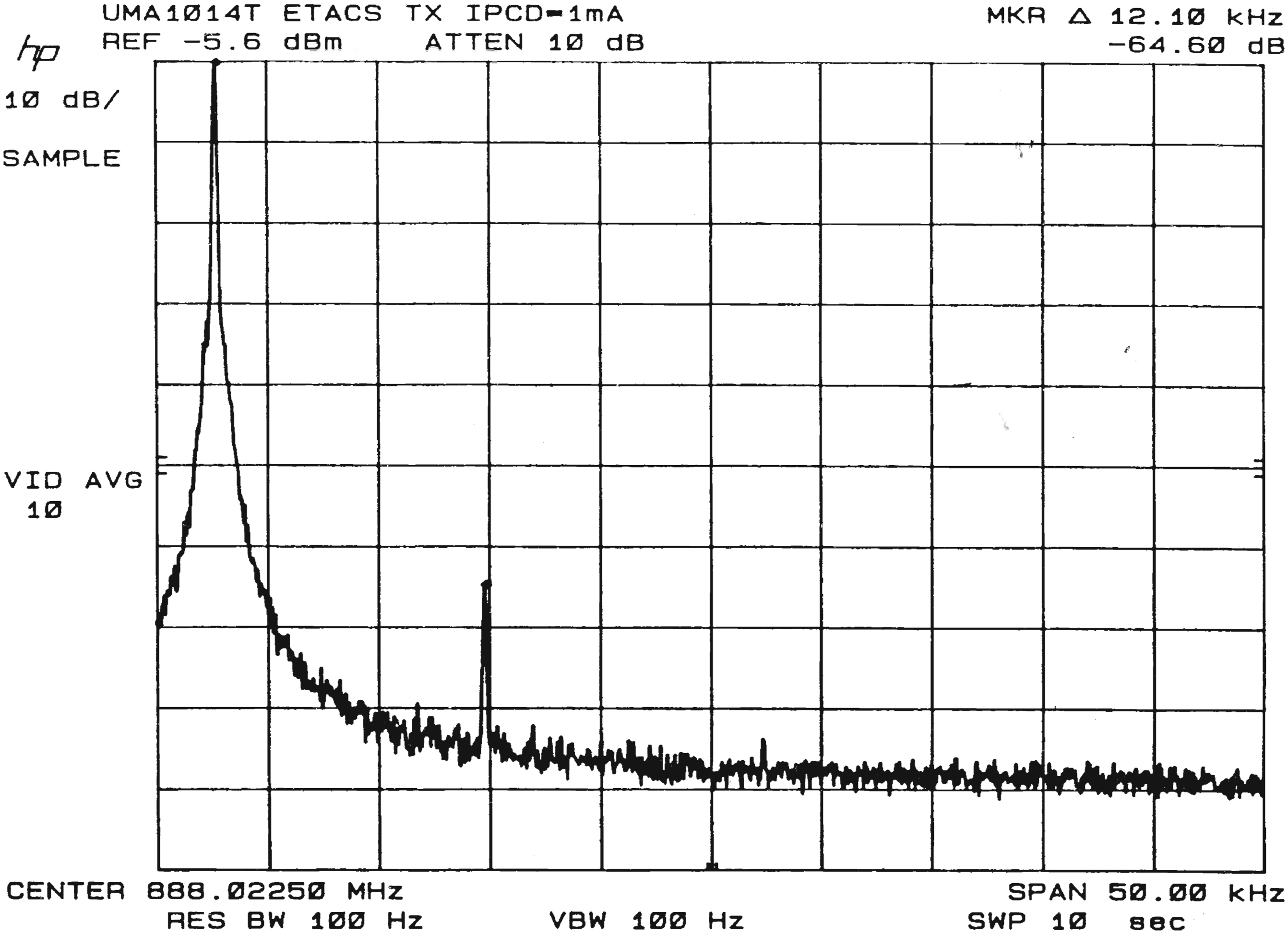


Fig 9 Typical Carrier Spectrum - 50 kHz Span

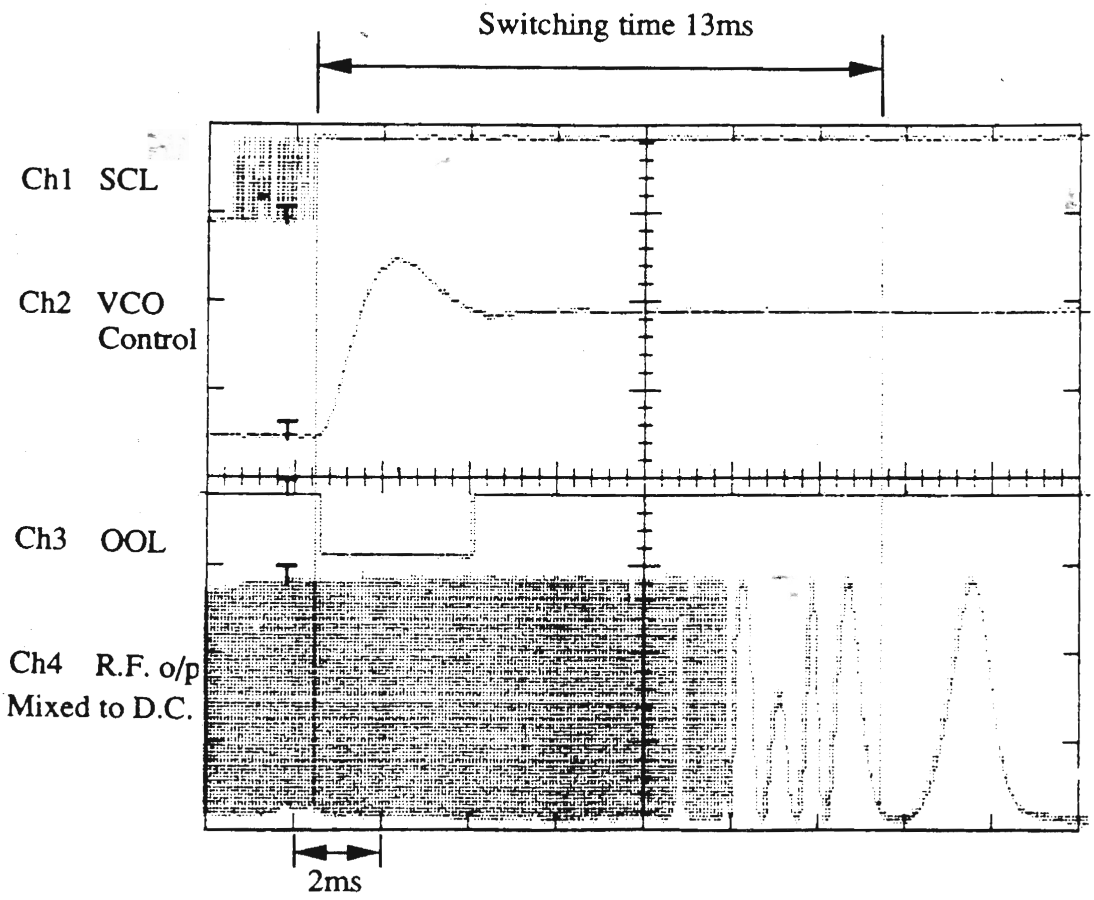


Fig 10 Typical Switching Waveforms

Low-power dual frequency synthesizer for radio communications

UMA1015M

FEATURES

- Two fully programmable RF dividers up to 1.1 GHz
- Fully programmable reference divider up to 35 MHz
- 2 : 1 or 1 : 1 ratio of selectable reference frequencies
- Fast three-line serial bus interface
- Adjustable phase comparator gain
- Programmable out-of-lock indication for both loops
- On-chip voltage doubler
- Low current consumption from 3 V supply
- Separate power-down mode for each synthesizer
- Up to 4 open-drain output ports.

APPLICATIONS

- Cordless telephone
- Hand-held mobile radio.

GENERAL DESCRIPTION

The UMA1015M is a low-power dual frequency synthesizer for radio communications which operates in the 50 to 1100 MHz frequency range. Each synthesizer consists of a fully programmable main divider, a phase and frequency detector and a charge pump. There is a fully programmable reference divider common to both synthesizers which operates up to 35 MHz. The device is programmed via a 3-wire serial bus which operates up to 10 MHz. The charge pump currents (gains) are fixed by an external resistance at pin 20 (I_{SET}). The BiCMOS device is designed to operate from 2.6 (3 Ni-Cd cells) to 5.5 V at low current. The charge pump supply can be provided by external source or on-chip voltage doubler. Each synthesizer can be powered-down independently via the serial bus to save current. It is also possible to power-down the device via the HPD input (pin 5).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}, V_{DD2}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.6	–	5.5	V
V_{CC}	charge pump supply voltage	external supply; doubler disabled; $V_{CC} \geq V_{DD}$	2.6	–	6.0	V
V_{CCvd}	charge pump supply from voltage doubler	doubler enabled	–	$2V_{DD1} - 0.6$	6.0	V
$I_{DDO1} + I_{DDO2} + I_{CCO}$	operating supply current	both synthesizers ON; doubler disabled; $V_{DD1} = 5.5$ V	–	9.6	–	mA
$I_{DD1pd} + I_{DD2pd} + I_{CCpd}$	current in power-down mode per supply	doubler disabled; $V_{DD1} = 5.5$ V	–	0.01	–	mA
I_{DD1pd}	current in power-down mode from supply V_{DD}	doubler enabled; $V_{DD1} = 3$ V	–	0.15	–	mA
f_{RFA}, f_{RFB}	RF input frequency for each synthesizer		50	–	1100	MHz
f_{XTALIN}	crystal input frequency		3	–	35	MHz
$f_{ref(min)}$	minimum phase comparator frequency	$f_{RF} = 50$ to 1100 MHz; $f_{XTAL} = 3$ to 35 MHz	–	10	–	kHz
$f_{ref(max)}$	maximum phase comparator frequency	$f_{RF} = 50$ to 1100 MHz; $f_{XTAL} = 3$ to 35 MHz	–	750	–	kHz
T_{amb}	operating ambient temperature	synthesizer A $2.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	−30	–	+85	°C
		synthesizer B $2.6\text{ V} \leq V_{DD} \leq 4.5\text{ V}$	−30	–	+85	°C
		synthesizer B $2.6\text{ V} \leq V_{DD} \leq 5.0\text{ V}$	0	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UMA1015M/C2	20	SSOP20	plastic	SOT266-1

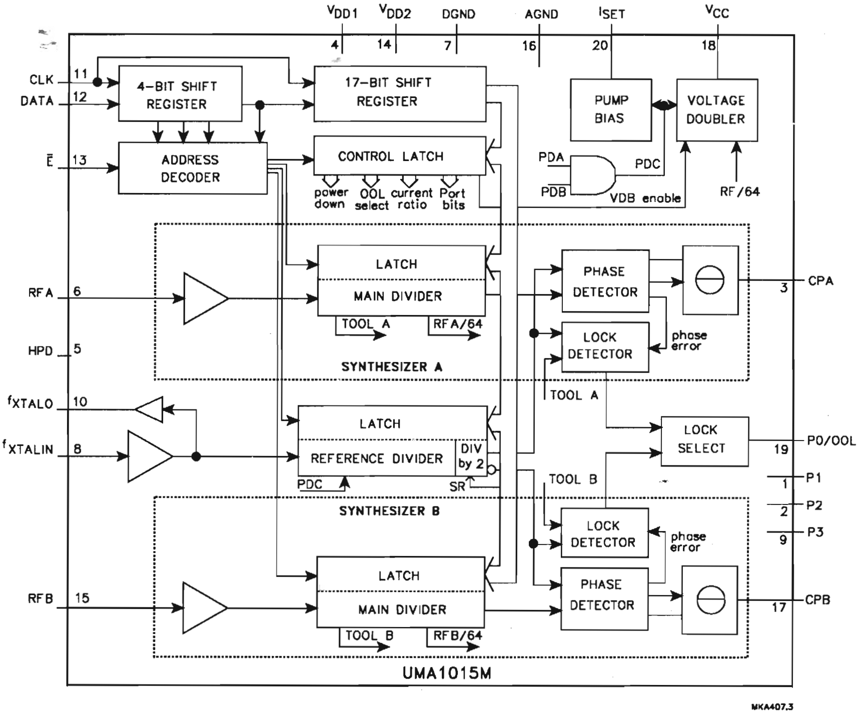


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
P1	1	output Port 1
P2	2	output Port 2
CPA	3	charge-pump output synthesizer A
V_{DD1}	4	digital supply voltage 1 (2.6 to 5.5 V)
HPD	5	hardware power-down (input LOW = power-down)
RFA	6	RF input synthesizer A
DGND	7	digital ground
f_{XTALIN}	8	common reference frequency input from TCXO
P3	9	output Port 3
f_{XTALO}	10	buffered output of f_{XTAL} signal
CLK	11	programming bus clock input
DATA	12	programming bus data input
$\overline{E}$	13	programming bus enable input (active LOW)
V_{DD2}	14	digital supply voltage 2 (2.6 to 5.5 V)
RFB	15	RF input synthesizer B
AGND	16	analog ground to charge pumps
CPB	17	charge pump output synthesizer B
V_{CC}	18	analog supply to charge pump; external or voltage doubler output (2.6 to 6.0 V)
P0/OOL	19	Port output 0/out-of-lock output
I_{SET}	20	regulator pin to set charge-pump currents

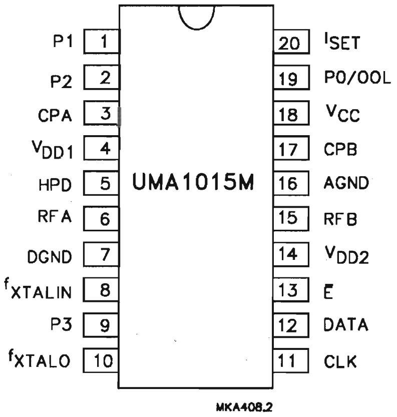


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Main dividers

Each synthesizer has a fully programmable 17-bit main divider. The RF input drives a pre-amplifier to provide the clock to the first divider bit. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from below 50 mV (RMS) up to 250 mV (RMS), and at frequencies up to 1.1 GHz. The high frequency sections of the divider are implemented using bipolar transistors, while the slower section uses CMOS technology. The range of division ratios is 512 to 131 071.

Reference divider

There is a common fully programmable 12-bit reference divider for the two synthesizers. The input f_{XTALIN} drives a pre-amplifier to provide the clock input for the reference divider. This clock signal is also buffered and output on pin f_{XTALO} (open drain). An extra divide-by-2 block allows a reference comparison frequency for synthesizer B to be half that of synthesizer A. This feature is selectable using the program bit SR. If the programmed reference divider ratio is R then the ratio for each synthesizer is as given in Table 1.

The range for the division ratio R is 8 to 4095. Opposite edges of the divider output are used to drive the phase detectors to ensure that active edges arrive at the phase detectors of each synthesizer at different times. This minimizes the potential for interference between the charge pumps of each loop. The reference divider consists of CMOS devices operating beyond 35 MHz.

Table 1 Synthesizer ratio of reference divider

SR	SYNTHESIZER A	SYNTHESIZER B
0	R	R
1	R	2R

Phase comparators

For each synthesizer, the outputs of the main and reference dividers drive a phase comparator where a charge pump produces phase error current pulses for integration in an external loop filter. The charge pump current is set by an external resistance R_{SET} at pin I_{SET}, where a temperature-independent voltage of 1.2 V is generated. R_{SET} should be between 12 kΩ and 60 kΩ (to give an I_{SET} of 100 μA and 20 μA respectively).
The charge-pump current, I_{CP}, can be programmed to be either ($12 \times I_{SET}$) or ($24 \times I_{SET}$) with the maximum being 2.4 mA. The dead zone, caused by finite switching of current pulses, is cancelled by an internal delay in the phase detector thus giving improved linearity. The charge pump has a separate supply, V_{CC}, which helps to reduce the interference on the charge pump output from other parts of the circuit. Also, V_{CC} can be higher than V_{DD1} if a wider range on the VCO input is required.

Voltage doubler

If required, there is a voltage doubler on-chip to supply the charge pumps at a higher level than the nominal available supply. The doubler operates from the digital supply V_{DD1}, and has a maximum output of 6 V. An external capacitor is required on pin V_{CC} for smoothing, the capacitor required to develop the extra voltage is integrated on-chip. To minimize the noise being introduced to the charge pump output from the voltage doubler, the doubler clock is suppressed (provided both loops are in-lock) for the short time that the charge pumps are active. The doubler clock (RF/64) is derived from whichever main divider is operating (synthesizer A has priority). While both synthesizers are powered down (and the doubler is enabled), the doubler clock is supplied by a low-current internal oscillator. The doubler can be disabled by programming the bit VDON to logic 0, in order to allow an external charge pump supply to be used.

Out-of-lock indication/output ports

There is a lock detector on-chip for each synthesizer. The lock condition of each, or both loops, is output via an open-drain transistor which drives the pin P0/OOL (when out-of-lock, the transistor is turned on and therefore the output is forced LOW). The lock condition output is software selectable (see Table 4). An out-of-lock condition is flagged when the phase error is greater than T_{00L}, the value of which is approximately equal to 80 cycles of the relevant RF input. The out-of-lock flag is only released after 8 consecutive reference cycles where the phase error is less than T_{00L}. The out-of-lock function can be disabled, via the serial bus, and the pin P0/OOL can be used as an output port. Three other port outputs P1, P2 and P3 (open-drain transistors) are also available.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. This is allowed when CLK is in either state without causing any consequences to the register data. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programming data even during power-down of both synthesizers.

However when either synthesizer A or synthesizer B or both are powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTALIN}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The address bits are decoded on the rising edge of $\overline{E}$. This produces an internal load pulse to store the data in the addressed latch. To avoid erroneous divider ratios, the pulse is inhibited during the period when data is read by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The data format and register bit allocations are shown in Table 2.

Table 2 Bit allocation

FIRST	REGISTER BIT ALLOCATION																			LAST
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
X	X	VDON	PO	OLA	OLB	CRA	CRB	X	X	sPDA	sPDB	P3	P2	P1	X	X	0	0	0	1
MA16	SYNTHESIZER A MAIN DIVIDER COEFFICIENT															MA0	0	1	0	0
0	0	0	0	SR	R11	REFERENCE DIVIDER COEFFICIENT										R0	0	1	0	1
MB16	SYNTHESIZER B MAIN DIVIDER COEFFICIENT															MB0	0	1	1	0
RESERVED FOR TEST(1)																	0	0	0	0

Note

1. The test register is not to be programmed. Normally all bits of the test register must be set to zero.

Table 3 Bit allocation description

SYMBOL	DESCRIPTION
sPDA, sPDB	software power-down for synthesizers A and B (0 = power-down)
P3, P2, P1 and P0	bits output to pins 1, 2, 9 and 19 (1 = high impedance)
VDON	voltage doubler enable (1 = doubler enabled)
OLA, OLB	out-of-lock select; selects signal output to pin 19 (see Table 4)
CRA, CRB	charge pump A/B current to I_{SET} ratio select (see Table 5)
SR	reference frequency ratio select (see Table 6)

Table 4 Out-of-lock select

OLA	OLB	OUTPUT AT PIN 19
0	0	P0
0	1	lock status of loop B; OOLB
1	0	lock status of loop A; OOLA
1	1	logic OR function of loops A and B

Table 5 Charge pump current ratio

CRA/CRB	CURRENT AT PUMP
0	$I_{CP} = 12 \times I_{SET}$
1	$I_{CP} = 24 \times I_{SET}$

Table 6 Reference division ratio

SR	RATIO A	RATIO B
0	R	R
1	R	2R

Power-down modes

The device can be powered down via pin HPD (active LOW = power-down) or via the serial bus (bits SPDA and SPDB, logic 0 = power-down). When only one synthesizer is powered down, the functions common to both will be maintained. When both synthesizers are switched off, only the voltage doubler (if enabled) will remain active drawing a reduced current. An internal oscillator will drive the doubler in this situation. If both synthesizers have been in a power-down condition, then when one or both synthesizers are reactivated, the reference and main dividers restart in such a way as to avoid large random phase errors at the phase comparator.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD1}, V_{DD2}	DC range of digital power supply voltage with respect to DGND	−0.3	+6.0	V
V_{CC}	DC charge pump supply voltage with respect to AGND	−0.3	+6.0	V
$\Delta V_{CC\text{-}DD}$	difference in voltage between V_{CC} and V_{DD1}, V_{DD2}	−0.3	+6.0	V
V_n	DC voltage at pins 1, 2, 5, 6, 8 to 15, 19 and 20 with respect to DGND	−0.3	V_{DD1} + 0.3	V
$V_{3,\ 17}$	DC voltage at pins 3 and 17 with respect to AGND	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

$V_{DD1} = V_{DD2} = 2.6$ to 5.5 V; $V_{CC} = 2.6$ to 6.0 V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; (V_{DD1}, V_{DD2} and V_{CC}) voltage doubler disabled, external supply on V_{CC}						
V_{DD1}, V_{DD2}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.6	–	5.5	V
$I_{DD1} + I_{DD2}$	total digital supply current from V_{DD1} and V_{DD2}	$f_{XTAL} = 12.8$ MHz; both synthesizers on; $V_{DD1} = V_{DD2} = 3$ V	–	8.5	–	mA
		$f_{XTAL} = 12.8$ MHz; both synthesizers on; $V_{DD1} = V_{DD2} = 5.5$ V	–	–	12.5	mA
I_{DDpda}, I_{DDpdb}	total digital supply current from V_{DD1} and V_{DD2} with one synthesizer in power-down mode	$f_{XTAL} = 12.8$ MHz; one synthesizer powered down; $V_{DD1} = V_{DD2} = 3$ V	–	5.5	–	mA
		$f_{XTAL} = 12.8$ MHz; one synthesizer powered down; $V_{DD1} = V_{DD2} = 5.5$ V	–	–	7.5	mA
I_{DDpd}	digital supply current in power-down mode	both synthesizers powered down; $V_{HPD} = 0$ V	–	–	60	µA
V_{CC}	charge pump supply voltage	$V_{CC} \geq V_{DD}$	2.6	–	6.0	V
I_{CC}	charge pump supply current	both synthesizers on and in lock; $f_{ref} = 12.5$ kHz	–	–	25	µA
I_{CCpd}	charge pump supply current in power-down mode	both synthesizers powered down	–	–	25	µA
Voltage doubler enabled						
I_{DD}	total digital supply current from V_{DD1} and V_{DD2}	$f_{XTAL} = 12.8$ MHz; both synthesizers on and in lock; $V_{DD1} = 3$ V; $f_{doubler} = 16$ MHz	–	8.5	12	mA
I_{DDpd}	total digital supply current in power-down mode from V_{DD1} and V_{DD2}	both synthesizers powered down; $V_{DD1} = 3$ V; $V_{HPD} = 0$ V	–	0.15	0.3	mA
V_{CCvd}	charge pump supply voltage	DC current drawn from $V_{CC} = 50$ µA	$2V_{DD1} - 1.2$	$2V_{DD1} - 0.6$	6.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF main divider input; RFA and RFB						
f_{RF}	RF input frequency		50	–	1100	MHz
$V_{RF(rms)}$	RF input signal voltage (RMS value; AC coupled)	$R_s = 50\ \Omega$; $V_{DD1} = V_{DD2} = 2.6$ to 3.5 V; $f_{RF} = 400$ to 1100 MHz	50	–	250	mV
		$R_s = 50\ \Omega$; $V_{DD1} = V_{DD2} = 3.5$ to 5.5 V; $f_{RF} = 400$ to 1100 MHz	100	–	250	mV
		$R_s = 50\ \Omega$; $V_{DD1} = V_{DD2} = 2.6$ to 5.5 V; $f_{RF} = 50$ to 400 MHz	150	–	400	mV
Z_I	input impedance (real part)	$f_{RF} = 1$ GHz; indicative, not tested	–	300	–	Ω
C_I	input capacitance	indicative, not tested	–	1	–	pF
R_{pm}	principle main divider ratio		512	–	131071	
Reference divider input; f_{XTALIN}						
f_{ref}	reference input frequency from crystal		3	–	35	MHz
$V_{XTALIN(rms)}$	sinusoidal input voltage (RMS value)		100	–	500	mV
Z_I	input impedance (real part)	$f_{XTALIN} = 12.8$ MHz; indicative, not tested	–	10	–	kΩ
C_I	input capacitance	indicative, not tested	–	1	–	pF
R_{rd}	reference divider ratio		8	–	4095	
Charge pump current setting resistor input; I_{SET}						
V_{SET}	voltage output on I_{SET}	$R_{SET} = 12$ kΩ to 60 kΩ	–	1.2	–	V
Charge pump outputs; CPA and CPB						
I_{CP}	charge pump sink or source current	$R_{SET} = 15$ kΩ; CRA/CRB = logic 1; $I_{cp} = I_{SET} \times 24$; $V_{cp} = 0.4$ V to $V_{CC} - 0.5$ V	1.4	1.9	2.4	mA
		$R_{SET} = 15$ kΩ; CRA/CRB = logic 0; $I_{cp} = I_{SET} \times 12$; $V_{cp} = 0.4$ V to $V_{CC} - 0.5$ V	0.7	0.96	1.2	mA
I_{LI}	charge pump off leakage current	$V_{cp} = 0.5V_{CC}$	–5	–	+5	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logic input signal levels; DATA, CLK, $\overline{E}$ and HPD						
V_{IH}	HIGH level input voltage	at logic 1	$0.7V_{DD1}$	–	V_{DD1} + 0.3	V
V_{IL}	LOW level input voltage	at logic 0	−0.3	–	$0.3V_{DD1}$	V
I_{bias}	input bias currents	at logic 1 or logic 0	−5	–	+5	μA
C_I	input capacitance	indicative, not tested	–	1	–	pF
Port outputs/Out-of-lock; P0/OOL, P1, P2, P3 and f_{XTALO} - open drain outputs						
V_{OL}	LOW level output voltage	I_{sink} = 0.4 mA	–	–	0.4	V

SERIAL TIMING CHARACTERISTICS

V_{DD1} = 3 V; T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r, t_f	input rise and fall times	–	10	40	ns
t_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	−20	–	–	ns
t_W	minimum inactive pulse width	2000	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

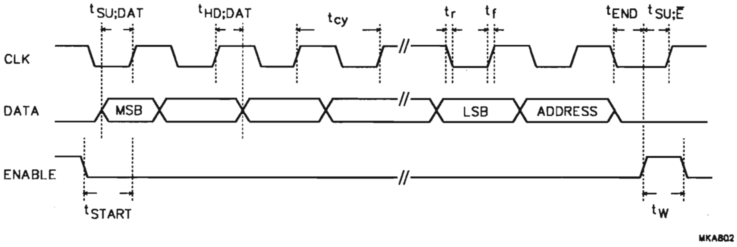
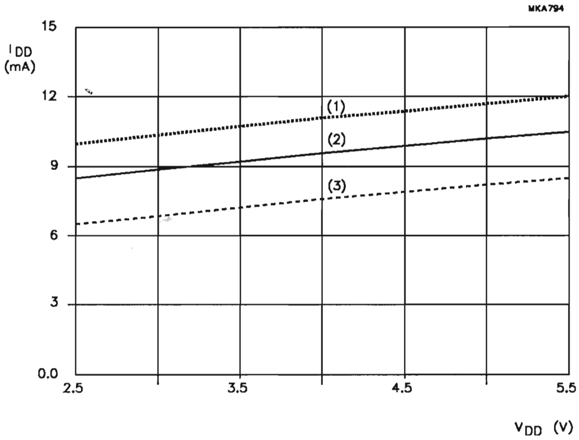


Fig.3 Serial bus timing diagram.

TYPICAL PERFORMANCE CHARACTERISTICS

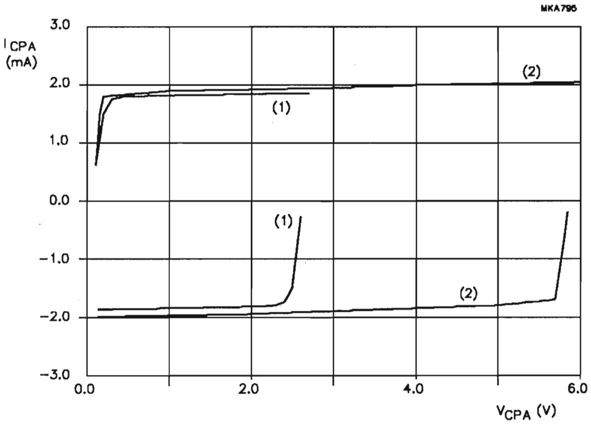


(1) T_{amb} = +85 °C.

(2) T_{amb} = +25 °C.

(3) T_{amb} = −30 °C.

Fig.4 I_{DD} as a function of V_{DD} with both synthesizers on and voltage doubler disabled.

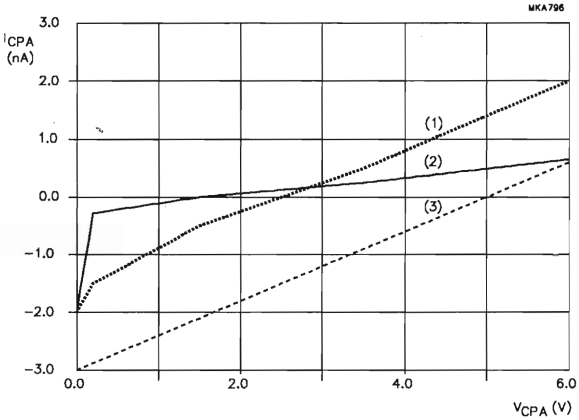


R_{SET} = 15 kΩ; CRA = 1.

(1) V_{CC} = 2.7 V.

(2) V_{CC} = 6.0 V.

Fig.5 Charge pump current as a function of CPA voltage.



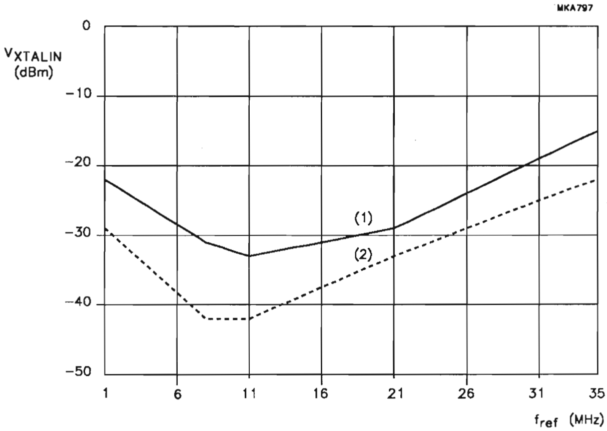
R_{SET} = 15 kΩ; CRA = 1.

(1) T_{amb} = +85 °C.

(2) T_{amb} = +25 °C.

(3) T_{amb} = −30 °C.

Fig.6 Charge pump 3-state current as a function of CPA voltage.

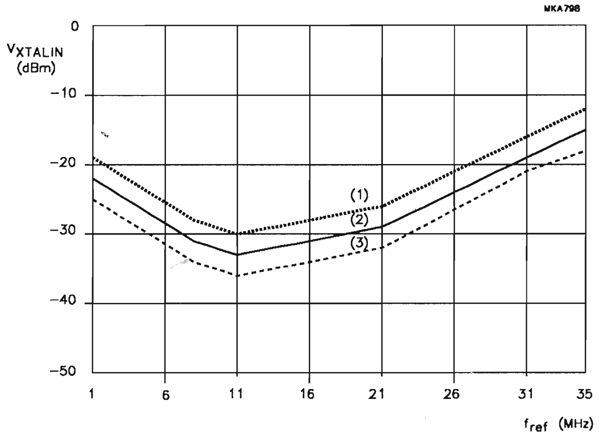


f_{XTALIN} externally terminated by 50 Ω load; AC-coupled.

(1) V_{DD} = 5.5 V.

(2) V_{DD} = 2.7 V.

Fig.7 Reference input sensitivity as a function of input frequency.



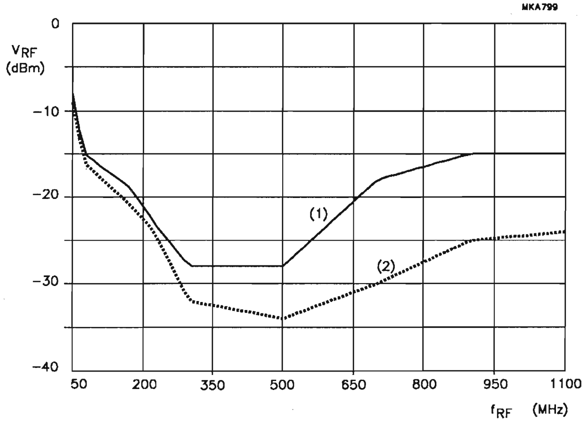
f_{XTALIN} externally terminated by 50 Ω load; AC-coupled.

(1) T_{amb} = −30 °C.

(2) T_{amb} = +25 °C.

(3) T_{amb} = +85 °C.

Fig.8 Reference input sensitivity as a function of input frequency with V_{DD} = 5.5 V.

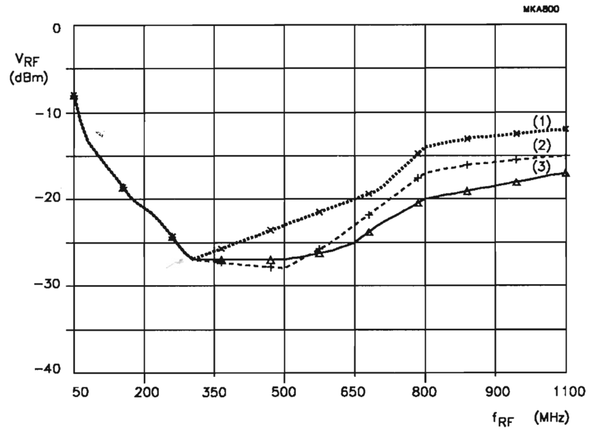


RF input externally terminated by 50 Ω load; AC-coupled.

(1) V_{DD} = 5.5 V.

(2) V_{DD} = 2.7 V.

Fig.9 RF input sensitivity as a function of input frequency.



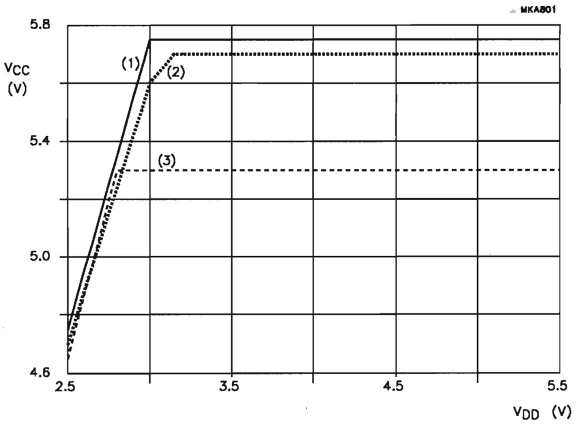
RF input externally terminated by 50 Ω load; AC-coupled.

(1) T_{amb} = −30 °C.

(2) T_{amb} = +25 °C.

(3) T_{amb} = +85 °C.

Fig.10 RF input sensitivity as a function of input frequency with V_{DD} = 5.5 V.

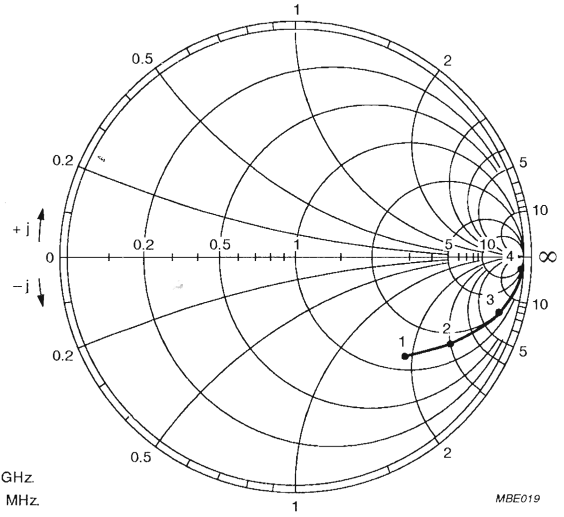


(1) T_{amb} = −30 °C.

(2) T_{amb} = +25 °C.

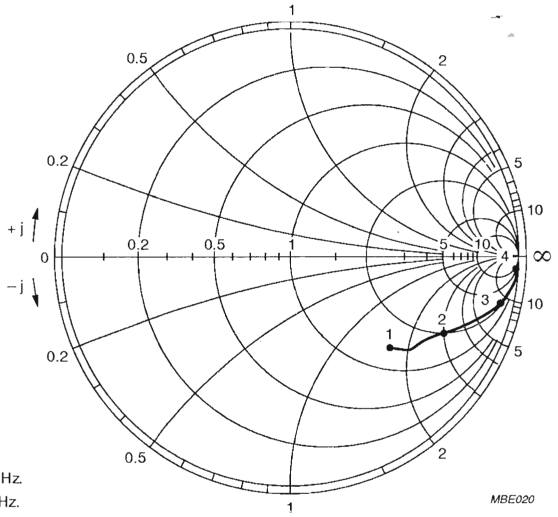
(3) T_{amb} = +85 °C.

Fig.11 Typical charge pump supply voltage as a function of V_{DD} voltage with voltage doubler enabled.



(1) 68.316 Ω, −92.457 Ω at 1.1 GHz.
(2) 85.914 Ω, −152.08 Ω at 800 MHz.
(3) 102.83 Ω, −354.66 Ω at 400 MHz.
(4) 853.75 Ω, −2.7735 kΩ at 50 MHz.

Fig.12 Input impedance as a function of input frequency; synthesizer A.



(1) 69.293 Ω, −78.027 Ω at 1.1 GHz.
(2) 100.2 Ω, −148.37 Ω at 800 MHz.
(3) 128.22 Ω, −378.81 Ω at 400 MHz.
(4) 674.25 Ω, −3.06 kΩ at 50 MHz.

Fig.13 Input impedance as a function of input frequency; synthesizer B.

APPLICATION INFORMATION

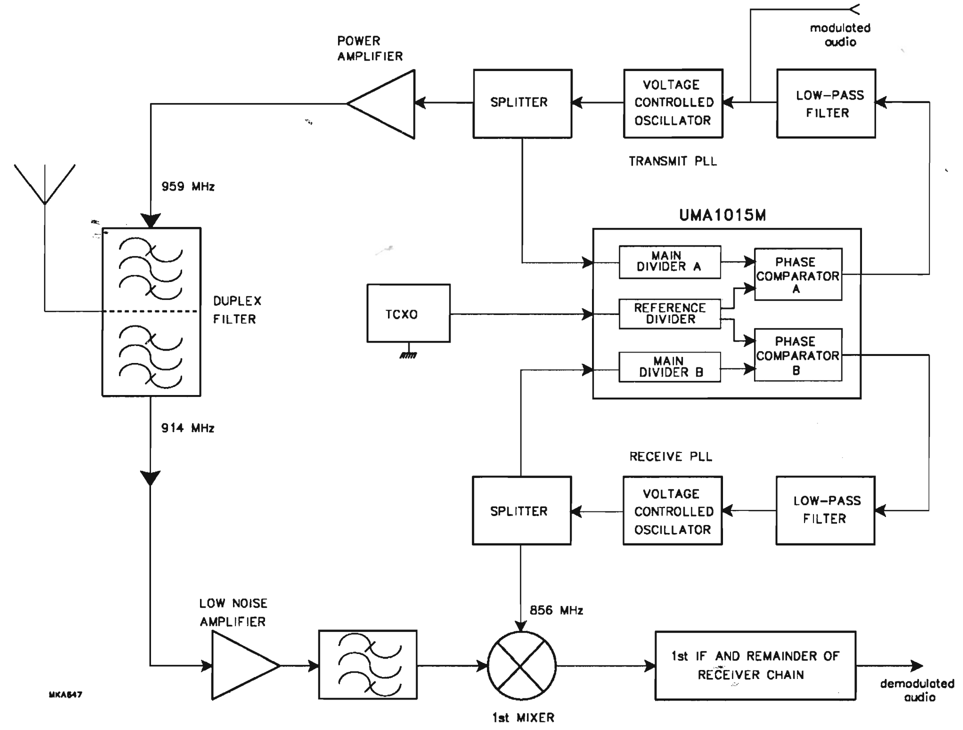


Fig.14 Typical application block diagram.

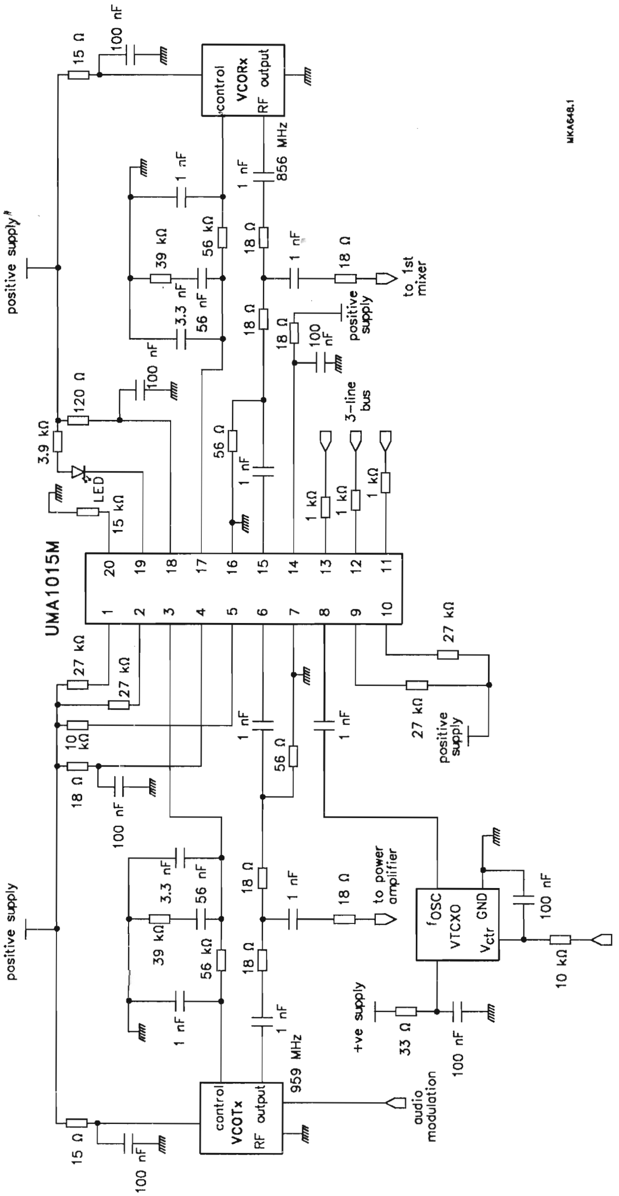


Fig.15 Typical CT1 application.

Transmit frequency = 959 MHz.
Receive frequency = 914 MHz.
1st IF = 58.1125 MHz.
2nd IF = 455 MHz.
VCO sensitivity = 2 MHz/V.
Channel spacing = 12.5 kHz.
Charge pump gain (CPA = CPB) = 1 mA/cycle.

Low-voltage frequency synthesizer for radiotelephones UMA1017M

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Independent fully programmable reference divider, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Dual power-down modes.

APPLICATIONS

- 900 MHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1017M BICMOS device integrates prescalers, a programmable divider, and phase comparator to implement a phase-locked loop. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The synthesizer operates at VCO input frequencies up to 1.2 GHz. The synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} may be higher than V_{DD} i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range.

The phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	supply current		–	6.9	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	12	–	μA
f_{VCO}	input frequency		50	–	1200	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PC}	phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1017M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

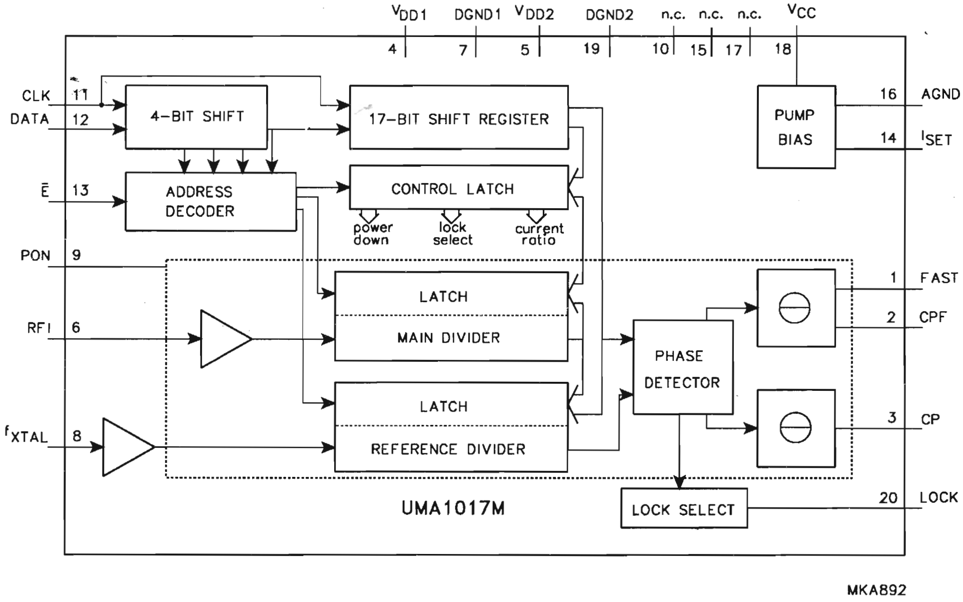


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPF	2	speed-up charge-pump output
CP	3	normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
RFI	6	1 GHz RF divider input
DGND1	7	digital ground 1
f_{XTAL}	8	reference frequency input from crystal oscillator
PON	9	power-on input
n.c.	10	not connected
CLK	11	serial clock input
DATA	12	serial data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
n.c.	15	not connected
AGND	16	analog ground
n.c.	17	not connected
V_{CC}	18	supply for charge-pump
DGND2	19	digital ground 2
LOCK	20	in-lock detect output; test mode output

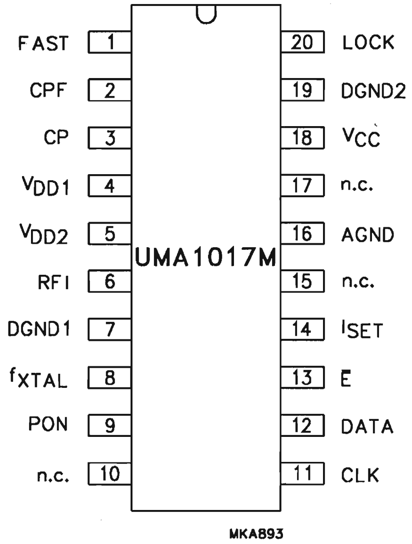


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

Programmable reference and main dividers drive the phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input PON (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The RFI input (pin 6) drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 50 mV up to 300 mV (RMS), and at frequencies as high as 1.2 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divide ratios (512 to 131 071) allow a 1 MHz phase comparison with the 500 MHz inputs, and a 10 kHz phase comparison at 1.2 GHz RF.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to improve noise and breakthrough levels.

The synthesizer speed-up charge pump (CPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector providing improved linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen to be of sufficient value to keep the sink current in the LOW state to below 400 μA. The output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison an out-of-lock or an in-lock flag is generated.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down.

However when the synthesizer is powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1017M uses 4 of the 16 available addresses. These are chosen to allow direct compatibility with the UAA2072M integrated front-end. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

Power-down mode

The power-down signal can be either hardware (POFF) or software (sPOFF). The dividers are on when both POFF and sPOFF are at logic 0.

When the synthesizer is reactivated after power-down the main and reference dividers are synchronized to avoid possibility of random phase errors on power-up.

Table 1 Format of programmed data

LAST IN	**PROGRAMMING REGISTER BIT USAGE**							**FIRST IN**
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT	**REGISTER BIT ALLOCATION**																			**LT**
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
TEST BITS[2]																	0	0	0	0
X	X	X	X	OOL	X	CR1	CR0	X	X	sPON	X	X	X	X	X	X	0	0	0	1
PM16	MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1

Notes

1. FT = first, LT = last; sPON = software power-up for synthesizer (1 = ON); OOL = out-of-lock (1 = enabled).
2. The test register is not to be programmed. Normally all bits of the test register must be set to zero.

Table 3 Fast and normal charge pumps current ratio (note 1)

CR1	**CR0**	I_{CP}	I_{CPF}	$I_{CPF} : I_{CP}$
0	0	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; bias current for charge pumps.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
$\Delta V_{CC}-V_{DD}$	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8, 9, 11 to 14 and 20	−0.3	V_{DD} + 0.3	V
$V_{2, 3}$	voltage at pins 2 and 3	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	–	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

All values refer to the typical measurement circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	synthesizer digital supply current	V_{DD} = 5.5 V	–	6.5	8.5	mA
I_{CC}	charge pumps analog supply current	V_{CC} = 5.5 V; R_{ext} =12 kΩ	–	0.4	1.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 or V_{DD}	–	12	50	μA
RF main divider input; pin 6						
f_{VCO}	VCO input frequency	2.7 V < V_{DD} < 4.5 V	50	–	1200	MHz
		2.7 V < V_{DD} < 5.5 V	50	–	1100	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	R_s = 50 Ω; 2.7 V < V_{DD} < 3.5 V; 0.5 < f_{VCO} < 1.2 GHz	50	–	300	mV
		R_s = 50 Ω; 2.7 V < V_{DD} < 5.5 V; 0.5 < f_{VCO} < 1.1 GHz	100	–	300	mV
		R_s = 50 Ω; 2.7 V < V_{DD} < 5.5 V; 50 < f_{VCO} < 500 MHz	150	–	300	mV
Z_I	input impedance (real part)	f_{VCO} = 1 GHz	–	1	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_m	main divider ratio		512	–	131071	
f_{PCmax}	maximum loop comparison frequency		–	2000	–	kHz
f_{PCmin}	minimum loop comparison frequency		–	10	–	kHz
Synthesizer reference divider input; pin 8						
f_{XTAL}	input frequency range from crystal		3	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	5 MHz < f_{XTAL} < 40 MHz	50	–	500	mV
		3 MHz < f_{XTAL} < 40 MHz	100	–	500	mV
Z_I	input impedance (real part)	f_{XTAL} = 30 MHz	–	2	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_r	reference division ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	R_{ext} = 12 kΩ	–	1.15	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Charge pump outputs; pins 3 and 2; R_{ext} = 12 kΩ						
I_{Ocp}	charge pump output current error		−25	−	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	−	±5	−	%
I_{Lcp}	charge pump off leakage current	$V_{cp} = \frac{1}{2}V_{CC}$	−5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	−	$V_{CC} - 0.4$	V
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	$V_{DD} + 0.3$	V
V_{IL}	LOW level input voltage		−0.3	−	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	−5	−	+5	μA
C_I	input capacitance	indicative, not tested	−	2	−	pF
Lock detect output signal; pin 20 (open-drain output)						
V_{OL}	LOW level output voltage	I_{sink} = 0.4 mA	−	−	0.4	V

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	2000(1)	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 2 μs provided all the following conditions are satisfied:
   a) Main divider input frequency $f_{VCO} > \frac{256}{t_W}$
   b) Reference dividers input frequency $f_{XTAL} > \frac{3}{t_W}$.

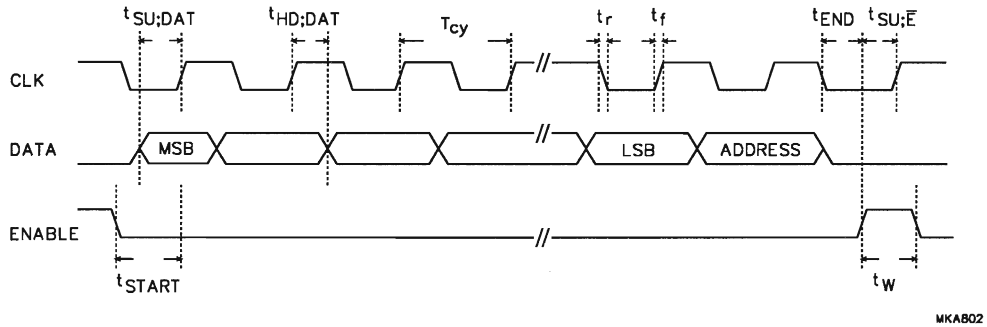


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

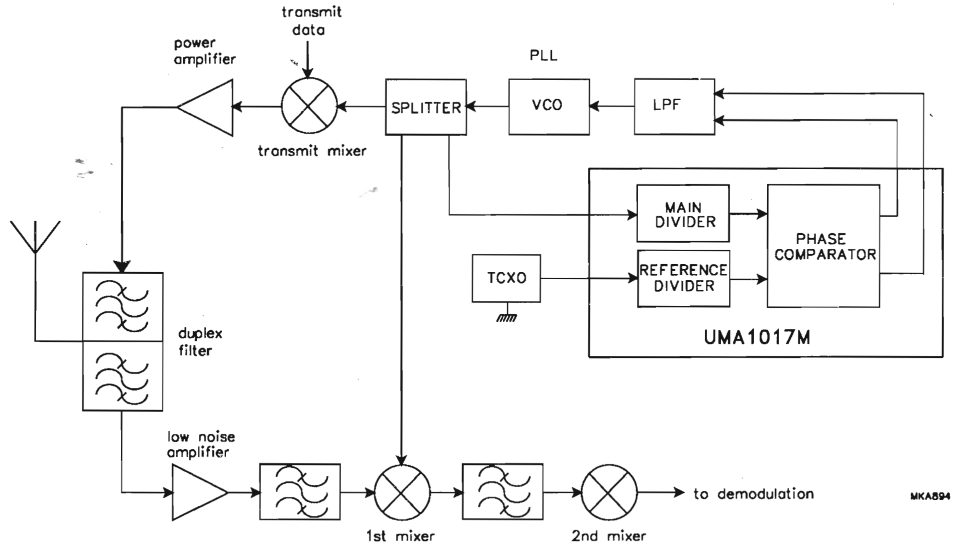


Fig.4 Typical application block diagram.

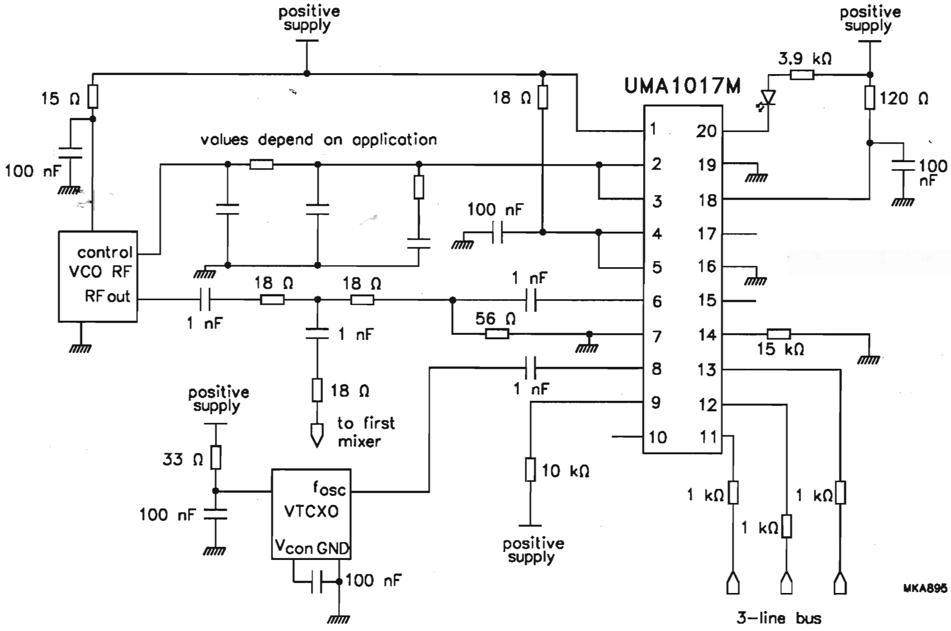


Fig.5 Typical test and application diagram.

Low-voltage dual frequency synthesizer for radio telephones

UMA1018M

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Second synthesizer to control first IF or offset loop frequency
- Independent fully programmable reference dividers for each loop, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Integrated digital-to-analog converter
- Dual power-down modes.

APPLICATIONS

- 900 MHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1018M BICMOS device integrates prescalers, programmable dividers, and phase comparators to implement two phase-locked loops. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The principal synthesizer operates at VCO input frequencies up to1.2 GHz the auxiliary synthesizer operates at 300 MHz. The auxiliary loop is intended for the first IF or to transmit offset loop-frequency settings. Each synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} may be higher than V_{DD} i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range.

The principal synthesizer phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. The auxiliary loop has a separate phase detector. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance. An on-chip 8-bit DAC enables adjustment of an external function, such as the temperature compensation of a crystal oscillator in Global System for Mobile communications (GSM).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	principal synthesizer supply current	auxiliary synthesizer in power-down mode	–	6.9	–	mA
	principal and auxiliary synthesizer supply current	principal and auxiliary synthesizer ON	–	9.6	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	12	–	μA
f_{PI}	principal input frequency		50	–	1200	MHz
f_{AI}	auxiliary input frequency		20	–	300	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PPC}	principal phase comparator frequency		–	200	–	kHz
f_{APC}	auxiliary phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

Low-voltage dual frequency synthesizer for radio telephones

UMA1018M

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1018M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

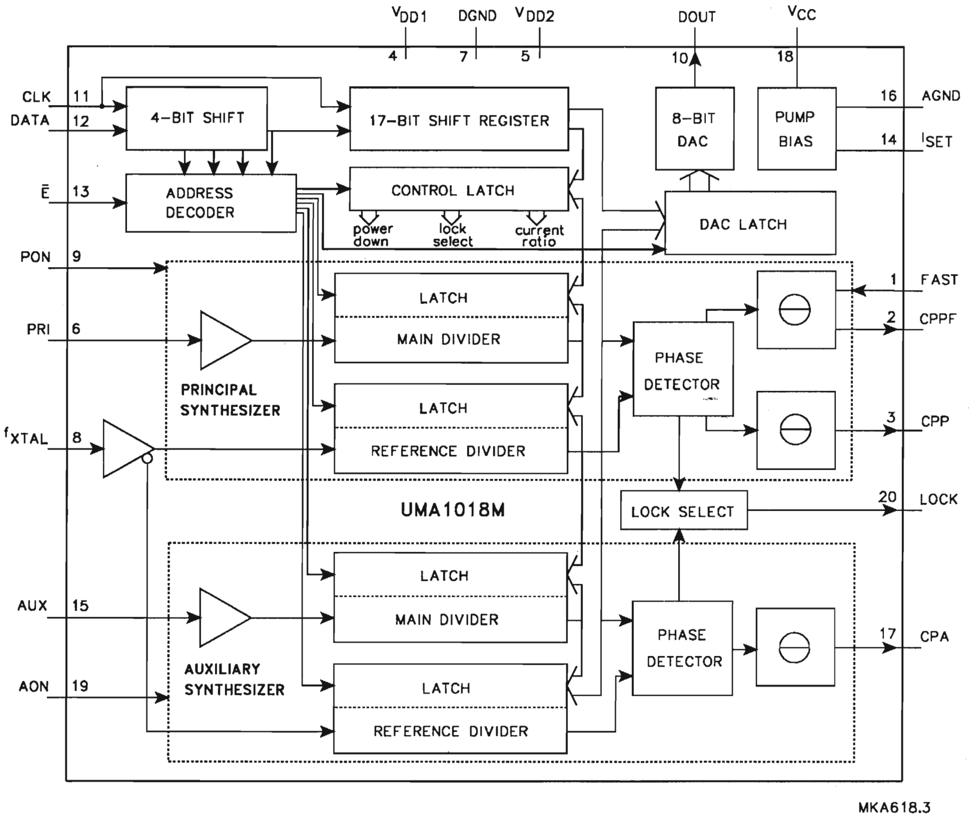


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPPF	2	principal synthesizer speed-up charge-pump output
CPP	3	principal synthesizer normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
PRI	6	1 GHz principal synthesizer RF divider input
DGND	7	digital ground
f_{XTAL}	8	common reference frequency input from crystal oscillator
PON	9	principal synthesizer power-on input
DOUT	10	8-bit digital-to-analog output
CLK	11	serial clock input
DATA	12	serial data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
AUX	15	auxiliary synthesizer frequency input
AGND	16	analog ground
CPA	17	auxiliary synthesizer charge-pump output
V_{CC}	18	supply for charge-pump and DAC circuits
AON	19	auxiliary synthesizer power-on input
LOCK	20	in-lock detect output (main PLL); test mode output

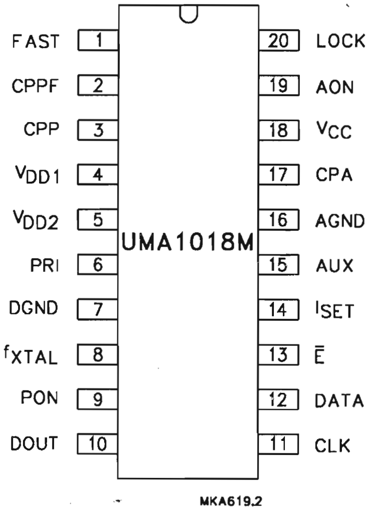


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Principal synthesizer

Programmable reference and main dividers drive the principal PLL phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input PON (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The PRI input (pin 6) drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 50 mV up to 300 mV (RMS), and at frequencies as high as 1.2 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divide ratios (512 to 131 071) allow a 1 MHz phase comparison with the 500 MHz inputs, and a 10 kHz phase comparison at 1.2 GHz RF.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus.

The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to improve noise and breakthrough levels.

The principal synthesizer speed-up charge pump (CPPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector providing improved linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen such that the value is high enough to keep the sink current in the LOW state below 400 μA. The circuit can be programmed to output either the phase error in the principal or auxiliary phase detectors or the combination from both detectors (OR function). The resultant output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison an out-of-lock or an in-lock flag is generated.

Auxiliary synthesizer

The auxiliary synthesizer has a 14-bit main divider and an 11-bit reference divider. A separate power-down input AON (pin 19), disables currents in the auxiliary dividers, phase detector, and charge pump. The auxiliary input signal is amplified and fed to the main divider. The input buffer presents a high impedance, dominated by pin and pad capacitance. First divider stages use bipolar technology operating at input frequencies up to 300 MHz; the slower bits are CMOS. The auxiliary loop phase detector and charge pump use similar circuits to the main loop low-current phase comparator, including dead-zone compensation feedback.

The auxiliary reference divider is clocked on the opposite edge of the main reference divider to ensure that active edges arrive at the auxiliary and principal phase detectors at different times. This minimizes the potential for interference between the charge pumps of each loop.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down of main and auxiliary loops.

However when either principal synthesizer or auxiliary synthesizer or both are powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1018M uses 6 of the 16 available addresses. These are chosen to allow direct compatibility with the UAA2072M integrated front-end. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

Table 1 Format of programmed data

LAST IN	PROGRAMMING REGISTER BIT USAGE							FIRST IN
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT	REGISTER BIT ALLOCATION																			LT
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
TEST BITS(2)																	0	0	0	0
X	X	X	X	OLP	OLA	CR1	CR0	X	X	sPON	sAON	X	X	X	X	X	0	0	0	1
PM16	PRINCIPAL MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	PRINCIPAL REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1
X	X	X	AM13	AUXILIARY MAIN DIVIDER COEFFICIENT												AM0	0	1	1	0
X	X	X	X	X	X	AR10	AUXILIARY REFERENCE DIVIDER COEFFICIENT									AR0	0	1	1	1
X	X	X	X	X	X	X	X	X	DA7	8-BIT DAC FOR EXTERNAL TRIM						DA0	1	0	0	0

Notes

1. FT = first, LT = last; sPON = software power-up for principal synthesizer (1 = ON); sAON = software power-up for auxiliary synthesizer (1 = ON).
2. The test register is not to be programmed. Normally all bits of the test register must be set to zero.

Table 3 Out-of-lock select

OLP	OLA	OUT-OF-LOCK ON PIN 20
0	0	output disabled
0	1	auxiliary phase error
1	0	principal phase error
1	1	both auxiliary and principal

Table 4 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CPA}	I_{CPP}	I_{CPPF}	$I_{CPPF} : I_{CPP}$
0	0	$4 \times I_{SET}$	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$4 \times I_{SET}$	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$4 \times I_{SET}$	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; common bias current for charge pumps and DAC.

Table 5 Power-down modes

AON	PON	FAST	PRINCIPAL DIVIDERS	AUXILIARY DIVIDERS	PUMP CPA	PUMP CPP	PUMP CPPF	DAC AND BIAS
0	0	X	OFF	OFF	OFF	OFF	OFF	OFF
0	1	0	ON	OFF	OFF	ON	OFF	ON
0	1	1	ON	OFF	OFF	ON	ON	ON
1	0	X	OFF	ON	ON	OFF	OFF	ON
1	1	0	ON	ON	ON	ON	OFF	ON
1	1	1	ON	ON	ON	ON	ON	ON

Digital-to-analog converter

The byte loaded via the bus into the appropriate latch drives a digital-to-analog converter. The internal current is scaled by the external resistance (R_{ext}) at pin I_{SET}, similar to the charge pumps. The nominal full-scale current is $4 \times I_{SET}$. The output current is mirrored to produce a full-scale voltage into a user-defined ground referenced resistance, thereby allowing optimum swing from power supply rails within the 2.7 to 5.5 V limits. The band gap reference voltage at pin I_{SET} is temperature and supply independent. The DAC signal is monotonic across the full range of digital input codes to enable fine adjustment of other system blocks. The typical settling time for full-scale switching is 400 ns into a 12 kΩ // 20 pF load. DAC functionality is neither tested nor guaranteed on the UMA1018M/C1/S1 version.

Power-down modes

The action of the control inputs on the state of internal blocks is defined by Table 5.

Note that in Table 5 PON and AON can be either the software or hardware power-down signals. The dividers are ON when both hardware and software power-down signals are at logic 1.

When either synthesizer is reactivated after power-down the main and reference dividers of that synthesizer are synchronized to avoid the possibility of random phase errors on power-up.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
ΔV_{CC-DD}	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8 to 15, 19 and 20	−0.3	V_{DD} + 0.3	V
$V_{2, 3, 17}$	voltage at pins 2, 3 and 17	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	–	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

All values refer to the typical measurement circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	principal synthesizer digital supply current	V_{DD} = 5.5 V	–	6.5	8.5	mA
	auxiliary synthesizer digital supply current	V_{DD} = 5.5 V	–	2.7	4.0	mA
I_{CC}	charge pumps and DAC analog supply current (DAC setting FFH)	V_{CC} = 5.5 V; R_{ext} = 12 kΩ	–	0.4	1.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 or V_{DD}	–	12	50	μA
RF principal main divider input; pin 6						
f_{VCO}	VCO input frequency	2.7 V < V_{DD} < 4.5 V	50	–	1200	MHz
		2.7 V < V_{DD} < 5.5 V	50	–	1100	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	R_s = 50 Ω; 2.7 V < V_{DD} < 3.5 V; 0.5 < f_{VCO} < 1.2 GHz	50	–	300	mV
		R_s = 50 Ω; 2.7 V < V_{DD} < 5.5 V; 0.5 < f_{VCO} < 1.1 GHz	100	–	300	mV
		R_s = 50 Ω; 2.7 V < V_{DD} < 5.5 V; 50 < f_{VCO} < 500 MHz	150	–	300	mV
Z_I	input impedance (real part)	f_{VCO} = 1 GHz	–	1	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pm}	principal main divider ratio		512	–	131071	
f_{PPCmax}	maximum principal loop comparison frequency		–	2000	–	kHz
f_{PPCmin}	minimum principal loop comparison frequency		–	10	–	kHz
Auxiliary loop main divider input; pin 15						
f_{AI}	input frequency		20	–	300	MHz
$V_{15(rms)}$	AC-coupled input signal level (RMS value)	R_s = 50 Ω; 2.7 V < V_{DD} < 3.5 V	50	–	500	mV
		R_s = 50 Ω; 3.5 V < V_{DD} < 5.5 V	100	–	500	mV
Z_I	input impedance (real part)	f_{AI} = 100 MHz	–	1	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{am}	auxiliary main divider ratio		64	–	16383	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{APCmax}	maximum auxiliary loop comparison frequency		–	2000	–	kHz
f_{APCmin}	minimum auxiliary loop comparison frequency		–	10	–	kHz
Dual synthesizer reference divider input; pin 8						
f_{XTAL}	input frequency range from crystal		3	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	5 MHz < f_{XTAL} < 40 MHz	50	–	500	mV
		3 MHz < f_{XTAL} < 40 MHz	100	–	500	mV
Z_I	input impedance (real part)	f_{XTAL} = 30 MHz	–	2	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pr}	principal reference division ratio		8	–	2047	
R_{ar}	auxiliary reference division ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	R_{ext} = 12 kΩ	–	1.15	–	V
Charge pump outputs; pins 17, 3 and 2; R_{ext} = 12 kΩ						
I_{Ocp}	charge pump output current error		–25	–	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	–	±5	–	%
I_{Lcp}	charge pump off leakage current	$V_{cp} = \frac{1}{2}V_{CC}$	–5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	$V_{CC} - 0.4$	V
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.3$	V
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	–5	–	+5	μA
C_I	input capacitance	indicative, not tested	–	2	–	pF
DAC output signal levels; pin 10, R_{ext} = 12 kΩ						
I_{DAC}	DAC full scale output current		$3 \times I_{SET}$	$4 \times I_{SET}$	$5 \times I_{SET}$	mA
V_{10}	output voltage compliance	all codes	0	–	$V_{DD} - 0.4$	V
I_{10min}	minimum DAC current	00 code	–	2	5	μA
I_{monot}	worst case monotonicity test: $\Delta I \times 256/400$ μA	note 1	0.1	–	1.9	
Lock detect output signal; pin 20 open-drain output						
V_{OL}	LOW level output voltage	I_{sink} = 0.4 mA	–	–	0.4	V

Note

1. ΔI is the change in DAC output current when making the code transitions: 7FH/80H, 3FH/40H or 1FH/20H.

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	2000(1)	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 2 μs provided all the following conditions are satisfied:
   a) Principal main divider input frequency $f_{VCO} > \frac{256}{t_W}$
   b) Auxiliary main divider input frequency $f_{AI} > \frac{32}{t_W}$
   c) Reference dividers input frequency $f_{XTAL} > \frac{3}{t_W}$

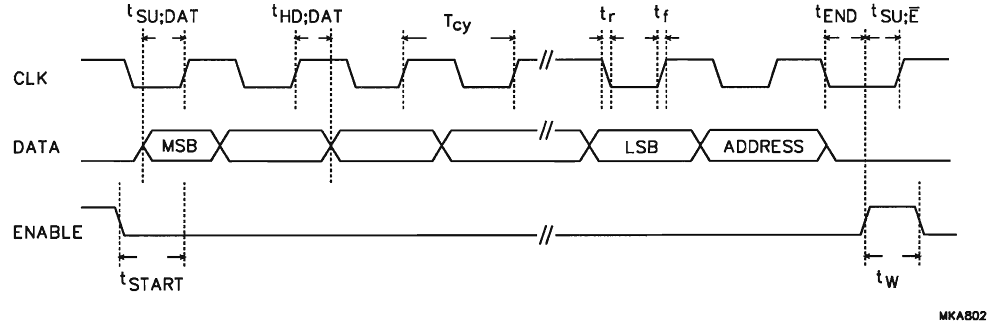


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

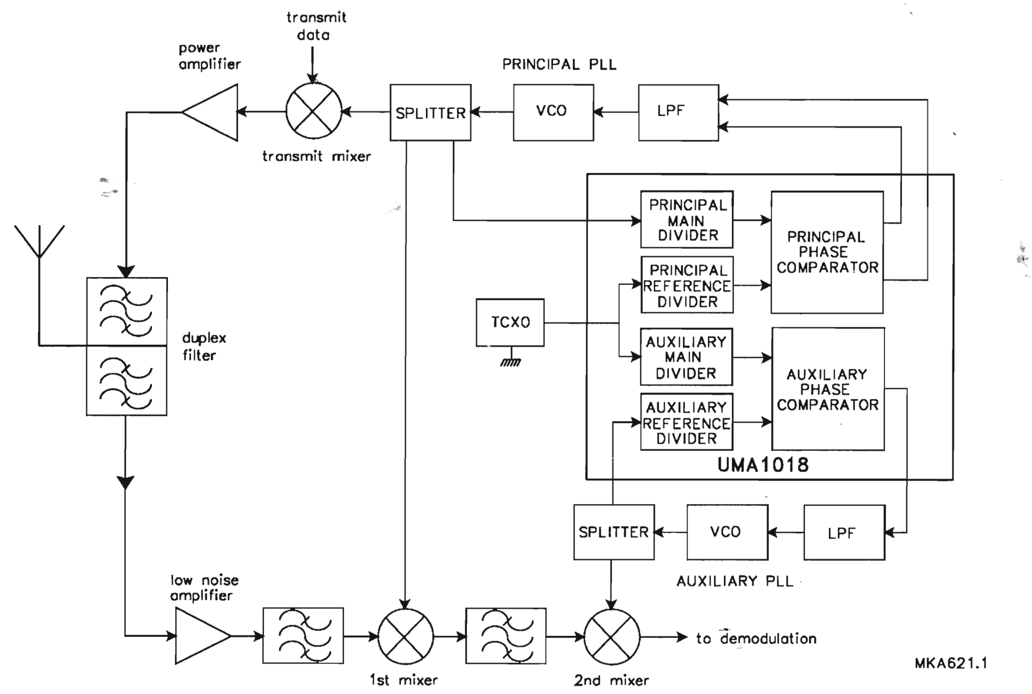


Fig.4 Typical application block diagram.

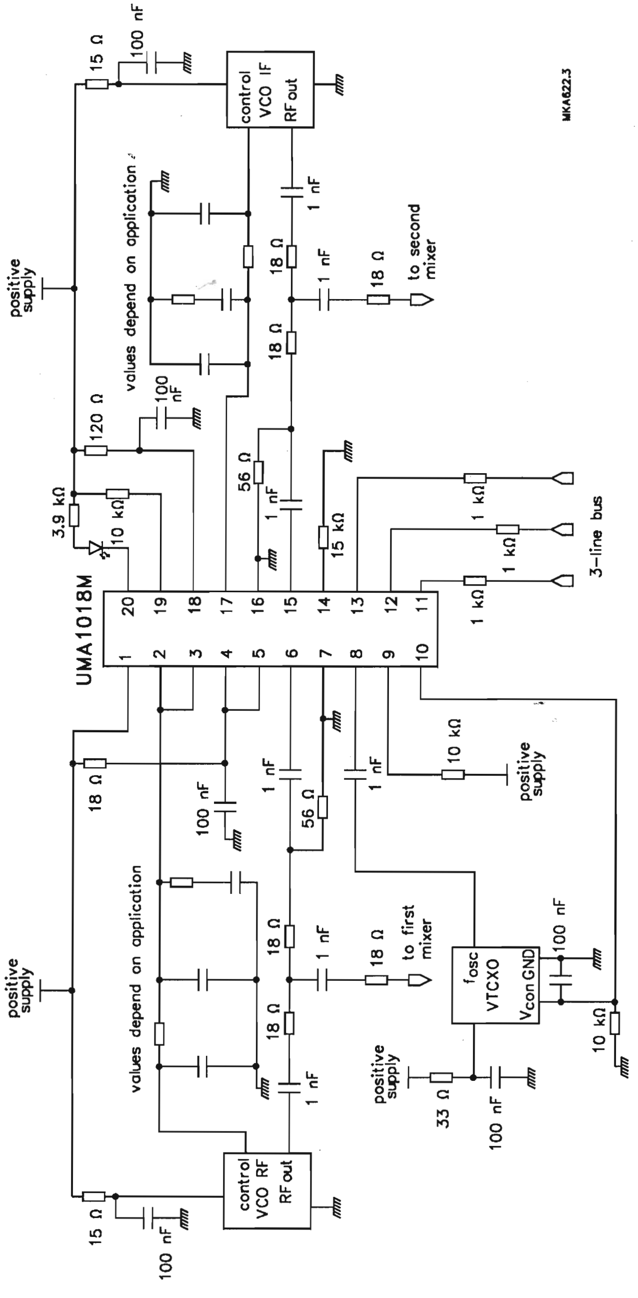


Fig.5 Typical test and application diagram.

Low-voltage frequency synthesizer for radio telephones UMA1019AM

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Independent fully programmable reference divider, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Dual power-down modes.

APPLICATIONS

- 1 to 1.7 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1019AM BICMOS device integrates prescalers, a programmable divider, and phase comparator to implement a phase-locked loop. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The synthesizer operates at VCO input frequencies up to 1.7 GHz. The synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} may be higher than V_{DD} i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range.

The phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	supply current		–	9.4	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	12	–	μA
f_{VCO}	input frequency		1000	1500	1700	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PC}	phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1019AM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

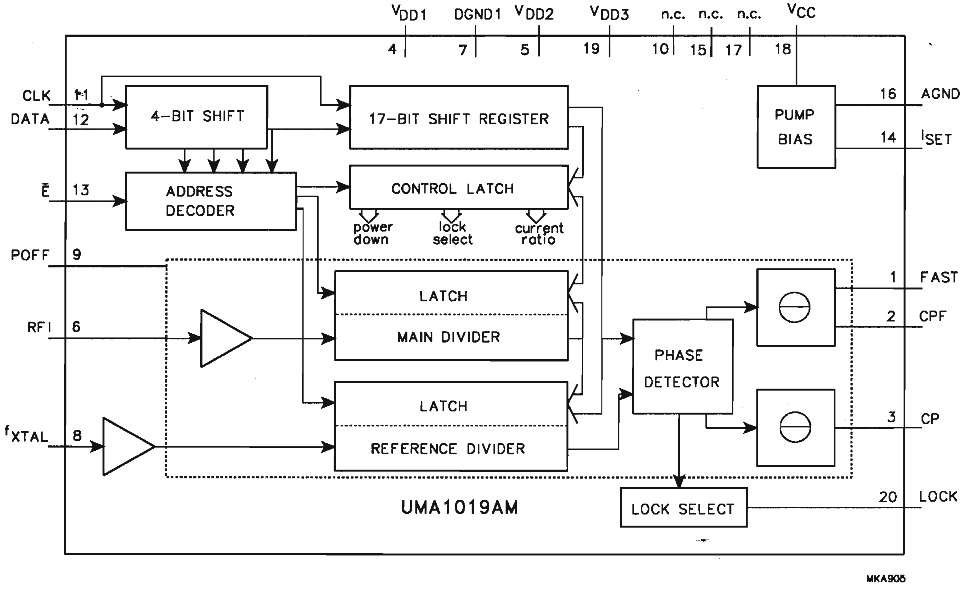


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPF	2	speed-up charge-pump output
CP	3	normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
RFI	6	1 GHz RF divider input
DGND1	7	digital ground 1
f_{XTAL}	8	reference frequency input from crystal oscillator
POFF	9	power-down input
n.c.	10	not connected
CLK	11	serial clock input
DATA	12	serial data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
n.c.	15	not connected
AGND	16	analog ground
n.c.	17	not connected
V_{CC}	18	supply for charge-pump
V_{DD3}	19	digital power supply 3
LOCK	20	in-lock detect output; test mode output

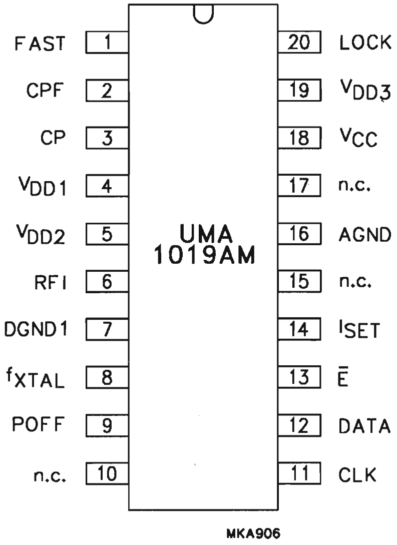


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

Programmable reference and main dividers drive the phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input POFF (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The RFI input (pin 6) drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 100 mV up to 500 mV (RMS), and at frequencies as high as 1.7 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divide ratios (512 to 131 071) allow up to 2 MHz phase comparison frequency.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to improve noise and breakthrough levels.

The synthesizer speed-up charge pump (CPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector providing improved linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen to be of sufficient value to keep the sink current in the LOW state to below 400 μA. The output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison an out-of-lock or an in-lock flag is generated.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down.

However when the synthesizer is powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1019AM uses 4 of the 16 available addresses. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

Power-down mode

The power-down signal can be either hardware (POFF) or software (sPOFF). The dividers are on when both POFF and sPOFF are at logic 0.

When the synthesizer is reactivated after power-down the main and reference dividers are synchronized to avoid possibility of random phase errors on power-up.

Table 1 Format of programmed data

LAST IN	**PROGRAMMING REGISTER BIT USAGE**							**FIRST IN**
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT	**REGISTER BIT ALLOCATION**																			**LT**
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
TEST BITS$^{(2)}$																	0	0	0	0
X	X	X	X	OOL	X	CR1	CR0	X	X	sPOFF	X	X	X	X	X	X	0	0	0	1
PM16	MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1

Notes

1. FT = first, LT = last; sPOFF = software power-down for synthesizer (1 = OFF); OOL = out-of-lock (1 = enabled).
2. The test register is not to be programmed. Normally all bits of the test register must be set to zero.

Table 3 Fast and normal charge pumps current ratio (note 1)

CR1	**CR0**	I_{CP}	I_{CPF}	$I_{CPF} : I_{CP}$
0	0	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; bias current for charge pumps.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
$\Delta V_{CC}-V_{DD}$	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8, 9, 11 to 14 and 20	−0.3	V_{DD} + 0.3	V
$V_{2,\,3}$	voltage at pins 2 and 3	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	–	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

All values refer to the typical measurement circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2} = V_{DD3}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	synthesizer digital supply current	$V_{DD} = 5.5$ V	–	9	11	mA
I_{CC}	charge pumps analog supply current	$V_{CC} = 5.5$ V; $R_{ext} = 12$ kΩ	–	0.4	1.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 or V_{DD}	–	12	50	µA
RF main divider input; pin 6						
f_{VCO}	VCO input frequency		1000	1500	1700	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50$ Ω	100	–	500	mV
Z_I	input impedance (real part)	$f_{VCO} = 2$ GHz	–	300	–	Ω
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_m	main divider ratio		512	–	131071	
f_{PCmax}	maximum loop comparison frequency		–	2000	–	kHz
f_{PCmin}	minimum loop comparison frequency		–	10	–	kHz
Synthesizer reference divider input; pin 8						
f_{XTAL}	input frequency range from crystal		3	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	5 MHz < f_{XTAL} < 40 MHz	50	–	500	mV
		3 MHz < f_{XTAL} < 40 MHz	100	–	500	mV
Z_I	input impedance (real part)	$f_{XTAL} = 30$ MHz	–	2	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_r	reference division ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	$R_{ext} = 12$ kΩ	–	1.15	–	V
Charge pump outputs; pins 3 and 2; R_{ext} = 12 kΩ						
I_{Ocp}	charge pump output current error		–25	–	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	–	±5	–	%
I_{Lcp}	charge pump off leakage current	$V_{cp} = \frac{1}{2}V_{CC}$	–5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	$V_{CC} - 0.4$	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.3$	V
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	–5	–	+5	μA
C_I	input capacitance	indicative, not tested	–	2	–	pF
Lock detect output signal; pin 20 (open-drain output)						
V_{OL}	LOW level output voltage	$I_{sink} = 0.4$ mA	–	–	0.4	V

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	2000(1)	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 2 μs provided all the following conditions are satisfied:
   a) Main divider input frequency $f_{VCO} > \frac{512}{t_W}$
   b) Reference dividers input frequency $f_{XTAL} > \frac{3}{t_W}$.

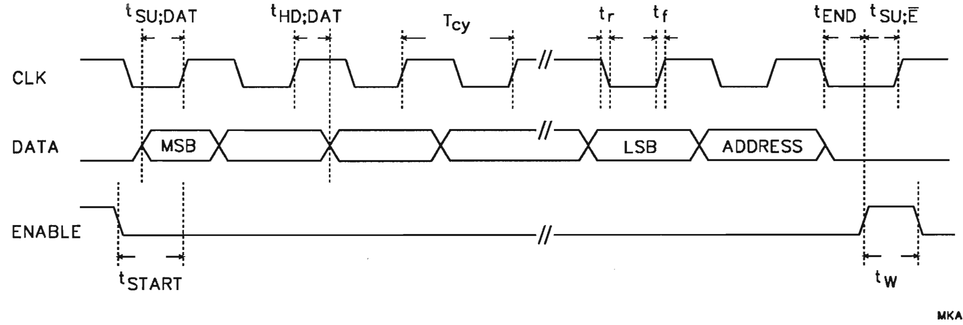


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

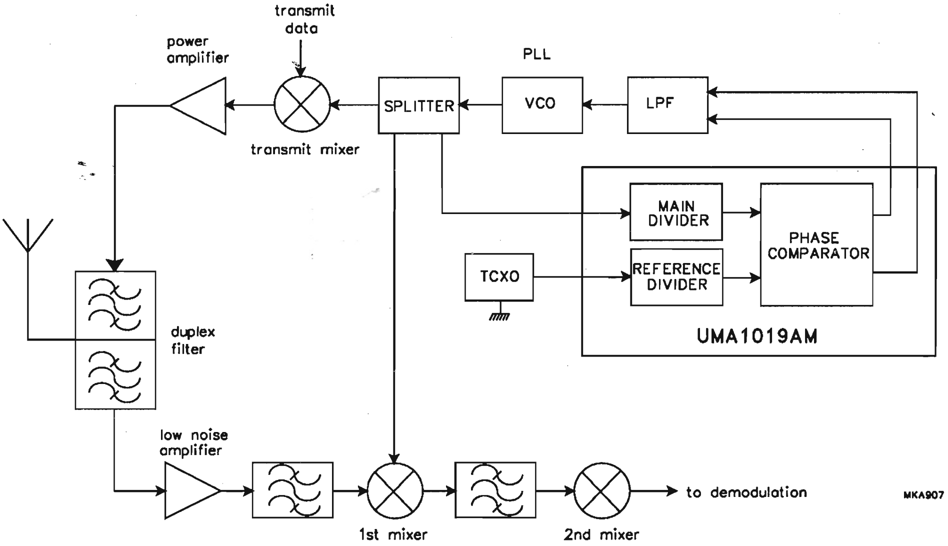


Fig.4 Typical application block diagram.

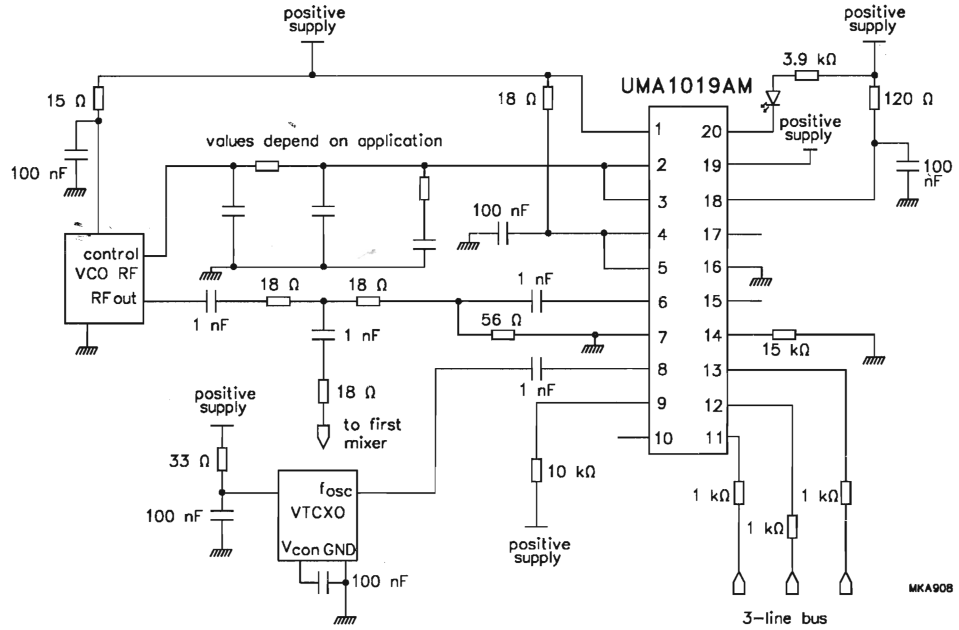


Fig.5 Typical test and application diagram.

Low-voltage dual frequency synthesizer for radio telephones

UMA1019M

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Independent fully programmable reference divider, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Dual power-down modes.

APPLICATIONS

- 2 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1019M BICMOS device integrates prescalers, a programmable divider, and phase comparator to implement a phase-locked loop. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The synthesizer operates at VCO input frequencies up to 2.4 GHz. The synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} may be higher than V_{DD} i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range.

The phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	supply current		–	9.4	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	12	–	μA
f_{VCO}	input frequency		1650	1900	2400	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PC}	phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1019M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

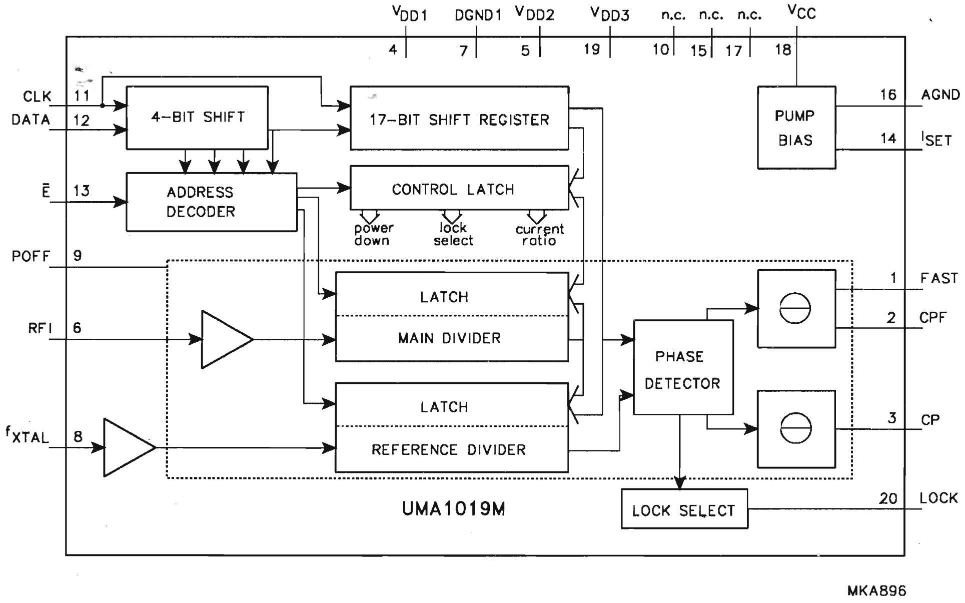


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPF	2	speed-up charge-pump output
CP	3	normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
RFI	6	1 GHz RF divider input
DGND1	7	digital ground 1
f_{XTAL}	8	reference frequency input from crystal oscillator
POFF	9	power-down input
n.c.	10	not connected
CLK	11	serial clock input
DATA	12	serial data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
n.c.	15	not connected
AGND	16	analog ground
n.c.	17	not connected
V_{CC}	18	supply for charge-pump
V_{DD3}	19	digital power supply 3
LOCK	20	in-lock detect output; test mode output

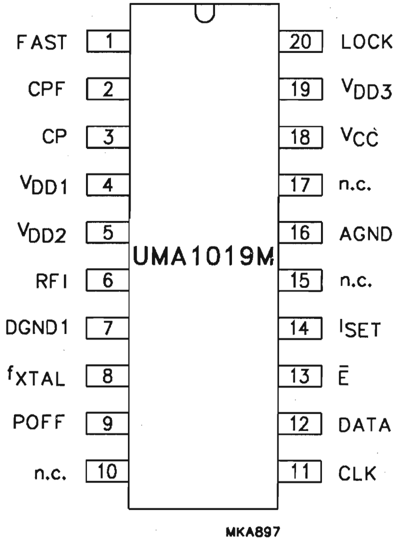


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

Programmable reference and main dividers drive the phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input POFF (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The RFI input (pin 6) drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 60 mV up to 180 mV (RMS), and at frequencies as high as 2.4 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divide ratios (512 to 131 071) allow a 2 MHz phase comparison frequency.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to improve noise and breakthrough levels.

The synthesizer speed-up charge pump (CPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector providing improved linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen to be of sufficient value to keep the sink current in the LOW state to below 400 μA. The output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison an out-of-lock or an in-lock flag is generated.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down.

However when the synthesizer is powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1019M uses 4 of the 16 available addresses. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

Power-down mode

The power-down signal can be either hardware (POFF) or software (sPOFF). The dividers are on when both POFF and sPOFF are at logic 0.

When the synthesizer is reactivated after power-down the main and reference dividers are synchronized to avoid possibility of random phase errors on power-up.

Table 1 Format of programmed data

LAST IN	PROGRAMMING REGISTER BIT USAGE							FIRST IN
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT	REGISTER BIT ALLOCATION																			LT
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
TEST BITS(2)																	0	0	0	0
X	X	X	X	OOL	X	CR1	CR0	X	X	sPOFF	X	X	X	X	X	X	0	0	0	1
PM16	MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1

Notes

1. FT = first, LT = last; sPOFF = software power-down for synthesizer (1 = OFF); OOL = out-of-lock (1 = enabled).
2. The test register is not to be programmed. Normally all bits of the test register must be set to zero.

Table 3 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CP}	I_{CPF}	$I_{CPF} : I_{CP}$
0	0	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; bias current for charge pumps.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
$\Delta V_{CC}-V_{DD}$	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8, 9, 11 to 14 and 20	−0.3	V_{DD} + 0.3	V
$V_{2,3}$	voltage at pins 2 and 3	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	–	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

All values refer to the typical measurement circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2} = V_{DD3}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	synthesizer digital supply current	$V_{DD} = 5.5$ V	–	9	11	mA
I_{CC}	charge pumps analog supply current	$V_{CC} = 5.5$ V; R_{ext} =12 kΩ	–	0.4	1.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 or V_{DD}	–	12	50	μA
RF main divider input; pin 6						
f_{VCO}	VCO input frequency		1650	1900	2400	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50$ Ω; $1.65 < f_{VCO} < 2$ GHz	60	–	400	mV
		$R_s = 50$ Ω; $1.65 < f_{VCO} < 2.4$ GHz	60	–	180	mV
Z_I	input impedance (real part)	$f_{VCO} = 2$ GHz	–	300	–	Ω
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_m	main divider ratio		512	–	131071	
f_{PCmax}	maximum loop comparison frequency		–	2000	–	kHz
f_{PCmin}	minimum loop comparison frequency		–	10	–	kHz
Synthesizer reference divider input; pin 8						
f_{XTAL}	input frequency range from crystal		3	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	5 MHz < f_{XTAL} < 40 MHz	50	–	500	mV
		3 MHz < f_{XTAL} < 40 MHz	100	–	500	mV
Z_I	input impedance (real part)	$f_{XTAL} = 30$ MHz	–	2	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_r	reference division ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	R_{ext} = 12 kΩ	–	1.15	–	V
Charge pump outputs; pins 3 and 2; R_{ext} = 12 kΩ						
I_{Ocp}	charge pump output current error		–25	–	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	–	±5	–	%
I_{Lcp}	charge pump off leakage current	$V_{cp} = \frac{1}{2}V_{CC}$	–5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	$V_{CC} - 0.4$	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.3$	V
V_{IL}	LOW level input voltage		−0.3	–	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	−5	–	+5	μA
C_I	input capacitance	indicative, not tested	–	2	–	pF
Lock detect output signal; pin 20 (open-drain output)						
V_{OL}	LOW level output voltage	$I_{sink} = 0.4$ mA	–	–	0.4	V

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	2000[1]	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 2 μs provided all the following conditions are satisfied:
   a) Main divider input frequency $f_{VCO} > \frac{512}{t_W}$
   b) Reference dividers input frequency $f_{XTAL} > \frac{3}{t_W}$.

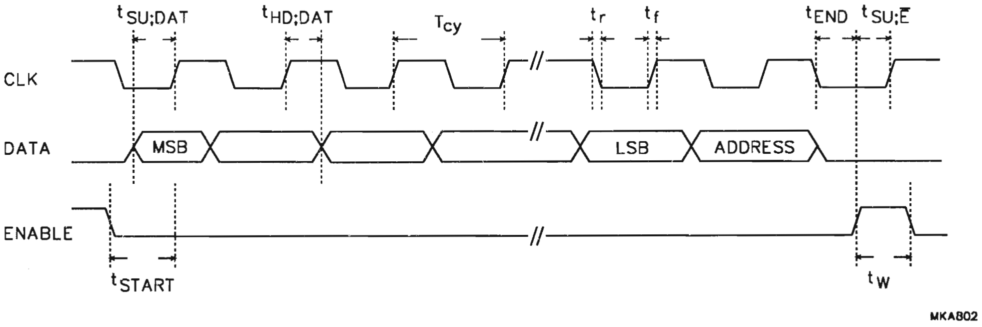


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

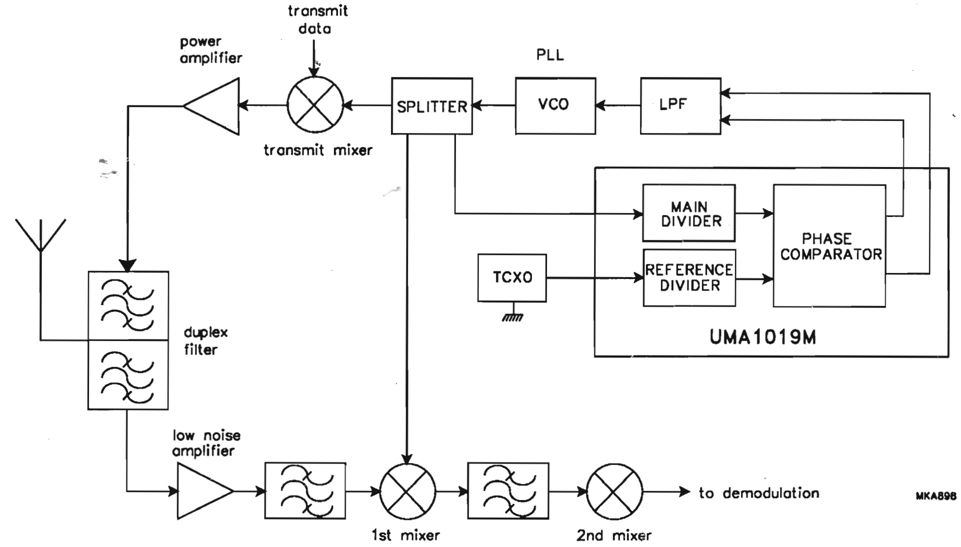


Fig.4 Typical application block diagram.

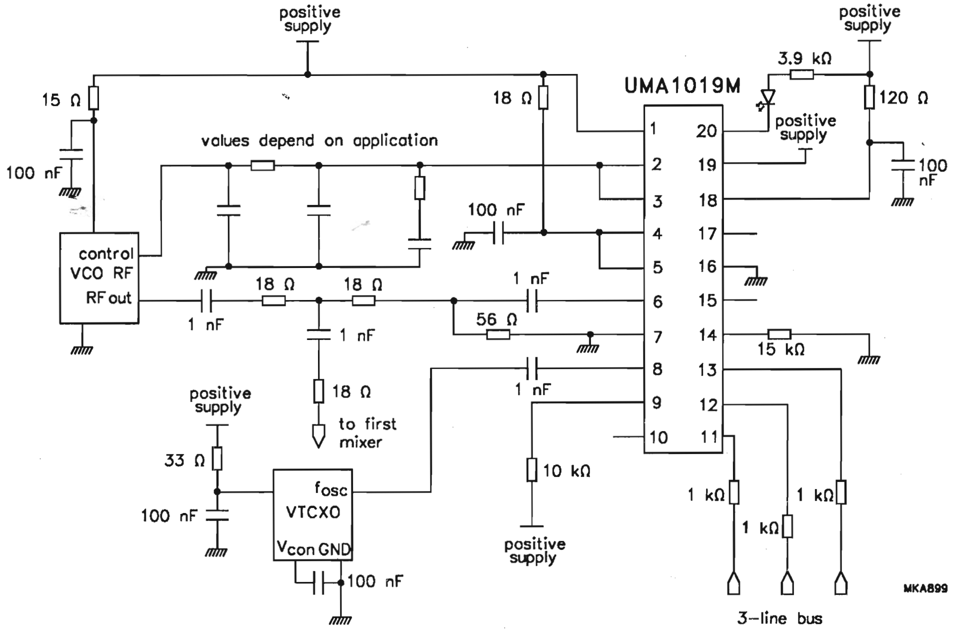


Fig.5 Typical test and application diagram.

Low-voltage dual frequency synthesizer for radio telephones

UMA1020AM

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Second synthesizer to control first IF or offset loop frequency
- Independent fully programmable reference dividers for each loop, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Dual power-down modes.

APPLICATIONS

- 1 to 1.7 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1020AM BICMOS device integrates prescalers, programmable dividers, and phase comparators to implement two phase-locked loops. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The principal synthesizer operates at VCO input frequencies up to 1.7 GHz the auxiliary synthesizer operates at 300 MHz. The auxiliary loop is intended for the first IF or to transmit offset loop-frequency settings. Each synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} may be higher than V_{DD} i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range.

The principal synthesizer phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. The auxiliary loop has a separate phase detector. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	principal synthesizer supply current	auxiliary synthesizer in power-down mode	–	9.4	–	mA
	principal and auxiliary synthesizer supply current	principal and auxiliary synthesizer ON	–	12.1	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	12	–	μA
f_{VCO}	principal input frequency		1000	1500	1700	MHz
f_{AI}	auxiliary input frequency		20	–	300	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PPC}	principal phase comparator frequency		–	200	–	kHz
f_{APC}	auxiliary phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1020AM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

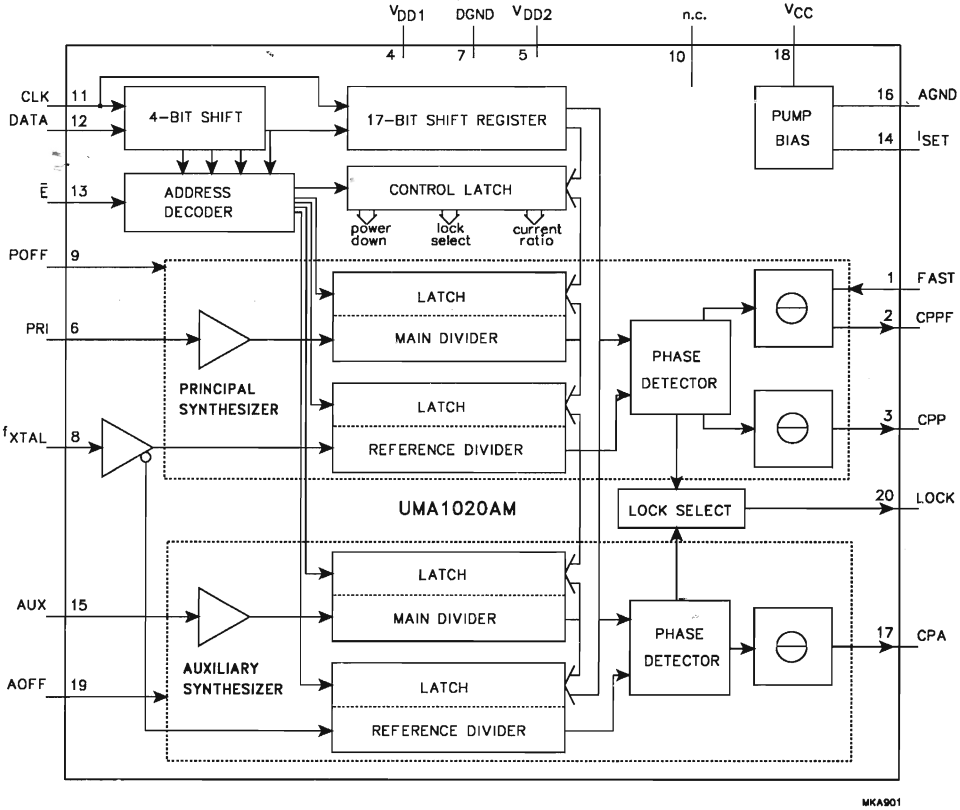


Fig.1 Block diagram.

Low-voltage dual frequency synthesizer for radio telephones

UMA1020AM

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPPF	2	principal synthesizer speed-up charge-pump output
CPP	3	principal synthesizer normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
PRI	6	1 GHz principal synthesizer RF divider input
DGND	7	digital ground
f_{XTAL}	8	common reference frequency input from crystal oscillator
POFF	9	principal synthesizer power-down input
n.c.	10	not connected
CLK	11	serial clock input
DATA	12	serial data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
AUX	15	auxiliary synthesizer frequency input
AGND	16	analog ground
CPA	17	auxiliary synthesizer charge-pump output
V_{CC}	18	supply for charge-pump and DAC circuits
AOFF	19	auxiliary synthesizer power-down input
LOCK	20	in-lock detect output (main PLL); test mode output

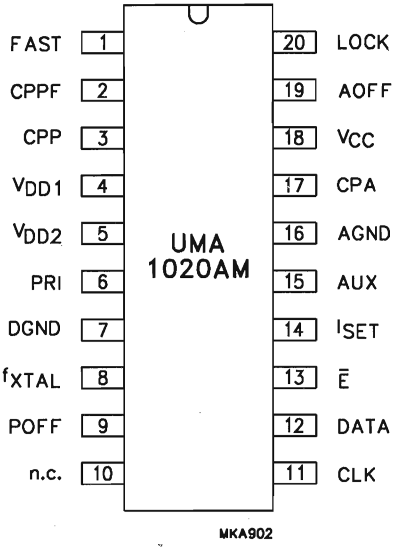


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Principal synthesizer

Programmable reference and main dividers drive the principal PLL phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input POFF (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The PRI input (pin 6) drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 100 mV to 500 mV (RMS), and at frequencies up to 1.7 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divide ratios (512 to 131 071) allow up to 2 MHz phase comparison frequency.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to improve noise and breakthrough levels.

The principal synthesizer speed-up charge pump (CPPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector providing improved linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen such that the value is high enough to keep the sink current in the LOW state below 400 μA. The circuit can be programmed to output either the phase error in the principal or auxiliary phase detectors or the combination from both detectors (OR function). The resultant output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison an out-of-lock or an in-lock flag is generated.

Auxiliary synthesizer

The auxiliary synthesizer has a 14-bit main divider and an 11-bit reference divider. A separate power-down input AOFF (pin 19), disables currents in the auxiliary dividers, phase detector, and charge pump. The auxiliary input signal is amplified and fed to the main divider. The input buffer presents a high impedance, dominated by pin and pad capacitance. First divider stages use bipolar technology operating at input frequencies up to 300 MHz; the slower bits are CMOS. The auxiliary loop phase detector and charge pump use similar circuits to the main loop low-current phase comparator, including dead-zone compensation feedback.

The auxiliary reference divider is clocked on the opposite edge of the main reference divider to ensure that active edges arrive at the auxiliary and principal phase detectors at different times. This minimizes the potential for interference between the charge pumps of each loop.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down of main and auxiliary loops.

However when either principal synthesizer or auxiliary synthesizer or both are powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1020AM uses 5 of the 16 available addresses. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers.

This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

Table 1 Format of programmed data

LAST IN				PROGRAMMING REGISTER BIT USAGE				FIRST IN
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT										REGISTER BIT ALLOCATION										LT
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
TEST BITS(2)																	0	0	0	0
X	X	X	X	OLP	OLA	CR1	CR0	X	X	sPOFF	sAOFF	X	X	X	X	X	0	0	0	1
PM16	PRINCIPAL MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	PRINCIPAL REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1
X	X	X	AM13	AUXILIARY MAIN DIVIDER COEFFICIENT												AM0	0	1	1	0
X	X	X	X	X	X	AR10	AUXILIARY REFERENCE DIVIDER COEFFICIENT									AR0	0	1	1	1

Notes

1. FT = first, LT = last; sPOFF = software power-down for principal synthesizer (1 = OFF); sAOFF = software power-down for auxiliary synthesizer (1 = OFF).
2. The test register is not to be programmed. Normally all bits of the test register must be set to zero.

Table 3 Out-of-lock select

OLP	OLA	OUT-OF-LOCK ON PIN 20
0	0	output disabled
0	1	auxiliary phase error
1	0	principal phase error
1	1	both auxiliary and principal

Table 4 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CPA}	I_{CPP}	I_{CPPF}	$I_{CPPF} : I_{CPP}$
0	0	$4 \times I_{SET}$	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$4 \times I_{SET}$	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$4 \times I_{SET}$	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; common bias current for charge pumps.

Table 5 Power-down modes

AOFF	POFF	FAST	PRINCIPAL DIVIDERS	AUXILIARY DIVIDERS	PUMP CPA	PUMP CPP	PUMP CPPF
1	1	X	OFF	OFF	OFF	OFF	OFF
1	0	0	ON	OFF	OFF	ON	OFF
1	0	1	ON	OFF	OFF	ON	ON
0	1	X	OFF	ON	ON	OFF	OFF
0	0	0	ON	ON	ON	ON	OFF
0	0	1	ON	ON	ON	ON	ON

Power-down modes

The action of the control inputs on the state of internal blocks is defined by Table 5.

Note that in Table 5 POFF and AOFF can be either the software or hardware power-down signals. The dividers are ON when both hardware and software power-down signals are at logic 0.

When either synthesizer is reactivated after power-down the main and reference dividers of that synthesizer are synchronized to avoid the possibility of random phase errors on power-up.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
ΔV_{CC-DD}	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8 to 15, 19 and 20	−0.3	V_{DD} + 0.3	V
$V_{2, 3, 17}$	voltage at pins 2, 3 and 17	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	–	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

All values refer to the typical measurement circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	principal synthesizer digital supply current	$V_{DD} = 5.5$ V	–	9	11	mA
	auxiliary synthesizer digital supply current	$V_{DD} = 5.5$ V	–	2.7	4.0	mA
I_{CC}	charge pumps supply current	$V_{CC} = 5.5$ V; $R_{ext} = 12$ kΩ	–	0.4	1.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 or V_{DD}	–	12	50	μA
RF principal main divider input; pin 6						
f_{VCO}	VCO input frequency		1 000	1 500	1 700	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50$ Ω	100	–	500	mV
Z_I	input impedance (real part)	$f_{VCO} = 2$ GHz	–	300	–	Ω
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pm}	principal main divider ratio		512	–	131 071	
f_{PPCmax}	maximum principal loop comparison frequency		–	2000	–	kHz
f_{PPCmin}	minimum principal loop comparison frequency		–	10	–	kHz
Auxiliary loop main divider input; pin 15						
f_{AI}	input frequency		20	–	300	MHz
$V_{15(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50$ Ω; $2.7 \text{ V} < V_{DD} < 3.5$ V	50	–	500	mV
		$R_s = 50$ Ω; $3.5 \text{ V} < V_{DD} < 5.5$ V	100	–	500	mV
Z_I	input impedance (real part)	$f_{AI} = 100$ MHz	–	1	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{am}	auxiliary main divider ratio		64	–	16383	
f_{APCmax}	maximum auxiliary loop comparison frequency		–	2000	–	kHz
f_{APCmin}	minimum auxiliary loop comparison frequency		–	10	–	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Dual synthesizer reference dividers input; pin 8						
f_{XTAL}	input frequency range from crystal		3	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	5 MHz < f_{XTAL} < 40 MHz	50	–	500	mV
		3 MHz < f_{XTAL} < 40 MHz	100	–	500	mV
Z_I	input impedance (real part)	f_{XTAL} = 30 MHz	–	2	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pr}	principal reference division ratio		8	–	2047	
R_{ar}	auxiliary reference division ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	R_{ext} = 12 kΩ	–	1.15	–	V
Charge pump outputs; pins 17, 3 and 2; R_{ext} = 12 kΩ						
I_{Ocp}	charge pump output current error		−25	–	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	–	±5	–	%
I_{Lcp}	charge pump off leakage current	$V_{cp} = \frac{1}{2}V_{CC}$	−5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	$V_{CC} - 0.4$	V
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.3$	V
V_{IL}	LOW level input voltage		−0.3	–	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	−5	–	+5	μA
C_I	input capacitance	indicative, not tested	–	2	–	pF
Lock detect output signal; pin 20 open-drain output						
V_{OL}	LOW level output voltage	i_{sink} = 0.4 mA	–	–	0.4	V

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	2000(1)	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 2 μs provided all the following conditions are satisfied:
   a) Principal main divider input frequency $f_{VCO} > \frac{512}{t_W}$
   b) Auxiliary main divider input frequency $f_{AI} > \frac{32}{t_W}$
   c) Reference dividers input frequency $f_{XTAL} > \frac{3}{t_W}$.

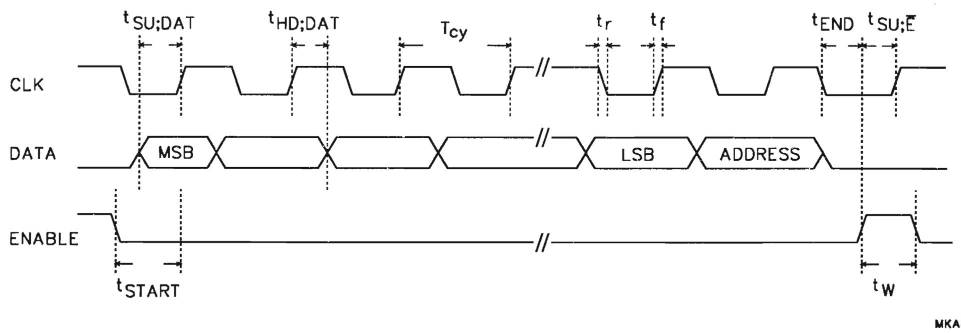


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

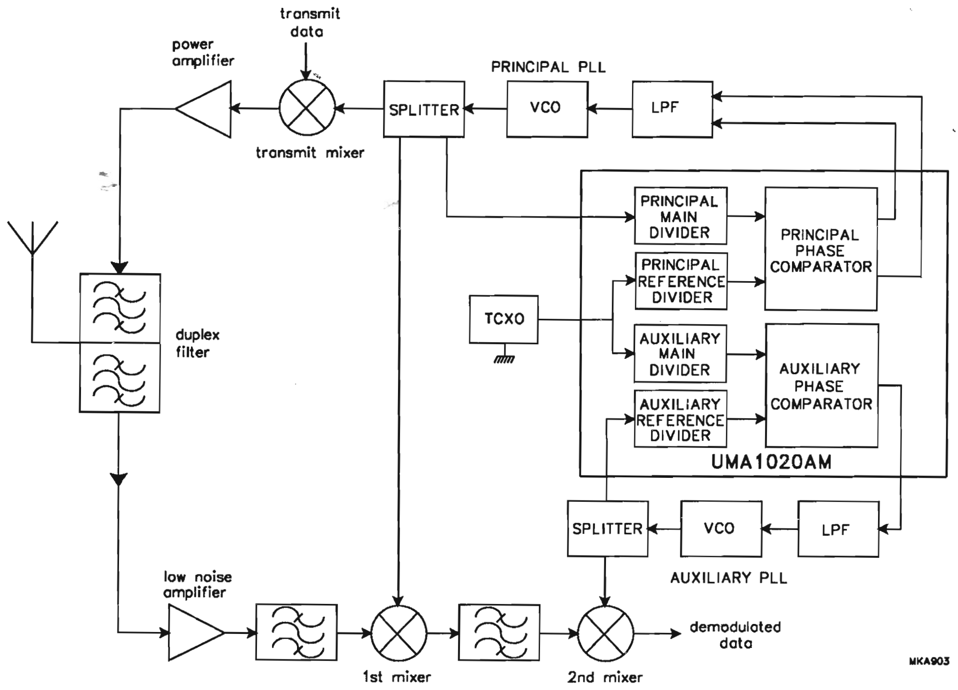


Fig.4 Typical application block diagram.

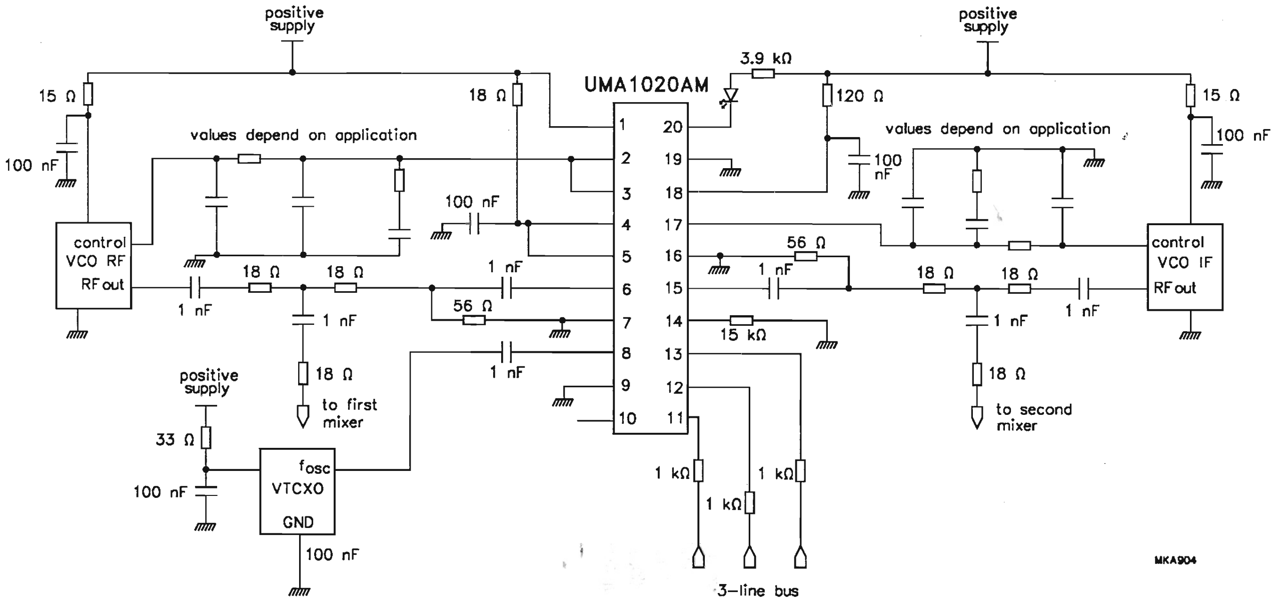


Fig.5 Typical test and application diagram.

Low-voltage dual frequency synthesizer for radio telephones

UMA1020M

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- 3-line serial interface bus
- Second synthesizer to control first IF or offset loop frequency
- Independent fully programmable reference dividers for each loop, driven from external crystal oscillator
- Dual phase detector outputs to allow fast frequency switching
- Integrated digital-to-analog converter
- Dual power-down modes.

APPLICATIONS

- 2 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1020M BICMOS device integrates prescalers, programmable dividers, and phase comparators to implement two phase-locked loops. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The principal synthesizer operates at VCO input frequencies up to 2.4 GHz the auxiliary synthesizer operates at 300 MHz. The auxiliary loop is intended for the first IF or to transmit offset loop-frequency settings. Each synthesizer has a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be at the same potential. V_{CC} may be higher than V_{DD} i.e. V_{DD} = 3 V and V_{CC} = 5 V for wider tuning range.

The principal synthesizer phase detector uses two charge pumps, one provides normal loop feedback, while the other is only active during fast mode to speed-up switching. The auxiliary loop has a separate phase detector. All charge pump currents (gain) are fixed by an external resistance at pin I_{SET} (pin 14). Only passive loop filters are used; the charge-pumps function within a wide voltage compliance range to improve the overall system performance. An on-chip 8-bit DAC enables adjustment of an external function, such as the temperature compensation of a crystal oscillator.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{DD}	supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{CC} + I_{DD}$	principal synthesizer supply current	auxiliary synthesizer in power-down mode	–	9.4	–	mA
	principal and auxiliary synthesizer supply current	principal and auxiliary synthesizer ON	–	12.1	–	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply		–	12	–	μA
f_{VCO}	principal input frequency		1650	–	2400	MHz
f_{AI}	auxiliary input frequency		20	–	300	MHz
f_{XTAL}	crystal reference input frequency		3	–	40	MHz
f_{PPC}	principal phase comparator frequency		–	200	–	kHz
f_{APC}	auxiliary phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1020M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

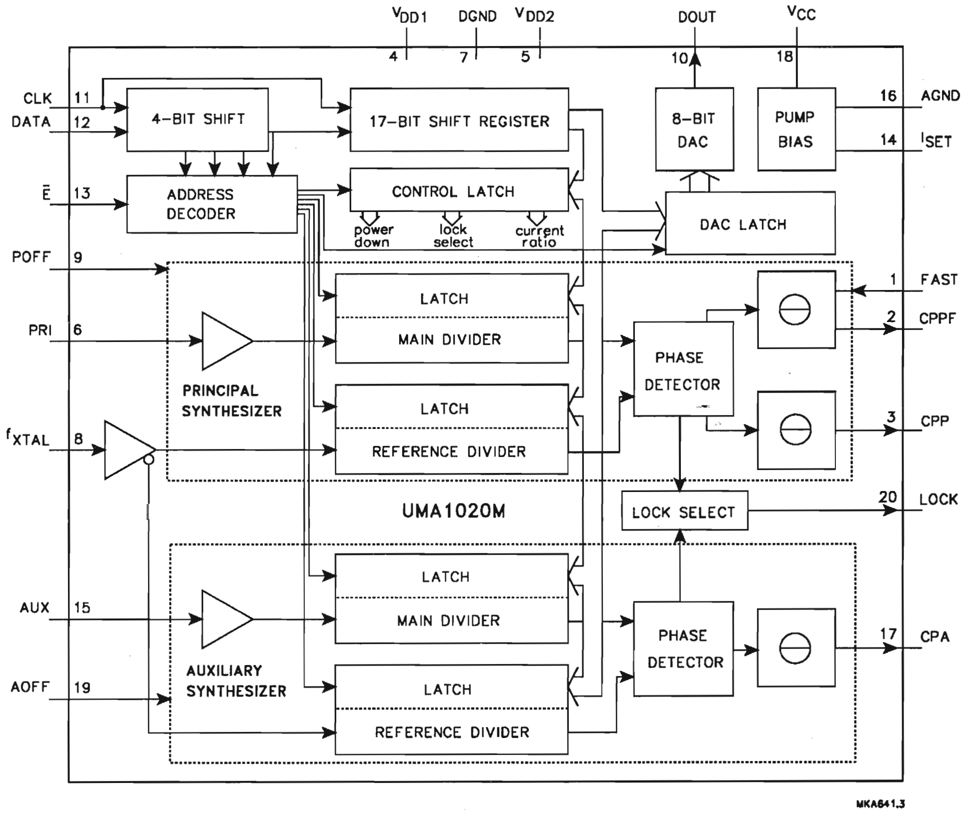


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed-up main synthesizer
CPPF	2	principal synthesizer speed-up charge-pump output
CPP	3	principal synthesizer normal charge-pump output
V_{DD1}	4	digital power supply 1
V_{DD2}	5	digital power supply 2
PRI	6	1 GHz principal synthesizer RF divider input
DGND	7	digital ground
f_{XTAL}	8	common reference frequency input from crystal oscillator
POFF	9	principal synthesizer power-down input
DOUT	10	8-bit digital-to-analog output
CLK	11	serial clock input
DATA	12	serial data input
$\overline{E}$	13	programming bus enable input (active LOW)
I_{SET}	14	regulator pin to set the charge-pump currents
AUX	15	auxiliary synthesizer frequency input
AGND	16	analog ground
CPA	17	auxiliary synthesizer charge-pump output
V_{CC}	18	supply for charge-pump and DAC circuits
AOFF	19	auxiliary synthesizer power-down input
LOCK	20	in-lock detect output (main PLL); test mode output

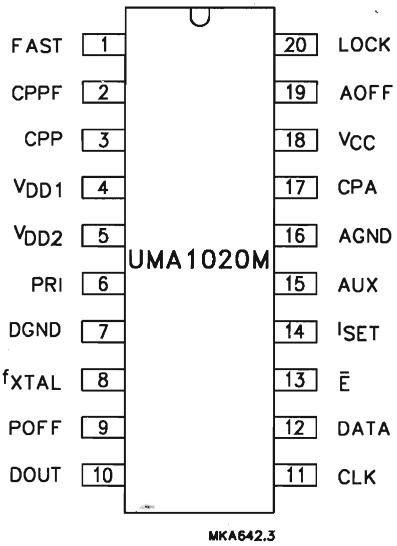


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Principal synthesizer

Programmable reference and main dividers drive the principal PLL phase detector. Two charge pumps produce phase error current pulses for integration in an external loop filter. A hardwired power-down input POFF (pin 9) ensures that the dividers and phase comparator circuits can be disabled.

The PRI input (pin 6) drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from 60 mV to 180 mV (RMS), and at frequencies up to 2.4 GHz. The high frequency divider circuits use bipolar transistors, slower bits are CMOS. Divide ratios (512 to 131 071) allow a 2 MHz phase comparison frequency.

The reference and main divider outputs are connected to a phase/frequency detector that controls two charge pumps. The two pumps have a common bias-setting current that is set by an external resistance. The ratio between currents in fast and normal operating modes can be programmed via the 3-wire serial bus. The low current pump remains active except in power-down. The high current pump is enabled via the control input FAST (pin 1). By appropriate connection to the loop filter, dual bandwidth loops are provided: short time constant during frequency switching (FAST mode) to speed-up channel changes and low bandwidth in the settled state (on-frequency) to improve noise and breakthrough levels.

The principal synthesizer speed-up charge pump (CPPF) is controlled by the FAST input in synchronization with phase detector operation in such a way that potential disturbances are minimized. The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by feedback from the normal pump output to the phase detector providing improved linearity.

An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen such that the value is high enough to keep the sink current in the LOW state below 400 μA. The circuit can be programmed to output either the phase error in the principal or auxiliary phase detectors or the combination from both detectors (OR function). The resultant output will be a current pulse with the duration of the selected phase error. By appropriate external filtering and threshold comparison an out-of-lock or an in-lock flag is generated.

Auxiliary synthesizer

The auxiliary synthesizer has a 14-bit main divider and an 11-bit reference divider. A separate power-down input AOFF (pin 19), disables currents in the auxiliary dividers, phase detector, and charge pump. The auxiliary input signal is amplified and fed to the main divider. The input buffer presents a high impedance, dominated by pin and pad capacitance. First divider stages use bipolar technology operating at input frequencies up to 300 MHz; the slower bits are CMOS. The auxiliary loop phase detector and charge pump use similar circuits to the main loop low-current phase comparator, including dead-zone compensation feedback.

The auxiliary reference divider is clocked on the opposite edge of the main reference divider to ensure that active edges arrive at the auxiliary and principal phase detectors at different times. This minimizes the potential for interference between the charge pumps of each loop.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down of main and auxiliary loops.

However when either principal synthesizer or auxiliary synthesizer or both are powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTAL}) for correct programming.

Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The UMA1020M uses 6 of the 16 available addresses. The data format is shown in Table 1. The first entered bit is p1, the last bit is p21.

The trailing address bits are decoded on the inactive edge of $\overline{E}$. This produces an internal load pulse to store the data in one of the addressed latches. To avoid erroneous divider ratios, the pulse is not allowed during data reads by the frequency dividers.
This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The corresponding relationship between data fields and addresses is given in Table 2.

Table 1 Format of programmed data

LAST IN				PROGRAMMING REGISTER BIT USAGE				FIRST IN
p21	p20	p19	p18	p17	p16	../..	p2	p1
ADD0	ADD1	ADD2	ADD3	DATA0	DATA1	../..	DATA15	DATA16
LATCH ADDRESS				LSB	DATA COEFFICIENT			MSB

Table 2 Bit allocation (note 1)

FT									REGISTER BIT ALLOCATION											LT
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
TEST BITS(2)																	0	0	0	0
X	X	X	X	OLP	OLA	CR1	CR0	X	X	sPOFF	sAOFF	X	X	X	X	X	0	0	0	1
PM16	PRINCIPAL MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10	PRINCIPAL REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1
X	X	X	AM13	AUXILIARY MAIN DIVIDER COEFFICIENT												AM0	0	1	1	0
X	X	X	X	X	X	AR10	AUXILIARY REFERENCE DIVIDER COEFFICIENT									AR0	0	1	1	1
X	X	X	X	X	X	X	X	X	DA7	8-BIT DAC FOR EXTERNAL TRIM						DA0	1	0	0	0

Notes

1. FT = first, LT = last; sPOFF = software power-down for principal synthesizer (1 = OFF); sAOFF = software power-down for auxiliary synthesizer (1 = OFF).
2. The test register is not to be programmed. Normally all bits of the test register must be set to zero.

Table 3 Out-of-lock select

OLP	OLA	OUT-OF-LOCK ON PIN 20
0	0	output disabled
0	1	auxiliary phase error
1	0	principal phase error
1	1	both auxiliary and principal

Table 4 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CPA}	I_{CPP}	I_{CPPF}	$I_{CPPF} : I_{CPP}$
0	0	$4 \times I_{SET}$	$4 \times I_{SET}$	$16 \times I_{SET}$	4 : 1
0	1	$4 \times I_{SET}$	$4 \times I_{SET}$	$32 \times I_{SET}$	8 : 1
1	0	$4 \times I_{SET}$	$2 \times I_{SET}$	$24 \times I_{SET}$	12 : 1
1	1	$4 \times I_{SET}$	$2 \times I_{SET}$	$32 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{14}}{R_{ext}}$; common bias current for charge pumps and DAC.

Table 5 Power-down modes

AOFF	POFF	FAST	PRINCIPAL DIVIDERS	AUXILIARY DIVIDERS	PUMP CPA	PUMP CPP	PUMP CPPF	DAC AND BIAS
1	1	X	OFF	OFF	OFF	OFF	OFF	OFF
1	0	0	ON	OFF	OFF	ON	OFF	ON
1	0	1	ON	OFF	OFF	ON	ON	ON
0	1	X	OFF	ON	ON	OFF	OFF	ON
0	0	0	ON	ON	ON	ON	OFF	ON
0	0	1	ON	ON	ON	ON	ON	ON

Digital-to-analog converter

The byte loaded via the bus into the appropriate latch drives a digital-to-analog converter. The internal current is scaled by the external resistance (R_{ext}) at pin I_{SET}, similar to the charge pumps. The nominal full-scale current is $4 \times I_{SET}$. The output current is mirrored to produce a full-scale voltage into a user-defined ground referenced resistance, thereby allowing optimum swing from power supply rails within the 2.7 to 5.5 V limits. The bandgap reference voltage at pin I_{SET} is temperature and supply independent. The DAC signal is monotonic across the full range of digital input codes to enable fine adjustment of other system blocks. The typical settling time for full-scale switching is 400 ns into a 12 kΩ // 20 pF load.

Power-down modes

The action of the control inputs on the state of internal blocks is defined by Table 5.

Note that in Table 5 POFF and AOFF can be either the software or hardware power-down signals. The dividers are ON when both hardware and software power-down signals are at logic 0.

When either synthesizer is reactivated after power-down the main and reference dividers of that synthesizer are synchronized to avoid the possibility of random phase errors on power-up.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	−0.3	+5.5	V
V_{CC}	analog supply voltage	−0.3	+5.5	V
ΔV_{CC-DD}	difference in voltage between V_{CC} and V_{DD}	−0.3	+5.5	V
V_n	voltage at pins 1, 6, 8 to 15, 19 and 20	−0.3	V_{DD} + 0.3	V
$V_{2, 3, 17}$	voltage at pins 2, 3 and 17	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
P_{tot}	total power dissipation	−	150	mW
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C
T_j	maximum junction temperature	−	95	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

All values refer to the typical measurement circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 5 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
V_{CC}	analog supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
I_{DD}	principal synthesizer digital supply current	V_{DD} = 5.5 V	–	9	11	mA
	auxiliary synthesizer digital supply current	V_{DD} = 5.5 V	–	2.7	4.0	mA
I_{CC}	charge pumps supply current	V_{CC} = 5.5 V; R_{ext} =12 kΩ	–	0.4	1.0	mA
I_{CCPD}, I_{DDPD}	current in power-down mode per supply	logic levels 0 or V_{DD}	–	12	50	μA
RF principal main divider input; pin 6						
f_{VCO}	VCO input frequency		1650	–	2400	MHz
$V_{6(rms)}$	AC-coupled input signal level (RMS value)	R_s = 50 Ω; 1.65 < f_{VCO} < 2.0 GHz	60	–	400	mV
		R_s = 50 Ω; 1.65 < f_{VCO} < 2.4 GHz	60	–	180	mV
Z_I	input impedance (real part)	f_{VCO} = 2 GHz	–	300	–	Ω
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pm}	principal main divider ratio		512	–	131071	
f_{PPCmax}	maximum principal loop comparison frequency		–	2000	–	kHz
f_{PPCmin}	minimum principal loop comparison frequency		–	10	–	kHz
Auxiliary loop main divider input; pin 15						
f_{AI}	input frequency		20	–	300	MHz
$V_{15(rms)}$	AC-coupled input signal level (RMS value)	R_s = 50 Ω; 2.7 V < V_{DD} < 3.5 V	50	–	500	mV
		R_s = 50 Ω; 3.5 V < V_{DD} < 5.5 V	100	–	500	mV
Z_I	input impedance (real part)	f_{AI} = 100 MHz	–	1	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{am}	auxiliary main divider ratio		64	–	16383	
f_{APCmax}	maximum auxiliary loop comparison frequency		–	2000	–	kHz
f_{APCmin}	minimum auxiliary loop comparison frequency		–	10	–	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Dual synthesizer reference dividers input; pin 8						
f_{XTAL}	input frequency range from crystal		3	–	40	MHz
$V_{8(rms)}$	sinusoidal input signal level (RMS value)	5 MHz < f_{XTAL} < 40 MHz	50	–	500	mV
		3 MHz < f_{XTAL} < 40 MHz	100	–	500	mV
Z_I	input impedance (real part)	f_{XTAL} = 30 MHz	–	2	–	kΩ
C_I	typical pin input capacitance	indicative, not tested	–	2	–	pF
R_{pr}	principal reference division ratio		8	–	2047	
R_{ar}	auxiliary reference division ratio		8	–	2047	
Charge pump current setting resistor input; pin 14						
R_{ext}	external resistor from pin 14 to ground		12	–	60	kΩ
V_{14}	regulated voltage at pin 14	R_{ext} = 12 kΩ	–	1.15	–	V
Charge pump outputs; pins 17, 3 and 2; R_{ext} = 12 kΩ						
I_{Ocp}	charge pump output current error		–25	–	+25	%
I_{match}	sink-to-source current matching	V_{cp} in range	–	±5	–	%
I_{Lcp}	charge pump off leakage current	$V_{cp} = \frac{1}{2}V_{CC}$	–5	±1	+5	nA
V_{cp}	charge pump voltage compliance		0.4	–	V_{CC} – 0.4	V
Interface logic input signal levels; pins 13, 12, 11 and 1						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	–5	–	+5	µA
C_I	input capacitance	indicative, not tested	–	2	–	pF
DAC output signal levels; pin 10, R_{ext} = 12 kΩ						
I_{DAC}	DAC full scale output current		3 × I_{SET}	4 × I_{SET}	5 × I_{SET}	mA
V_{10}	output voltage compliance	all codes	0	–	V_{DD} – 0.4	V
I_{10min}	minimum DAC current	00 code	–	2	5	µA
I_{monot}	worst case monotonicity test: ΔI × 256/400 µA	note 1	0.1	–	1.9	
Lock detect output signal; pin 20 open-drain output						
V_{OL}	LOW level output voltage	i_{sink} = 0.4 mA	–	–	0.4	V

Note

1. ΔI is the change in DAC output current when making the code transitions: 7FH/80H, 3FH/40H or 1FH/20H.

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	−20	–	–	ns
t_W	minimum inactive pulse width	2000(1)	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 2 μs provided all the following conditions are satisfied:
   a) Principal main divider input frequency $f_{VCO} > \frac{512}{t_W}$
   b) Auxiliary main divider input frequency $f_{AI} > \frac{32}{t_W}$
   c) Reference dividers input frequency $f_{XTAL} > \frac{3}{t_W}$.

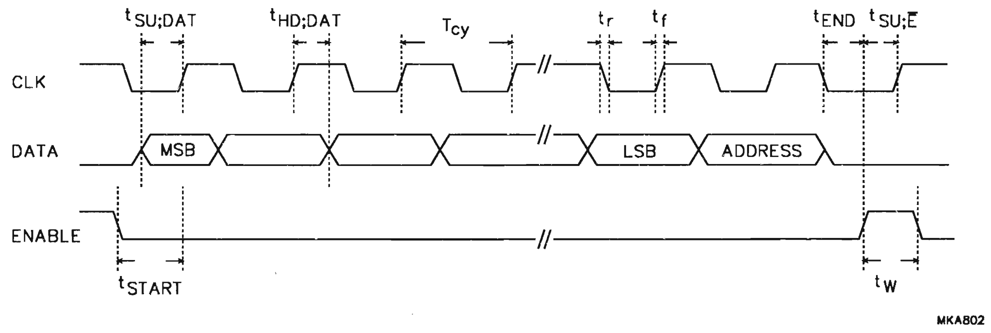


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

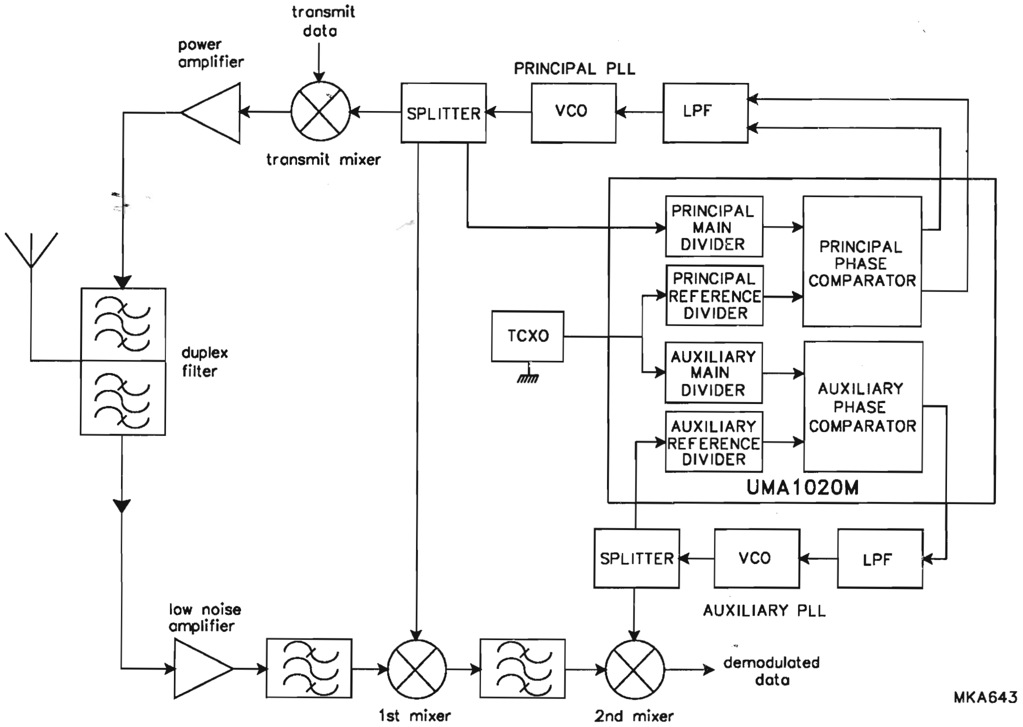


Fig.4 Typical application block diagram.

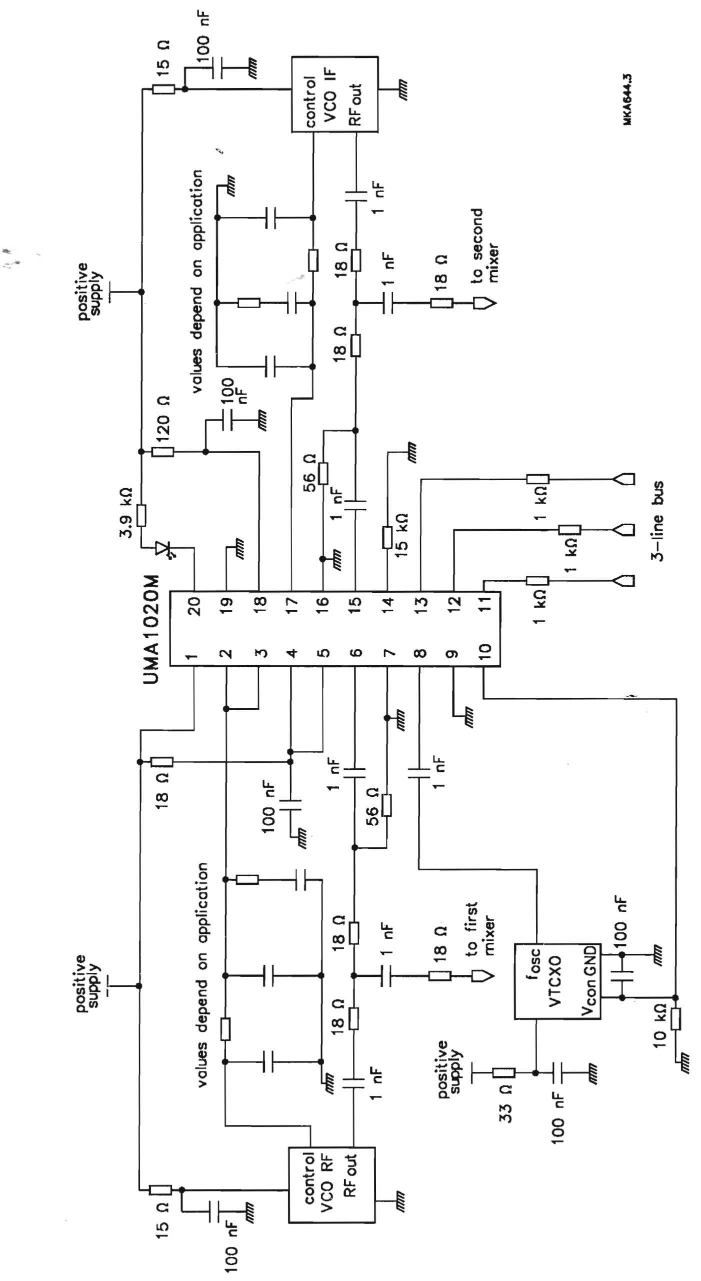


Fig.5 Typical test and application diagram.

Section 6
Transmitters

INDEX

NE/SA630 Single pole double throw (SPDT) switch 995
SA900 I/Q transmit modulator 1005
AN1892 SA900 I/Q transmit modulator for 1GHz applications 1019

Single pole double throw (SPDT) switch NE/SA630

DESCRIPTION

The NE630 is a wideband RF switch fabricated in BiCMOS technology and incorporating on-chip CMOS/TTL compatible drivers. Its primary function is to switch signals in the frequency range DC - 1GHz from one 50Ω channel to another. The switch is activated by a CMOS/TTL compatible signal applied to the enable channel 1 pin (ENCH1).

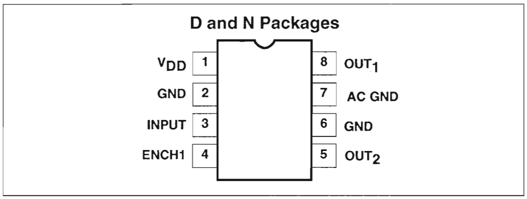
The extremely low current consumption makes the NE/SA630 ideal for portable applications. The excellent isolation and low loss makes this a suitable replacement for PIN diodes.

The NE/SA630 is available in an 8-pin dual in-line plastic package and an 8-pin SO (surface mounted miniature) package.

FEATURES

- Wideband (DC - 1GHz)
- Low through loss (1dB typical at 200MHz)
- Unused input is terminated internally in 50Ω
- Excellent overload capability (1dB gain compression point +18dBm at 300MHz)
- Low DC power (170μA from 5V supply)
- Fast switching (20ns typical)
- Good isolation (off channel isolation 60dB at 100MHz)
- Low distortion (IP_3 intercept +33dBm)
- Good 50Ω match (return loss 18dB at 400MHz)
- Full ESD protection
- Bidirectional operation

PIN CONFIGURATION



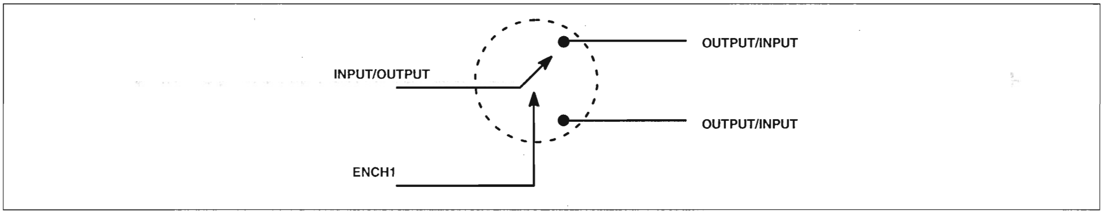
APPLICATIONS

- Digital transceiver front-end switch
- Antenna switch
- Filter selection
- Video switch
- FSK transmitter

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	0 to 70°C	NE630N	0404B
8-Pin Plastic Small Outline (SO) package (Surface-mount)	0 to 70°C	NE630D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA630N	0404B
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA630D	0174C

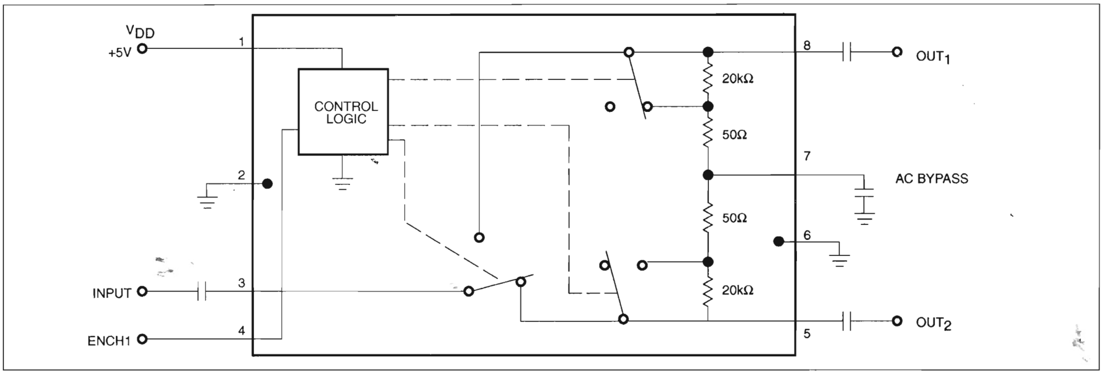
BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	3.0 to 5.5V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	-0.5 to +5.5	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 8-Pin Plastic DIP 8-Pin Plastic SO	 1160 780	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   8-Pin DIP: θ_{JA} = 108°C/W
   8-Pin SO: θ_{JA} = 158°C/W

DC ELECTRICAL CHARACTERISTICS

V_{DD} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA630			
			MIN	TYP	MAX	
I_{DD}	Supply current		40	170	300	µA
V_T	TTL/CMOS logic threshold voltage[1]		1.1	1.25	1.4	V
V_{IH}	Logic 1 level	Enable channel 1	2.0		V_{DD}	V
V_{IL}	Logic 0 level	Enable channel 2	-0.3		0.8	V
I_{IL}	ENCH1 input current	ENCH1 = 0.4V	-1	0	1	µA
I_{IH}	ENCH1 input current	ENCH1 = 2.4V	-1	0	1	µA

NOTE:

1. The ENCH1 input must be connected to a valid Logic Level for proper operation of the NE/SA630.

AC ELECTRICAL CHARACTERISTICS[1] - D PACKAGE

V_{DD} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA630			
			MIN	TYP	MAX	
S_{21}, S_{12}	Insertion loss (ON channel)	DC - 100MHz 500MHz 900MHz		1 1.4 2	 2.8	dB
S_{21}, S_{12}	Isolation (OFF channel)[2]	10MHz 100MHz 500MHz 900MHz	70 24	80 60 50 30		dB
S_{11}, S_{22}	Return loss (ON channel)	DC - 400MHz 900MHz		20 12		dB
S_{11}, S_{22}	Return loss (OFF channel)	DC - 400MHz 900MHz		17 13		dB
t_D	Switching speed (on-off delay)	50% TTL to 90/10% RF		20		ns
t_r, t_f	Switching speeds (on-off rise/fall time)	90%/10% to 10%/90% RF		5		ns
	Switching transients			165		mV_{P-P}
P_{-1dB}	1dB gain compression	DC - 1GHz		+18		dBm
IP_3	Third-order intermodulation intercept	100MHz		+33		dBm
IP_2	Second-order intermodulation intercept	100MHz		+52		dBm
NF	Noise figure (Z_O = 50Ω)	100MHz 900MHz		1.0 2.0		dB

NOTE:

1. All measurements include the effects of the D package NE/SA630 Evaluation Board (see Figure 1B). Measurement system impedance is 50Ω.
2. The placement of the AC bypass capacitor is critical to achieve these specifications. See the applications section for more details.

AC ELECTRICAL CHARACTERISTICS[1] - N PACKAGE

V_{DD} = +5V, T_A = 25°C; all other characteristics similar to the D-Package, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA630			
			MIN	TYP	MAX	
S_{21}, S_{12}	Insertion loss (ON channel)	DC - 100MHz 500MHz 900MHz		1 1.4 2.5		dB
S_{21}, S_{12}	Isolation (OFF channel)	10MHz 100MHz 500MHz 900MHz	58	68 50 37 15		dB
NF	Noise figure (Z_O = 50Ω)	100MHz 900MHz		1.0 2.5		dB

NOTE:

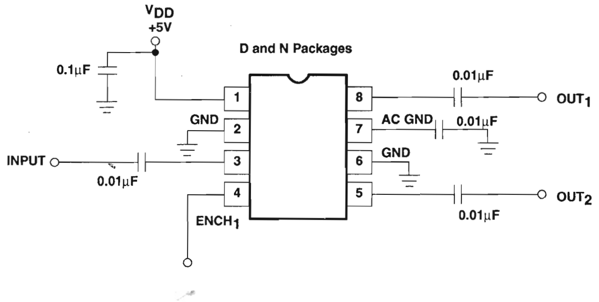
1. All measurements include the effects of the N package NE/SA630 Evaluation Board (see Figure 1C). Measurement system impedance is 50Ω.

APPLICATIONS

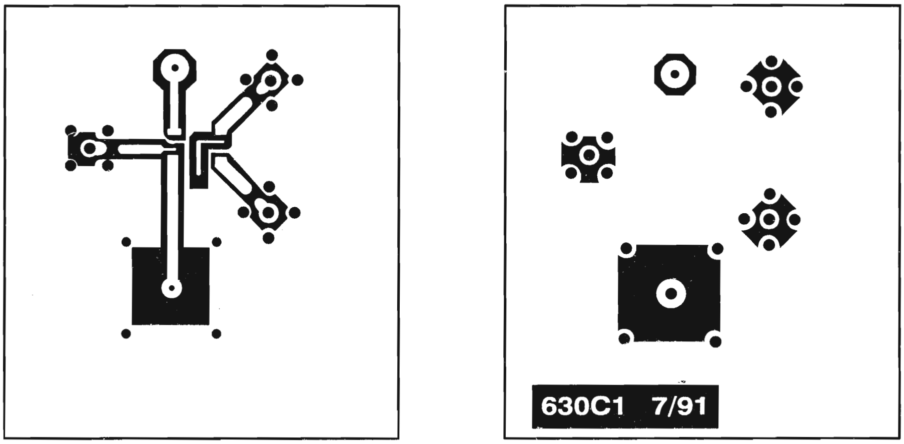
The typical applications schematic and printed circuit board layout of the NE/SA630 evaluation board is shown in Figure 1. The layout of the board is simple, but a few cautions need to be observed. The input and output traces should be 50Ω. The placement of the AC bypass capacitor is *extremely critical* if a symmetric isolation between the two channels is desired. The trace from Pin 7 should be drawn back towards the package and then be routed downwards. The capacitor should be placed straight down as close to the device as practical. For better isolation between the two channels at higher frequencies, it is also advisable to run the two output/input traces at an angle. This also minimizes any inductive coupling between the two traces. The power supply bypass capacitor should be placed close to the device. Figure 7 shows the frequency response of the NE/SA630. The loss matching between the two channels is excellent to 1.2GHz as shown in Figure 10.

Single pole double throw (SPDT) switch

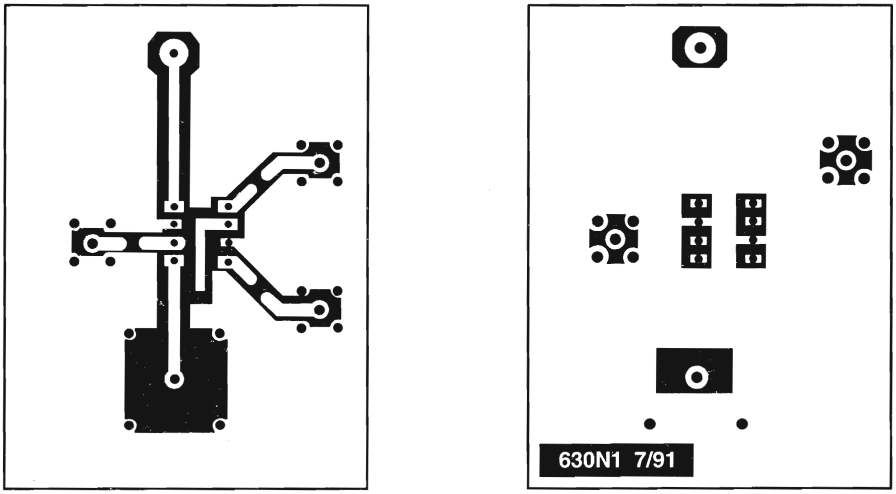
NE/SA630



a. NE/SA Evaluation Board Schematic



b. NE/SA630 D-Package Board Layout



c. NE/SA630 N-Package Board Layout

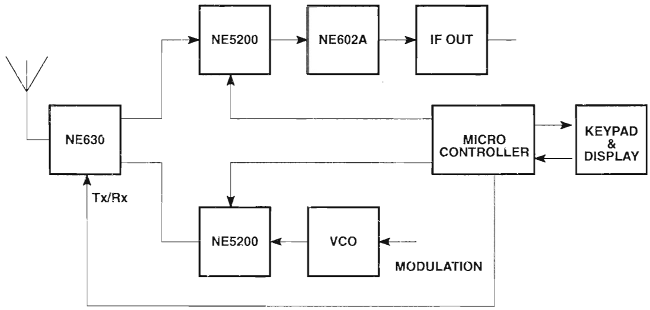
Figure 1.

The isolation and matching of the two channels over frequency is shown in Figures 12 and 14, respectively.

The NE630 is a very versatile part and can be used in many applications. Figure 2 shows a block diagram of a typical Digital RF transceiver front-end. In this application the NE630 replaces the duplexer which is typically very bulky and lossy. Due to the low power consumption of the device, it is ideally suited for handheld applications such as in CT2 cordless telephones. The NE630 can also be used to generate Amplitude Shift Keying (ASK) or On-Off Keying (OOK) and Frequency Shift Keying (FSK) signals for digital RF communications systems. Block diagrams for these applications are shown in Figures 3 and 4, respectively.

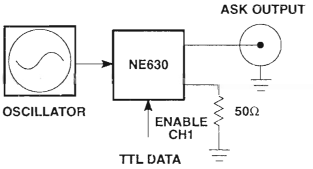
For applications that require a higher isolation at 1GHz than obtained from a single NE630, several NE630s can be cascaded as shown in Figure 5. The cascaded configuration will have a higher loss but greater than 35dB of isolation at 1GHz and greater than 65dB @ 500MHz can be obtained from this configuration. By modifying the enable control, an RF multiplexer/ de-multiplexer or antenna selector can be constructed. The simplicity of NE630 coupled with its ease of use and high performance lends itself to many innovative applications.

The NE/SA630 switch terminates the OFF channel in 50Ω. The 50Ω resistor is internal and is in series with the external AC bypass capacitor. Matching to impedances other than 50Ω can be achieved by adding a resistor in series with the AC bypass capacitor (e.g., 25Ω additional to match to a 75Ω environment).



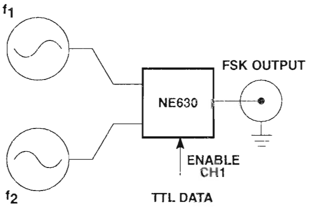
A TYPICAL TDMA/DIGITAL RF TRANSCEIVER SYSTEM FRONT-END

Figure 2.



AMPLITUDE SHIFT KEYING (ASK) GENERATOR

Figure 3.



FREQUENCY SHIFT KEYING (FSK) GENERATOR

Figure 4.

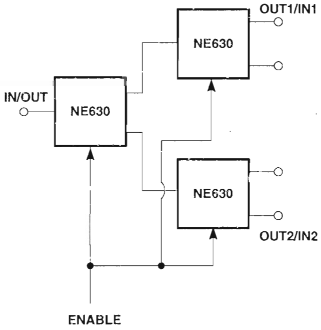


Figure 5.

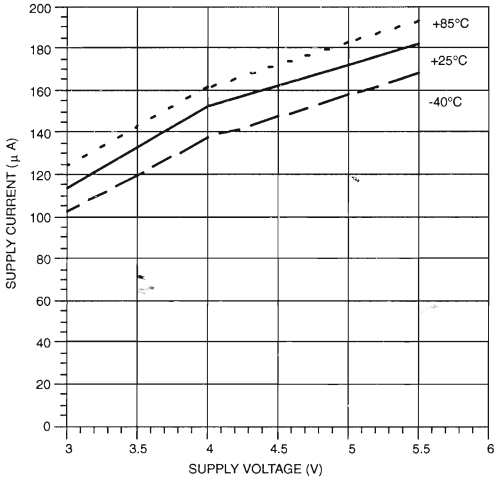


Figure 6. Supply Current vs. V_{DD} and Temperature

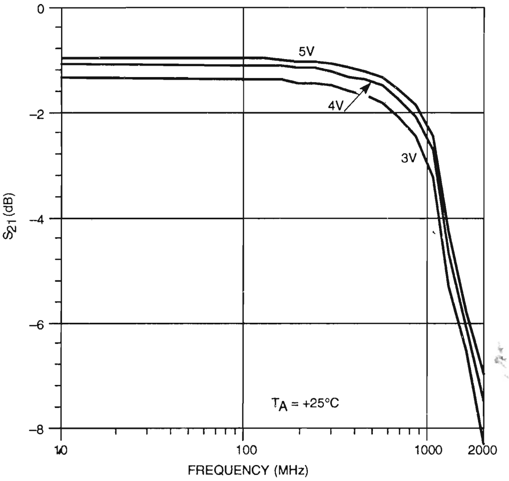


Figure 7. Loss vs. Frequency and V_{DD} for D-Package

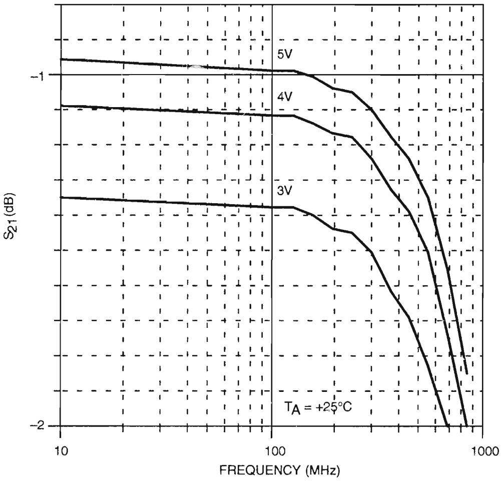


Figure 8. Loss vs. Frequency and V_{DD} for D-Package -Expanded Detail-

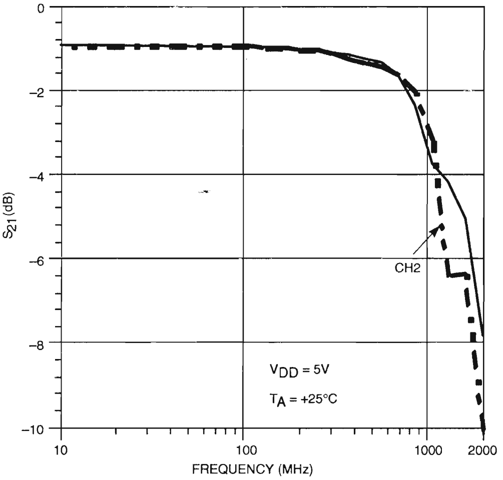


Figure 9. Loss Matching vs. Frequency for N-Package (DIP)

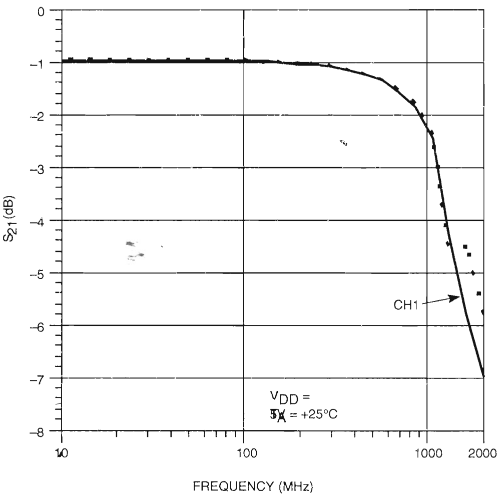


Figure 10. Loss Matching vs. Frequency; CH1 vs. CH2 for D-Pakage

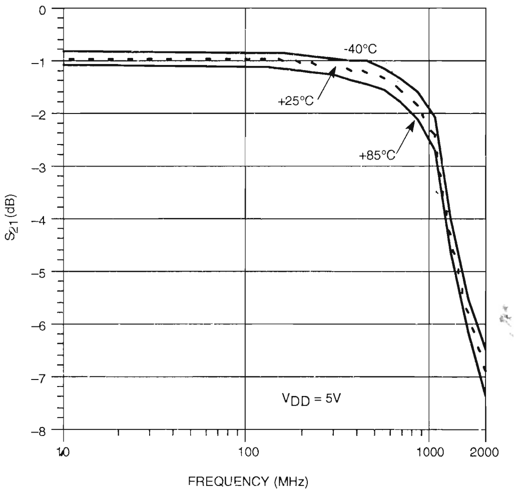


Figure 11. Loss vs. Frequency and Temperature for D-Package

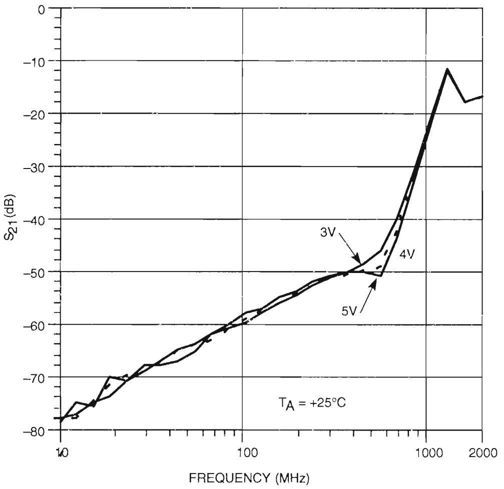


Figure 12. Isolation vs. Frequency and V_{DD} for D-Package

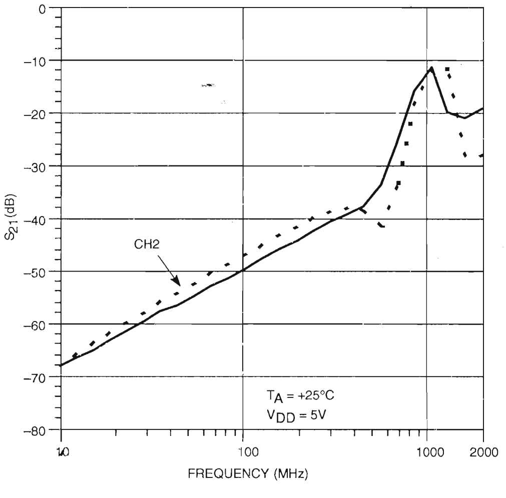


Figure 13. Isolation Matching vs. Frequency for N-Package (DIP)

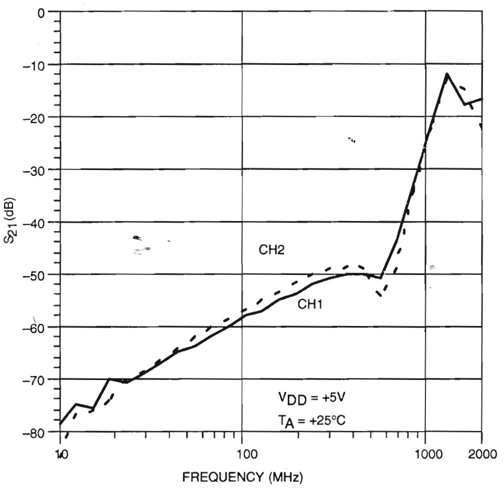


Figure 14. Isolation Matching vs. Frequency; CH1 vs. CH2 for D-Package

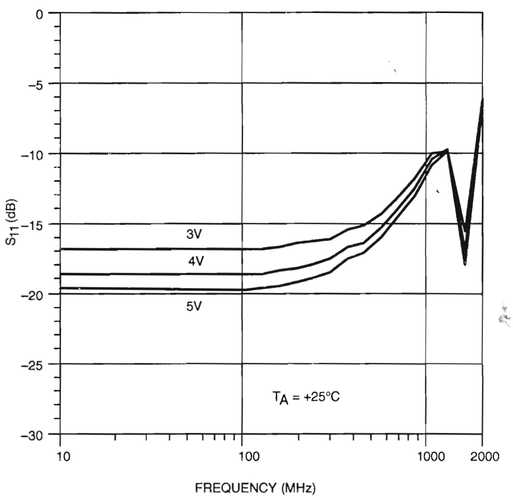


Figure 15. Input Match On-Channel vs. Frequency and V_{DD}

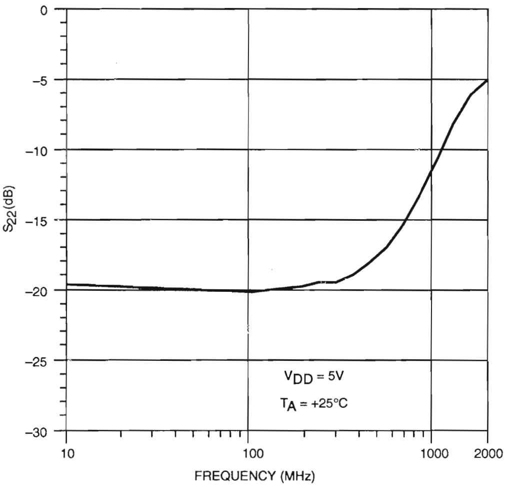


Figure 16. Output Match On-Channel vs. Frequency

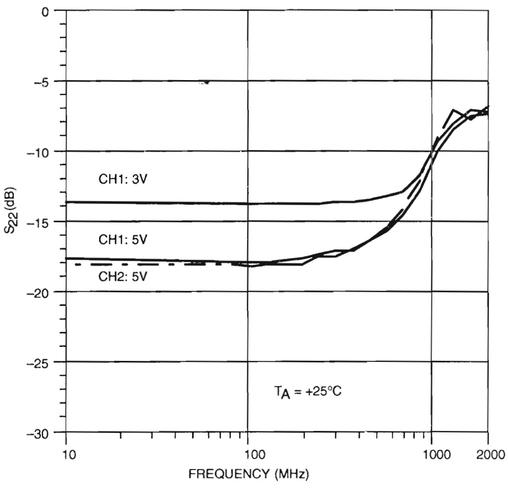


Figure 17. OFF-Channel Match vs. Frequency and V_{DD}

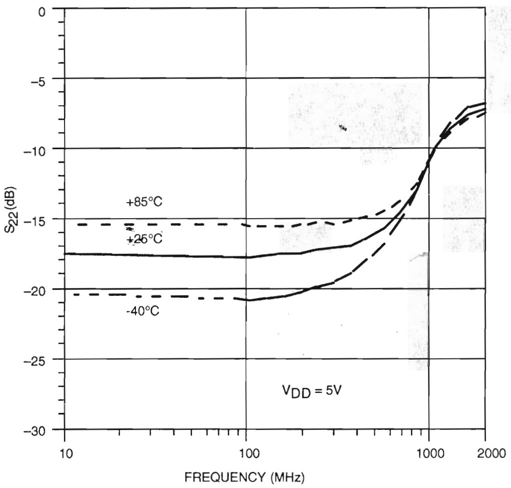


Figure 18. OFF Channel Match vs. Frequency and Temperature

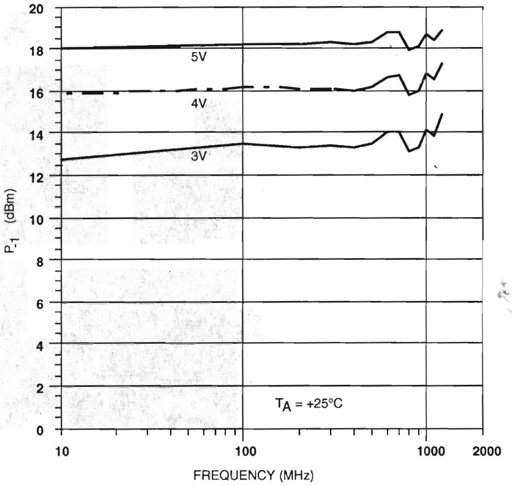


Figure 19. P$_{-1}$ dB vs. Frequency and V$_{DD}$

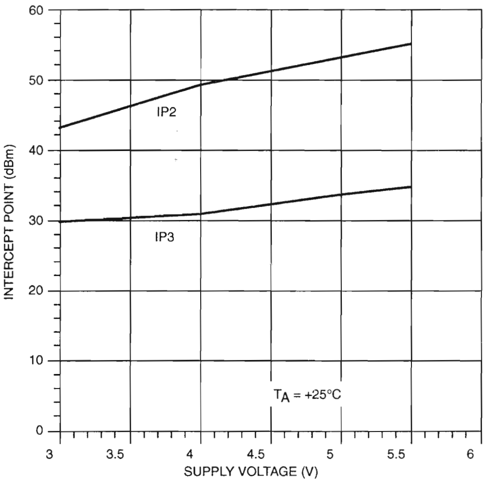


Figure 20. Intercept Points vs.V$_{DD}$

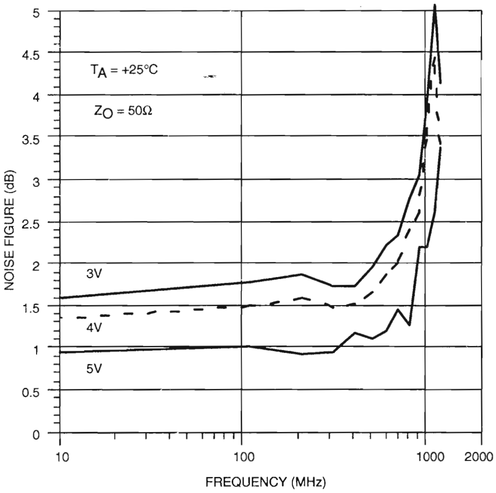


Figure 21. Noise Figure vs. Frequency and V$_{DD}$ for D-Package

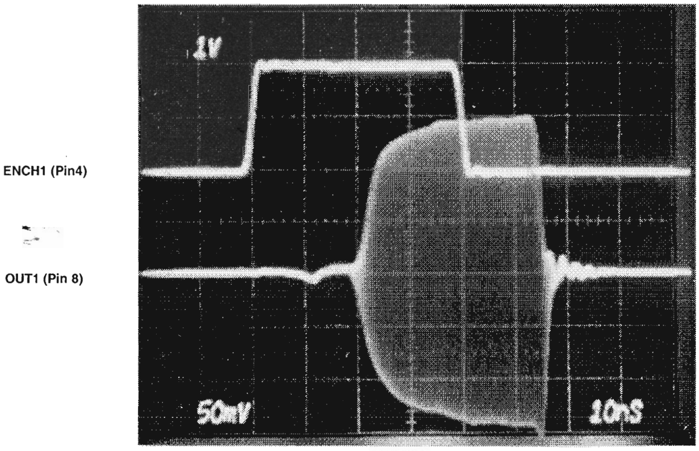


Figure 22. Switching Speed; f_{IN} = 100MHz at -6dBm, V_{DD} = 5V

I/Q transmit modulator | SA900

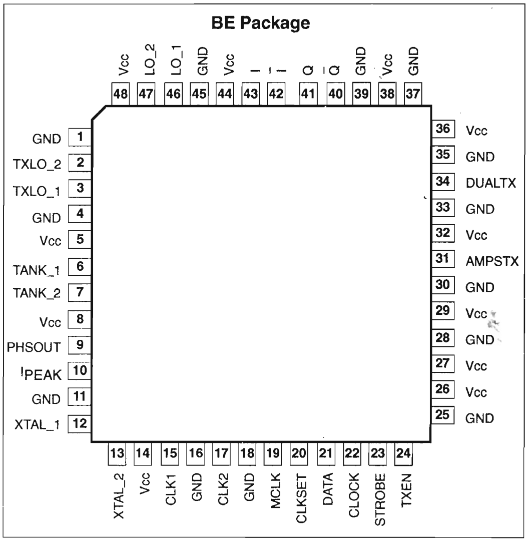
DESCRIPTION

The SA900 is a monolithic high performance, multi-function transmit modulator for use in cellular radio applications, fabricated in QUBiC BiCMOS technology. The SA900 features both analog (AMPS) mode and complex, I/Q digital (NADC IS54) mode quadrature modulation functions, a PLL synthesizer with VCO, crystal oscillator, programmable prescalers and Gilbert cell multiplier phase detector with programmable charge pump output. The DUALTX output can be used in DUAL mode cellular phone applications with the AMPS and NADC modulation being applied to the I/Q baseband inputs. The DUALTX output also provides 6-bit power control with 40dB of gain control in 0.63dB steps. In addition, buffered crystal oscillator programmable prescaler outputs are provided to support system clock reference needs. Programming of the SA900 functions are realized by a high speed 3-wire serial interface. The SA900 can be programmed into a sleep mode (low current mode providing crystal oscillator and Master Clock functions), a standby mode (providing crystal oscillator, Master Clock, System Clock 1 and Transmit LO buffer functions), and the AMPS mode and the DUAL mode configurations.

FEATURES

- V_{CC} = 4.8V
- Tx output frequency = 900MHz
- Direct modulation of RF
- DUAL mode, on-chip PA control
- I/Q modulator
- Single sideband quadrature LO generation with no external adjustments required
- On-chip crystal oscillator with 3 buffered outputs
- AMPS/TACS
- On-chip VCO
- Selective power-down
  - Low power AMPS/TACS mode
  - Low power dual mode NADC
- 48-Pin TQFP package

PIN CONFIGURATION



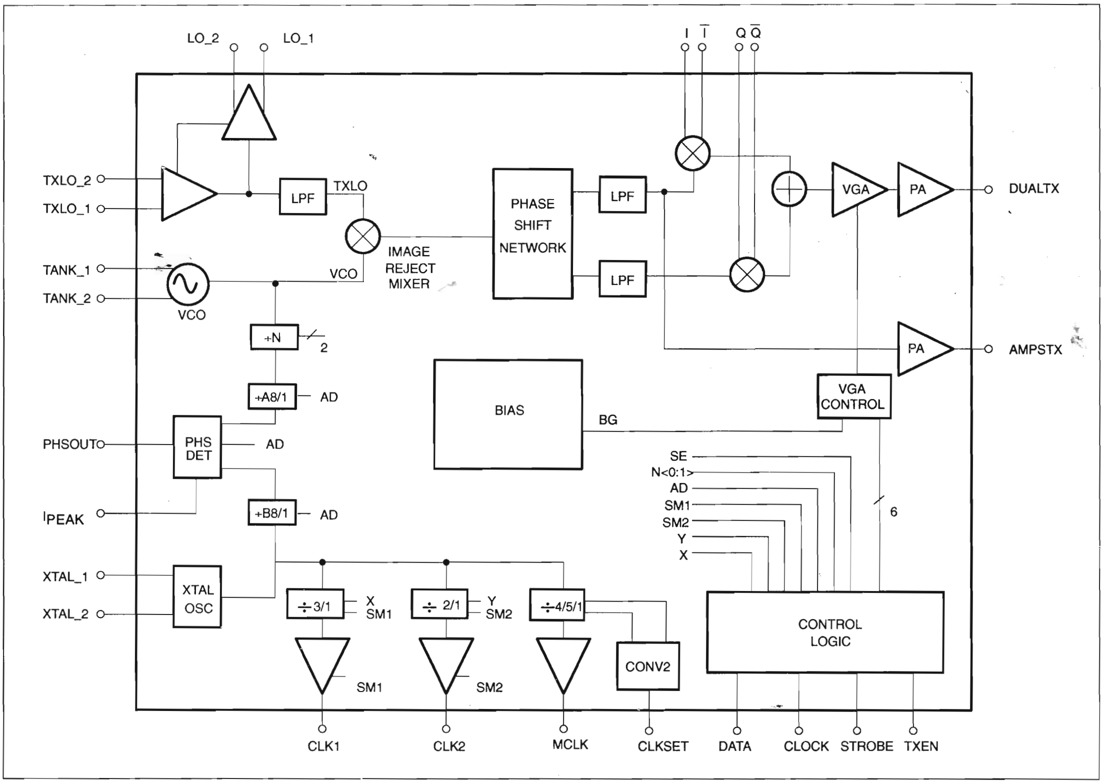
APPLICATIONS

- North American Digital Cellular (NADC IS-54)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48-Pin Thin Quad Flat Pack (TQFP)	-40 to +85°C	SA900BE	1706B

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin	Description
I	Non-inverting I Mod Signal
$\overline{I}$	Inverting I Mod Signal
TXLO_1/2	Second LO Input (differential/single-ended input)
DUALTX	RF output (850MHz) digital (DUAL) mode, complex modulated output
Q	Non-inverting Q Mod Signal
$\overline{Q}$	Inverting Q Mod Signal
CLK1	Buffered oscillator output (XO ÷3/÷1)
MCLK	Buffered oscillator output (XO ÷4/÷5/÷1)
CLK2	Buffered oscillator output (XO ÷2/÷1)
AMPSTX	RF output (850MHz) AMPS mode
V_{CC}	+5V_{DC} power supply
GND	Ground
Data	Serial data input
Clock	Serial clock input
Strobe	Data strobe input
TXEN	AMPS and Dual Mode transmit enable
CLKSET	Program control pin for MCLK prescaler
XTAL1	Crystal oscillator base input
XTAL2	Crystal oscillator emitter output
PHSOUT	Phase comparator charge pump output
TANK_1	VCO differential tank
TANK_2	VCO differential tank
LO_1/2	Buffered differential TXLO output
I_{PEAK}	Phase comparator current programming

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)	600	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+10	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}.
   48-pin TQFP: θ_{JA} = 67°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	4.5 to 5.1	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +4.8V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply range		4.5		5.1	V
I_{CC}	Supply current	Sleep mode		3.4		mA
		Standby mode		8.7		
		AMPS mode		42		
		DUAL mode		68		
$I / \overline{I}$	In-phase differential baseband input	DC		$0.5V_{CC}$		V
$Q / \overline{Q}$	Quadraphase differential baseband input	DC		$0.5V_{CC}$		V
CLKSET	Divide by 4/5/1	÷ 4		V_{CC}		V
		÷ 5		$0.5V_{CC}$		
		÷ 1		0		
V_{IL}	Clock, data, strobe, TXEN	Input low	–0.3		$0.3V_{CC}$	V
V_{IH}	Clock, data, strobe, TXEN	Input high	$0.7V_{CC}$		V_{CC}+0.3	V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +4.8V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
TXLO_1/2	Transmit LO input (AC couple) (50Ω)	Input power	-13		-10	dBm
		VSWR (50Ω)		2:1		
		Frequency range	900		1040	MHz
TANK_1/2	VCO tank differential inputs	Frequency range	90		140	MHz
PHSOUT	Phase detector charge pump output	Output level	0.5		V_{CC}–0.5	V
I_{PEAK}	PHSOUT programming	R_{SET} = 75kΩ, AD=0		100		µA
		R_{SET} = 4.7kΩ, AD=1		6.4		mA
XTAL_1	XO transistor base	XO frequency	10		45	MHz
		External drive	150		500	mV_{P-P}
CLK1	XO divide 3/1, power down SM1=0, 50% duty cycle	Frequency range	3.33		45	MHz
	÷3, X=1, ÷1, X=0	Output level, 5kΩ ∥ 7pF		1		V_{P-P}
CLK2	XO divide 2/1, power down SM2=0	Frequency range	5		45	MHz
	÷2, Y=1, ÷1, Y=0	Output level, 5kΩ ∥ 7pF		1		V_{P-P}
MCLK	XO divide 4/5/1, 50% duty cycle	Frequency range	2		45	MHz
	÷4, CLKSET = V_{CC}, ÷5, CLKSET = 0.5V_{CC}, ÷1, CLKSET = 0V	Output level, 5kΩ ∥ 7pF		1		V_{P-P}
CLOCK	Serial data clock input, 33% duty cycle	Max clock rate			10	MHz
	Serial interface (CMOS levels)	Logic LOW			0.3V_{CC}	V
	DATA, CLOCK, STROBE, TXEN	Logic HIGH	0.7V_{CC}			V
AMPSTX	AMPS output, SE=1, AD=0, TXEN=1 (AC couple)	Frequency range	820		860	MHz
		VSWR		2:1		
		Output level	0	+2		dBm
	Spurious output	869 to 894MHz		-104		dBm
		824 to 849MHz		-47		dBc
		2 to 824MHz		-41		dBc
		849 to 869MHz		-41		dBc
		894MHz to 8.49GHz		-41		dBc
	TXLO and harmonics			-21		dBc
	Adjacent channel noise power	@30kHz		-95		dBc/Hz
	Alternate channel noise power	@60kHz		-101		dBc/Hz
	Broadband noise power	869 to 894MHz		-136		dBm/Hz
DUALTX	DUAL output, SE=1, AD=1, TXEN=1 (with external matching Figure 5)	Frequency range	820		920	MHz
		VSWR		2:1		
		Output level (avg min) (I and Q quad, 0dB VGA)	0	+2		dBm
		Gain flatness		1		dB

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
DUALTX (cont.)	Linearity (0dB VGA, I and Q inphase)	3rd order		-42		dBc
		5th order		-55		dBc
		7th order		-65		dBc
	Carrier suppression (I and Q quadrature)	VGA = 0dB	-35	-45		dBc
	Carrier suppression (I and Q quadrature)	VGA = –40dB		-33		dBc
	Sideband suppression	I and Q quadrature	-35	-45		dBc
	Spurious output	869 to 894MHz		–104		dBm
		824 to 849MHz		–47		dBc
		2 to 824MHz		–41		dBc
		849 to 869MHz		–41		dBc
		894MHz to 8.49GHz		–41		dBc
	TXLO and harmonics			–21		dBc
	Broadband noise (0dB VGA)	869 to 894MHz		–136		dBm/Hz
		935 to 960MHz		–136		dBm/Hz
	Adjacent channel noise power	@30kHz		–95		dBc/Hz
	Alternate channel noise power	@60kHz		–101		dBc/Hz
$Q/\overline{Q}$	Baseband quadrature differential input	Max frequency			2	MHz
		Differential modulation level	0.6	0.8	1.0	V_{P-P}
		Differential input impedance	10			kΩ
$I/\overline{I}$	Baseband inphase differential input	Max frequency			2	MHz
		Differential modulation level	0.6	0.8	1.0	V_{P-P}
		Differential input impedance	10			kΩ
LO_1/2	Buffered TXLO differential outputs (AC coupled)	Frequency range	900		1040	MHz
		VSWR (single-ended)		2:1		
	Output impedance	single-ended		50		Ω
		differential		100		Ω
	Output level	single-ended, 50Ω		90		mV_{P-P}
		differential, 100Ω		180		mV_{P-P}

FUNCTIONAL DESCRIPTION

Dual Mode Operation

The SA900 transmit modulator provides direct single sideband quadrature modulation of the difference of the TXLO and VCO frequencies, while providing quadrature LO signals for the I/Q modulator. The quadrature LO signals are modulated with high linearity by the baseband inphase (I) and quadrature (Q) signals. The summed modulator output produces the lower sideband, while rejecting the upper sideband. The I and Q inputs also provide DC biasing for the modulator inputs. The summed output of the modulator goes to a variable gain amplifier (VGA) to control the output level, it has 40.0dB of attenuation control range, with 0.63dB steps. The power control function is programmed by means of a 6-bit word (see Table 3). The VGA output drives the power amp output stage to provide +2dBm average minimum power level (at 0dB power control) into 50Ω, in conjunction with external matching components on DUALTX. The AD (AMPS/DUAL) and the SE (synthesizer enable) bit control the power up/down of the DUAL mode function. The transition of the TXEN, from low to high turns on the modulator. The falling edge of the TXEN signal disables the synthesizer and modulator. The TXLO is a system supplied LO signal. The SA900 buffers the TXLO signal (LO_1/2) for use with the system synthesizer (such as the SA7025) to form the system LO synthesizer loop. The DUAL mode can also be used for AMPS operation. The AMPS and DUAL mode modulation is generated by the system DSP IC to provide the required I/Q baseband modulation for the SA900. The DUAL output provides low broadband noise output power (so that the receiver sensitivity is not degraded) and high linearity to meet cellular phone system needs. Table 1 provides the VGA power control limits.

The SA900 DUALTX output is externally matched with either a shunt inductor to V_{CC} and a series capacitor or a shunt inductor to V_{CC} and a series inductor. This matches the DUALTX output to 50Ω. Values of the matching components are dependent on PCB layout, typical values are shown in Figure 5.

Table 1. VGA Power Control Limits

Attenuation (dB)	Tolerance[1]
0.0 to 21.4	±0.4dB
22.0 to 27.7	±1.0dB
28.4 to 40.0	±2.0dB

1. Guaranteed to be monotonic.

AMPS Mode Operation

The SA900 can be configured to operate in the AMPS mode, where FM modulation is applied to the SA900's VCO. For the AMPS mode, the VCO is configured with the proper synthesizer bandwidth to allow the application of the AMPS modulation to the VCO varactor tuned tank circuit. The modulated VCO signal is input into an image reject mixer along with the TXLO signal, where the upper sideband is rejected. This single sideband modulated signal then drives the AMPS output power amplifier. The PA provides +2dBm power level into 50Ω, with no external matching components required. The AD (AMPS/DUAL) and the SE (synthesizer enable) bit control the power up/down of the AMPS mode function. The transition of the TXEN signal from low to high turns on the modulator. The falling edge of TXEN signal disables the synthesizer and the modulator.

Synthesizer Operation

The SA900 synthesizer is comprised of the differential VCO circuit, with external tank components, the Gilbert cell multiplier phase detector with programmable charge pump current, crystal oscillator and programmable prescalers. The charge pump output drives an external second order loop filter. The output of the loop filter is used to provide the control voltage to the VCO tuning varactor to complete the PLL synthesizer. The synthesized VCO output frequency is mixed with the TXLO signal to generate the transmit LO from the lower sideband (the difference of the VCO and TXLO frequencies). The output of VCO is fed to a programmable /N prescaler with user selectable divides of 6, 7, 8 and 9 (all divides configured to provide 50% duty cycle). The output of the /N divider drives the A8/1 prescaler. The A8/1 divide is selected by the AD control bit (AD=1 for /1, and AD=0 for /8). The output of the divide A8/1 is fed into one input of the phase detector. The reference input for the phase comparator is generated from the crystal oscillator (XO) output from the B8/1 prescaler. The B8/1 divide is selected by the AD control bit (AD=0 for /8, and AD=1 for /1). The phase detector compares the prescaled XO reference phase to the VCO prescaled phase, to generate a charge pump output current proportional to the phase error. The phase detector, a Gilbert cell multiplier type, having a linear output from 0 to π ($\pi/2 \pm \pi/2$). The charge pump peak output current is programmable from 100µA for the AMPS mode (AD=0) to a maximum of 6.4mA for the DUAL mode (AD=1) by way of an external current setting resistor placed from I_{PEAK} to circuit ground. The typical loop filter network

Table 2. Data Word Format

Mnemonics	Bits	Function
A0	1 (MSB)	Address bit 0 (1)
A1	2	Address bit 1 (0)
A2	3	Address bit 2 (1)
A3	4	Address bit 4 (1)
PC0	5	Power control bit 0
PC1	6	Power control bit 1
PC2	7	Power control bit 2
PC3	8	Power control bit 3
PC4	9	Power control bit 4
PC5	10	Power control bit 5
N0	11	Divide N bit 0
N1	12	Divide N bit 1
AD	13	AMPS/DUAL mode select bit
SE	14	Synthesizer enable bit
NA	15	NA
SM1	16	Sleep mode 1 control bit
SM2	17	Sleep mode 2 control bit
X	18	Divide 3/1 control bit
Y	19	Divide 2/1 control bit
NA	20	NA
NA	21	NA
NA	22	NA
NA	23	NA
NA	24 (LSB)	NA

is shown in Figure 1. The charge pump current output is programmed by

$$AD = 0 \qquad I_{OUT} = 6 \cdot \left(\frac{1.25V}{R_{SET}}\right)$$

$$AD = 1 \qquad I_{OUT} = 24 \cdot \left(\frac{1.25V}{R_{SET}}\right)$$

where R_{SET} is placed between I_{PEAK} and GROUND.

The PLL frequency is determined by

$$VCO = XO \cdot N \cdot \frac{\left(\frac{A8}{1}\right)}{\left(\frac{B8}{1}\right)}$$

where N=6, 7, 8, 9 and A8/1 and B8/1 are controlled by the AD bit (AD=1 A8/1 and B8/1 are divide by 1, AD=0 A8/1 and B8/1 are divide 8).

VCO Operation

The VCO is designed to operate from 90MHz to 140MHz. The VCO tank is configured using a parallel inductor and a dual common cathode tuning varactor diodes. DC blocking capacitors are used to isolate the varactor control voltage from the VCO tank DC bias voltages. The VCO tuning voltage is generated from the output of the PLL loop filter. The VCO tank configuration is shown in Figure 2.

Crystal Oscillator (XO) Operation

For cellular radio applications, the SA900 will most likely utilize an external reference TCXO in order to provide the frequency stability necessary to operate to system requirements. The output of the system TCXO can be AC coupled to the XTAL_1 input. However, for applications that do not require such accuracy the XO circuit can be configured as a Colpitts type oscillator with the addition of two external capacitors along with the reference crystal and a trim capacitor as shown in Figure 3.

Programmable Clock Outputs

The SA900 generates three buffered XO outputs used for external reference signals. The XO feeds three sets of programmable prescalers, the prescaler outputs are buffered to provide the CLK1, CLK2 and MCLK signals. The CLK1 signal is a selectable divide 3/1 (X=1 divide 3, X=0 divide 1), 50% duty cycle, of the XO reference signal. The CLK2 signal is a selectable divide 2/1 (Y=1 divide 2, Y=0 divide 1), 50% duty cycle, of the XO reference signal. The MCLK signal is a selectable divide 4/5/1 (CLKSET = V_{CC} divide 4, CLKSET = $V_{CC}/2$ divide 5, and CLKSET = 0V divide 1), 50% duty cycle, of the XO reference signal. MCLK is externally set by means of the tri-level CLKSET input to provide a default master system clock prior to programming the SA900.

Programming Operation

The SA900 is configured by means of a 3-wire input (CLOCK, STROBE, DATA) to program the AMPS and DUAL modes, in addition there are two power saving modes of operation, SLEEP and STANDBY. The control logic section of the SA900 is designed using low power CMOS logic. During SLEEP mode only the circuitry required to provide a master clock (MCLK) to the digital portion of the system is enabled. During the STANDBY mode of operation MCLK, CLK1 and the TXLO and buffered LO outputs are powered on, which may be the case when the system is in the receive only mode. In the AMPS or DUAL operational modes all functions of the SA900 are powered on to support receive, transmit and system clock functions. The programming of the SA900 is identical to the programming format of the SA7025 low-voltage 1GHz fractional-N synthesizer, that can be used in conjunction with the SA900 to provide the cellular radio channel selection.

The programming data is structured as a 24 bit long serial data word; the word includes 4 address bits (dedicated 1 0 1 1) for chip select. Data bits are shifted in on the leading edge of the clock, with the least significant bit (LSB) first and the most significant bit (MSB) last. Table 2 shows data word format, the 15th and last 5 bits are not used. Figure 4 shows the chip timing diagram.

Address

A0	A1	A2	A3
1	0	1	1

Divide By N

N0	N1	Divide
0	0	6
1	0	7
0	1	8
1	1	9

AMPS/DUAL Mode

The A/D mode select enables or disables that portion of the circuitry used for either the AMPS or DUAL mode of operation.

AD	Mode
0	AMPS
1	DUAL

Synthesizer Enable

The SE bit turns on and off the synthesizer circuitry.

SE	Operation
0	Disabled
1	Enabled

Sleep Mode 1

The SM1 bit is used to power down the TXLO buffer, the divide 3/1 prescaler and the CLK1 output buffer.

SM1	Operation
0	Power down
1	Power up (STANDBY)

Sleep Mode 2

The SM2 bit is used to power down the divide 2/1 prescaler and the CLK2.

SM2	Operation
0	Power down
1	Power up (with SM1=1 normal operation)

Divide 3

X	Operation
0	Divide 1
1	Divide 3

Divide 2

Y	Operation
0	Divide 1
1	Divide 2

Table 3. Power Control

Atten (dB)	PC0 (0.6dB)	PC1 (1.3dB)	PC2 (2.5dB)	PC3 (5.0dB)	PC4 (10.0dB)	PC5 (20.0dB)
0	0	0	0	0	0	0
0.6	1	0	0	0	0	0
1.3	0	1	0	0	0	0
1.9	1	1	0	0	0	0
2.5	0	0	1	0	0	0
3.2	1	0	1	0	0	0
3.8	0	1	1	0	0	0
4.4	1	1	1	0	0	0
5.0	0	0	0	1	0	0
5.7	1	0	0	1	0	0
6.3	0	1	0	1	0	0
⋮						
23.3	1	0	1	0	0	1
⋮						
39.7	1	1	1	1	1	1

Component Designator	Value	
	DUAL Mode	AMPS Mode
R1	560Ω	560Ω
R2	1kΩ	5.6kΩ
C1	2.2nF	2.7µF
C2	No Load	.27µF
C3	33pF	6.8nF
R_{SET}	15kΩ	75kΩ

Typical Filter Network

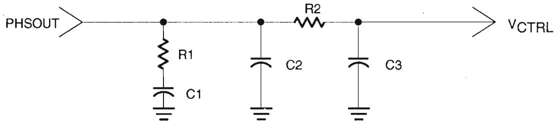
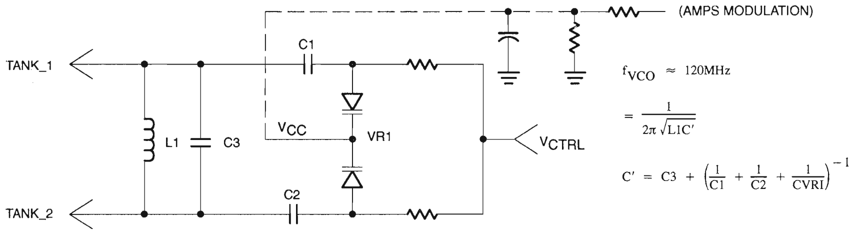


Figure 1. PLL Loop Filter



$$f_{VCO} \approx 120\text{MHz}$$

$$= \frac{1}{2\pi\sqrt{L1C'}}$$

$$C' = C3 + \left(\frac{1}{C1} + \frac{1}{C2} + \frac{1}{CVR1}\right)^{-1}$$

C1 = C2 = 33pF
C3 = 12pF
L1 = 82nH
VR1 TOKO KV1470

Figure 2. VCO Tank Configuration

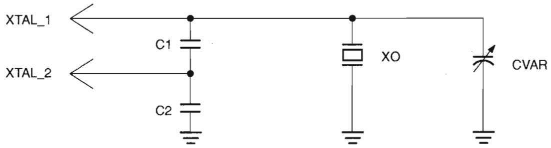
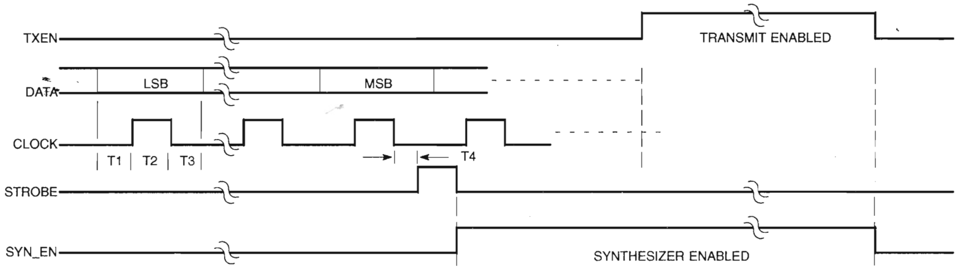


Figure 3. Crystal Oscillator Configuration



$T1 = T2 = T3 = \frac{1}{3CLOCK}, \; T_4 = \frac{1}{3CLOCK}$

Figure 4. Chip Timing Diagram

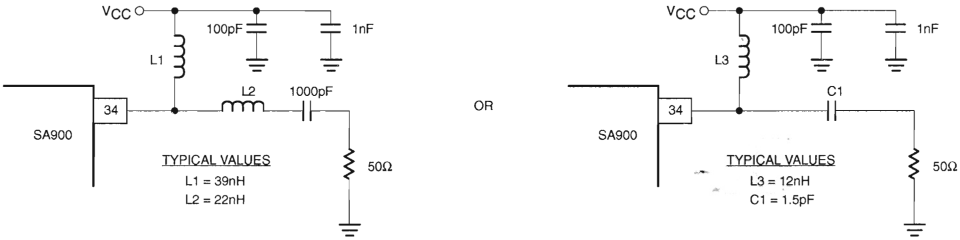
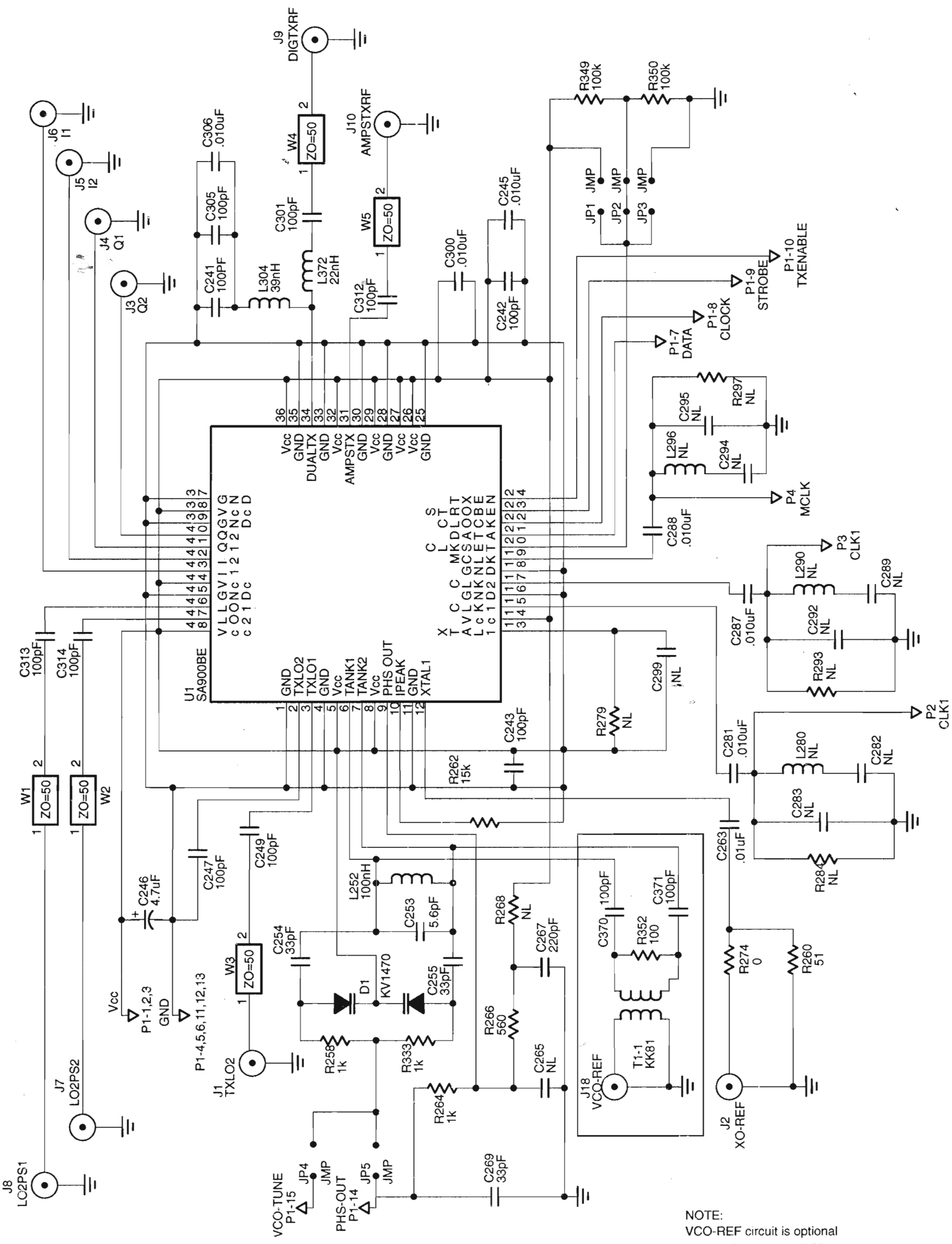


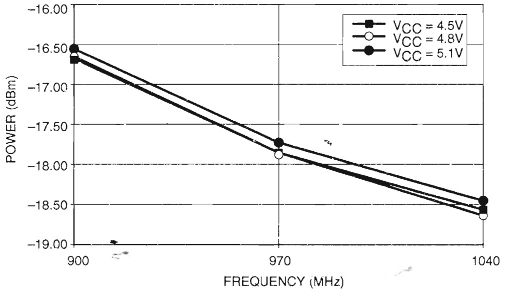
Figure 5. DUALTX Output Matching



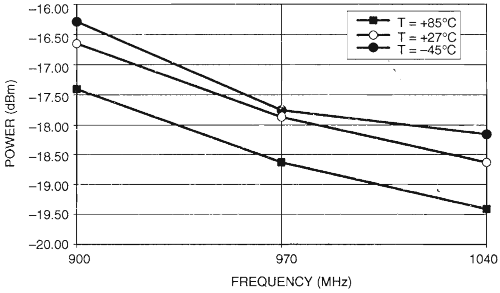
NOTE:
VCO-REF circuit is optional
L372 is C307 on the PCB
C246 combines C240 and C244 on the PCB

Figure 6. SA900 Application Circuit

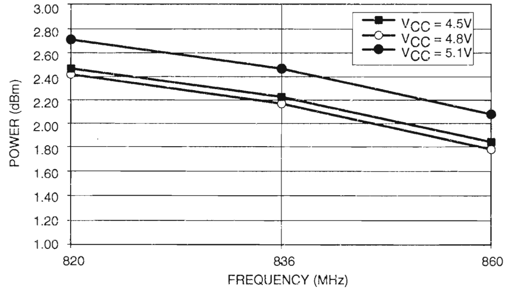
PERFORMANCE CHARACTERISTICS



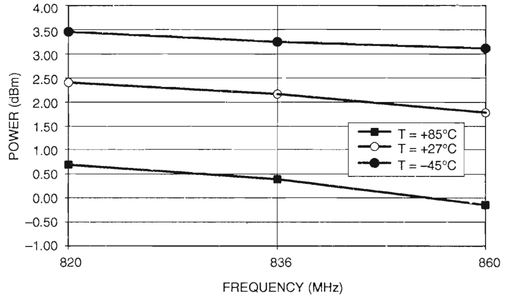
LO Buffer vs. Frequency (27°C, TXLO = –10dBm)



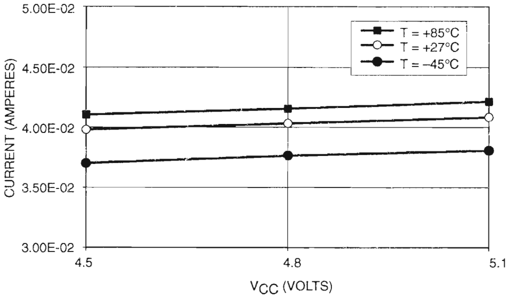
LO Buffer vs. Frequency (V_{CC} = 4.8V, TXLO = –10dBm)



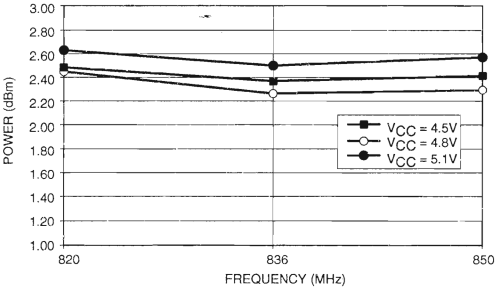
AMPTX vs. Frequency (27°C, TXLO = –10dBm)



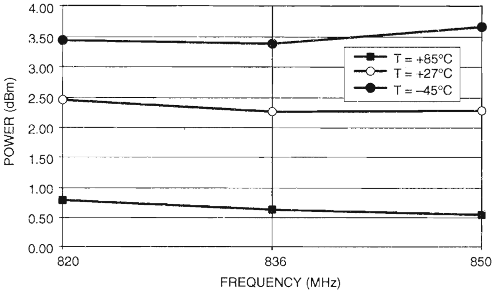
AMPTX vs. Frequency (V_{CC} = 4.8V, TXLO = –10dBm)



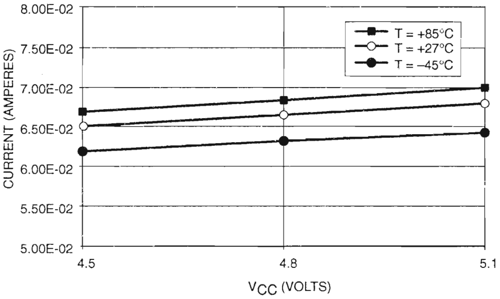
AMP I_{CC} vs. V_{CC}



DUALTX vs. Frequency (27°C, TXLO = –10dBm)

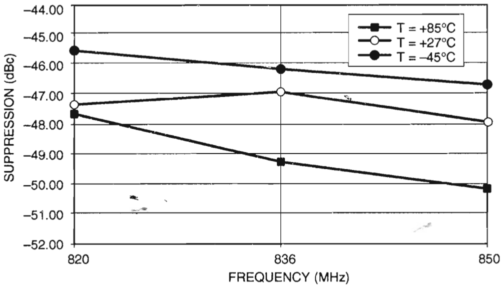


DUALTX vs. Frequency (V_{CC} = 4.8V, TXLO = –10dBm)

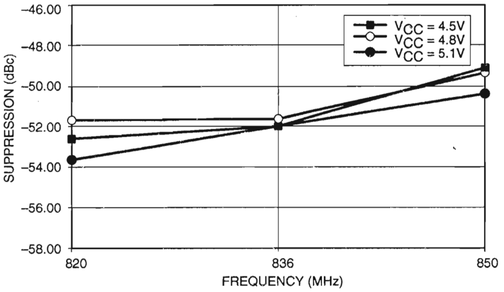


DUAL I_{CC} vs. V_{CC}

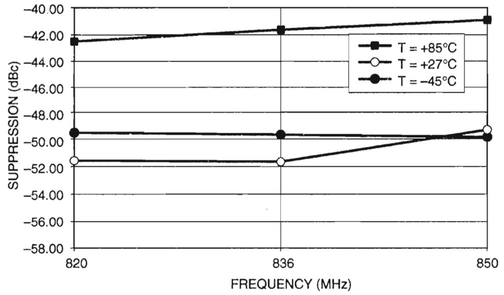
PERFORMANCE CHARACTERISTICS



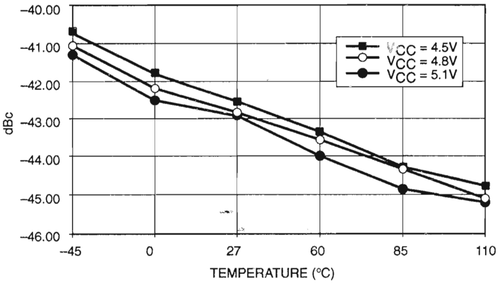
DUALTX Carrier Suppression vs. Frequency (V_{CC} = 4.8, TXLO = –10dBm Single Sideband Mode, With Respect to Lower Sideband)



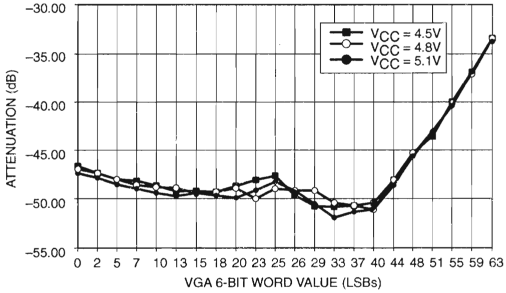
DUALTX Sideband Suppression vs. Frequency (Temperature = 27°C, TXLO = –10dBm Single Sideband Mode, With Respect to Lower Sideband)



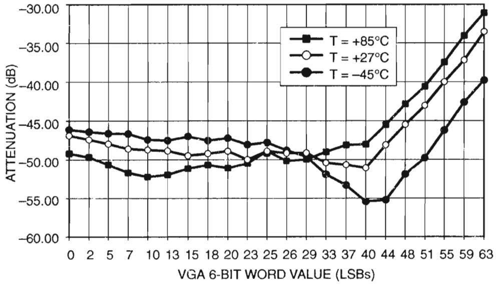
DUALTX Sideband Suppression vs. Frequency (V_{CC} = 4.8, TXLO = –10dBm Single Sideband Mode, With Respect to Lower Sideband)



DUALTX 3rd Order Products vs Temperature (TXLO = –10dBm, f = 836MHz, 0dB VGA I/Q Inphase)

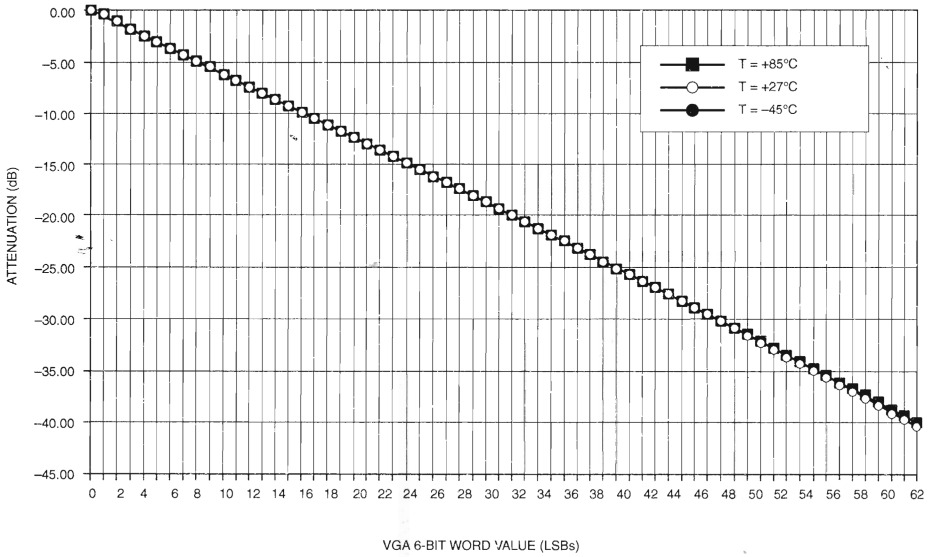


DUALTX Carrier Suppression vs VGA Range (27°C, f = 836MHz, TXLO = –10dBm)

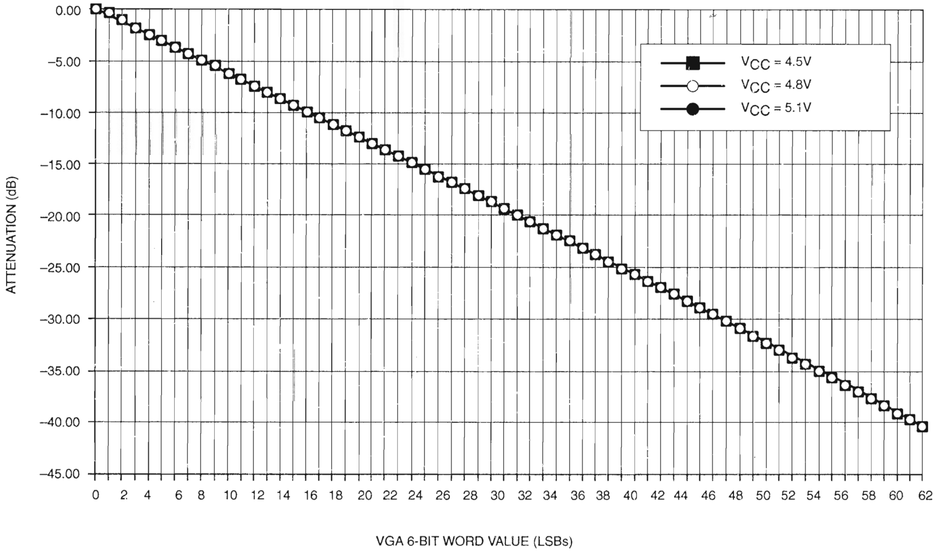


DUALTX Carrier Suppression vs VGA Range (V_{CC} = 4.8V, f = 836MHz, TXLO = –10dBm)

PERFORMANCE CHARACTERISTICS



DUALTX VGA Attenuation Profile vs. Temperature (V_{CC} = 4.8V, f = 836MHz, TXLO = –10dBm)



DUALTX VGA Attenuation Profile vs. V_{CC} (27°C, f = 836MHz, TXLO = –10dBm)

SA900 I/Q transmit modulator for 1GHz applications

AN1892

Author: Wing S. Djen

INTRODUCTION

The SA900 (Figure 1) is a truly universal in-phase and quadrature (I/Q) radio transmitter that can perform many types of analog and digital modulation including AM, FM, SSB, QAM, BPSK, QPSK, FSK, etc. It is a highly integrated system which saves space and cost for the manufacturers producing cellular and wireless products. The device allows baseband signals to directly modulate the I/Q carriers, which are generated by internal phase shift network, in the 1GHz range, and to maintain good linearity required for linear modulation scheme (e.g., $\pi/4$-DQPSK). It contains an on-chip frequency divider, phase detector, and VCO, which can be built into a phase-locked loop (PLL) frequency synthesizer to create a transmit offset frequency. Its unique internal design allows frequency conversion without having an external image rejection filter for eliminating the sum term after mixing. The SA900 meets the specifications required by the IS-54, the industry standard for North America Digital Cellular (NADC) system. This application note reviews the basic concept of I/Q modulation and discusses the key points when designing the SA900 for an RF transmitter.

I/Q MODULATION

Any bandpass RF signals can be represented in polar form by

$$s(t) = A(t)\cos[\omega_c t + \phi(t)] \qquad \text{(EQ. 1)}$$

where A(t) is the signal envelope and $\phi(t)$ is the phase. By using the trigonometric identities, we can represent EQ. 1 in rectangular form by

$$s(t) = I(t)\cos[\omega_c t] - Q(t)\sin[\omega_c t] \qquad \text{(EQ. 2)}$$

$$I(t) = A(t)\cos[\phi(t)]$$

$$Q(t) = A(t)\sin[\phi(t)]$$

Since the baseband signals I(t) and Q(t) modulate two exactly 90° out-of-phase carriers $\cos(w_c t)$ and $-\sin(w_c t)$ respectively, we call the system implementing EQ. 2 an in-phase and quadrature (I/Q) modulator. Figure 2 shows the mathematics and hardware implementation of an I/Q modulator.

The local oscillator, usually a VCO within a PLL, generates the carrier and is split into two equal signals. One goes directly into a double-balanced mixer to form the I-channel and the other one goes into the other mixer via a 90° phase shifter (realized by passive elements) to provide the Q-channel. The baseband signals I(t) and Q(t), either analog or digital in nature, modulate the carrier to produce the I and Q components which are finally combined to form the desired RF transmitting signal. Since any RF signal can be represented in the I/Q form, any modulation scheme can be implemented by an I/Q modulator.

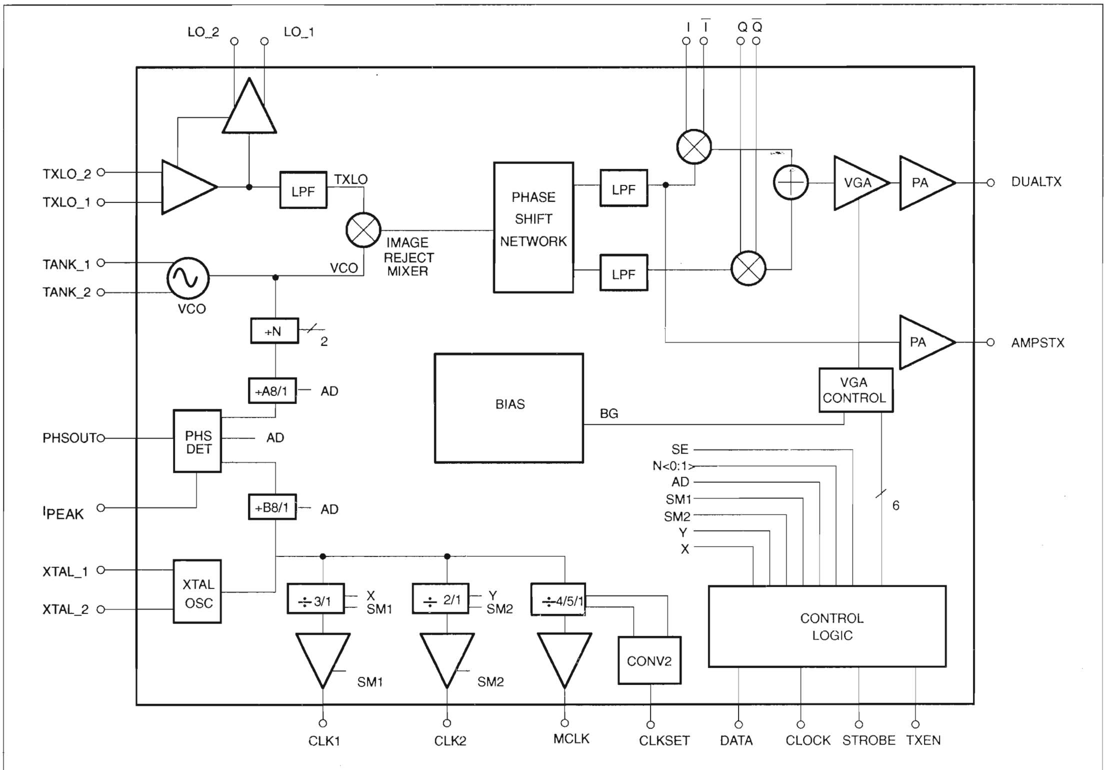


Figure 1. SA900 Transmit Modulator

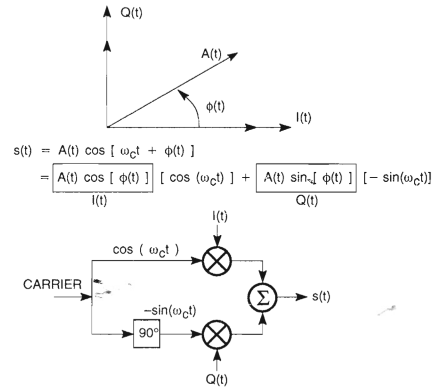

Q(t)
A(t)
φ(t)
I(t)
s(t) = A(t) cos [ω_Ct + φ(t)]
= A(t) cos [φ(t)] [cos (ω_Ct)] + A(t) sin [φ(t)] [− sin(ω_Ct)]
I(t)
Q(t)
I(t)
cos (ω_Ct)
CARRIER
Σ
s(t)
−sin(ω_Ct)
90°
Q(t)

Figure 2. Mathematical Representation and Hardware Implementation of I/Q Modulator

Linear Digital Modulation

Linear digital modulation techniques depend on varying the phase and/or magnitude of an analog carrier according to some digital information: ones and zeros. This digital information can be the output of an analog-to-digital converter (e.g. voice codec), or it can be digital data in some standard formats (e.g. ASCII). The most popular digital signaling format is non return-to-zero (NRZ), where 1s and 0s are converted into signal with amplitude of 1 and -1, respectively, in a symbol duration. Since NRZ signal has infinite bandwidth, transmit filters have to be used to limit the spectral spreading. To ensure each NRZ symbol does not smear into its neighbors due to low-pass filtering and channel distortion causing inter-symbol interference (ISI), the frequency response of the low-pass filter has to satisfy Nyquist criteria. One example of this type of filter is the linear phase square-root-raised cosine filter. Together with the same type of filter for receive low-pass filtering, the signal is guaranteed ISI free in a Gaussian environment. One straight-forward technique of transmitting these bandlimited signals through communication channels would be applying it directly to the mixer of the I-channel to generate the RF signal. This is known as binary phase shift keying (BPSK), where the phase of the carrier is shifted 180° to transmit a data change from 0 to 1 or 1 to 0.

Quadrature or quaternary phase shift keying (QPSK) is a much more common type of modulation scheme used in mobile and satellite communications. It has four possible states (90° apart) and each of them represents two bits of data. Figure 3 shows the baseband generator for QPSK (without the differential phase encoder). NRZ data bits go through the serial-to-parallel converter (see Figure 4) and are mapped in accordance to some rules to generate I and Q values. The generic rule will be the values of I and Q components are 1 and 1 for the data bits “11” (45°) and -1 and -1 for the data bits “00” (-135°). These discrete signals have to be bandlimited by Nyquist low-pass filters to be ISI free.

A more sophisticated way of mapping results in π/4-DQPSK (D for differential encoding), which is chosen for North America Digital Cellular (IS-54), Personal Digital Cellular (PDC) in Japan, and Personal Handy Phone System (PHS) in Japan. In this scheme, consecutive pairs of bits are encoded into one of the four possible phases: π/4 for “11”, 3π/4 for “01”, -3π/4 for “00”, and -π/4 for “10”. However, unlike the previous case that “11” is always π/4 and “00” is always -3π/4, the encoded phases are the degrees that the carrier has to shift at each sampling instances. Thus, the information is contained in the phase difference (differential) instead of absolute phase for π/4-DQPSK.

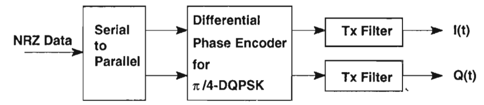


Figure 3. QPSK and π/4-DQPSK Baseband Generator

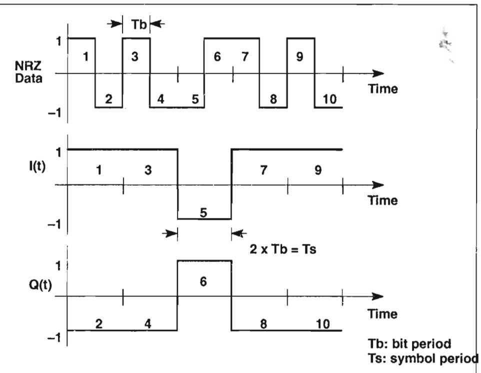


Figure 4. Serial-to-Parallel Conversion

A better way to tell the difference between QPSK and π/4-DQPSK is by looking at the signal constellation diagram, shown in Figure 5, which displays the possible values of I and Q vectors and change of states. Constellation diagram is also known as phase diagram because it shows the phase of the carrier at the sampling point. Notice that the phases of QPSK are assigned for every two bits of data; therefore, it can transmit twice as much information as BPSK in a given bandwidth, i.e., more bandwidth efficient. 8-PSK is another type of modulation used for high efficiency requirements. It maps three bits into 8 phases, 45° apart, in the constellation. More spectral efficient modulation can be created by mapping more bits into one phase at each sampling point. However, as you put more dots in the signal constellation, the signal susceptibility to noise is lower because the decision distance is shorter (dots are closer). Then, it requires higher carrier-to-noise (C/N) ratio to maintain the same bit error rate (BER).

One common misconception is that since π/4-DQPSK has 8 states in the constellation, it is just another type of 8-PSK. Notice that at every sampling instant, the carrier of π/4-DQPSK is only allowed to switch to one of the 4 possible states (see Figure 5). So, we still have two data bits which get encoded into 4 phases. Thus, it has the same spectral efficiency as QPSK for the same carrier power. The reason for using this modulation scheme is twofold. First, the envelope fluctuation, which causes spectral spreading due to nonlinearity of transmitter and amplifier, is reduced because the maximum phase shift is 135° instead of 180°. Second, the signal can be demodulated non-coherently which simplifies the receiver circuitry by eliminating the need for carrier recovery.

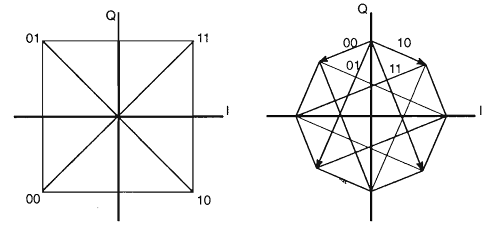


Figure 5. Signal Constellation of QPSK and π/4-DQPSK

Digital and Analog FM

Another family of digital modulation is categorized by frequency change of the carrier instead of phase and/or amplitude change. One of them is frequency shift keying (FSK), where the carrier switches between two frequencies. FSK is also known as digital FM because it can be generated by feeding the NRZ data stream into an analog VCO. FSK appears as a unit circle in the signal constellation because the RF signal envelope is constant and the phase is continuous. Baseband filtering is usually applied for FSK to limit the RF bandwidth of the signal so that more channels can fit into a given frequency band.

One common modulation of this type is known as Gaussian minimum shift keying (GMSK), which is used for GSM and some other wireless applications. GMSK can be generated by following its definition: bandlimit the NRZ data stream by a Gaussian low-pass filter, then modulate a VCO with modulation index (2 x frequency deviation/bit rate) set to 0.5. In other words, the single-sided frequency deviation is one fourth of the bit rate ($\Delta f = R/4$).

Another way of generating GMSK is by I/Q modulator. Referring back to EQ. 2, any RF signal can be split into I and Q components. Unlike the QPSK mentioned before, baseband I(t) and Q(t) are not discrete points for FM signals; rather, they are continuous functions of time. The way to produce FM is shown in Figure 6. We first store all the possible values of cos[$\phi(t)$] and sin[$\phi(t)$] in a ROM lookup table, which will be addressed by the incoming data to generate the I and Q samples. The output data from the ROM is then applied to D/A converters, after low-pass filtering for signal smoothing, to produce the analog baseband I and Q signals. This method guarantees the modulation index to be exactly 0.5, which is required for coherent detection of GMSK (e.g. GSM system). The same I/Q principle can also be applied to generating analog FM signals.

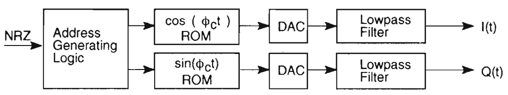


Figure 6. Digital FM (e.g. GMSK) Baseband I/Q Generator

Single sideband AM (SSB-AM)

AM signals can be divided into 3 types: the conventional AM, double sideband suppressed carrier AM (DSB-AM) and SSB-AM. The first type is not attractive because for 100% modulation, two-thirds of the transmit signal power appears in the carrier, which itself conveys no information at all. By using a balanced mixer (e.g. Gilbert cell), one can generate DSB-AM, where the carrier is totally suppressed and only the upper and lower sidebands are present. However, this is still not the best because the information is transmitted twice, once in each sideband. To further increase the efficiency of transmission, only one sideband is needed to deliver the information. The SSB-AM can be generated by an I/Q modulator with the baseband information feeding the modulator (by quadrature), as shown in Figure 7. This modulation technique can greatly reduce the bandwidth of the signal and allows more signals to be transmitted in a given frequency band. This topic is discussed in detail in Philips RF application note, #AN1981, "New low-power single sideband circuits".

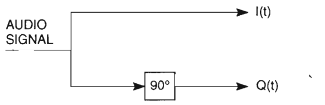


Figure 7. Baseband Processing for SSB-AM

SYSTEM ARCHITECTURE

There are usually two schemes, the dual conversion and direct conversion, used for implementing transmit modulators. Dual conversion is simpler to implement by modulating an oscillator at lower frequency and then up-converting to the carrier frequency. This scheme, however, is more expensive due to the need for additional filtering and more PC board space. By using only one mixer, direct conversion requires fewer components but is harder to implement.

The problems that direct conversion suffers are carrier leakage and modulated signal coupling. Poor RF isolation of the surface mount packages will allow the carrier to be present at the transmitter output thus making it difficult to have -40dBc carrier suppression. In addition to that, modulated RF signal would couple back to the oscillator (usually a VCO in a PLL synthesizer loop) and cause modulation distortion.

Based on the concept of dual conversion, the SA900 uses an image rejection mixer to eliminate the need for IF filtering and allow monolithic integration. The transmit carrier (LO) is down-converted by the frequency synthesized by the on-chip VCO, which operates from 90 to 140MHz. This LO is then modulated by the baseband I/Q signals to obtain a complex modulation scheme. The image (sum term) after mixing and LO is sufficiently suppressed by the image rejection mixer. Any residual amounts can be further suppressed by an external duplex filter.

Figures 8 and 9, respectively, show how the SA900 can be used in frequency division duplex (FDD) and time division duplex (TDD) transceivers. Notice that the LO for both systems is running at a frequency which is higher than the transmit frequency, thus minimizing carrier leakage. In the FDD system only one external VCO is required for generating both transmit and receive LO when using the SA900.

Figure 10 shows the IS-54 front-end chip set which consists of the SA601, SA7025, SA900, and SA637. This receiver architecture (SA637) supports a digital magnitude/phase baseband demodulator. An alternate configuration will be using the SA606 FM/IF receiver in conjunction with an external I/Q demodulator IC. The following table shows the possible configurations for the IS-54 handsets using the SA900 as transmitters.

Rx 1st IF	On-Chip VCO Frequency	On-Chip ÷N Value	Crystal Frequency
83.16MHz	128.16MHz	6	21.36MHz
71.64MHz	116.64MHz	6	19.44MHz
45MHz	90MHz	6	15MHz
84.6MHz	129.6MHz	9	14.4MHz

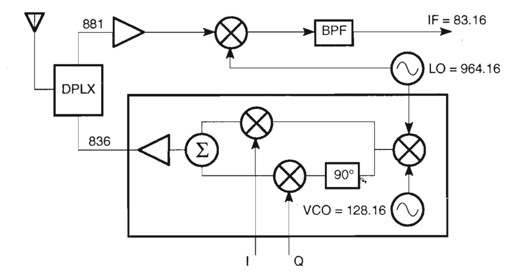


Figure 8. FDD System Using SA900

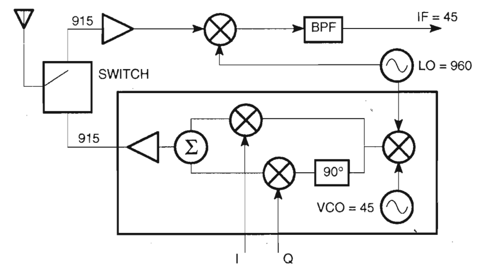


Figure 9. TDD System Using SA900

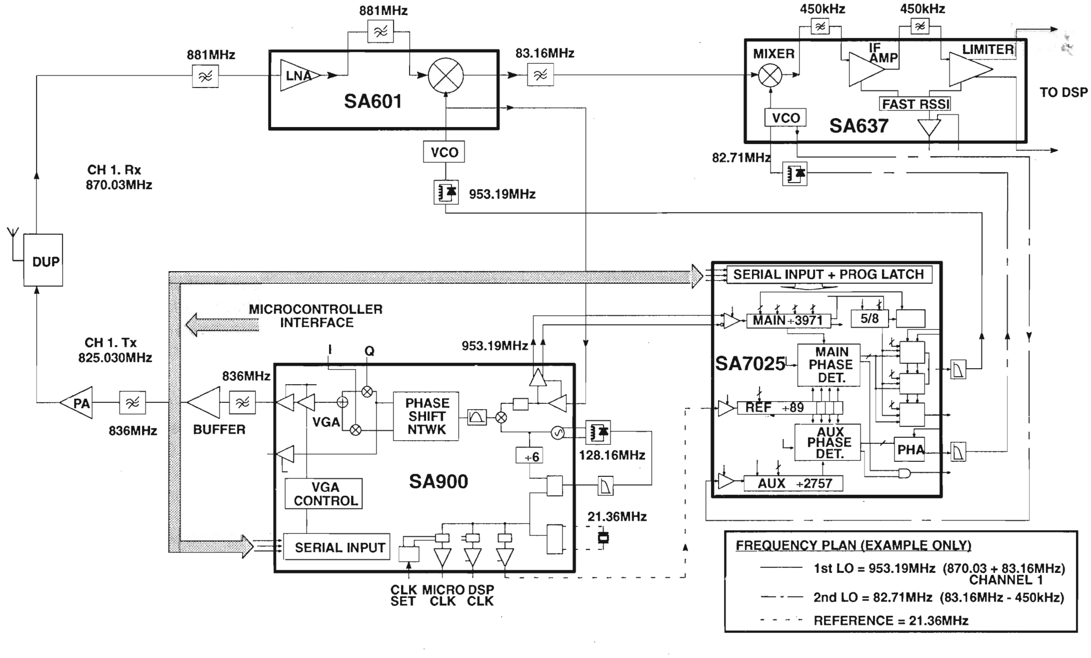


Figure 10. IS-54 front-end chip set from Philips

DESIGNING WITH THE SA900

Baseband I/Q Inputs

The baseband modulation inputs are designed to be driven differentially for the SA900 to operate at its best. The I and Q inputs should have a DC offset of $V_{CC}/2$, which is externally provided by common DSP chips. If all four inputs are biased from the same source, the device can tolerate $\pm 0.5V_{DC}$ error; however, inaccuracy of DC bias between I1/I2 or Q1/Q2 causes reduced suppression of the carrier. Thus, it is important to have a well regulated DC supply for I and Q signal biasing. The bandwidth of the inputs is much higher than the specified 2MHz. Approximately 2dB of power loss will be experienced if the I and Q inputs are 50MHz.

The SA900 generates a minimum of 0dBm of power to a 50Ω load when the amplitude of the I and Q signals are $400mV_{P-P}$. The output power will decrease by 6dB for every 50% decrease in I/Q amplitude. Single-ended I and Q sources can be used but are not recommended due to the degradation in carrier suppression (more than 10dB compared to differential). In addition, the entire noise performance of the device will suffer. $V_{CC}/2$ should be applied to I2 and Q2 pins if the part is driven single-endedly.

Transmit Local Oscillator

The transmit local oscillator path consists of a TXLO input buffer, LO output buffer, VCO, image rejection mixer and phase shift network. Together with a few external components, this section provides the I and Q carrier for modulation.

The TXLO inputs and LO outputs are designed to be used in an external PLL which synthesizes different frequencies for channel selection. The RF signal being generated is fed into TXLO inputs and then comes out of LO outputs to complete the system synthesizer loop. The TXLO inputs are differential in nature and have a VSWR of 2:1 with input impedance of 50Ω. Single-ended sources can be used by AC grounding the TXLO_2, as done on the demoboard. This signal should also be AC coupled into the

TXLO_1. The frequency range for these inputs is from 900 to 1040MHz while the input power should be between -10 to -13dBm. The output level will be changed significantly if the input level is below -25dBm.

The output power of the LO buffered signal changes by about 2dB when the SA900 is in a different mode of operation. Typical values are -13.5dBm and -15.5dBm for DUAL mode and STANDBY mode, respectively.

The 90° phase shift network, realized by RC networks, is capable of operating over a wide frequency range. Even though their frequency characteristics are optimized for cellular band, the part can also be used in other applications in a different band. In such cases, designers have to test the part experimentally to find out the performance, such as sideband suppression, carrier suppression, and image rejection.

Crystal Oscillator

The crystal oscillator (XTAL_1 and XTAL_2 pins) is used to provide reference frequency between 10 and 45MHz for the phase detector and the three on-chip clocks. It can be configured as a crystal oscillator using external crystal and capacitors, or it can be driven by an external source. In the latter case, pin XTAL_2 can be left floating. Information regarding crystal oscillator design can be found in Philips RF application note, #AN 1982, "Apply the Oscillator of the NE602 in Low-Power Mixer Applications."

VCO

The VCO, together with the phase detector, the divider and external low-pass filter, can form a PLL for the transmit offset frequency. The image reject mixer down-converts the TXLO signal to the RF carrier by the amount of VCO frequency. Thus, the TXLO frequency should be the desired channel frequency plus the IF offset generated by the VCO. Notice that the part will not function if the VCO section is not used.

The VCO is designed for generating IF frequency between 90MHz and 140MHz. Together with an external varactor diode and resonator, it can be configured as an oscillator as shown in Figure 11.

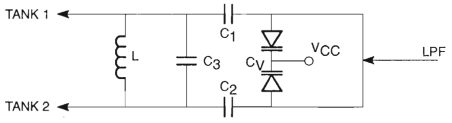


Figure 11. VCO Tank Circuit

The resonant frequency of such a circuit is

$$f_{VCO} = \frac{1}{2\pi\sqrt{LC_T}} \qquad \text{(EQ. 3)}$$

where $C_T = (C_1 // C_2 // C_V) + C_3$. C_V is a varactor diode of which capacitance changes linearly with the voltage across it.

Calculation:
$C_1 = C_2 = 33\text{pF}$
$C_3 = 5.6\text{pF}$
$C_V = 33.5\text{pF}$ @ 2.5V
$L = 100\text{nH}$
$C_T = 5.6 + (1/33 + 1/33 + 1/33.5)^{-1} = 16.7\text{pF}$

$$f_{VCO} = \frac{1}{2\pi\ (100e\text{-}9 \cdot 16.7e\text{-}12)^{0.5}} = 123\text{MHz}$$

On the demoboard, a 1:1 ratio RF transformer is also included to allow single-ended external source driving differential inputs when the VCO is not used.

When designing the VCO, careful PCB layout has to be made. Traces have to be short to avoid the parasitic capacitance and inductance which may cause unwanted oscillation. Referring to EQ. 3, there is a large combination of L and C_T values that will give the same resonant frequency. If undesired spurs are found in the design due to PCB layout, experimenting with a different set of LC values may sometimes solve the problem.

Output impedance matching

The equivalent output impedance at the DUALTX pin is approximately equal to 600Ω in parallel with 2pF at 830MHz. It has to be matched properly to generate maximum power into a 50Ω load (e.g. SAW filter). Figure 12 shows the recommended matching network. The shunt inductor (L1) is used to provide maximum swing at the output (short at DC) and also provide reactance to make the real impedance 50Ω looking into the matching network. The remaining negative reactance is canceled by the series inductor (L2). The values used on the demoboard can be used as a reference but may not be suitable if a different layout is implemented. The two shunt capacitors are included to bypass the high frequency RF signal, avoiding direct coupling into V_{CC}. The series AC coupling capacitor is used to maintain the proper bias for the output stage. Their values are big enough to be left out in impedance matching calculation.

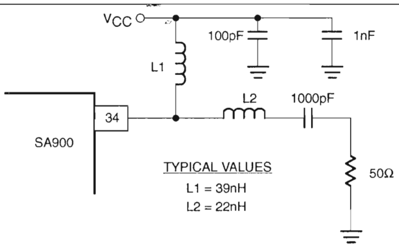
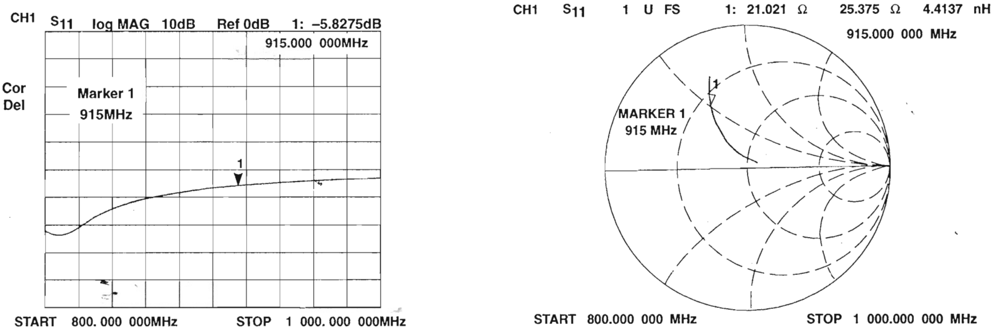
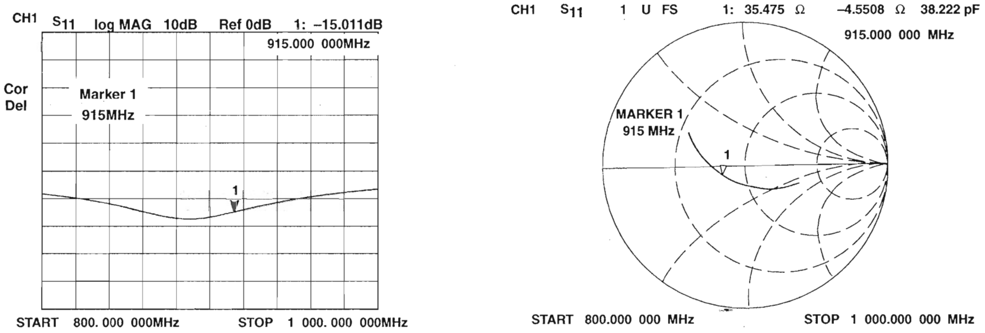


Figure 12. DUALTX Output Matching Network

Using a network analyzer to measure the S characteristic is necessary for obtaining optimum matching which generates maximum output power. Figure 13a-d shows how to match the output impedance to a 50Ω load at 915MHz. First, calibrate the network analyzer to the DUALTX SMA connector on the demoboard. Then, short the point where the series inductor is located and use the DELAY feature of the network analyzer to move the point of reference in the Smith Chart to the leftmost point. Now the network analyzer is calibrated to the beginning of the matching network, not just the SMA connector. The frequency response (Figure 13a) shows that the "dip" is around 830MHz, the frequency where the board was originally matched. The Smith Chart shows that it requires less inductance to bring the marker to the center of the chart (50Ω). By using a 15nH series inductor, the "dip" was moved closer to 915MHz (-15dB) and a better matching is achieved (Figure 13b).



a. S_{11} Response and Smith Chart when L2 = 22nH



b. S_{11} Response and Smith Chart when L2 = 15nH

Figure 13.

On-Chip Clocks

The crystal oscillator is buffered to provide three external clock signals: CLK1, CLK2, and MCLK. Table 1 shows the divide ratio and the controlling mechanism:

Table 4.

CLK1	divide by 3	X (bit 18) = 1
	divide by 1	X (bit 18) = 0
CLK2	divide by 2	Y (bit 19) = 1
	divide by 1	Y (bit 19) = 0
MCLK	divide by 4	CLKSET pin = V_{CC}
	divide by 5	CLKSET pin = $V_{CC}/2$
	divide by 1	CLKSET pin grounded

CLK1 is usually used for the system synthesizer (e.g. SA7025) reference. Since MCLK is active all the time, it is ideal for providing the master clock for the microcontroller. When the device is in STANDBY mode, CLK1 and MCLK provide the clock signals necessary for receiving RF signals. CLK2 can also be used as a clock for digital signal processing (DSP) chip.

Modes of Operation

The SA900 is intended for either AMPS mode (analog cellular) or DUAL mode (digital cellular, IS-54) operation. When the device is running in AMPS mode, the I/Q modulator, variable gain amplifier (VGA) and phase shifter are disabled. The fixed gain amplifier is powered up during AMPS mode operation. However, since the divide ratio is too low (6, 7 or 8), the comparison frequency of the on-board PLL is too high, making it very difficult for the loop bandwidth to be less than 300Hz for analog FM modulation.

The device includes two power saving modes of operation which disable partial circuitry to reduce the power consumption of the overall chip. The SLEEP mode disables all the circuitry except the master clock (MCLK pin) of the SA900. The STANDBY mode shuts down everything except the TXLO buffer, MCLK, and CLK1, which allows the system synthesizer (e.g. SA7025) to continue running. These two power saving modes are common to both AMPS and DUAL mode operation. The SA900 draws 60mA in DUAL mode, reduced to 3mA and 8mA, respectively, in SLEEP and STANDBY modes.

TXEN pin is for hardware powering down the modulator and synthesizer. The falling edge of the signal disables the modulator and synthesizer while the rising edge enables the modulator. To power down the synthesizer using software, send a data word with SE bit set to '0' ('1' for enable). The synthesizer will be disabled right after the strobe signal is transmitted. Either SE or TXEN going low will turn off the synthesizer. This operation is common to both AMPS and DUAL mode.

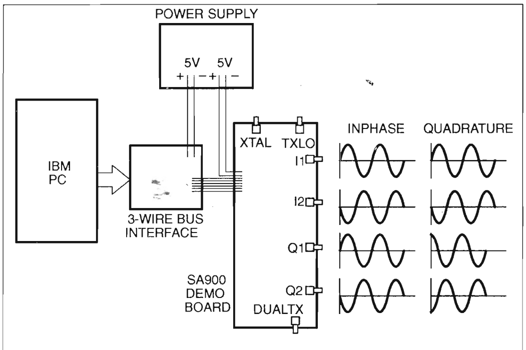


Figure 14. In-phase and Quadrature Modulation Test

PERFORMANCE OF THE SA900

Performance Criteria

Since the I/Q modulator is a universal transmitter, measuring only the frequency stability and modulation index of a generated FM signal would not be useful for other modulation schemes. Measurement parameters should be general enough so that they can represent the performance of modulators when applying different types of modulation and allow fair comparisons among different I/Q modulators. Based on this idea, two measurement techniques, in-phase modulation and quadrature modulation, are used for evaluating I/Q modulators.

The in-phase modulation relies on injecting two equal frequencies and phase signals at f_{mod} into the I and Q inputs. The result of this modulation is two sidebands appearing at f_{mod} offset from the carrier, with the carrier totally suppressed. This is also known as double-sideband (DSB) conversion. The quadrature modulation requires two equal frequencies (but 90° out-of-phase signals) being injected into the I and Q inputs. The result is a single-sideband suppressed carrier (SSB-SC) signal with either the upper or lower sideband at f_{mod} carrier offset being suppressed. This is also known as single-sideband (SSB) up-conversion. Figure 14 summarizes these two tests.

In a practical system, imperfection of an I/Q modulator is directly related to these two measurements. Sideband and carrier suppression from the quadrature modulation test will show the amount of gain imbalance, phase imbalance, and DC offset. On the other hand, intermodulation product suppression from the in-phase modulation test will show the linearity of an I/Q modulator. When making measurements, it is important to have well-balanced I and Q baseband modulating signals for measurement since the signal imperfection will translate into degradation in sideband and carrier suppression.

Performance Graphs

In making those measurements for the demoboard, the following parameters were used:

In-phase modulation:

PIN 43 $I1=400mV_{P-P}$, $DC=V_{CC}/2$ at 200kHz, Phase=0°

PIN 42 $I2=400mV_{P-P}$, $DC=V_{CC}/2$ at 200kHz, Phase=180°

PIN 41 $Q1=400mV_{P-P}$, $DC=V_{CC}/2$ at 200kHz, Phase=0°

PIN 40 $Q2=400mV_{P-P}$, $DC=V_{CC}/2$ at 200kHz, Phase=180°

Quadrature modulation:

PIN 43 $I1=400mV_{P-P}$, $DC=V_{CC}/2$ at 200kHz, Phase=0°

PIN 42 $I2=400mV_{P-P}$, $DC=V_{CC}/2$ at 200kHz, Phase=180°

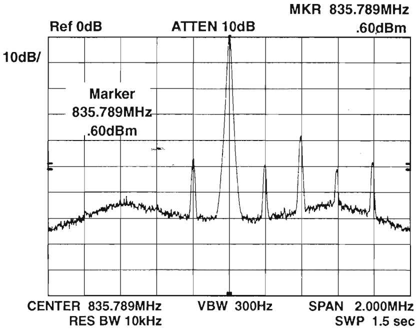
PIN 41 $Q1=400mV_{P-P}$, $DC=V_{CC}/2$ at 200kHz, Phase=90°

PIN 40 $Q2=400mV_{P-P}$, $DC=V_{CC}/2$ at 200kHz, Phase=270°

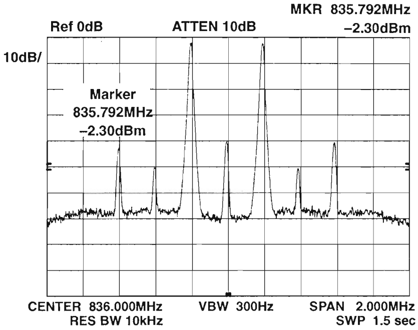
Figures 15a and 15b illustrate what the typical output spectrum would be if in-phase and quadrature modulation were applied to an I/Q modulator. Quadrature modulation will produce lower sideband (LSB) or upper sideband (USB) signal, depending on the phase angle between the I and Q signals. The SA900 was designed to have USB suppressed when the I signal is leading the Q signal. The undesired signals are carrier breakthrough and the harmonic products of the baseband modulating signals sitting at

$f_c \pm nf_{mod}$, where n is an integer ≥2.

Referring to Figure 15a, the output power is 1.3dBm (cable loss = 0.7dB) for the LSB while better than -38dBc of carrier, sideband, and harmonics suppression is measured. The USB better than -26dBc implies the residual AM of the transmit signal is better than 5%, a requirement of the IS-54 specification.



a. Quadrature Test (SSB Up-conversion)



b. In-phase Test (DSB Up-conversion)

Figure 15.

In-phase modulation test will generate both LSB and USB. Beside these two tones, the carrier breakthrough and the harmonics, intermodulation (IM) products will all appear at the output. The odd IM products are dominant, and they satisfy the following rules:

Let $f_1 = f_c - f_{mod}$, $f_2 = f_c + f_{mod}$

3rd order IM:	$2f_1 - f_2 = f_c - 3f_{mod}$,	$2f_2 - f_1 = f_c + 3f_{mod}$
5th order IM:	$3f_1 - 2f_2 = f_c - 5f_{mod}$,	$3f_2 - 2f_1 = f_c + 5f_{mod}$
7th order IM:	$4f_1 - 3f_2 = f_c - 7f_{mod}$,	$4f_2 - 3f_1 = f_c + 7f_{mod}$

Referring to Figure 15b, both LSB and USB are -1.6dBm (cable loss = 0.7dB) in power, which is 3dB less than the measured power for the quadrature modulation test. The IM3 is better than -35dBc. Much higher order IM products are totally suppressed.

Amplitude and phase unbalance

Both amplitude and phase unbalance (error) of an I/Q modulator can be calculated directly from the SSB performance plots. Assume phase error equals ϕ radian and amplitude error equals K, the sideband suppression, X, in dBc can be expressed as follows (see APPENDIX for derivation):

$$\text{SSB suppression, } X(\text{dBc}) = 10\log\left(\frac{K^2 + 2\cdot K\cdot\cos(\phi) + 1}{K^2 - 2\cdot K\cdot\cos(\phi) + 1}\right) \qquad \text{(EQ. 4)}$$

Collecting the like terms and express ϕ in terms of K and X, it becomes:

$$\phi = \cos^{-1}\left(\frac{10^{x/10}\cdot K^2 + 10^{x/10} - 1 - K^2}{2\cdot K + 2\cdot K\cdot 10^{x/10}}\right) \qquad \text{(EQ. 5)}$$

For a given X, there will be a set of ϕ and K that satisfies EQ. 5. We can represent this relationship graphically, as shown in Figure 16. The contours show the phase and amplitude errors for SSB suppression, X, from -44 to -26dBc. When X equals -40dBc, phase error is less than 1.2° with a 0dB amplitude error. By the same token, the amplitude error is less than 0.2dB with a 0° phase error.

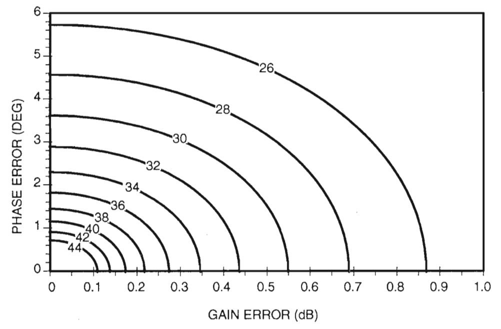
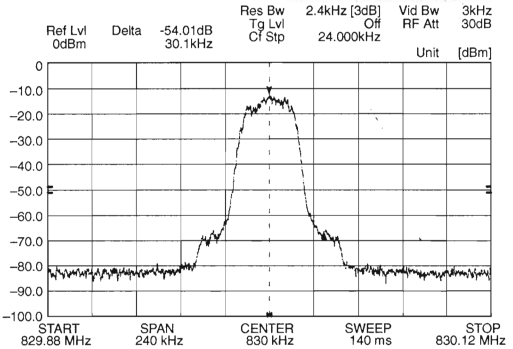


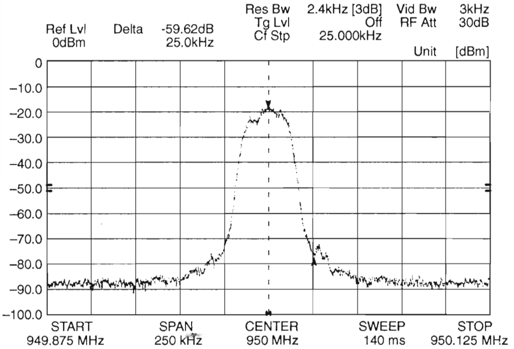
Figure 16. SSB Suppression Contours

Spectral mask

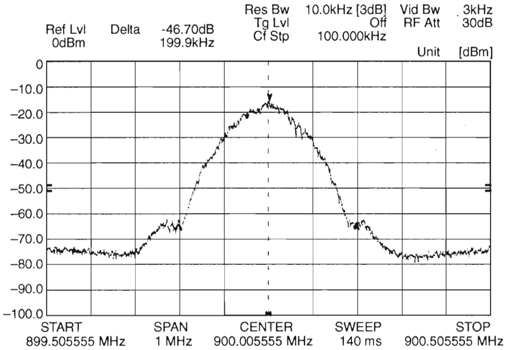
To fully characterize the performance of an I/Q modulator, measurements of the power spectral density of various digital modulation schemes have to be made. Figures 17a and 17b show the measured spectral masks of IS-54 and PDC standards, which designate $\pi/4$-DQPSK as the modulation format.



a. Power Spectrum of ADC Modulation
Bit rate = 48.6 kb/s; $\alpha = 0.35$



b. Power Spectrum of PDC Modulation
Bit rate = 42 kb/s; $\alpha = 0.5$



c. Power Spectrum of GSM Modulation
Bit rate = 270.833 kb/s; $BT_b = 0.3$

Figure 17.

GMSK is a digital modulation scheme widely used for wireless and mobile communications. Figure 17c shows the spectral mask of the modulation format required by GSM, the digital cellular standard in Europe. At 200kHz and 300kHz carrier offset, the power of the signal is suppressed by 46dB and 58dB, respectively, which is well within the GSM specification.

Power ON time

The power ON time for the SA900 is mainly determined by the loop bandwidth of the on-board PLL frequency synthesizer. It can be measured by using the HP 53310A Modulation Domain Analyzer set to the EXTERNAL TRIGGERED mode. The STROBE signal from 3-wire bus is used to trigger the equipment. Figure 18 shows that the part can be powered up and locked in about 62µs.

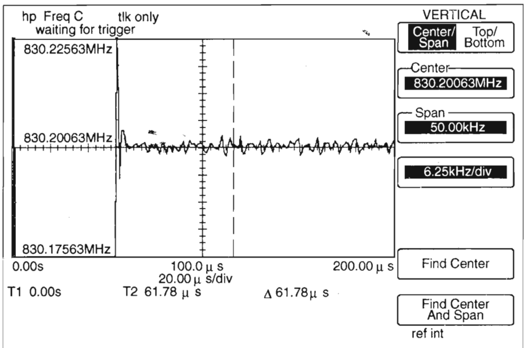


Figure 18. Power ON Time Measurement

ISM band application

The FCC has recently assigned three bands for ISM type of application. The one below 1GHz is from 902 to 928MHz. This band becomes very attractive because users are allowed, without having a license, to transmit up to 1 Watt of power when frequency hopping or direct sequence CDMA is used. The wide bandwidth nature of the SA900 fits well into this application. Figures 19a and 19b are the output spectrum of the SA900 showing how well the image reject mixer works. A common IF (45MHz) was chosen to be the offset frequency, and then injected externally into the VCO pins. The closest images are sitting at 45MHz apart and are better than -36dBc.

COMPONENTS FUNCTION

C241, C242, C243, C245, C246 - Supply bypassing capacitors

C247 - provides AC ground for TXLO2 pin

C249 - AC couples an external signal into TXLO1 pin

C253, C254, C255 - part of the LC tank circuit

C263 - AC couples an external signal into XTAL1 pin

C267, C269 - part of the PLL low-pass filter

C281, C287, C288 - AC coupling capacitors for the clocks

C301 - AC coupling capacitor for the DUALTX pin

C305, C306 - Bypass RF signal coming from DUALTX pin

C312, C313, C314 - AC coupling capacitors

C370, C371 - AC couples an external signal into TANK1 and TANK2 pins when on-board PLL is not used

L252 - part of the LC tank circuit

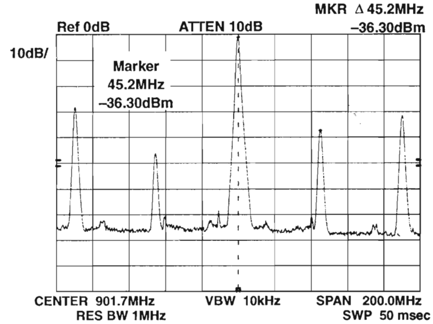
L304, L372 - matching network for the DUALTX output

R260 - termination resistor

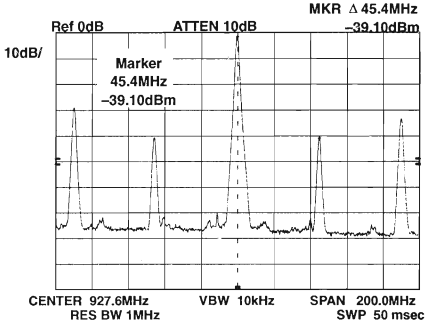
R262 - current setting resistor for the charge pump

R264, R266 - part of the PLL low-pass filter

R274 - jumper



a. TXLO = 947MHz, VCO = 45MHz



b. TXLO = 973MHz, VCO = 45MHz

Figure 19. Output Spectrum of the SA900 in the ISM Band

R349, R350 - make up a voltage divider for selecting divide ratio of the MCLK

R352 - termination resistor

R333, 358 - isolation resistors between the LC tank and the PLL low-pass filter

FREQUENTLY ASKED QUESTIONS

Q. What is the bandwidth of the phase shifter for generating I/Q carriers?

A. The bandwidth is between 820 and 920MHz. The part is still functional below 820MHz and above 920MHz, but the carrier and sideband suppression are not guaranteed. In addition, the DUALTX output matching network needs to be optimized for a different frequency.

Q. Can I frequency modulate (FM) the on-board VCO to generate RF signal for AMPS system?

A. Since the divide ratio for the VCO is too low, it is very difficult to obtain the required loop bandwidth (<300Hz) to do AMPS modulation.

Q. What signals constitute the spurious output referred to under the DUALTX function of the AC electrical characteristics in the data sheet?

A. Those spurs could be N*TXLO, N*VCO, TXLO+VCO, N*XO, and TXLO ±N*VCO.

Q. Can external circuitry be added or modified to reduce the broadband noise floor below -136dBm/Hz?

SA900 I/Q transmit modulator for 1GHz applications

A. Customers can put a bandpass SAW filter at the output of the TXLO to improve the broadband noise floor.

Q. Can the SA900 generate BPSK signal?
A. Yes, it can. Feed the baseband signal into I1 and I2 and leave Q1 and Q2 open or tie them to $V_{CC}/2$.

Q. What is the response of the image rejection filter?
A. It is actually a SSB mixer; not an image rejection filter.

Q. What happens if the VCO is not used?
A. There will not be any signal at the DUALTX and AMPS output if the VCO is not used.

REFERENCES:

"Implementation of a 900 MHz Transmitter System Using Highly Integrated ASIC", Wing S. Djen and Prasanna M. Shah, Proceedings of the 44th IEEE Vehicular Technology Conference, June 1994, pp. 1341-1345.

"Digital and Analog Communications Systems," Leon W. Couch II, Macmillan, 1990.

"Cellular System Dual-Mode Mobile Station-Base Station Compatibility Standard", IS-54-B, EIA/TIA, April 1992.

"Physical Layer on the Radio-Path", GSM Standard, July 1988.

"π/4-QPSK MODEMS for Satellite Sound/Data Broadcast Systems", Chia-Liang Liu and Kamilo Feher, IEEE Transactions on Broadcasting, March 1991, pp. 1-8.

"PCD5070 GSM Baseband Interface", Preliminary specification, Philips Semiconductors, September, 1992.

APPENDIX

Assume an imperfect I/Q modulator with gain error, K, and phase error, ϕ, modulated by quadrature I/Q signals (SSB up-conversion) wm. Then the signal, s(t), at the output of the I/Q modulator becomes,

$$s(t) = K\cos(\omega_c t + \phi)\cos(\omega_m t) - \sin(\omega_c t)\cos(\omega_m t + 90^\circ) \quad \text{(EQ. A.1)}$$

Using trigonometric identity and let $\omega c - \omega_m = A$ and $\omega_c + \omega_m = B$, we obtain,

$$s(t) = \frac{K}{2}\cos[At + \phi] + \frac{K}{2}\cos[Bt + \phi] + \frac{1}{2}\cos[At] - \frac{1}{2}\cos[Bt] \quad \text{(EQ. A.2)}$$

Assume the information is in LSB, i.e. A, and the spur is the USB, i.e., B, we have,

$$\text{Signal} = \frac{K}{2}\cos A\cos\phi + \frac{1}{2}\cos A - \frac{K}{2}\sin A\sin\phi \quad \text{(EQ. A.3)}$$

$$\text{Noise} = \frac{K}{2}\cos B\cos\phi + \frac{1}{2}\cos B - \frac{K}{2}\sin B\sin\phi \quad \text{(EQ. A.4)}$$

To find the power, we have to evaluate the envelope (amplitude) of these two signals. Recall that for any given bandpass signal in rectangular form,

Bandpass signal = $X\cos\omega t - Y\sin\omega t$,

the envelope is

Envelope = $(X^2 + Y^2)^{0.5}$

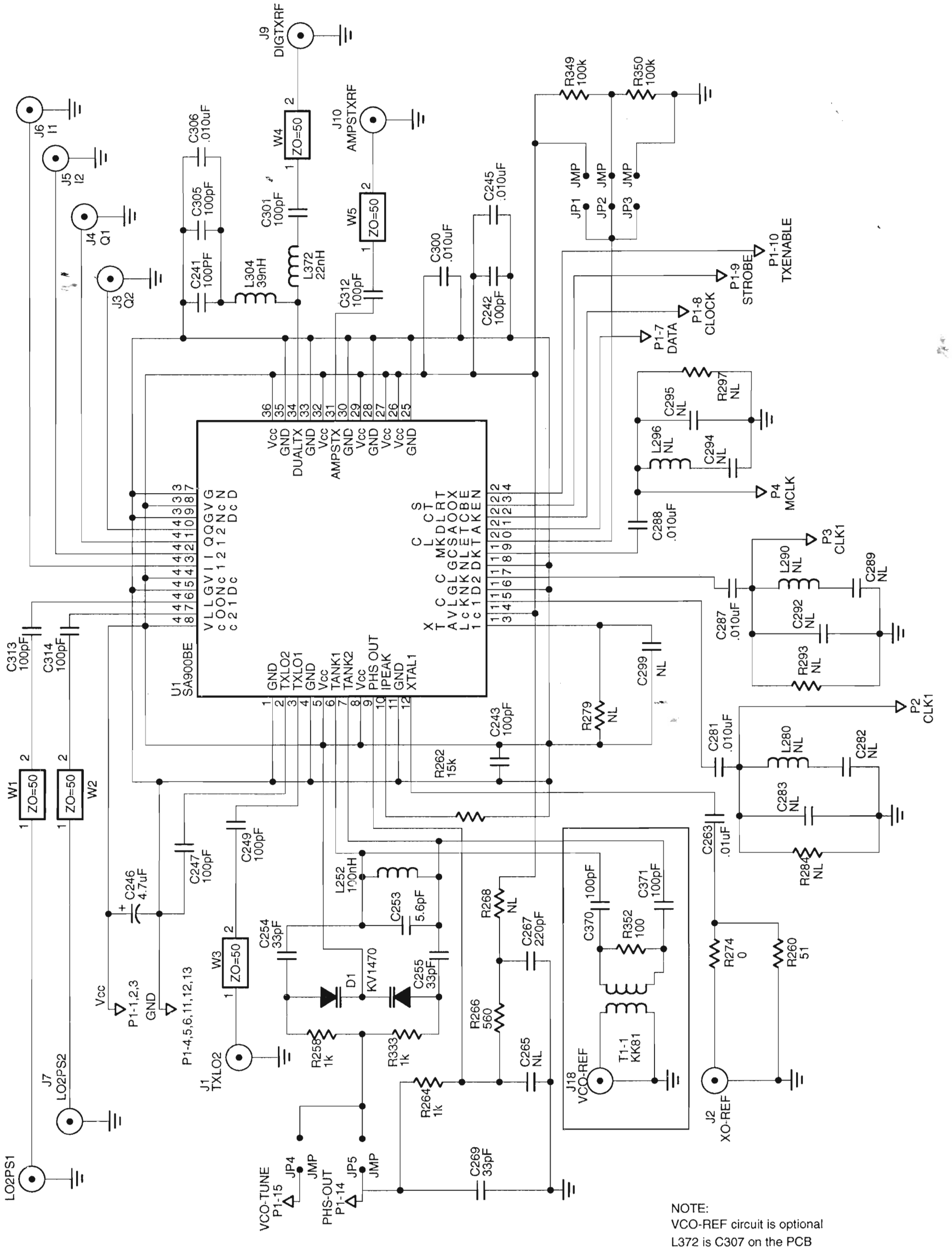
Therefore, from EQ. A.3 and A.4,

$$\text{Signal} = \left[\left(\frac{K}{2}\cos\phi + \frac{1}{2}\right)^2 + \left(\frac{K}{2}\sin\phi\right)^2\right]^{0.5} \quad \text{(EQ. A.5)}$$

$$\text{Noise} = \left[\left(\frac{K}{2}\cos\phi - \frac{1}{2}\right)^2 + \left(\frac{K}{2}\sin\phi\right)^2\right]^{0.5} \quad \text{(EQ. A.6)}$$

Finally, the S/N ratio can be found by taking 20 log the ratio of EQ. A.5 and A.6.

$$\frac{S}{N} = 10\log\left(\frac{K^2 + 2K\cos\phi + 1}{K^2 - 2K\cos\phi + 1}\right)$$



NOTE:
VCO-REF circuit is optional
L372 is C307 on the PCB
C246 combines C240 and C244 on the PCB

Figure 20. SA900 Demoboard

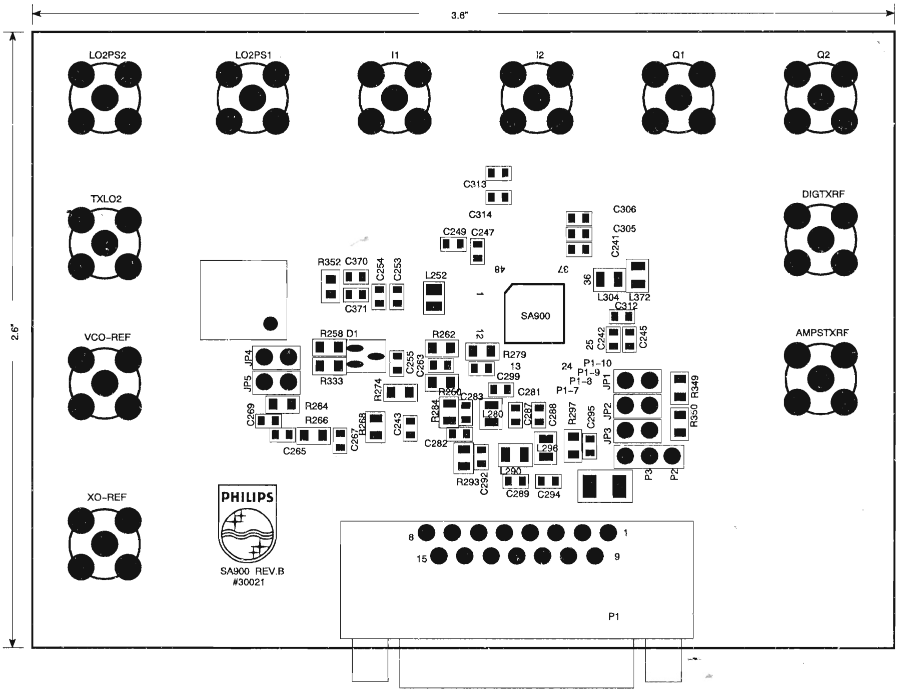


Figure 21. SA900 Board Layout

Table 5. Customer Application Component List for SA900BE

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	5.6pF	50V	C253	Cap. cer. 0603 NPO ±0.25pF	Garrett	Rohm	MCH185A5R6CK
3	33pF	50V	C254, C255, C269	Cap. cer. 0603 NPO ±5%	Garrett	Rohm	MCH185A330JK
13	100pF	50V	C241, C242, C243, C247, C249, C300, C301, C305, C312, C313, C314, C370, C371	Cap. cer. 0603 NPO ±5%	Garrett	Rohm	MCH185A101JK
1	1000pF	50V	C301	Cap. cer. 0603 X7R ±10%	Garrett	Rohm	MCH185C102KK
1	2200pF	50V	C267	Cap. cer. 0603 X7R ±10%	Garrett	Rohm	MCH185C222KK
6	0.01µF	25V	C245, C263, C281, C287, C288, C306	Cap. cer. 0603 X7R ±10%	Garrett	Philips	MCH182C103KK
1	4.7µF	10V	C246	Tant. chip cap. B 3528 ±10%	Garrett	Philips	49MC475B010KOAS
8	NL		C265, C282, C283, C289, C292, C294, C295, C299				
Surface Mount Resistors							
1	0Ω		R274	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW000E
1	51Ω		R260	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW510E
1	100Ω		R352	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW101E
1	560Ω		R266	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW561E
1	1KΩ		R258, R264, R333	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW102E
1	15KΩ		R262	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW153E
2	100KΩ		R349, R350	Res. chip 0603 1/16W ±5%	Garrett	Rohm	MCR03JW104E
Surface Mount Diodes							
1			D1	SMD Diode (Varactor)	Digikey	TOKO	KV1470TR00
Surface Mount Inductors							
1	0.022µH		L372	Inductor SM Mold/WW A	Garrett	J.W. Miller	PM20-R022M
1	0.039µH		L304	Inductor SM Mold/WW A	Garrett	J.W. Miller	PM20-R039M
1	0.10µH		L252	Inductor SM Mold/WW A	Garrett	J.W. Miller	PM20-R10M
Surface Mount Integrated Circuits							
1			U1	I/Q Transmit modulator	Philips	Philips	SA900BE
Miscellaneous							
1			K353	RF Transformer	Mini-Circuits	Mini-Circuits	T1-1 KK81
11			J1, J2, J3, J4, J5, J6, J7, J8 ,J9, J10, J18	SMA Right Angle Jack Receptacle	Newark	EF Johnson	142-0701-301
5			JP1, JP2, JP3, JP4, JP5	straight, dual row	Newark	IPI	929836-01-36-ND
1			P1	15 pins receptacle D-sub. conn.	Newark	Dupont	51F2456
1				Printed circuit board	Philips	Philips	SA900-30021
66 Total Parts							

Section 7
Baseband Processors: Audio and Data

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Baseband Processor Selector Guide

Baseband Processors

PART TYPE		APPLICATION	V_{DD}	I_{DD}	PACKAGE
PCD5032	ADPCM Codec	DECT	2.7 - 6.0 2.7 - 6.0	7mA Typ. Active 20µA Typ. Stdby	28-Pin SO28 44-Pin QFP
PCD5040	BMC (Burst Mode Controller)	DECT	2.7 - 6.0	15mA Typ. Active	64-Pin QFP
PCD5081	Signal Processor – Mobile	GSM	5.0	——	80-Pin QFP
PCD5082	Signal Processor – Base	GSM	5.0	——	160-Pin QFP
PCD5071	Baseband Interface	GSM	5.0	31mA Typ. Rx 7mA Typ. Tx	44-Pin QFP 44-Pin QFP
NE/SA5750	Audio Companding Amplifier	AMPS TACS	5.0	8.4mA Typ. 1.8mA Stdby	24-Pin DIP 28-Pin SOL
NE/SA5751	Audio Filter and Control	AMPS TACS	5.0	2.7mA Typ. 0.9mA Stdby	24-Pin DIP 28-Pin SOL
SA5752	Audio Companding VOX and Amplifier	AMPS TACS	2.7	3.1mA Typ. 125µA Stdby	20-Pin SOL 20-Pin SSOP
SA5753	Audio Filter and Control	AMPS TACS	2.7	2.7mA Typ. 600µA Stdby	20-Pin SOL 20-Pin SSOP
PCF5001	POCSAG decoder	PAGERS	1.5 - 6.0	60µA Typ.	28-Pin Mini-Pack 32-Pin QFP
PCD5003	Advanced POCSAG paging decoder	GSM	1.5 - 6.0	50µA Typ. (ON) 25µA Typ. (OFF)	32-Pin TQFP
UMA1000LT	Data processor for cellular radio	AMPS TACS	3.0 - 5.5	2.5µA Typ.	28-Pin SOL

Audio processor - companding and amplifier section NE/SA5750

DESCRIPTION

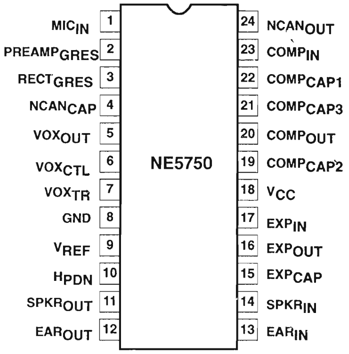
The NE/SA5750 is a high performance low power audio signal processing system. The NE/SA5750 subsystems include a low noise microphone preamplifier with adustable gain, a noise cancellation switching amplifier with adjustable threshold, a voice operated transmitter (VOX) switch, VOX control, an audio compressor with buffered input, audio expandor, a unity gain power amplifier to drive a speaker, a summing power amplifier for sidetone attenuation and headphone (earpiece) drive, and an internal bandgap voltage regulator with power down capability. When used with Philips Semiconductors NE/SA5751, the complete audio processing function of an AMPS or TACS cellular telephone is easily implemented. The NE/SA5750 can also be used without the NE/SA5751 in a wide variety of radio communications applications.

FEATURES

- High performance
- 5V supply
- Adjustable VOX and noise cancellation threshold
- Adjustable gain preamplifier
- Audio companding
- ESD protected
- Open collector VOX output
- Logic inputs CMOS compatible
- Power down mode
- Built-in drivers for speaker and earpiece
- Few external components
- SOL and DIP packages

PIN CONFIGURATION

D^1 and N PACKAGE



NOTE:
1. Available only in SOL (large SO) package.

BENEFITS

- Very compact applications
- Long battery life in portable equipment
- Complete cellular audio function with the SA5751

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5750N	0411B
24-Pin Plastic Small Outline Large (SOL) package	0 to +70°C	NE5750D	0173D
24-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5750N	0411B
24-Pin Plastic Small Outline Large (SOL) package	-40 to +85°C	SA5750D	0173D

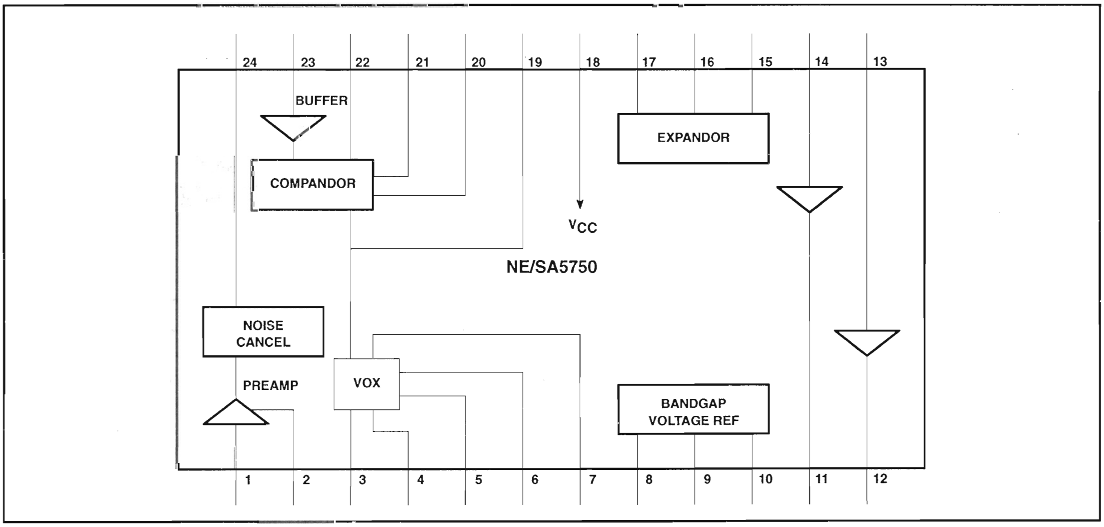
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage Voltage applied to any pin	6 -0.3 to (V_{CC} + 0.3)	V V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Ambient operating temperature NE5750 SA5750	 0 to 70 -40 to +85	°C

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	MIC_{IN}	Microphone input
2	$PREAMP_{GRES}$	Preamplifier gain resistor
3	$RECT_{GRES}$	Reactifier gain resistor
4	$NCAN_{CAP}$	Noise cancellation timing capacitor
5	VOX_{OUT}	Voice operated transmission output
6	VOX_{CTL}	Voice operated transmission control
7	VOX_{TR}	Voice operated transmission threshold resistor
8	GND	Ground
9	V_{REF}	Reference voltage
10	H_{PDN}	Hardware power down
11	$SPKR_{OUT}$	Speaker output
12	EAR_{OUT}	Earpiece output
13	EAR_{IN}	Earpiece input, side tone input
14	$SPKR_{IN}$	Speaker input
15	EXP_{CAp}	Expandor timing capacitor
16	EXP_{OUT}	Expandor output
17	EXP_{IN}	Expandor input
18	V_{CC}	Positive supply
19	$COMP_{CAP2}$	Compressor timing capacitor 2
20	$COMP_{OUT}$	Compressor output
21	$COMP_{CAP3}$	Compressor timing capacitor 3
22	$COMP_{CAP1}$	Compressor timing capacitor 1
23	$COMP_{IN}$	Compressor input
24	$NCAN_{OUT}$	Noise cancellation output

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

$T_A = 25^oC$, $V_{CC} = +5.0V$, 0dB = 77.5mV$_{RMS}$. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4.75	5.0	5.25	V
I_{CC}	Supply current	No signal Power down mode		8.4 1.8	12.0 3.0	mA mA
Z_L	Load impedance pins NCAN$_{OUT}$, EXP$_{OUT}$		50			kΩ
	COMP$_{OUT}$[1]		10			kΩ
Z_{IN}	Input impedance COMP$_{IN}$, MIC$_{IN}$, SPKR$_{IN}$		40	50	60	kΩ
	EXP$_{IN}$[2]		2.0	2.5		kΩ
	Noise cancellation current[4]	Pin 7, grounded	40	50	60	µA
V_{OS}	DC offset NCAN$_{OUT}$[3]		-50		50	mV

NOTES:
1. Compressor is tested in production with 50kΩ load.
2. Not tested in production.
3. Offset values are identical for both gain states of noise reduction circuit.
4. VOX threshold resistor at Pin 7, R3, should be greater than 3kΩ.

AC ELECTRICAL CHARACTERISTICS

$T_A = 25^oC$, $V_{CC} = +5.0V$, 0dB level = 77.5mV$_{RMS}$. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	Preamplifier gain range Preamplifier voltage gain 0dB Preamplifier voltage gain 40dB	 Pin 2 open Pin 2 AC ground	0 -1.0 39.0	 0 40	40 1.0 41.0	dB dB dB
	Preamplifier noise density	Pin 2 AC grounded RS = 0 - 50kΩ unweighted 20Hz-20kHz		7		$nV/\sqrt{Hz}$
		weighted CCIR DIN45405 20-20kHz		8		
	Switch amplifier gain		9	10	11	dB
	Sidetone attenuation range				30	dB
Compandor 1kHz, all tests[1]						
COMP$_{OUT}$	Compressor error at -21dB output level	Input level = -42dB		0.38		dB
COMP$_{OUT}$	Compressor error at -10dB output level	Input level = -20dB	-1.0		1.0	dB
COMP$_{OUT}$	Compressor error at 0dB output level	Input level = 0dB	-1.5	0.12	1.5	dB
COMP$_{OUT}$	Compressor error at +5dB output level	Input level = +10dB	-1.0		1.0	dB
COMP$_{OUT}$	Compressor error at +12.3dB output level	Input level = +24.6dB	-1.0		1.0	dB
EXP$_{OUT}$	Expandor error at -42dB output level	Input level = -21dB		-0.41		dB
EXP$_{OUT}$	Expandor error at -21dB output level	Input level = -10.5dB	-1.0		1.0	dB
EXP$_{OUT}$	Expandor error at -10dB output level	Input level = -5dB	-1.0		1.0	dB
EXP$_{OUT}$	Expandor error at 0dB output level	Input level = 0dB	-1.5	-0.18	1.5	dB
EXP$_{OUT}$	Expandor error at +10dB output level	Input level = +5dB	-1.0		1.0	dB
EXP$_{OUT}$	Expandor error at +24.6dB output level[2]	Input level = +12.3dB	-1.5		1.5	dB
EXP$_{OUT}$	Expandor V_{OS}	No signal	-50.0		50.0	mV
EXP$_{OUT}$	Expandor output DC shift	No signal to 0dB	-100		100	mV

AC ELECTRICAL CHARACTERISTICS

$T_A = 25^oC$, $V_{CC} = +5.0V$, 0dB level = $77.5mV_{RMS}$. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	Timing capacitors compandor			2.2		µF
THD	Total harmonic distortion					%
	Compressor	1kHz, 0dB		0.09	1	
	Expandor	1kHz, 0dB		0.09	1	
	$NCAN_{OUT}$	1kHz. Pin 2 open output level = 0dB		0.18	1	
		1kHz, Pin 2 open output level = +25dB		0.13	1	
	Speaker amplifier Drive capability				40	mA_{P-P}
	Output swing (<1% THD)	50Ω load	2	3.2		V_{P-P}
		100Ω load	3	4.1		V_{P-P}
		No load	4	4.9		V_{P-P}
	Ear amplifier Drive capability				10	mA_{P-P}
	Output swing (<1% THD)	300Ω load	3	4.3		V_{P-P}
		2000Ω load	4	4.9		V_{P-P}
		No load	4	4.9		V_{P-P}
VOX_{OUT}	Sink current				0.5	mA
	Low level	Open collector I_L = 0.5mA		0.07	0.4	V
	High level		4	5		V
VOX_{CTL}	Input current Low		-50	-21	0	µA
	High		-10		+10	µA
	Input level Low		0		1.5	V
	High		3.5		5	V
H_{PDN}	Input current Low		-10		+10	µA
	High		-10		+10	µA
	Input level Low		0		1.5	V
	High		3.5		5	V
	Reference filter capacitor			10		µF

NOTE:

1. Measurements are relative to 0dB output.
2. Measurement is absolute and indicative of the output dynamic range capability.

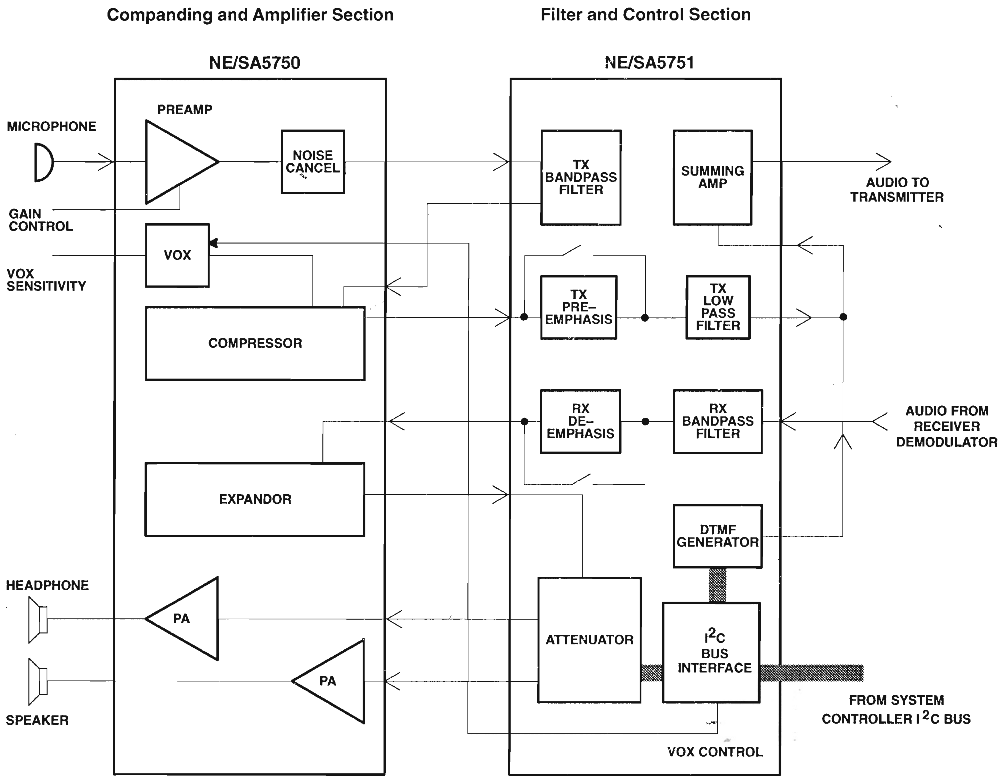


Figure 1. Typical Configuration of Audio Processor (APROC) System Chip Set

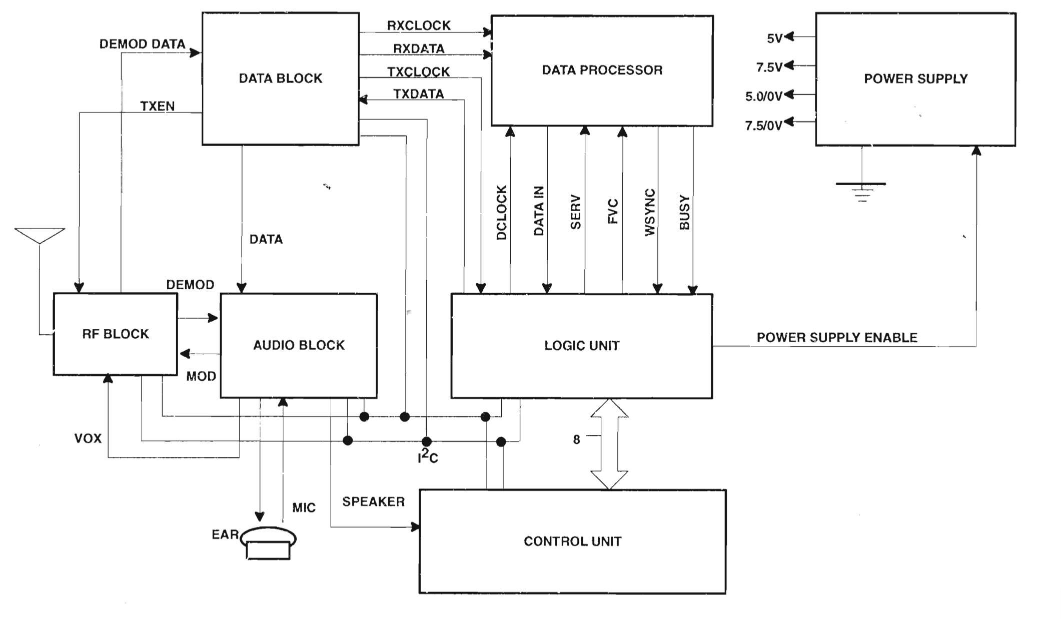


Figure 2. Cellular Radio System

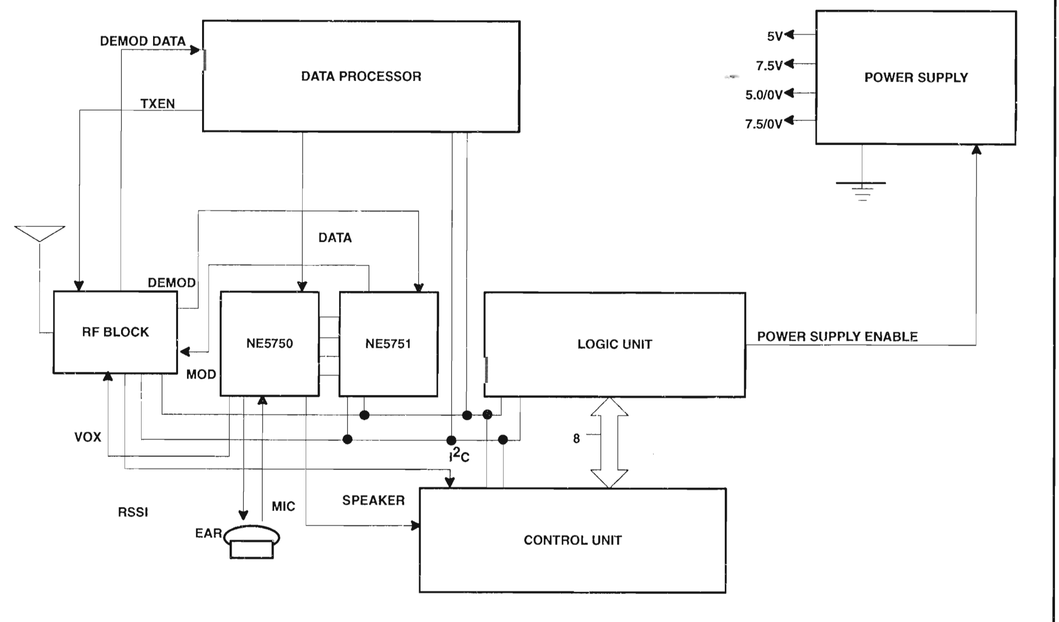


Figure 3. APROC Application Diagram

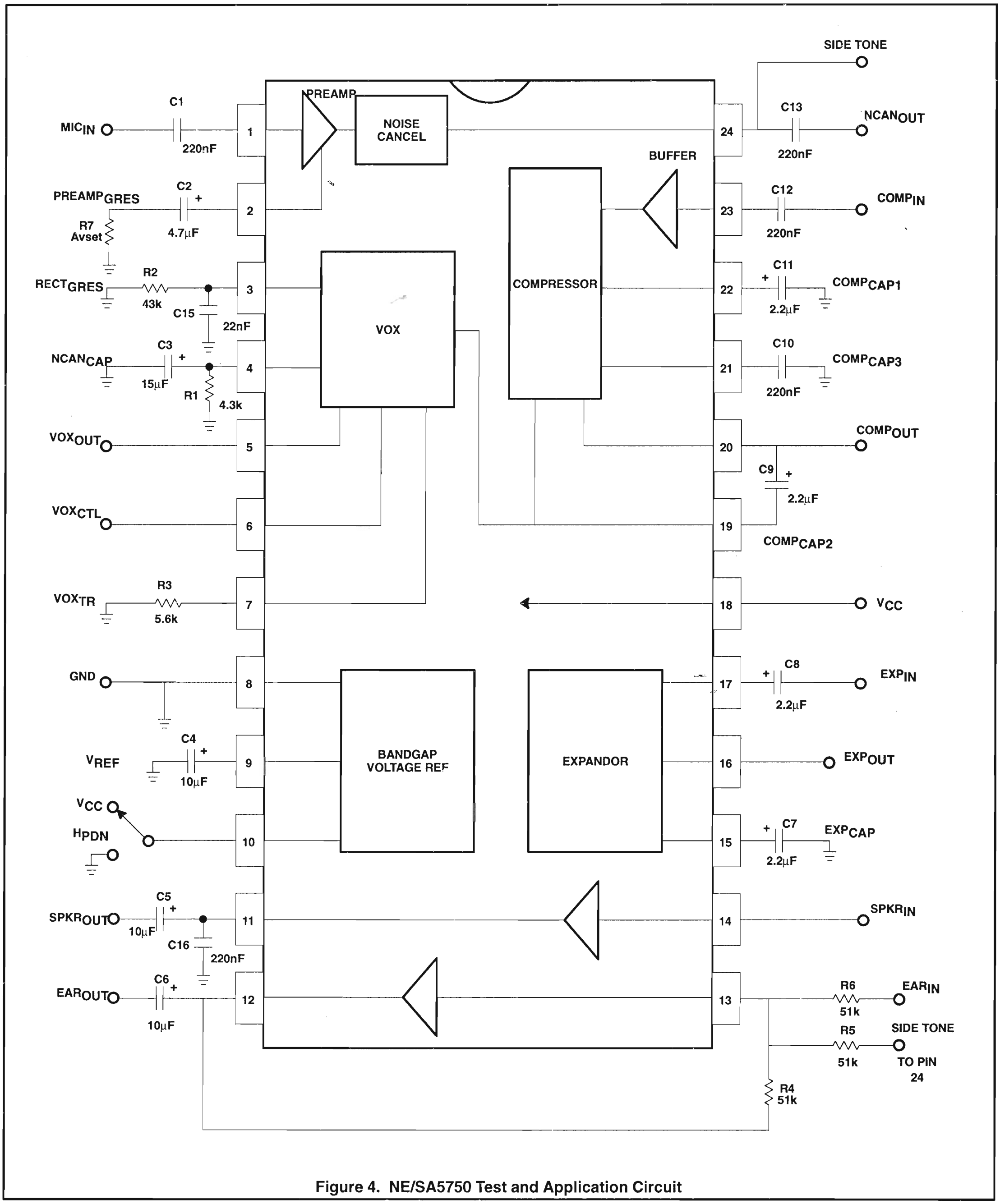


Figure 4. NE/SA5750 Test and Application Circuit

Audio processor - filter and control section NE/SA5751

DESCRIPTION

The NE/SA5751 is a high performance low power CMOS audio signal processing system. The NE/SA5751 subsystems include complementary transmit/receive voice band (300-3000Hz), switched capacitor bandpass filters with pre-emphasis and de-emphasis respectively, a transmit low pass filter, peak deviation limiter for transmit, a digitally controlled volume control with 30dB range (in 2dB steps), audio path mute switches, a programmable DTMF generator, power- down circuitry for low current standby, power-on reset capability, and an I^{2}C interface. When the SA5751 is used with an SA5750 (companding function), the complete audio processing system of an AMPs or TACs cellular telephone is easily implemented.

FEATURES

- Low power
- High performance
- 5V supply
- Built-in programmable DTMF generator
- Built-in digitally controlled volume control
- Built-in peak-deviation limit
- I^{2}C Bus controlled
- Power-on reset
- Power-down capability

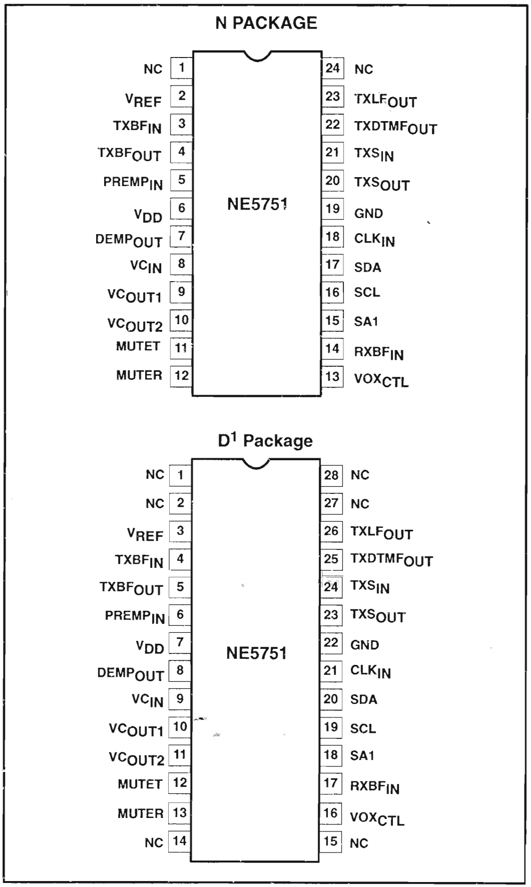
BENEFITS

- Very compact application
- Long battery life in portable equipment
- Complete cellular audio function with the SA5750

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

PIN CONFIGURATION



NOTE:
1. Available in SOL (large surface mount) package only.

ORDERING INFORMATION

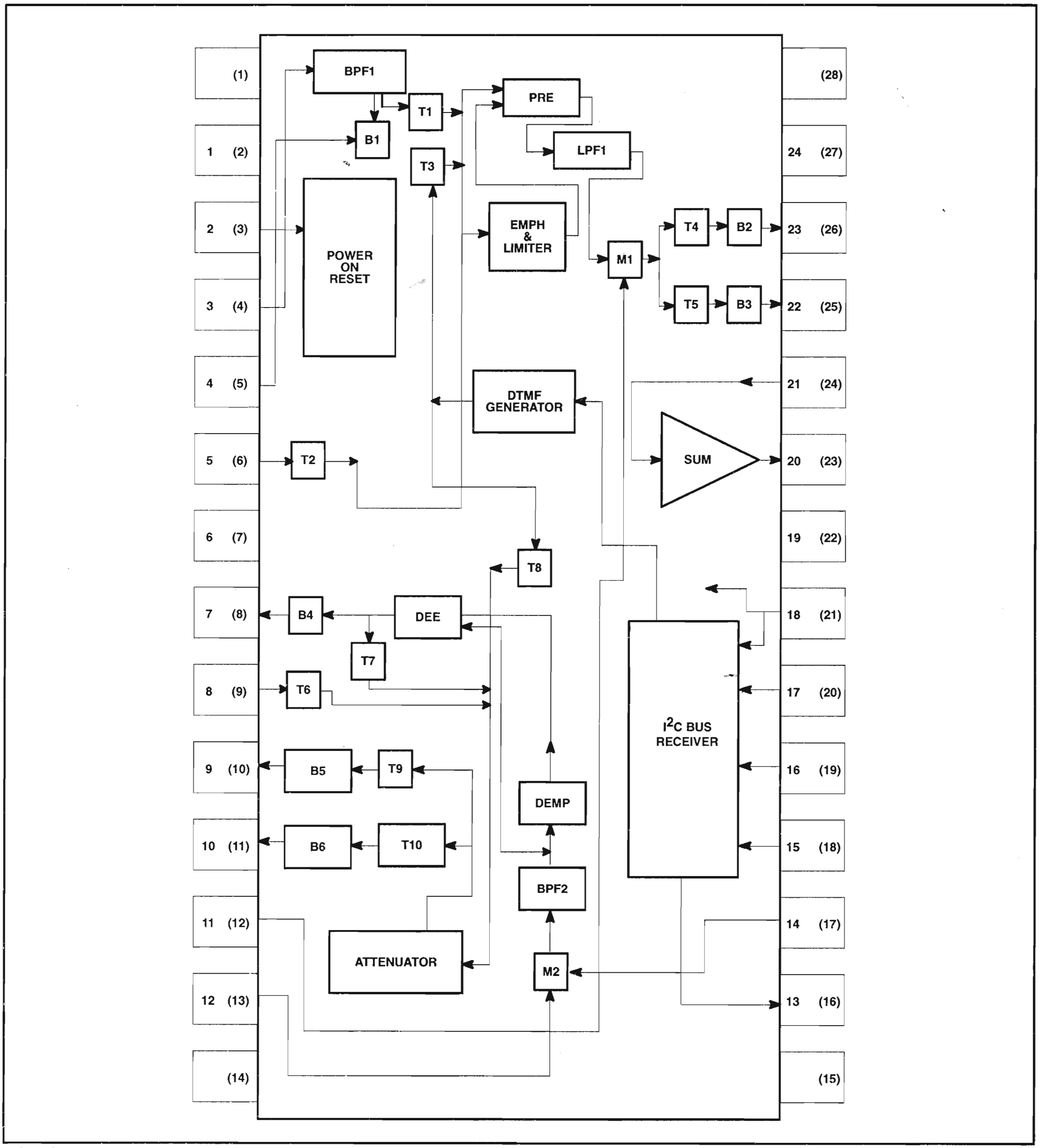
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5751N	0411B
28-Pin Plastic Small Outline Large (SOL) package	0 to +70°C	NE5751D	0006C
24-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5751N	0411B
28-Pin Plastic Small Outline Large (SOL) package	-40 to +85°C	SA5751D	0006C

PIN DESCRIPTIONS

PIN NO.		SYMBOL	DESCRIPTION
	(1)	NC	Not connected
1	(2)	NC	Not connected
2	(3)	V_{REF}	Reference voltage
3	(4)	$TXBF_{IN}$	Transmit bandpass filter input
4	(5)	$TXBF_{OUT}$	Transmit bandpass filter output
5	(6)	$PREMP_{IN}$	Pre-emphasis input
6	(7)	V_{DD}	Positive supply
7	(8)	$DEMP_{OUT}$	De-emphasis output
8	(9)	VC_{IN}	Volume control input
9	(10)	VC_{OUT1}	Volume control output 1
10	(11)	VC_{OUT2}	Volume control output 2
11	(12)	MUTET	TX analog voice path mute input
12	(13)	MUTER	RX analog voice path mute input
	(14)	NC	Not connected
	(15)	NC	Not connected
13	(16)	VOX_{CTL}	Vox control output
14	(17)	$RXBF_{IN}$	Receive bandpass filter input
15	(18)	SA1	Serial bus address
16	(19)	SCL	Serial clock line
17	(20)	SDA	Serial data line
18	(21)	CLK_{IN}	Clock input
19	(22)	GND	Ground
20	(23)	TXS_{OUT}	Transmit summer output
21	(24)	TXS_{IN}	Transmit summer input
22	(25)	$TXDTMF_{OUT}$	Transmit DTMF output
23	(26)	$TXLF_{OUT}$	Transmit low-pass filter output
24	(27)	NC	Not connected
	(28)	NC	Not connected

NOTE:
1. Callouts are for N package; those in parentheses are for the D (SOL) package.

BLOCK DIAGRAM



NOTES:

1. T1 to T10 represent the signal path switches.
2. M1 and M2 represent the mute switches.
3. PRE and DEE represent the bypass switches for pre-emphasis and de-emphasis, respectively.
4. B1 to B6 represent the output buffers.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Power supply voltage[1]	6	V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Ambient operating temperature NE5751	0 to 70	°C
	SA5751	-40 to +85	°C

NOTE:

1. Voltage applied to any pin -0.3 to V_{DD} +0.3V

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +5.0V, unless otherwise specified. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{DD}	Power supply voltage range		4.75	5.0	5.25	V
I_{DD}	Supply current	Operating Standby		2.7 0.9	5.0 2.0	mA mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +5.0V. See test circuit, Figure 4. Clock frequency = 1.2MHz; test level = 0dBV = 77.5mV$_{RMS}$ = -20dBm, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	RX BPF anti alias rejection			40		dB
	RX BPF input impedance	f= 1kHz		500		kΩ
	RX BPF gain with de-emphasis	f = 1kHz	-0.5	0	0.5	dB
	RX BPF gain with de-emphasis	f = 100Hz		-31	-29	dBm0
	RX BPF gain with de-emphasis	f = 300Hz	9.0	9.6	11.0	dBm0
	RX BPF gain with de-emphasis	f = 3kHz	-11.0	-10.0	-9.0	dBm0
	RX BPF gain with de-emphasis	f = 5.9kHz		-68	-50	dBm0
	RX BPF noise with de-emphasis	300Hz-3kHz		170		μV$_{RMS}$
	RX dynamic range	with deemphasis		80		dB
	DEMP$_{OUT}$ output impedance	f = 1kHz		40		Ω
	DEMP$_{OUT}$ output swing (1%)	2.3kΩ to V_{REF}; f = 1kHz	V_{DD} -3	3.5		V_{P-P}
	VC$_{OUT1}$ ouput swing (1%)	50kΩ toV_{REF}; f = 1kHz	V_{DD} -1	4.5		V_{P-P}
	VC$_{OUT2}$ output swing (1%)	50kΩ to V_{REF}; f = 1kHz	V_{DD} -1	4.5		V_{P-P}
	VC$_{OUT1}$ noise	VC$_{IN}$ grounded C - message		25		μV$_{RMS}$
	VC$_{OUT2}$ noise	VC$_{IN}$ grounded C - message		25		μV$_{RMS}$
	Mute threshold off		0		0.8	V
	Mute threshold on		2.0		5.0	V
	CLK1, 2 high		4.0		5.0	V
	CLK1, 2 low		0		1.0	V
	TX BPF anti alias rejection			40		dB
	TX BPF input impedance	f = 3kHz		500		KΩ

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	TX BPF noise	300 - 3000kHz		90		μV_{RMS}
	TX LPF gain	f = 5.9kHz		-39	-36	dB
	TX LPF gain with pre-emphasis	f = 1kHz, 20dBV		12.06		dB
	TX LPF gain with pre-emphasis	f = 100Hz		-19		dBm0
	TX LPF gain with pre-emphasis	f = 300Hz		-10.45		dBm0
	TX LPF gain with pre-emphasis	f = 3kHz		9.14		dBm0
	TX LPF gain with pre-emphasis	f = 5900Hz		-39		dBm0
	TX LPF gain with pre-emphasis	f = 9kHz		-51		dBm0
	TX overall gain	1kHz	11.3	11.8	12.5	dB
	TX overall gain	100Hz		-47	-45	dBm0
	TX overall gain	300Hz	-11	-10.4	-9	dBm0
	TX overall gain	3kHz	8	9	9.6	dBm0
	TX overall gain	5.9kHz		-52	-45	dBm0
	TX BPF output impedance	f = 1kHz		360		Ω
	TX BPF output swing (1%THD)	50kΩ to V_{REF} f = 1kHz		4.5		V_{P-P}
	TX BPF dynamic range			90		dB
	$PREMP_{IN}$ input impedance	f = 3kHz		500		kΩ
	Summing op amp					
	Slew rate	C_L = 15pF		0.75		V/µs
	Output impedance	Unity gain; f = 3kHz		40		Ω
	Output swing (1% THD)	1kHz, 5kΩ load (25°C)		4.3		V_{P-P}
	Volume control accuracy	-30dB to 0dB	-1	0	+1	dB
	Analog switches					
	Insertion loss			60		dB
	On time transition	MUTET, MUTER 0.8V ->2.0V		3		µs
	Off time transition	MUTET, MUTER 2.0V ->0.8V		0.25		µs

I²C CHARACTERISTICS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL are bidirectional lines connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are high. Data transfer may be initiated only when the bus is not busy.

The output devices, or stages, connected to the bus must have an open drain or open collector output in order to perform the wired-AND function.

Data at the I²C bus can be transferred at a rate up to 100kbits/s. The number of devices connected to the bus is solely dependent on the maximum allowed bus capacitance of 400pF.

Due to the variety of different devices which can be connected to the I²C bus, the levels of the logical "0" and "1" are not fixed and depend on the appropriate level of V_{DD}. For the typical supply voltage of 5V which is chosen here, logical "1" and logical "0" are, however, fixed respectively on maximum input LOW voltage, 1.5V and minimum input HIGH voltage, 3.0V.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock's cycle. If it does not remain HIGH, it may be interrupted as a control signal.

START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH to LOW transition of the data line while the clock line is HIGH is defined as a start condition S. A LOW to HIGH transition of the data line while the clock is HIGH is defined as a stop condition.

SYSTEM CONFIGURATIONS

A device generating a message is a "transmitter"; a device receiving a message is the "receiver". The device that controls the message is the "master"; and devices which are controlled by the master are the "slaves".

ACKNOWLEDGE

The number of data bytes transferred between the start and the stop condition from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set up and hold times must be taken into account.

I^{2}C BUS DATA CONFIGURATIONS

The NE5751 is always a slave receiver in the I^{2}C bus configuration (R/W bit-0). The slave address consists of seven bits in the serial mode where the least significant bit is selectable by hardware on input A0 and the other more significant bits are internally fixed.

POWER ON RESET

In order to avoid undefined states of the NE5751 when the power is switched on, a power on reset is supplied. The reset is active when Pin V_{REF} is held below 0.8V. The reset is off when Pin V_{REF} is above 2.0V. Pin V_{REF} is normally at 2.5V generated by a resistive divider from V_{DD}. Nominal impedance is 20kΩ. In a typical application a capacitor is connected to Pin V_{REF} to improve power supply rejection. The time delay of the network resets the internal registers when power is first applied. The signal paths are off in the reset condition. The NE5751 must be programmed via the I^{2}C bus for normal operation. The Power Down mode is defined only when all register values are zero.

CONTROL REGISTERS

Register Map

The address register is as follows:

MSB							LSB
A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	SA1	0

SA1 is controlled by serial bus address pin.

Signal Path Register

MSB							LSB
T10	T9	T8	T6	VOX_{EN}	T4	T3T5	T2

T2	is the transmission gate between Pin $PREEMP_{IN}$ and the emphasis input.
T3T5	connects the output of the DTMF generator to the emphasis input and connects the output of the XMT LPF to Pin $TXDTMF_{OUT}$.
T4	connects the output of the XMT LPF to Pin $TXLF_{OUT}$.
VOX_{EN}	enables the VOX function of NE5750.
T6	connects Pin VC_{IN} to the volume control.
T8	connects the output of the DTMF generator to the volume control.
T9	enables VC_{OUT1}.
T10	enables VC_{OUT2}.

Volume Control and Test Register

MSB							LSB
PDW	T1T7	DEE	PRE	V1	V2	V3	V4

V4	is volume control bit 4. This is the MSB. A zero is 16dB attenuation.
V3	is volume control bit 3. A zero is 8dB attenuation.
V2	is volume control bit 2. A zero is 4dB attenuation.
V1	is volume control bit 1. A zero is 2dB attenuation.
PRE	is the bypass for the pre-emphasis.
DEE	is the bypass for the de-emphasis.
T1T7	is the bypass for the compressor and expandor.
PDW	is the control for power down mode.

This mode is defined only when all register values are reset to zero.

High Tone DTMF Register

MSB							LSB
HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0

The eight bits determine the output frequency by the following formula.:

High Frequency = 1200kHz/6/HD
where HD is the value of the register.

Low Tone DTMF Register

MSB							LSB
LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0

The eight bits determine the output frequency by the following formula.:

Low Frequency = 1200kHz/12/LD
where LD is the value of the register.

The operation of the 96ms DTMF timer is initiated by the loading of the low tone DTMF register. This timer terminates transmission of the tones as the generated tones cross the reference level after 96ms. The on time of the tones can thus vary by up to one cycle of the tones.

Continuous tones can be obtained by again loading the two DTMF registers before 96ms have elapsed.

Single tones can be obtained by loading 0, 1 or 2 into one of the registers to silence it.

Phase continuous frequency modulation can be produced by loading a new value into a DTMF register during operation.

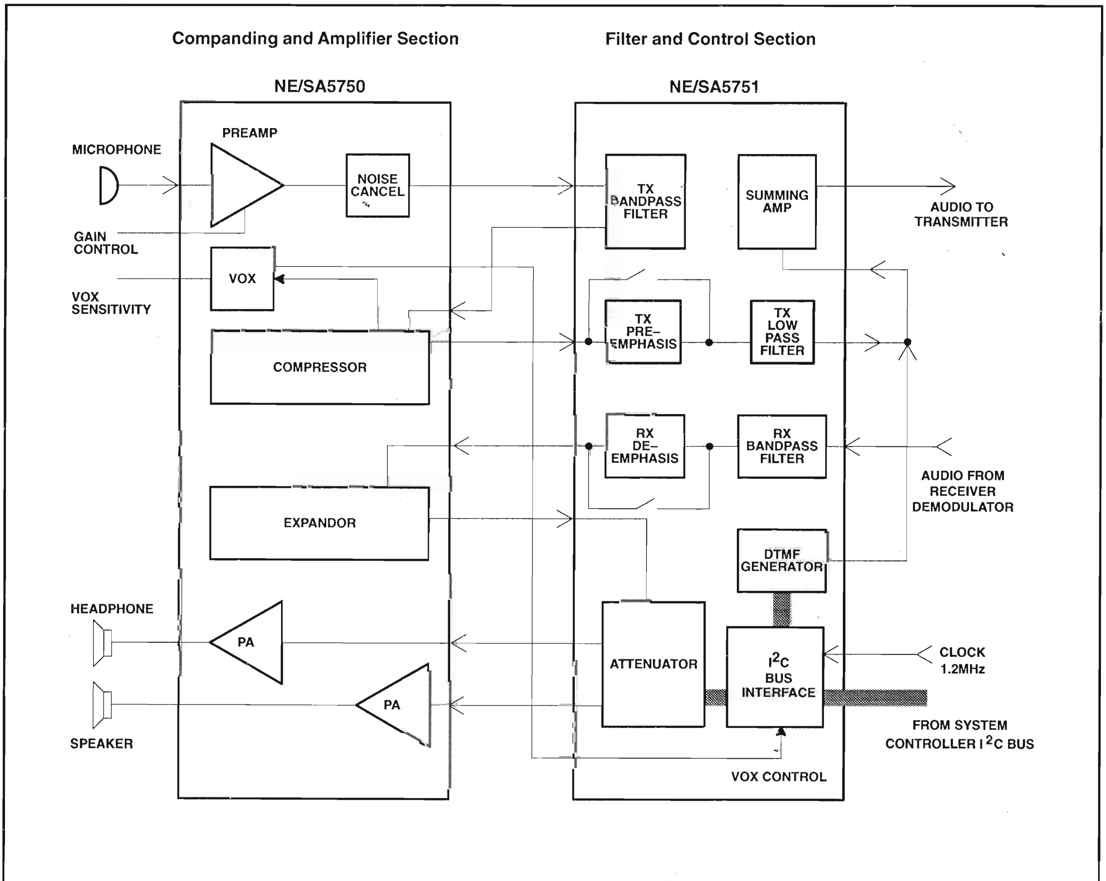


Figure 1. Typical Configuration of Audio Processor (APROC) System Chip Set

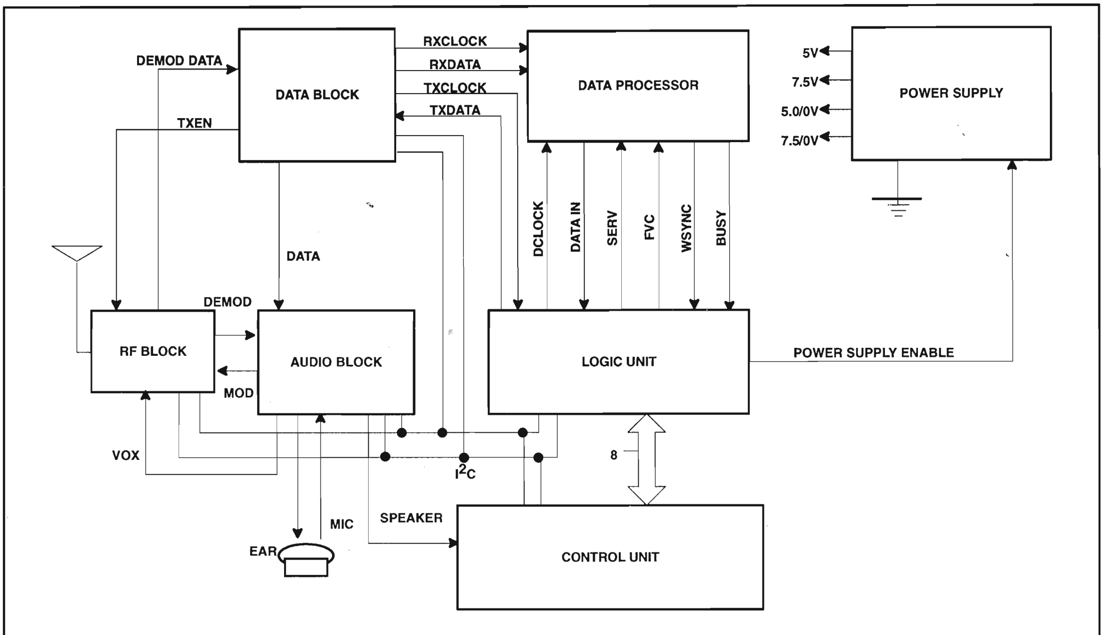


Figure 2. Cellular Radio System

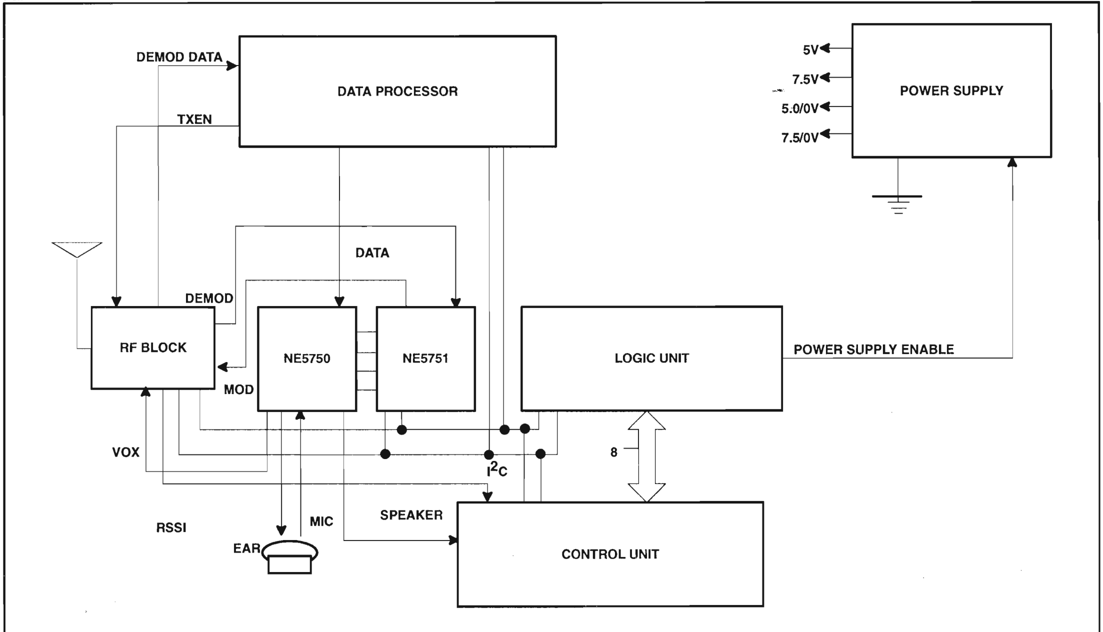


Figure 3. APROC Application Diagram

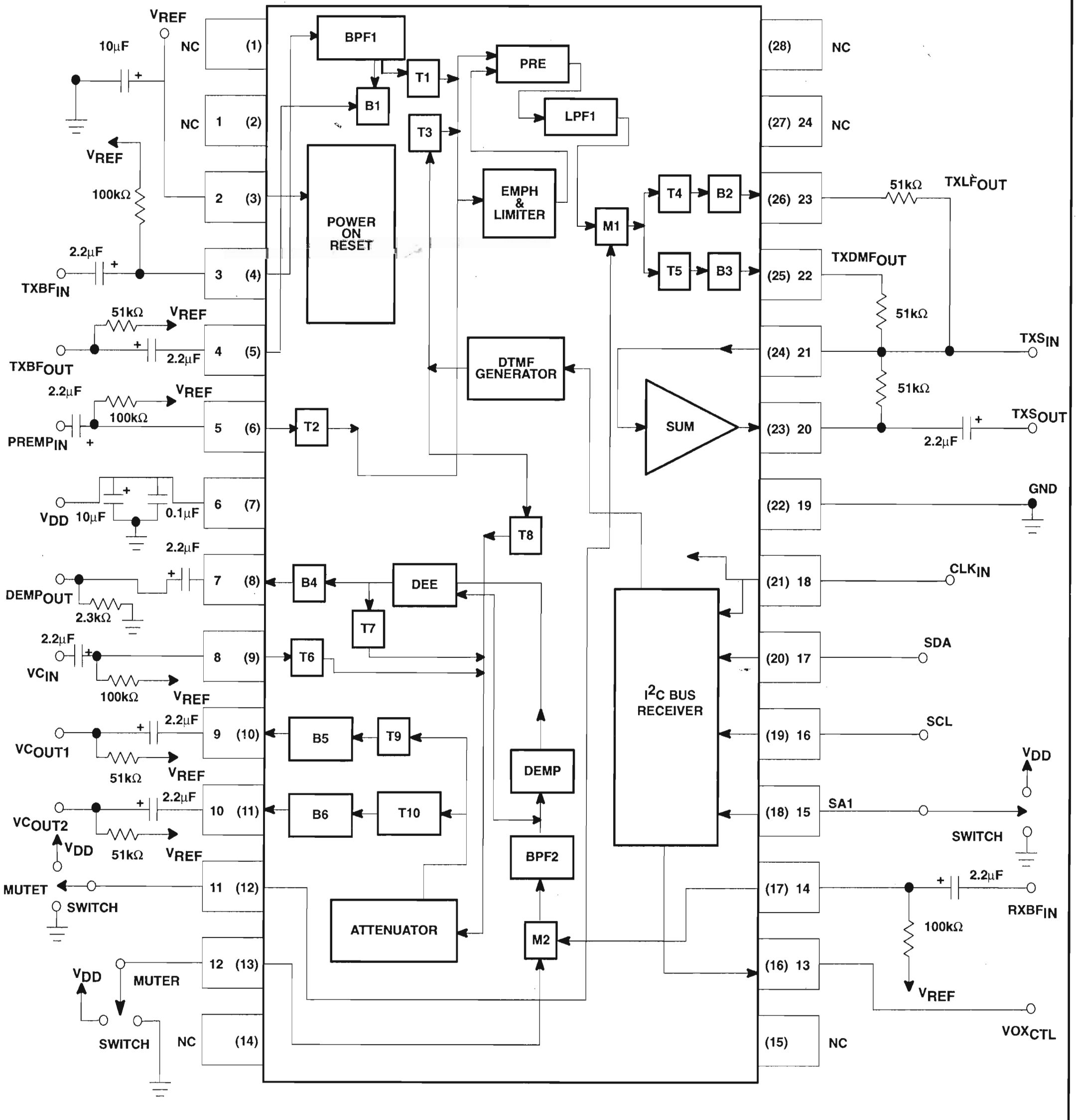
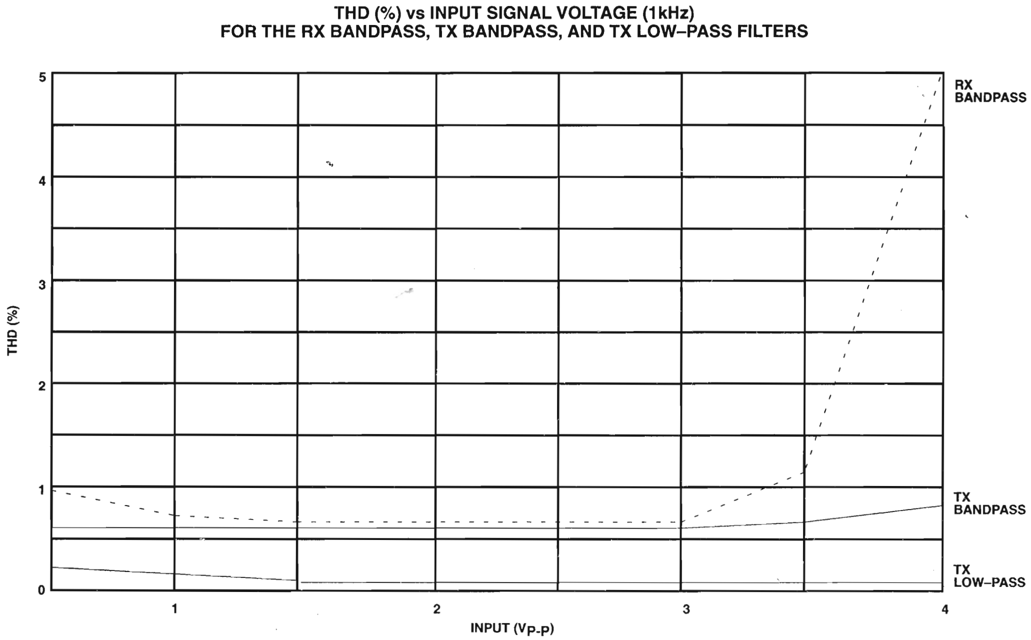


Figure 4. NE/SA5751 Test and Application Circuit

PERFORMANCE CHARACTERISTIC



Using the NE5750 and NE5751 for audio processing

AN1741

Author: Alvin K. Wong

INTRODUCTION

The NE5750 and the NE5751 are two audio processor chips that can be used in RF communications. The chip-set processes a voice so that by the time it is transmitted and received, the quality is preserved. This is accomplished through the use of compression/expansion and pre-emphasis/ de-emphasis.

The audio processor chip-set (APROC) has a wide variety of high performance applications such as cellular phones, cordless voice microphones, cordless intercom systems, standard phones, and hand-held, base, or mobile two-way communications equipment.

Below is an outline of this application note:

I. WHAT IS AUDIO PROCESSING

- How the Voice is Processed by the NE5750 and NE5751
- More Detail on the Key Features
- Performance Graphs

II. NE5750

- A Breakdown of the NE5750
  - preamp
  - noise canceller
  - VOX
    - VOX_{OUT} and VOX_{CTRL}
    - setting the threshold
  - Compandor
    - compressor
    - expandor
    - how to measure the attack and recovery time
  - Amplifier Section
    - speaker amplifier
    - earphone amplifier
- How to Power Down

III. NE5751

- A closer look at the NE5751
  - transmit path
    - limiter and all-pass circuit
  - receive path
- I^{2}C Bus Receiver

IV. APROC DEMO-BOARD

- How to Power Down the Chip set
- Component list and layout

V. NE5750 DEMO-BOARD

- Component list and layout

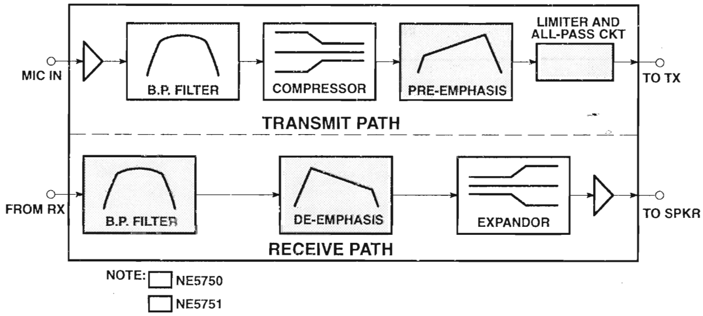


Figure 1. Key Functions of the NE5750 and NE5751 That Contribute to Improving the S/N Ratio and Sensitivity in the System.

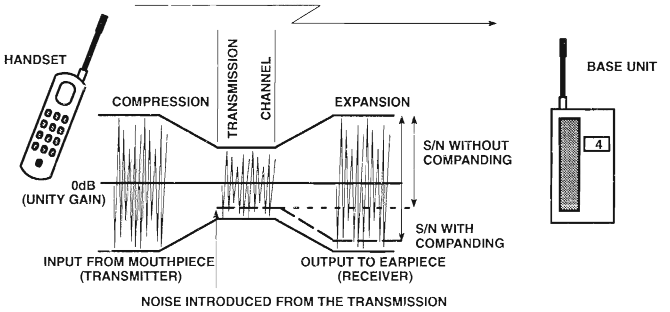


Figure 2. S/N Ratio With Companding vs Without Companding

VI. QUESTION AND ANSWER SECTION

I. WHAT IS AUDIO PROCESSING

HOW THE VOICE IS PROCESSED BY THE NE5750 and NE5751:

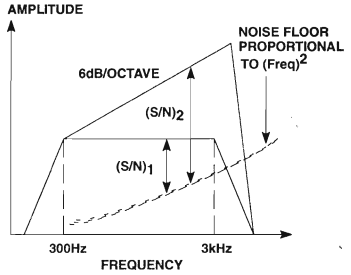
Audio processing begins when a person speaks into a microphone (see Figure 1). The signal is first amplified by the preamp, then screened by a bandpass filter. After the noise is filtered out, the voice signal is processed by the compressor. The function of the compressor is to attenuate loud voices and amplify soft ones. The upper voice frequencies are then amplified by pre-emphasis before their voltage amplitudes are restricted by the limiter and all-pass circuit. When this is completed, the processed voice is ready for transmission.

Since the voice signal was processed by the APROC before transmission, it must be unprocessed upon reception. The received signal is screened again so that the unwanted received noise is blocked before it goes

through de-emphasis. In de-emphasis, the upper voice frequencies are attenuated. Then the signal is expanded back to its primary dynamic range by the expandor. Because the voice is restored to its original state, it is ready for amplification by the power amp whose output can be connected to an external speaker. The receiving party will now be able to hear the transmitting party.

MORE DETAIL ON THE KEY FEATURES:

During compression, low level signals are amplified to "jump" over the transmitter channel noise, while the high level signals are compressed to prevent distortion. In general, because we are dealing with a limited dynamic range transmission medium, it is desirable to compress the signal prior to transmission. However, in order to preserve the dynamic range of the original voice signal, the compressed signal is expanded at reception. Figure 2 shows a diagram of a cordless phone application using companding. Note the signal-to-noise ratio with and without companding.
Another key function of the APROC is the pre-emphasis/de-emphasis capability which is used to overcome the "colored" noise, present in all FM receivers, generated by the FM demodulator. This noise worsens at the upper voice band as shown in Figure 3. Therefore, to keep the same signal-to-noise ratio in the lower and upper voice bands, pre-emphasis/de-emphasis is required. A person with a high-pitched voice will now be heard just as well as a person with a low, deep voice.



WHY PRE-EMPHASIS?
(S/N)$_1$ = SIGNAL-TO-NOISE RATIO WITHOUT
(S/N)$_2$ = SIGNAL-TO-NOISE RATIO WITH

Figure 3. Pre-emphasis Response

Another key stage of the APROC is the limiter with the all-pass circuit. Its main function is to limit the amplitude of the voice signal so that the maximum frequency deviation is limited to 12kHz. Cellular radio specifications allow for a 30kHz channel spacing with an audio bandwidth of 3kHz. Therefore, by Carson's rule the maximum frequency deviation of the limiter must be 12kHz as shown below.

1. Bandwidth = 2 (Modulating Freq + Max Freq Dev)

or

2. Max Freq Dev = Bandwidth/2 – (Mod Freq)
= 30kHz/2 - 3kHz
= 15kHz-3kHz
= 12kHz

PERFORMANCE GRAPHS OF APROC DEMO-BOARD:

Figure 4 shows the general diagram of the audio processor chip set without the external components. External components for the chip set can be found in Figure 31, and the values were chosen for AMPS/TACS specs. To demonstrate the performance of the chip set, data was taken in the lab and resulted in the following figures.

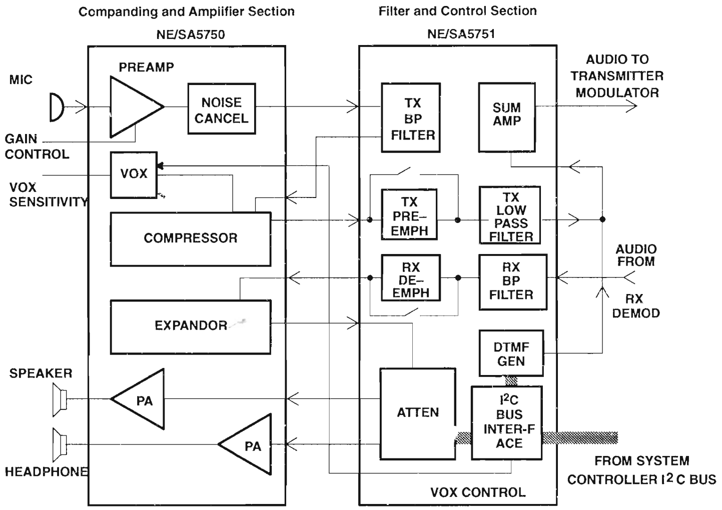


Figure 4. Typical Configuration of Audio Processor (APROC) System Chip Set

Figure 5 Description

Figure 5 reveals what the signal would look like on the bench with different input levels. Figures 5a, b, and c all use the same audio input signal. The audio signal (0-6kHz) varies from 20dB to -30dB in 10dB steps.

Figure 5a

This graph shows the Tx channel. Notice the signal's increase in amplitude as the frequency is increased due to pre-emphasis. Additionally, the slope of the signal decreases as the input increases.

The compressor function is readily shown where a 5dB change in the output level occurs for every 10dB change in the input.

Figure 5b

The 2:1 expansion of audio (20dB change for every 10dB), bandpass filtering and the de-emphasis filter response (300-3kHz) are shown. The graph shows the Rx channel. Notice the signal's decrease in amplitude as the frequency increases due to de-emphasis.

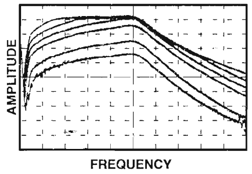
Figure 5c

This shows that a flat frequency response is achieved upon normal reception. Notice the 20dB gap, although the input steps are for 10dB. This is due to the noise canceller turning on. The decrease in amplitude for higher level, higher frequency tones is the result of the deviation limiter action.

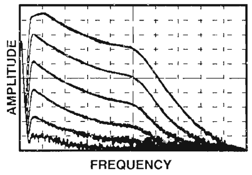
After studying these figures, a designer will have a graphical understanding of how the APROC processes a signal.

Figure 6 shows the test set-up using the APROC demo-board to simulate a real cellular phone call. Audio noise is added to the input of the microphone and RF noise is added to the receiver. The table for Figures 7-10 describes what the associated waveforms reveal when certain key stages of the APROC are activated or bypassed.

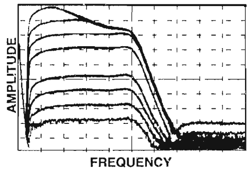
As seen from the following figures, there is a definite advantage in using the chip set in high performance communication systems.



a) TRANSMIT CHANNEL (AUDIO LEVEL DECREASING)



b) RECEIVE CHANNEL



c) LOOPBACK

All Graphs:
10dB/Div CENTER: 3000Hz SPAN: 6000Hz

Figure 5.

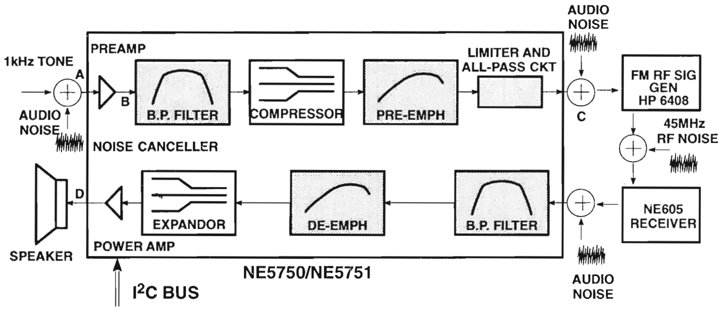
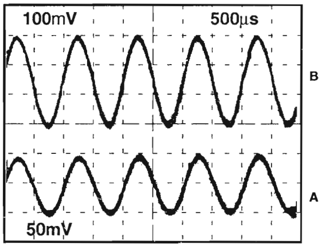
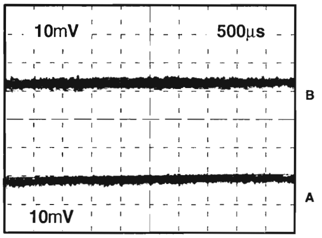


Figure 6. NE5750/NE5751 Test Set-Up



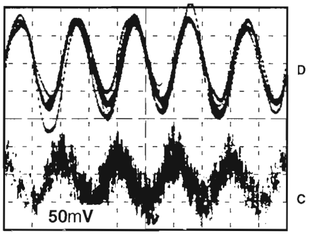
THERE IS GAIN IN THE PREAMP WITH A TONE PRESENT.



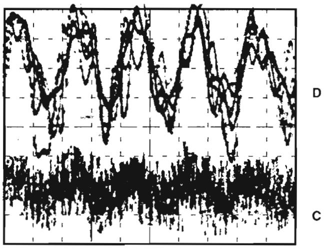
NO GAIN IS OBSERVED IN THE NOISE LEVEL.

Figure 7.

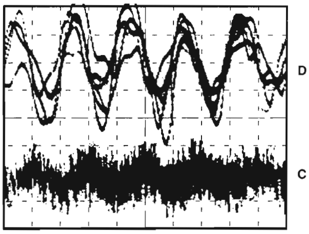
Figure	Description
7	No noise gain is observed at the output of the Tx channel because of the noise canceller circuit.
8	Shows why companding and emphasis are needed to improve the quality of the audio signal when BASEBAND NOISE is present in the system
9	Shows why companding and emphasis are needed to improve the quality of the audio signal when RF NOISE is present in the system.
10	Shows that the sensitivity and the signal-to-noise ratio of a receiver improved due to audio processing.



WITH COMPANDING AND PRE-EMPHASIS/DE-EMPHASIS



NO COMPANDING, NO PRE-EMPHASIS/DE-EMPHASIS

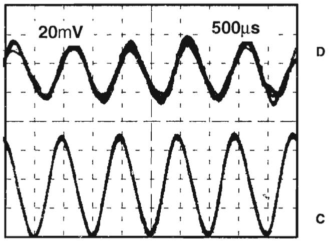


NO COMPANDING, PRE-EMPHASIS/DE-EMPHASIS ONLY

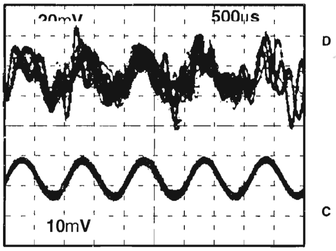
C = BOTTOM TRACE AUDIO SIGNAL BEFORE GOING TO THE RF TRANSMITTER

D = TOP TRACE FINAL SPEAKER OUTPUT

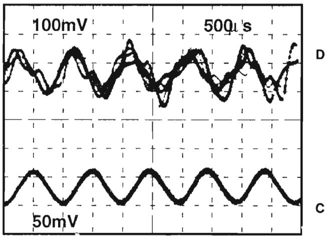
Figure 8. Audio Output with Baseband Channel Noise



WITH COMPANDING AND PRE-EMPHASIS/DE-EMPHASIS



NO COMPANDING, NO PRE-EMPHASIS/DE-EMPHASIS



NO COMPANDING, PRE-EMPHASIS/DE-EMPHASIS ONLY

C = BOTTOM TRACE AUDIO SIGNAL BEFORE GOING TO THE RF TRANSMITTER

D = TOP TRACE FINAL SPEAKER OUTPUT

Figure 9. Audio Output with a Noisy RF Channel

II. NE5750

A CLOSER LOOK AT THE NE5750:

Referring to Figure 11, the NE5750 has seven main features which make this chip unique: preamp, noise canceller, VOX, compressor, expandor, buffer, and power amplifiers. (NOTE: All component labels in this section are referenced to Figure 11, unless otherwise indicated.)

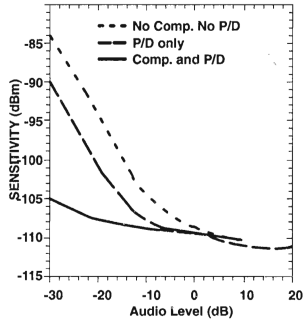
Preamp:

The NE5750 provides a preamp with adjustable gain. This allows the designer to boost the low level audio signal coming out of the microphone. The microphone can be connected to Pin 1 through a DC blocking capacitor, C1 (see Figure 12). The input impedance at this Pin is 50kΩ.

The preamp gain of the NE5750 can be adjusted from 0dB to 40dB by an external resistor, R7, connected to Pin 2 through a capacitor C2. Below is a formula which allows the designer to determine the value of R7 for a certain value of gain.

If a designer wanted a preamp gain of 20dB, a 5kΩ resistor would be required (see Table 6).

FINAL AUDIO SENSITIVITY FOR 12dB SINAD



SIGNAL TO BACKGROUND NOISE (-100dBm RF)

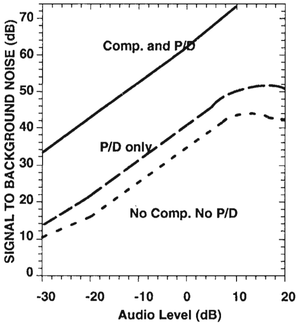


Figure 10.

$$R7 = \left[\frac{50,000}{10^{\left(\frac{X(dB)}{20}\right)} - 1}\right] - 500 \qquad (1)$$

"X" in dB

Table 6. Calculated R7 Values for Different Preamp Gains

X (dB)	R7
0	Leave Pin 2 open
5	64k
10	22k
15	10k
20	5.1k
25	2.5k
30	1.1k
35	405
40	Pin 2 AC grounded

Noise Canceller:

The output of the preamp is connected to the input of the noise canceller circuit which is internal to the device. The function of the noise canceller is to automatically provide a set gain of either 0dB when no signal is present, or 10dB when a signal is present. With this feature, background noise is minimized from transmission.

This automatic gain setting can only be implemented when the noise canceller circuitry is used in conjunction with the VOX circuitry. The threshold and attack and release time can be set externally. This will be described in more detail in the "VOX" section.

Although the noise canceller circuit is really designed to be used with the VOX circuitry, it can be implemented without it. The noise canceller circuit can be set up to provide either 0dB or 10dB of gain at all times (regardless of the presence of a signal). Table 7 shows how to achieve either gain settings when the VOX function is bypassed.

Table 7. Setting Up the Gain of the Noise Canceller

Pin No.	Gain of Noise Canceller	
	0dB	10dB
3	Ground	Ground
4	Ground	V_{CC}
7	10k to GND	Ground

The output of the noise canceller is accessible to the designer at Pin 24. C13 is used as a DC blocking capacitor.

VOX:

As mentioned earlier, the VOX circuitry works together with the noise canceller circuit. Pins 3, 4, 5, 6, and 7 all deal with the VOX's performance.

All of the resistor and capacitor values given in the NE5750 data sheet are chosen to meet AMPS/TACS specification for cellular radio. So any deviation from these values should be considered carefully if the application is in cellular radio.

Connected to Pin 3 is a resistor R2 and capacitor C15, as shown in Figure 13. These components set the gain of the VOX. The values here are for internal use only and have no direct relationship with the performance. So the values should be kept as shown. In some special applications, R2 may be adjusted such that the voltage on Pin 4 can be increased. By increasing this voltage, the voltage on Pin 7 can be set to a higher range (more details later).

Pin 4 has C3 and R1 connected to it which affects the attack and release time of the VOX circuit. In general the attack time should be faster than the release time.

The values given for C3 and R1 provide an approximate attack time of 12ms and release time of 120ms. These values should be kept as shown.

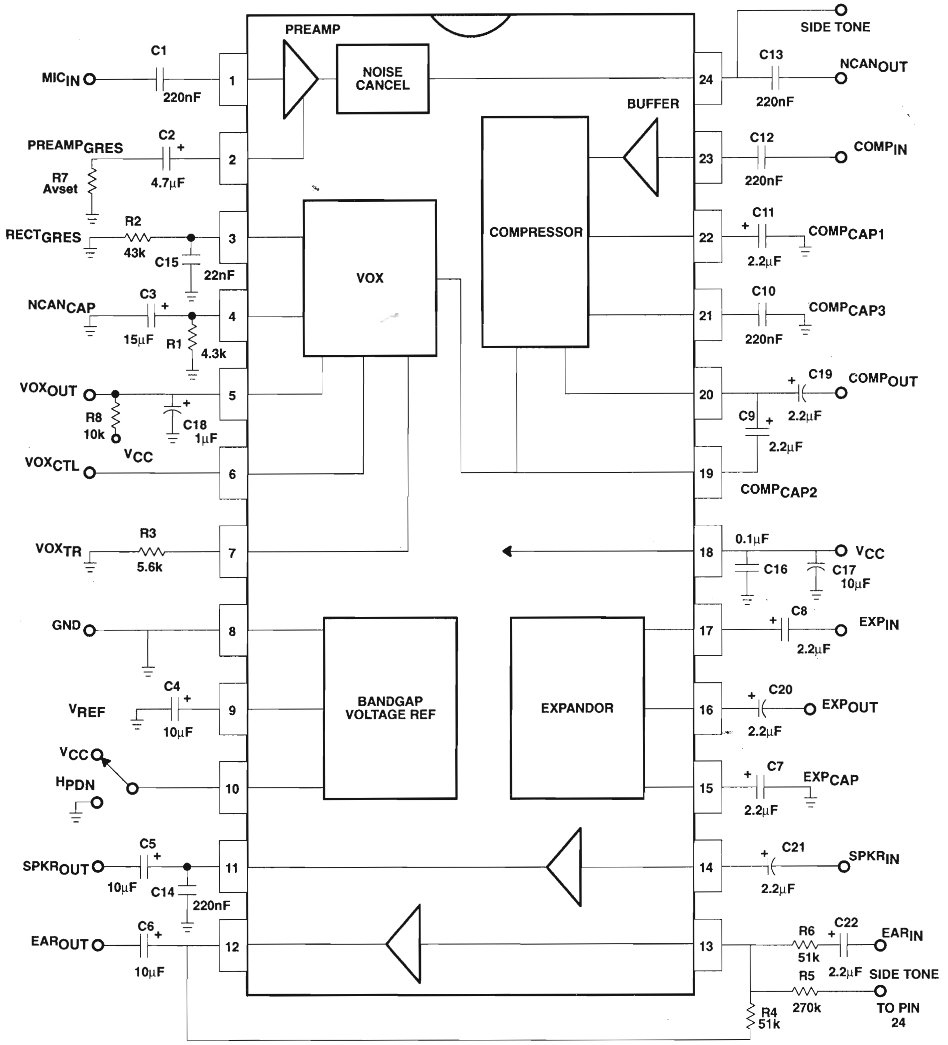
The timing of the VOX circuit is important because it controls the gain of the noise canceller, and can also turn the transmitter on and off.

- VOX_{OUT} and VOX_{CTRL}

By using VOX_{OUT} and VOX_{CTRL}, Pins 5 and 6 respectively, the NE5750 can control the status of the transmitter. The VOX_{OUT} Pin should have a 10kΩ pull-up resistor to V_{CC}. When probing Pin 5, a logic '1' or '0' will be read. The VOX_{CTRL} pin should have a logic '1' or '0' connected to it. Table 8 shows how Pins 5 and 6 can be used:

Having a logic '0' on Pin 6 is sufficient in most applications. When voice is present, the noise canceller kicks on while the VOXout Pin supplies a logic '1'; when voice is not present, VOXout Pin supplies a logic '0'. In a cordless phone application this logic level could be used to turn the transmitter on and off, thereby conserving power for any battery operated applications.

Supplying a logic '1' on Pin 6 would cause the transmitter to stay on regardless of any signal input to Pin 1. However, the functionality of the noise canceller will still be signal dependent.



NE5750 COMPONENT LIST

C1	DC blocking cap for Mic amp
C2	DC blocking cap for Mic gain
C3	used to set attack and release time of VOX
C4	V$_{REF}$ filter capacitor
C5	DC blocking cap for speaker at Pin 11
C6	DC blocking cap for EAR$_{OUT}$ pin
C7	sets attack and release time for expandor
C8	DC blocking cap for expandor's input
C9	AC bypassing for compressor
C10	passes AC to GND
C11	sets attack and release time of compressor
C12	DC blocking cap for compressor's input
C13	DC blocking cap
C14	low pass filtering for speaker output
C15	used for filtering, internal use only

R1	used to set release time of VOX
R2	set gain of VOX, but for internal use only effects voltage on Pin 4
R3	sets threshold level of VOX
R4	feedback resistor for ear amp
R5	sets gain of ear amp for side tone signals
R6	sets gain of ear amp for baseband signals
R7	sets microphone preamp gain

ADDED FOR NE5750 DEMO-BOARD

R8	pull-up resistor to get logic levels out
C16	bypass capacitor
C17	bypass capacitor
C18	passes AC to GND (low pass)
C19	DC blocking cap for compandor out
C20	DC blocking cap for expandor out
C21	DC blocking cap for speaker in
C22	DC blocking cap for ear in

Figure 11. NE/SA5750 Application Demo-Board

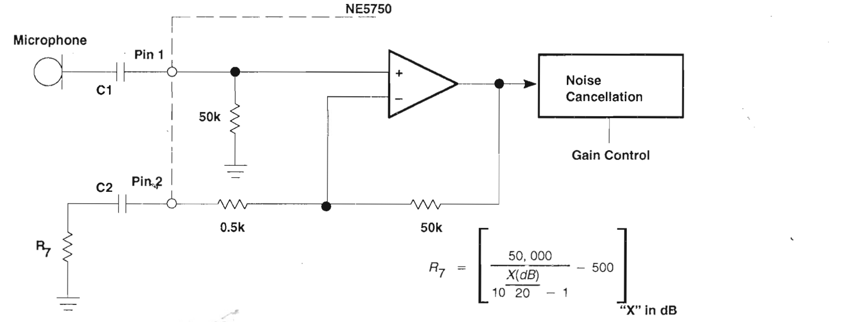


Figure 12. Setting Microphone Preamplifier Gain

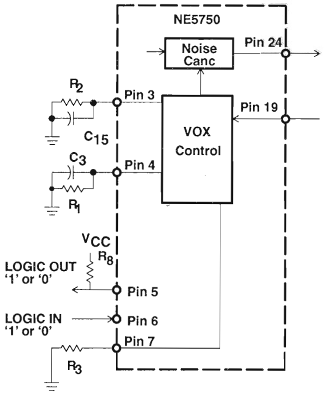


Figure 13. VOX Circuit

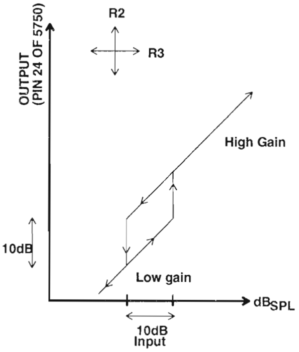


Figure 14.

This condition is mainly used if the battery consumption is not a problem. Such a condition would be for any car cellular radios.

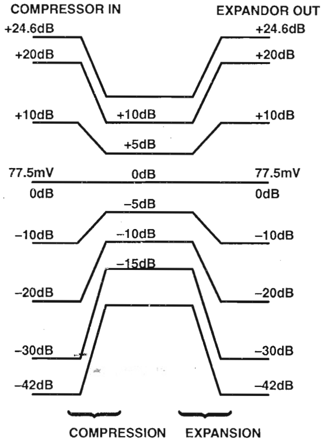


Figure 15. Compandor Dynamic Range

- setting the threshold

R3 at Pin 7 is used to set the threshold of the VOX. Setting the threshold determines the voltage level input at which the noise canceller and VOX will activate. Formula 4 shows how to calculate the VOX's threshold.

$$VOX_{THRESH}\ (mV) = 50\mu A \cdot R3\ (K\Omega) \qquad (4)$$

Where $R3 > 3k\Omega$)

If R3 = 5.6k, the measured voltage at Pin 7 should be approximately 280mV.

The way to adjust the VOX is to first determine what signal level is desired at Pin 1 to activate the VOX noise canceller circuits. Once that level is applied to Pin 1, connect a voltmeter to Pin 4. The voltage level measured here should be plugged into formula 4 to determine R3.

As mentioned earlier, the voltage at Pin 4 can be increased by R2. But one should only deviate from the R2 value if the voltage at Pin 7 cannot come down. In most cases, setting R2 to 43kΩ and setting Pin 7 to the voltage at Pin 4 is sufficient.

Figure 14 shows graphically how R3 and R2 affect the location of the "box". The "box" is always 10dB, which is due to the noise canceller circuit.

EXAMPLE I : Set the VOX threshold such that it "kicks on" when $30mV_{P-P}$ is applied to Pin 1 of the NE5750 with a preamp gain of 0dB.

Step 1: Make sure:

a. Pin 7 is left open.

b. The VOX attack and recovery components are in place at Pin 4.

c. R2 and C15 are connected to Pin 3.

d. If using the NE5750 alone, be sure to connect the preamp output (Pin 24) to the compressor input (Pin 23) with a DC blocking cap.

e. The preamp gain is already set (in this instance the preamp gain is 0dB).

f. Make sure that the compressor's components are also connected; compressor's attack time has to be functional

Step 2: Apply a constant 1kHz sinewave signal to Pin 1 with the desired threshold. In this case, $30mV_{P-P}$.

Step 3: Measure the DC voltage on Pin 4; V4=260mV

Step 4: Calculate R3:

$$\begin{aligned} R3 &= V4(V)/(50\mu A) \\ &= 0.260/50\mu A \\ &= 5.2k \end{aligned}$$

let's use a 5.3kΩ

Step 5: Connect R3 to Pin 7 and verify that VOX "kicks on" at the desired threshold.

- This set-up has the VOX kicking on at $30mV_{P-P}$ and kicking off at $11mV_{P-P}$.

Referring to the above example, if a preamp gain of 10dB was chosen before setting the threshold, the threshold will also change. So it is vital that the preamp gain be set before setting the VOX threshold.

Table 8. VOX Truth Table

Inputs		Outputs	
Voice (Pin 1)	**VOX_{CTRL} (Pin 6 of NE5750)**	**Noise Canceller Gain**	**VOX_{OUT}**
Not Present	logic '0'	0dB	logic '0'
Present	logic '0'	10dB	logic '1'
Not Present	logic '1'	0dB	logic '1'
Present	logic '1'	10dB	logic '1'

NOTE: To apply a logic '0' on Pin 6 by the I^2C evaluation program, be sure that the VOX_{EN} is high, and low for a logic '1' on Pin 6. If the NE5750 is used alone, be sure that the output of the noise canceller is AC coupled to the input of the compressor. Also, make sure that all of the components for the compressor are connected.

Compandor:

- compressor

The compressor input at Pin 23 requires an external DC blocking capacitor (C12). The input impedance is roughly 50kΩ. Unlike the older compandors, this input can be directly driven from CMOS circuits (e.g. NE5751).

The gain from the preamp should be adjusted such that there is enough signal getting to the compandor. However, one must be careful not to overdrive the inputs. Additionally, do not forget the extra 10dB gain from the noise canceller (assuming it is being used).

Figure 15 shows the typical dynamic range of the compandor. The maximum input signal that the compressor can handle is $3.72V_{P-P}$ or 24.6dB. The minimum input is approximately $1.74mV_{P-P}$ or -42dB. Knowing that the 0dB point of the compandor is at $77.5mV_{RMS}$, one can easily convert from volts to dB. Formula 5 shows the conversion from V_{RMS} to dB.

$$X(dB) = 20\log\left(\frac{V_{RMS}}{77.5(mV_{RMS})}\right) \quad (5)$$

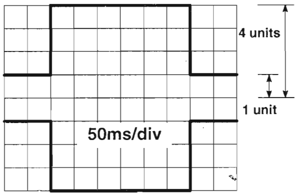
where
X = value in dB
V = voltage in RMS.

Usually it is easier to work in voltages, but in this case it is better to work in dB. If one knows the input signal in dB, the designer can predict the output of the compressor (also in dB) to be half or two times the input. For instance, if the input were 10dB, we could expect the output to be 5dB. On the other hand, if the input was -20dB, we could expect the output to be -10dB.

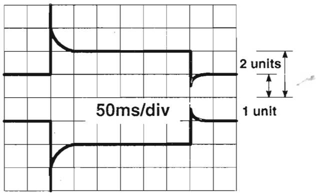
Capacitor C11 on Pin 22 controls both the attack and release time of the compressor. The attack time may be calculated by Formula 6.

$$\text{Attack time} = R \cdot C \quad (6)$$

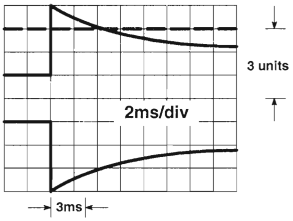
where R=10kΩ



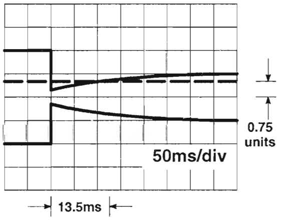
a. Input



b. Output



c. Attack time



d. Release time

Figure 16. Compressor Dynamic Response

NOTE: The release time is roughly 4 times slower than the attack time by design.

$$\text{Release time} = 4 \cdot \text{Attack time}$$

Capacitor C10 on Pin 21 is used for AC bypassing. Capacitor C9 on Pins 19 and 20 is also for AC bypassing.

- expandor
The expandor input at Pin 17 requires an external DC blocking capacitor (C8). The input impedance is around 2.5kΩ. Referring to Figure 15, the input range of the expandor is from 19.53mV$_{P-P}$ (-21dB) to 903mV$_{P-P}$ (12.3dB). The output range is from 1.74mV$_{P-P}$ (-42dB) to 3.72V$_{P-P}$ (24.6dB).

Capacitor C7 is used to set the attack and release time of the expandor. Formula 6 can also be used to determine those values.

- how to measure attack and recovery time
In this section we will briefly describe the bench procedure for measuring attack and recovery times. Additional information can be found in AN174 in the "Attack and Decay Time" section.

Let's assume that C_{RECT} =2μF and $R_{INTERNAL}$=10k. Since T=R · C, then T=20ms. If we wanted a different "RC" time constant we would change the C_{RECT} value ($R_{INTERNAL}$ is a fixed value).

Using these component values let's measure the attack and recovery times to see if the CCITT and EIA specifications are met.

measurement at compressor:
EIA Specifications

Attack time is the time required for the transmitter deviation to settle to a value equal to "1.5" times the final steady state value, for a 12dB step up.

Release time is the time required for the transmitter deviation to settle to a value equal to "0.75" times the final steady state value, for a 12dB step down.

The compressor must have a nominal attack time of 3ms and a nominal recovery time of 13.5ms as defined by CCITT.

Bench Procedure for Compressor Test

1. Apply a 1kHz sinewave signal at 0dB to the input of the compressor (0dB is defined where the compandor passes the input signal through to the output — unity gain level for the APROC is 77.5mV$_{RMS}$.
2. Modulate the 1kHz input signal with a 1Hz-2Hz square wave.
3. Connect an oscilloscope probe to the input of the compressor and adjust both the modulation and oscilloscope (uncalibrate it) so that a 1:4 ratio is achieved on the screen of the oscilloscope (see Figure 16a).

Adjusting for a 1:4 ratio produces a 0dB to 12dB step at the input. The unit "1" represents the 0dB input level and the unit "4" represents the 12dB input level (20log (4/1) =12dB).

4. Connect another oscilloscope probe to the output of the compressor and observe the waveform (see Figure 16b). The "final steady-state" value for the attack time is "2" units while the release time is "1" unit. These output values are expected because, for a compressor, the ratio is 2:1 unless the input is at 0dB, in which case, the ratio is 1:1.
5. Now to measure the attack and release time, capture the beginning and end of the output waveform where the changes occur (see Figures 16c and 16d).

To measure the attack time (T_A):

-According to the EIA specifications:

$$T_A = 1.5 \cdot \text{Final Steady} - \text{State Value}$$

-therefore

$$T_A = 1.5 \cdot 2 \text{ units} = 3 \text{ units}$$

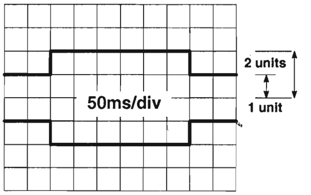
-Measure the time it takes for the output to drop to the 3rd unit. According to Figure 16c, our attack time is 3ms. This indeed meets CCITT specs..

To measure the release time (T_R):

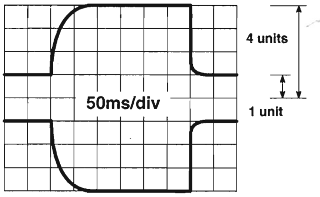
-According to the EIA specifications:

$T_R = 0.75 \cdot \text{Final Steady} - \text{State Value}$

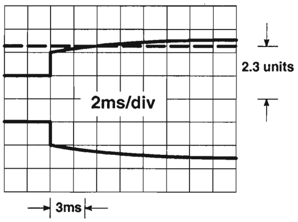
-therefore



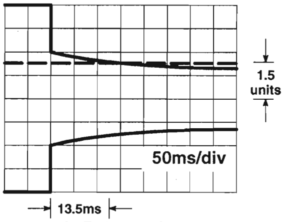
a. Input



b. Output



c. Attack time



d. Release time

Figure 17. Expandor Dynamic Response

$T_A = 0.75 \cdot 1 \text{ unit} = 0.75 \text{ units}$

-Measure the amount of time it takes for the output to rise up to 0.75 units. According to Figure 16d, our release time is 13ms. Again the CCITT spec. is met.

measurement at expandor:
EIA Specifications

Attack time is the time required for the transmitter deviation to settle to a value equal to "0.57" times the final steady state value, for a 6dB step up.

Release time is the time required for the transmitter deviation to settle to a value equal to "1.5" times the final steady state value, for a 6dB step down.

The expandor must have a nominal attack time of 3ms and a nominal recovery time of 13.5ms as defined by CCITT.

Bench Procedure for Expandor Test

1. Apply a 1kHz sinewave signal at 0dB to the input of the expandor (0dB is defined where the compandor passes the input signal through to the output — unity gain level).
2. Modulate the 1kHz input signal with a 1Hz-2Hz square wave.
3. Connect an oscilloscope probe to the input of the expandor and adjust both the modulation and oscilloscope (uncalibrate it) so that a 1:2 ratio is achieved on the screen of the oscilloscope (see Figure 17a).

Adjusting for a 1:2 ratio produces a 0dB to 6dB step at the input. The unit "1" represents the 0dB input level and the unit "2" represents the 6dB input level (20log(2/1)=6dB).

4. Connect another oscilloscope probe to the output of the expandor and observe the waveform (see Figure 17b). The "final steady-state" value for the attack time is "4" units while the release time is "1" unit.
5. These output values are expected because for an expandor the ratio is 1:2 unless the input is at 0dB, in which case, the ratio is 1:1.
6. Now to measure the attack and release time, capture the beginning and end of the output waveform where the changes occur (see Figures 17c and 17d).

To measure the attack time (T_A):

-According to the EIA specifications:

$T_A = 0.57 \cdot \text{Final Steady} - \text{State Value}$

-therefore

$T_A = 0.57 \cdot 4 \text{ units} = 2.28 \text{ units}$

-Measure the time it takes for the output to reach 2.28 units. According to Figure 17c, our attack time is 3ms. This indeed meets CCITT specs..

To measure the release time (T_R):

-According to the EIA specs.:

$T_R = 1.5 \cdot \text{Final Steady} - \text{State Value}$

-therefore

$T_A = 1.5 \cdot 1 \text{ unit} = 1.5 \text{ units}$

-Measure the amount of time it takes for the output to drop to 1.5 units. According to Figure 17d, our release time is 13ms. Again the CCITT specification is met.

These results show that the release time is about 4 times slower than the attack time. All Signetics compandors are internally set up this way so that once the attack time is set by C_{RECT}, the release time is automatically set.

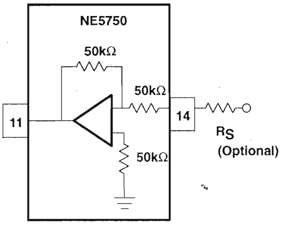
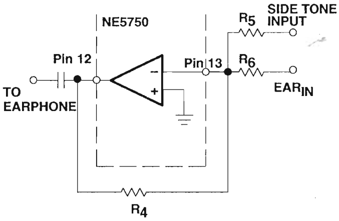


Figure 18. Speaker Amplifier for the NE5750



$$\text{Earphone Gain } A_V = -\frac{R_4}{R_6}$$

$$\text{Sidetone Gain } A_V = -\frac{R_4}{R_5}$$

Figure 19. Setting Gain for Earphone Amplifier

Special Note: In AN174, Figures 10 and 11 show the X-axis as being in fractions of the time constant. The way to clarify this is by multiplying 20ms to these numbers to convert them to the measured attack and recovery time. The 20ms comes from the "RC" time constant which can be varied by varying the C_{RECT} value. But again, once these numbers are converted, one can see that these figures show similar results as ours in the lab.

Amplifier Section:

-speaker amplifier

The speaker amplifier is a unity gain amplifier with a high input impedance. Located on Pin 11, the output of the amplifier, are two capacitors C5 and C16. Capacitor C5 is for DC blocking, while C16 is for high pass filtering.

Since the amplifier's input is not directly accessible to the designer (see Figure 18), it is impossible to exceed a gain of one. However, if external attenuation is desired, use formula 7 to determine the series resistor that would connect to Pin 14.

$$A_V = \frac{-R_F}{R_{IN}} \qquad (7)$$

$$= \frac{-50k}{(50k + R_S)}$$

In most cases, the attenuation takes place in the NE5751 before the signal gets to the amplifier. Therefore, adding external attenuation is rare.

-earphone amplifier:

Unlike the speaker amplifier, the gain of the earphone amplifier can be set by external resistors. In this case, the required output and input are directly accessible. Figure 19 is a diagram of the earphone amplifier with the required equations. Sidetone gain can also be implemented with an external resistor.

How To Power Down

"Power down" or "power up" can be implemented by Pin 10 of the NE5750. When Pin 10 is connected to V_{CC}, the chip is in the "power up" state. In this mode, the chip is fully functional. However, when Pin 10 is connected to ground, the chip is in the "power down" state where the current consumption drops dramatically (CMOS or TTL levels will suffice). In this mode, the chip is not expected to be functional, but all of the capacitors remain charged so that "power up" can occur quickly. Having this capability allows the system to conserve battery power.

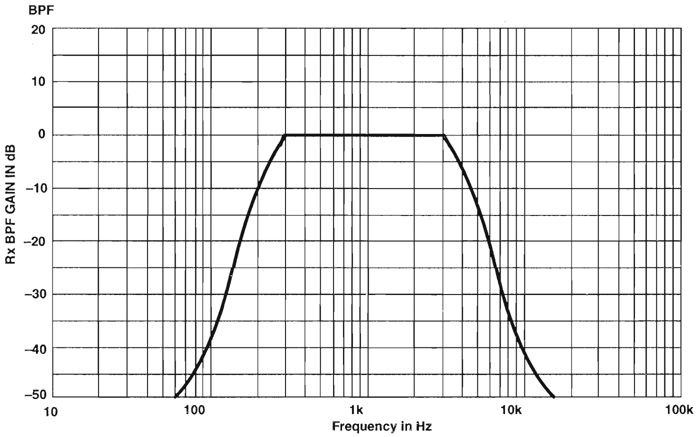


Figure 20. NE5751 Tx Bandpass Filter

III. NE5751

A CLOSER LOOK AT THE NE5751:

Figure 24 shows a block diagram of the NE5751. Key functions for this chip include a TX bandpass filter, TX pre-emphasis filter, TX low pass filter, summing amplifier, RX bandpass filter, RX de-emphasis, programmable DTMF generator, programmable attenuator, and an I^2C bus interface.

-TX path

The input and output of the TX bandpass filter are located on Pins 3 and 4, respectively. The 4th-order Chebyshev bandpass filter is designed to pass 300 to 3000Hz (voice band). (see Figure 20).

The input to the pre-emphasis circuit is accessible through Pin 5. This filter shapes the spectrum with a +6dB per octave slope in the pass band (see Figure 21). The output is then connected internally to a low pass filter and limiter circuit (see Figure 22). The functions of the last two filters guarantee that the 12kHz maximum frequency deviation for cellular radio is not violated.

The output of the limiter filter (Pin 23) and the output of the programmable DTMF generator (Pin 22) can be connected to the input of the summing amplifier. The gain of this amplifier can be controlled with external resistors. In Figure 24, the resistors are all 51kΩ which creates a unity gain configuration. The output of the amp is then connected to the transmitter.

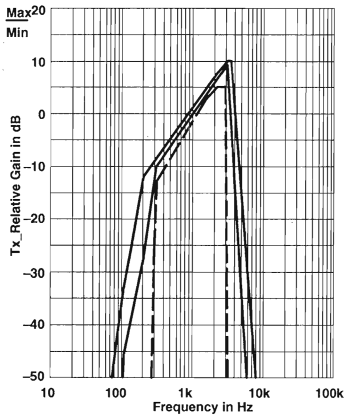


Figure 21. Pre-emphasis Curve

The Limiter and All-pass Circuit:

An important aspect of the AMPS specification is concerned with the 12kHz maximum frequency deviation. The output of the APROC should be less than 12kHz regardless of the input signal. Figure 23 shows the equipment used for the test measurements and how the signal was processed. A 1kHz signal was applied to the input of the demo-board until a 5% distorted signal was measured at the limiter output. This waveform's peak-to-peak voltage was recorded as a reference, then, at various chosen frequencies, the input of the demo-board was overdriven so we could record the distorted peak-to-peak waveform. (See Figure 26)

Formula 8 was used to calculate maximum frequency deviation from the waveforms shown in Figure 26.

$$\text{Max Freq Dev with All-Pass Ckt} = \frac{BW_F}{BW_R} \cdot 8\text{kHz} \qquad (8)$$

where

BW_F = the bottom waveform's peak-to-peak voltage from one of the observed Figures.

BW_R = the bottom waveform's peak-to-peak voltage from the reference Figure.

Table 9. Maximum Frequency Deviation Results for the 12kHz Test

Frequency (Hz)	With All-Pass (kHz)
300	5.91
500	9.04
800	10.09
1000	10.09
1200	10.09
2000	11.13
3000	10.78

Table 9 reveals the calculated results for maximum frequency deviation over the voice band. The test results show that the NE5750 and NE5751 will meet the 12kHz AMPS specification. If a customer needs further assurance that the 12kHz specification will be satisfied, an Automatic Level Control (ALC) circuit can be placed after the summing amplifier output of the NE5751. Keep in mind, though, that this ALC will only provide attenuation.

- RX path

For the receive side of the NE5751, the signal goes to the input of the RX bandpass filter (Pin 13) which has the same characteristics as the TX bandpass filter. The only difference is that this filter also has a stop-band notch filter at 6kHz to reject the Supervisory Audio Tone (SAT) signals as seen in Figure 27.

The output is then internally connected to the de-emphasis filter. This filter provides a -6dB/octave slope over the passband to compensate for the pre-emphasis function (see Figure 28).

The attenuator can be digitally programmed by I^2C. The input signal level can be attenuated 16 steps in 2dB increments. This gives a range from 0dB to -30dB. The attenuator error is shown in Figure 29.

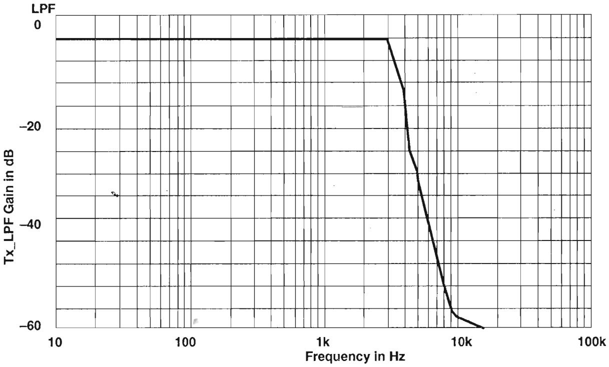


Figure 22. NE5751 Tx Low Pass Filter

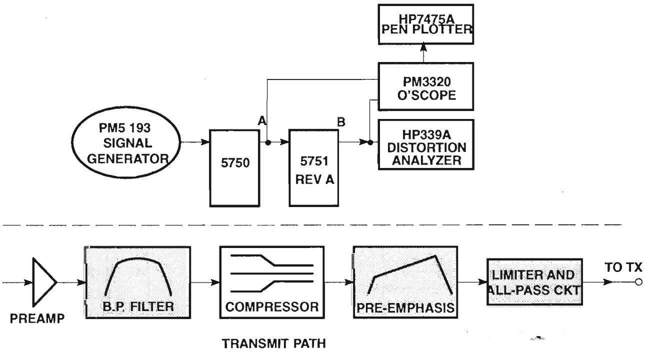


Figure 23. Test Set-up and Tx Path of Signal

I^{2}C Bus Interface:

The NE5751 is controlled by a serial control bus comprised of a clock input, serial bus address, serial clock line, and serial data line.

A designer who is unfamiliar with I^{2}C can refer to the following documents for assistance: 1) I^{2}C Bus Specification and 2) Signetics AN168. Both of these documents can be found in the 1989 Signetics Linear Data Manual or the 1991 RF Communications Handbook.

The clock input requires an input frequency of 1.2MHz. This frequency is vital for the operation of the part because it effects the DTMF generator and the 3dB point of all the switch capacitor filters.

The output of the DTMF generator can be determined by Formula 8.

$$\text{Low Freq} = \frac{\frac{\text{Clock Input Freq}}{12}}{\text{LD}} \tag{8a}$$

where LD is the value of the register This translates to: DTMF LO REG = 100000/ LO REG (Hz)

$$\text{High Freq} = \frac{\frac{\text{Clock Input Freq}}{6}}{\text{HD}} \tag{8b}$$

where HD is the value of the register

This translates to: DTMF HI REG = 200000/ HI REG (Hz)

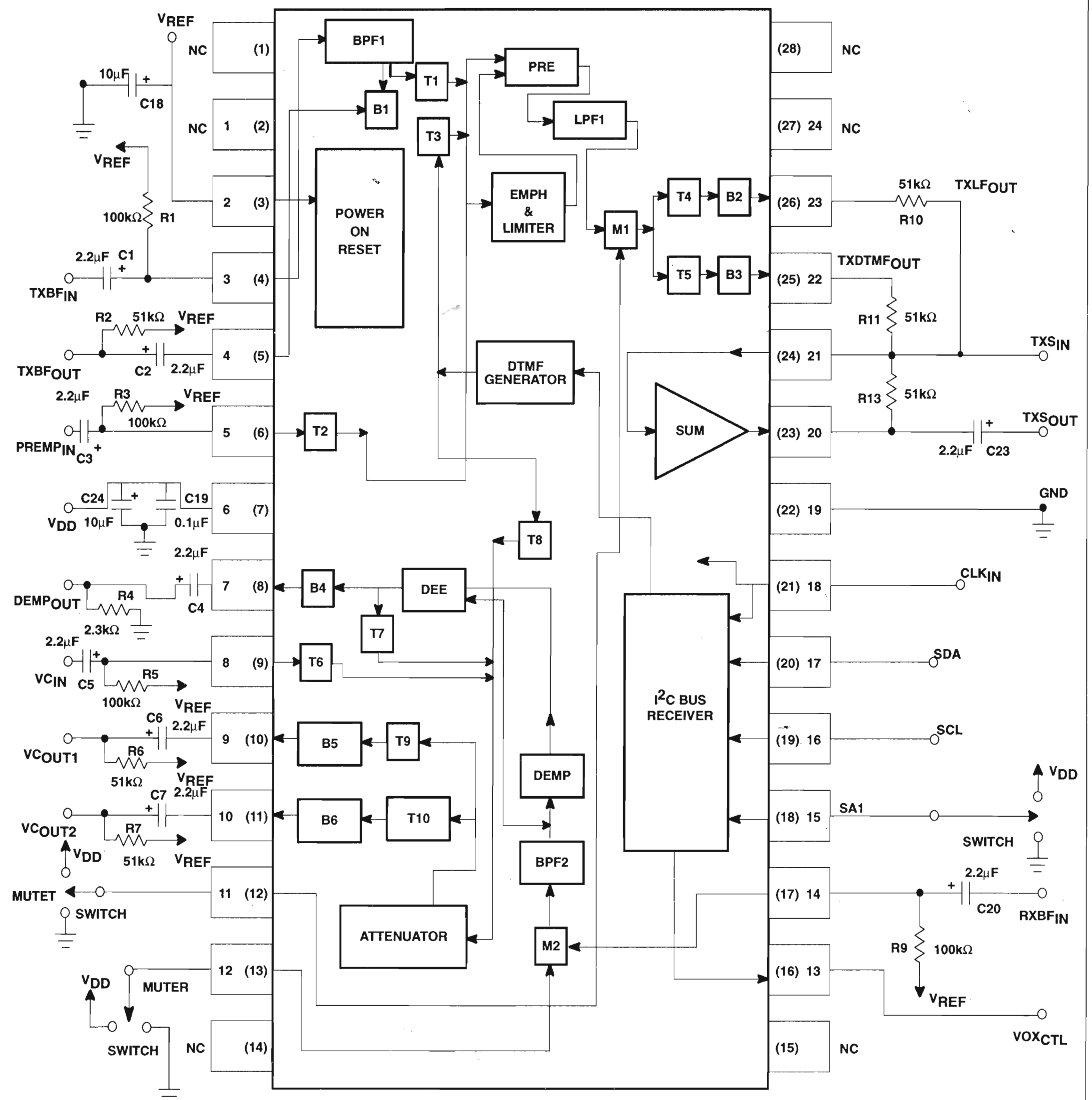
Table 10 can be used to help the designer program the DTMF generator.

There are a few key points that should not be overlooked when programming the NE5751. The control registers consist of the

1. Register map
2. Signal path register
3. Volume control and test register
4. High tone DTMF register
5. Low tone DTMF register

To generate a single tone from the DTMF generator, use the appropriate registers (high or low DTMF) and load the other one with a '0', '1', or '2' to silence it.

The order of these registers is important. If the programmer wanted to turn down the volume, he/she would have to re-program the register map, signal path, and then give the new data to the volume control and test register.



R10	Input resistor for summing amp out can be used to set gain of signal Input
R11	Resistor for summing amp out can be used to set gain of DTMF feedback
R13	Resistor for sum amp can be used to set gain of all the inputs Used to bias up

R1
R2
R3
R4
R5
R6
R7
R9
} Used to bias respective pins to 2.5V by connecting the other end of the resistor to the V_{REF} pin without loading down the V_{REF} source

C18	Used to AC GND V_{REF} pin
C19	Power supply bypass cap
C20	DC blocking cap for Rec input
C23	DC blocking cap for sum amp out
C24	Power supply bypass cap

C1
C2
C3
C4
C5
C6
C7
} Provides DC blocking for the respective pins

Figure 24. NE/SA5751 Test and Application Circuit

Table 10. **Maximum Frequency Deviation Results for the 12kHz Test**

Number Dialed	High Freq.	Low Freq.	DTMF HI	DTMF LO
1	1209	697	A5	8F
2	1336	697	96	8F
3	1477	697	87	8F
4	1209	770	A5	82
5	1336	770	96	82
6	1477	770	87	82
7	1209	852	A5	75
8	1336	852	96	75
9	1447	852	87	75
0	1336	941	96	6A
*	1209	941	A5	6A
#	1477	941	87	6A

IV. APROC DEMO-BOARD

About the APROC demo-board:

The NE5750/51 demo-board layout can be seen in Figures 30, 31, and 32. It incorporates the use of DIP packages. However, an SO adapter could be made to test the SO APROC chips.

A separate board is used to interface the APROC demo-board with the computer's parallel port. This converter utilizes the 74LS05 as a buffer scheme.

An I^{2}C program for the APROC is provided so that a designer can easily program and evaluate the chip set. This eliminates the need to write an evaluation program. However, it does not eliminate the need for a final system program.

The evaluation program has a graphic display that shows the transmit and receive path of the APROC on the terminal, as seen in Figure 33. By selecting a function, one can toggle the space bar on the key board to turn on or off any key features. The designer could also type in the codes for any registers to control the functions.

Figure 25 shows how the interface board and the demo-board can be used in conjunction with a computer. Once everything is connected properly, one can make his own evaluations on the chip set.

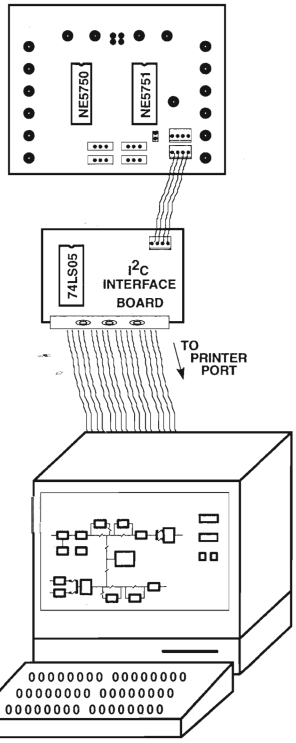


Figure 25. Interfacing the APROC Demo-board with the I^{2}C Evaluation Program

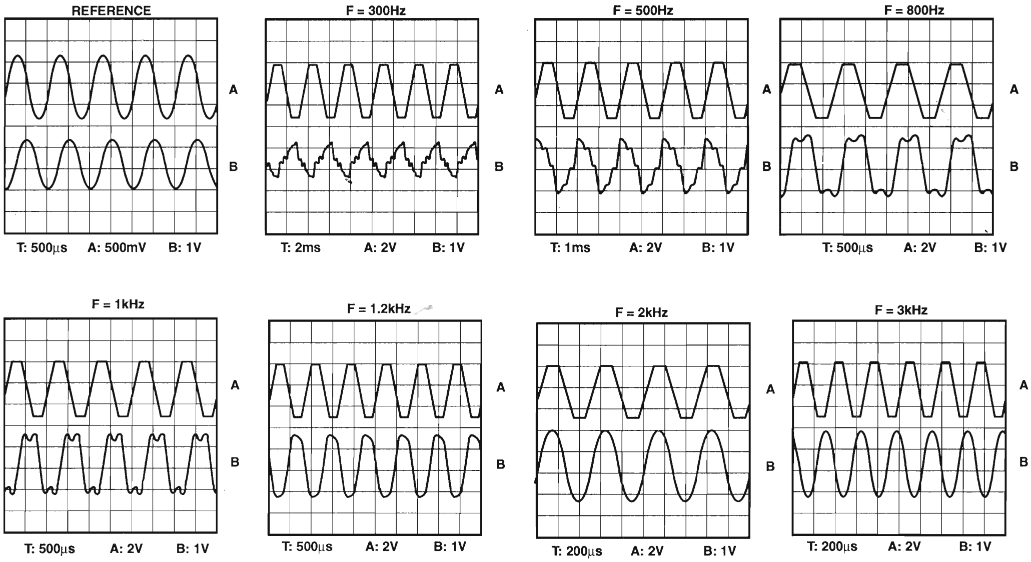


Figure 26. Results From the 12kHz Maximum Frequency Deviation Test

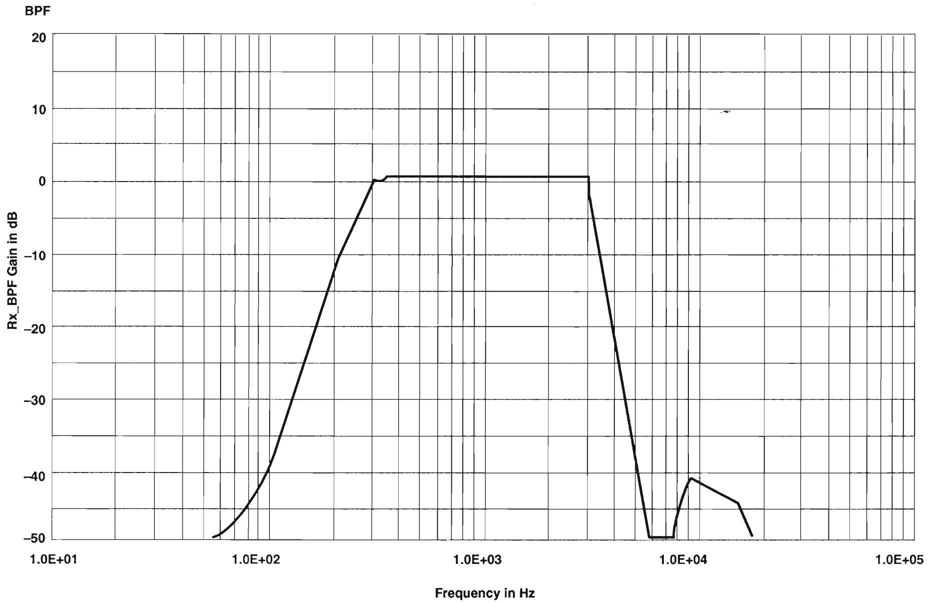


Figure 27. NE5751 Rx Bandpass Filter

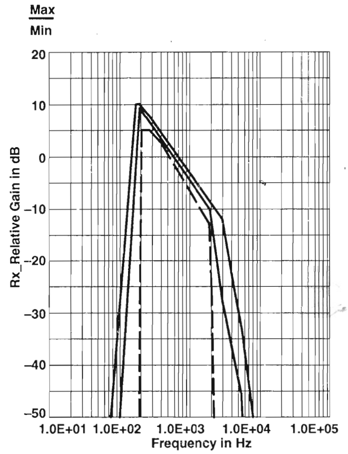


Figure 28. NE5751 Rx De-emphasis

How to Power Down on the NE5750/51 Demo-Board:

In general, power down mode is a condition where a system has just enough power to "stay alive" and, therefore, is not expected to be fully operational. When called upon, the system can quickly get out of this mode and into the power up mode and be ready to perform its functions. This fast reaction time is possible because all of the capacitors have maintained their charges. This is because power was not cut-off completely. The power down function reduces overall current consumption when the system is not fully operational, and is especially helpful when the system is operating from a battery powered source.

There are three power down conditions when we refer to to the NE5750/51 demo-board. They are listed and described as follows:

1. NE5750 Power Down

Purpose:

- to reduce current consumption

- to maintain all DC voltages on the device pin to keep the capacitors charged

How To:

- use hardware switch on demo-board which forces Pin 10 to ground

- or use a CMOS logic output into Pin 10

Benefits:

- reduces current consumption while maintaining readiness

- current drops from 8.4mA to 1.8mA (typically)

Mode of Operation:

- Everything is semi-functional, although performance is not, and will not be, guaranteed

2. NE5751 Power Down

Purpose:

- to reduce current consumption

- to maintain all DC voltages on the device Pin to keep the capacitors charged up

- to open all voice paths so that no signals will flow

How To:

- program the I^{2}C bus under the condition that all registers are set to zero

Benefits:

- all the registers are always at zero when powering up from the power down mode

- reduces current consumption while maintaining readiness

- current drops from 2.7mA to 1.1mA (typically)

Mode of Operation:

- Everything is semi-functional, although performance is not, and will not be, guaranteed

3. Chip-Set Power Down

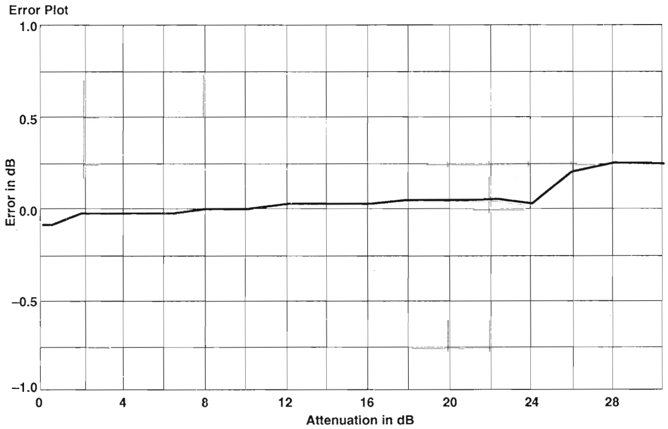


Figure 29. NE5751 Attenuation Error

Definition:

-the NE5750 and NE5751 demo-board is in the power down mode when:

1. The transmitter and receiver are muted on the NE5751
2. The NE5751 is powered down (all registers are set to zero), and
3. The NE5750 is powered down

How to Power Down the Chip-Set Properly (1st Choice):
Please follow this recommended sequence;

1. Mute both the transmitter and receiver on the NE5751.
2. Program the following registers as follows:

Signal Path Register: 00000000

Volume Control Register: 00000000

High DTMF Register: 00

Low DTMF Register: 00

3. Power Down the NE5750.

How to Simulate the Power Down on the Chip-Set (2nd choice)*
Please follow this recommended sequence;

1. Program the following registers as follows:

Signal Path Register: 00010000

Volume Control Register: 01100000

High DTMF Register: 00

Low DTMF Register: 00

2. Power Down the NE5750

*NOTE: this method is only used when the NE5751 mute switches are not accessible, by design.

Comments

1. Muting both the transmitter and receiver on the NE5751 can be done by the two "hardware" switches on the demo-board (forces Pins 11 and 12 to V_{CC}).
2. Powering down the NE5751 can be done by programming the correct assigned register to zero (For more details, consult the NE5751 data sheet).
3. Powering down the NE5750 can be done by the "hardware" switch on the demo-board (forces Pin 10 to ground).
4. When coming out of the power down mode to the power up mode, reverse the procedure given above.
5. If functions are activated while in the power down mode before power up occurs, the "chip-set power down" is no longer valid.
6. We recommend that a 2.2µF capacitor be placed between the NE5751 de-emphasis output to the NE5750 expandor input. The purpose of this capacitor is to block any DC offset that might occur between the two chips while in the power down mode. If this capacitor is not used, an abnormal reaction might occur where white noise is generated.

V. NE5750 DEMO-BOARD

Figure 34 shows the layout for the NE5750 demo-board. This board can be used to evaluate the NE5750, alone, and allows the designer to do extensive testing without having to worry about other external factors. Again, this board makes use of dip packages only. However, a SO adapter can be made to implement the SO version of the NE5750.

VI. QUESTION AND ANSWER SECTION

NE5750 and NE5751 (APROC):

Q: Is it OK to connect the V_{REF} pins together for the NE5750 and NE5751? My circuit seems to be working properly.

A: No, this is not a good idea. Although both V_{REF}s are at 2.5V ($V_{REF} = V_{CC}/2$), there is no guarantee that they will be exactly equal over temperature. One of the V_{REF}s might influence the function of the other chip which, in turn, might have a detrimental effect on the performance of the chips.

Q: Will the APROC chip set work for TACS, NMT or NAMPS specifications as it does for AMPS specification?

A: The APROC was designed to meet AMPS and TACS specifications, however, as it stands now, the chip set will also meet the NAMPs requirements. The chip set will not work for NMT specifications.

Q: In the power down mode, is it OK to program the DTMF registers before powering up?

A: No. This will break the rules of powering down. All the registers are set to zero in this mode. Please review the section on powering down the chip set properly.

NE5750:

Q: Even though I have all the required external components in place on Pins 1,2,3,4,5,6 and 7, my VOX circuit does not work. What is wrong?

A: The VOX circuit is not a trivial connection. Even though all the components are connected, be sure that the output of the NE5750 noise canceller is AC coupled to the input of the compressor to complete the VOX loop. This holds true if the NE5750 is used alone. However, if the NE5751 is used make sure that the signal is fed from the band-pass filter to the input of the NE5750 compressor input. For further advice, please read example 1 in the "setting the threshold" section of this application note.

Q: Do I have to use I^2C if I use the NE5750 alone?

A: No, the NE5750 can be used by itself and does not require the use of I^2C.

Q: Can I speed up the release time of the compressor?

A: Not directly. The release time is dependent on the attack time setting. Once the attack time is set by C11 on Pin 22 of the NE5750, the release time is set internally to be four times slower. So to increase the release time requires that the attack time be increased. One should be careful because setting the attack time too fast could cause more distortion on the output.

Q: The NE5750 compressor input impedance is around 50kΩ. Why is this impedance higher than that of others in your family of compandors?

A: The NE5750 was designed to be compatible with the NE5751. The NE5750 compressor input was modified to accept CMOS driven outputs like the NE5751. This internal modification eliminates the need for an external buffer.

NE5751:

Q: Can I change the filter characteristics?

A: Yes, by changing the master clock input frequency the 3dB points will be effected. For example, if F=1.2MHz, then BPF1=3kHz. Now, if F=600kHz, BPF1=1.5kHz; and if F=2.4MHz, BPF1=6kHz. This type of application is not recommended because the part was not designed to be used this way and, therefore, performance will not be guaranteed. Additionally, the DTMF generator will be off in frequency from the calculated values because of the assumption of a 1.2MHz clock, and the I^2C interface will not be functional.

Q: Besides I^2C, can I communicate to the NE5751 with another type of operating scheme?

A: Yes, by bit banging. Instead of using the I^2C hardware one can supply the clock and data defined in the I^2C protocol software. But this takes up a lot of memory, therefore, it is preferable to implement the I^2C hardware.

Q: The limiter seems to work when I overdrive the input with a strong signal. However, when I try to pass DTMF tones, the limiter's level varies when switches T3/T5 and T4 are set to different settings Why is this? Isn't the output supposed to stay constant regardless of the input being overdriven or passing DTMF tones?

A: Yes, the limiter should hold the output constant when an overdriven signal is applied, but only when the switches are used properly. When passing DTMF tones, T1, T2, and T4 should be left open, while T3/T5 are closed. The voice path should be disconnected when DTMF tones are being passed. Hence, T3/T5 should be left open when DTMF is not used.

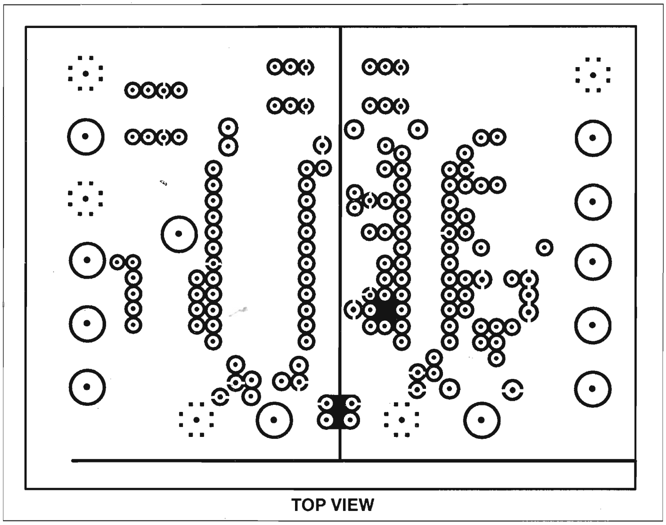
Q: When I program a DTMF tone, it only stays on for 96ms. How can I make it stay on longer?

A: The way to make it stay on longer than 96ms is to re-load the DTMF registers (re-program the DTMF registers before 96ms expires).

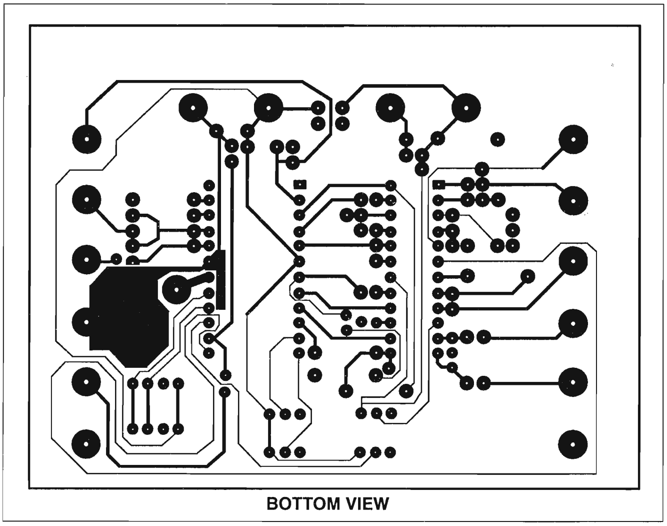
REFERENCES:

"Audio Processing for Cellular Radio or High Performance Transceivers", proceedings of R.F. Expo 1989, A. Fotowat, S. Navid, L. Engh, pp. 195-203.

"Designing Cellular Radios with the Philips Components-Signetics Cellular Chip Set", Cellular Radio Chip Set Design Manual, Feb. 25, 1990.



TOP VIEW



BOTTOM VIEW

Figure 30. Layout of the APROC Demo-board

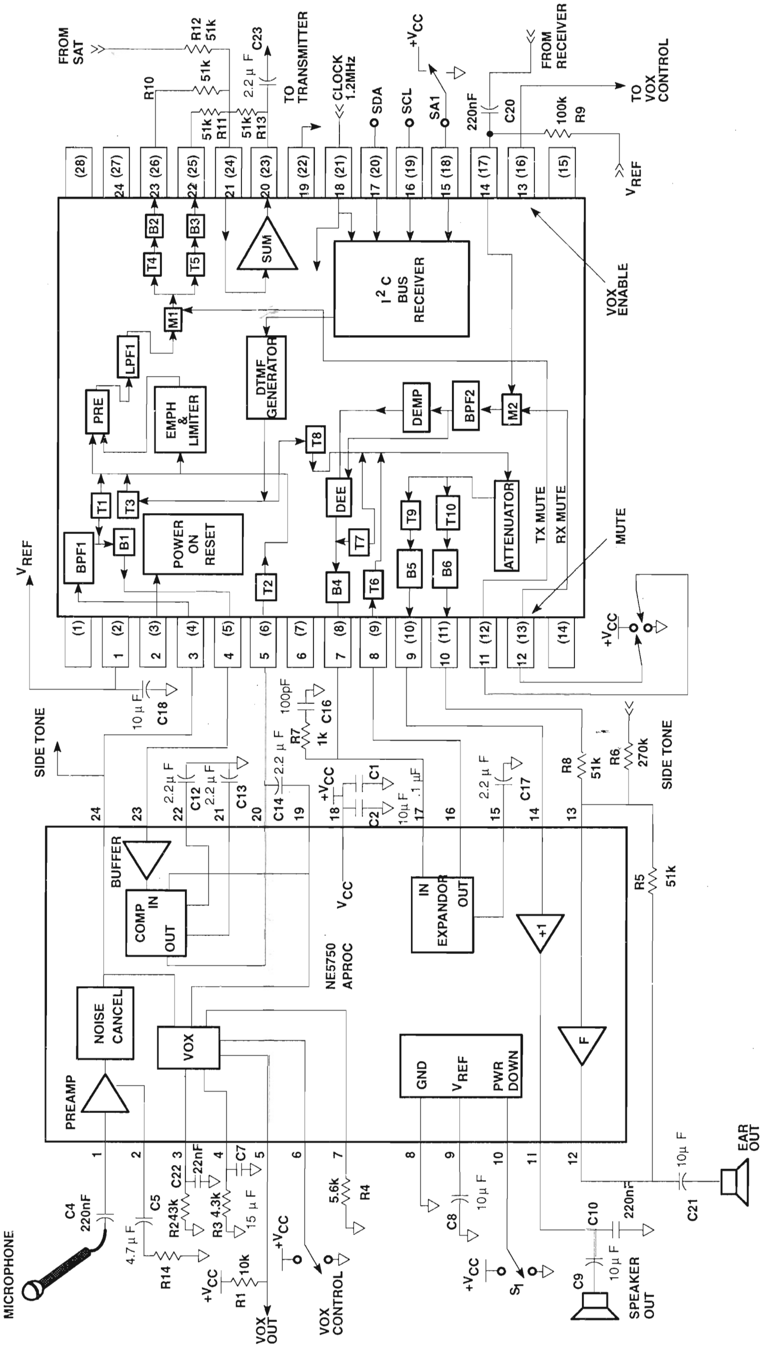
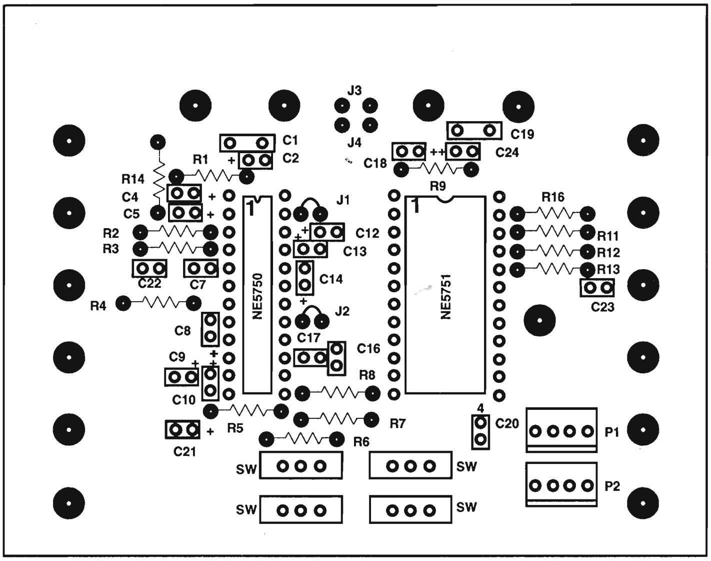


Figure 31. NE5750, NE5751 Cellular Radio Application Circuit



Component Values

C1	0.1µF	R1	10kΩ
C2	10µF	R2	43kΩ
C4	0.22µF	R3	4.3kΩ
C5	4.7µF	R4	5.6kΩ
C7	15µF	R5	51kΩ
C8	10µF	R6	270kΩ
C9	10µF	R7	1kΩ
C10	0.22µF	R8	51kΩ
C12	2.2µF	R9	100kΩ
C13	2.2µF	R10	51kΩ
C14	2.2µF	R11	51kΩ
C16	100pF	R12	51kΩ
C17	2.2µF	R13	51kΩ
C18	10µF	R14	OPTIONAL
C19	.1µF	J1	JUMPER
C20	0.22µF	J2	JUMPER
C21	10µF	IC	NE5750 NARROW 24-PIN SOCKET
C22	.022µF	IC	NE5751 WIDE 24-PIN SOCKET
C23	2.2µF	P1	4 PRONG HEADER
C24	10µF	P2	4 PRONG HEADER
		SW	MINI SLIDE SWITCH

Component Functions

R1	Pull-up resistor for VOX$_{OUT}$ logic levels
R2	Sets gain of VOX, but for internal use only effects voltage on Pin 4
R3	Used to set release time of VOX
R4	Sets threshold level of VOX
R5	Feedback resistor for ear amplifier
R6	Sets gain of ear amplifier for the side tone input
R7	Used in conjunction with C10 to filter out unwanted noise. Optional
R8	Sets gain of ear amplifier
R9	Used to bias up Pin 14 to 2.5V by connecting V$_{THRESH}$ to V$_{REF}$ without loading down V$_{REF}$ source
R10	Input resistor for summing amp out. Can be used to set gain of signal
R11	Input resistor for summing amp out. Can be used to set the gain of the DTMF
R12	Input resistor for summing amp. Can be used to set gain of the side tone input
R13	Feedback resistor for summing amp. Can be used to set gain of all the inputs
R14	Used to set gain of the preamp of NE5750 (OPTIONAL)
J1	JUMPER
J2	JUMPER

C1	Bypass cap for VCC of NE5750
C2	Bypass cap for VCC of NE5750
C4	DC blocking cap for mic input
C5	DC blocking cap for mic gain setting resistor
C7	Used to set attack a release time of VOX
C8	Used to AC ground the V$_{REF}$ pin (5750)
C9	DC blocking cap for speaker out
C10	filter for speaker out
C12	Sets attack and release time of compressor
C13	Used to AC short the DC path for the compressor
C14	Provides AC path to the VOX circuitry
C16	OPTIONAL. Basically to filter out noise
C17	Sets attack and release time for the expandor
C18	Used to AC ground V$_{REF}$ pin (5751)
C19	Bypass cap for V$_{CC}$ of NE5751
C20	DC blocking cap for receiver input
C21	DC blocking cap for ear amplifier output
C22	Sets gain of VOX, internal use only
C23	DC blocking cap for summing amp out
C24	Bypass cap for V$_{CC}$ of NE5751

NOTE: The board is constructed in such a way as to allow a single power supply to power the chip set, or for each chip to be powered by a separate power supply. Using separate power supplies will permit monitoring of current consumption of each part when Jumpers 3 and 4 are removed.

Figure 32. Parts and Function List of APROC Demo-board

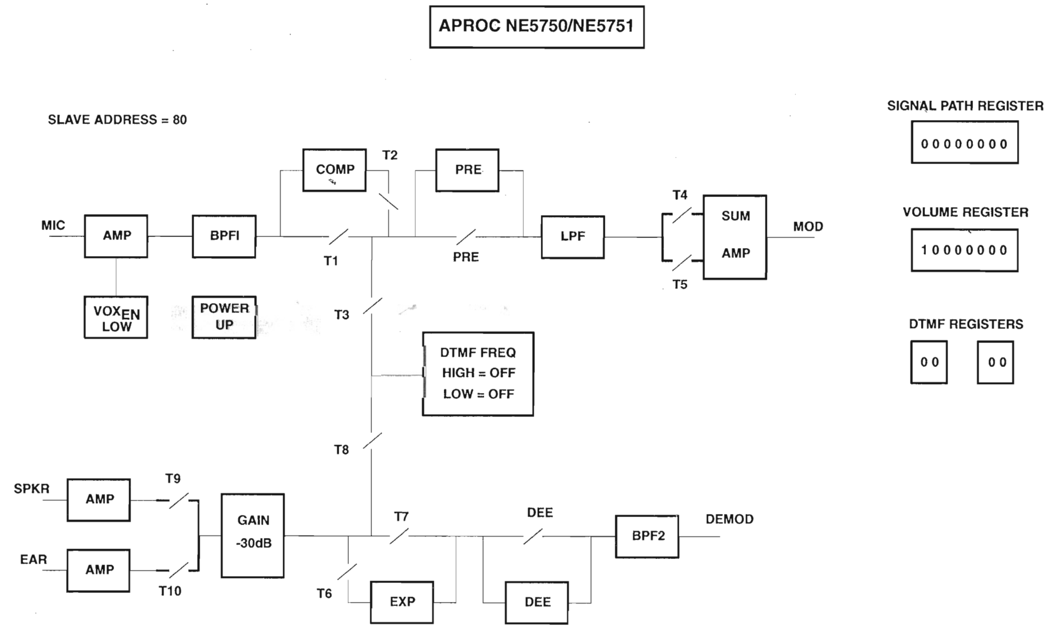


Figure 33. Graphical Display of the I^{2}C Evaluation Program

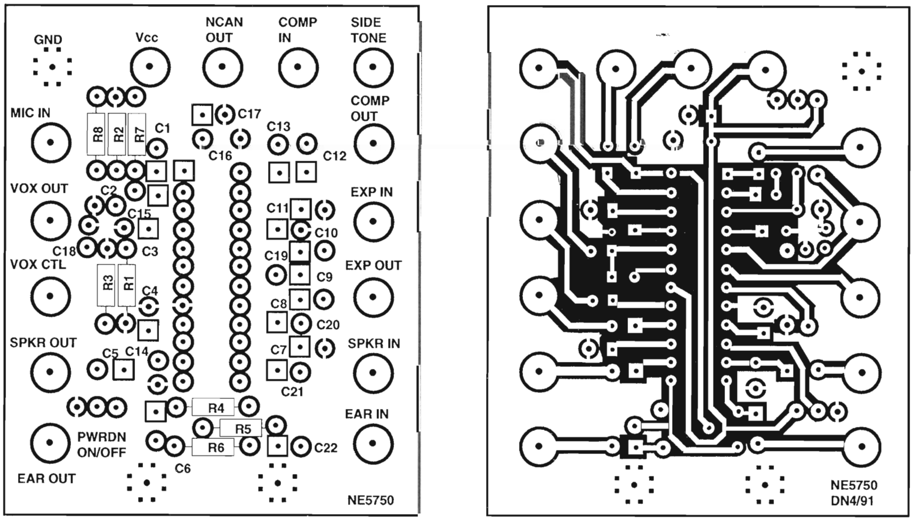


Figure 34. NE5750 Demo-board Layout

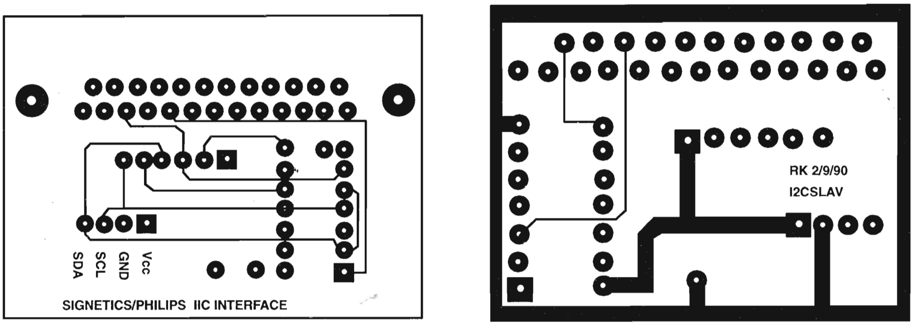

SDA
SCL
GND
Vcc
SIGNETICS/PHILIPS IIC INTERFACE
RK 2/9/90
I2CSLAV

Figure 35.

Audio processor – companding, VOX and amplifier section SA5752

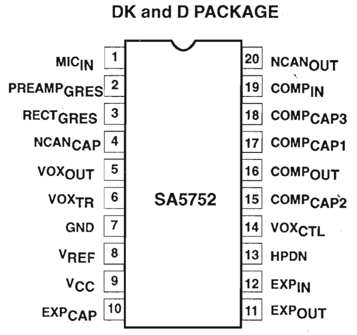
DESCRIPTION

The SA5752 is a high performance low power audio signal processing system especially designed to meet the requirements for small size and low voltage operation of hand-held equipment. The SA5752 subsystem includes a low noise microphone preamplifier with adustable gain, a noise cancellation switching amplifier with adjustable threshold, a voice operated transmitter (VOX) switch, VOX control, an audio compressor with buffered input, audio expandor, and an internal bandgap voltage regulator with power down capability. When used with Philips Semiconductors' SA5753, the complete audio processing function of an AMPS or TACS cellular telephone is easily implemented. The system also meets the requirements of the proposed NAMPS or NTACS specifications. The SA5752 can also be used without the SA5753 in a wide variety of radio communications applications.

FEATURES

- Operating voltage range: 2V to 5.5V
- Miniature SSOP and SO packages
- High performance
- Adjustable VOX and noise cancellation threshold
- Adjustable gain preamplifier
- Audio companding
- ESD protected
- Open collector VOX output
- Logic inputs CMOS compatible
- Power down mode
- Few external components
- Meets AMPS/TACS/NAMPS/NTACS requirements

PIN CONFIGURATION



BENEFITS

- Very compact applications
- Long battery life in portable equipment
- Complete cellular audio function with the SA5753

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

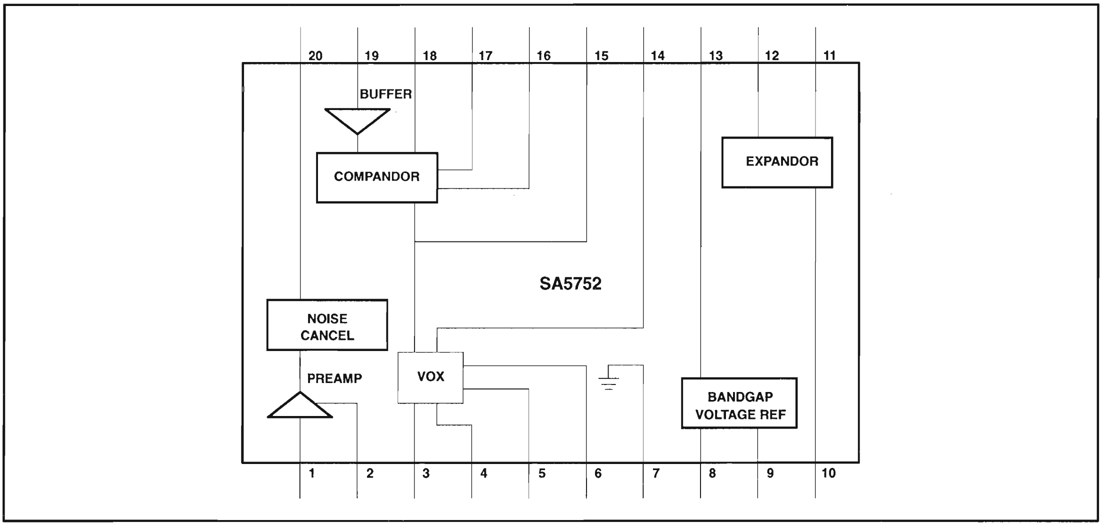
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) package	-40 to +85°C	SA5752D	0172D
20-Pin Plastic Shrink Small Outline Package (SSOP)	-40 to +85°C	SA5752DK	1563

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	MIC_{IN}	Microphone input
2	$PREAMP_{GRES}$	Preamplifier gain resistor
3	$RECT_{GRES}$	Rectifier gain resistor
4	$NCAN_{CAP}$	Noise cancellation timing capacitor
5	VOX_{OUT}	Voice operated transmission output
6	VOX_{TR}	Voice operated transmission threshold resistor
7	GND	Ground
8	V_{REF}	Reference voltage
9	V_{CC}	Positive supply
10	EXP_{CAP}	Expandor timing capacitor
11	EXP_{OUT}	Expandor output
12	EXP_{IN}	Expandor input
13	HPDN	Hardware power-down
14	VOX_{CTL}	Voice operated transmission control
15	$COMP_{CAP2}$	Compressor capacitor 2 DC block
16	$COMP_{OUT}$	Compressor output
17	$COMP_{CAP1}$	Compressor timing capacitor 1
18	$COMP_{CAP3}$	Compressor capacitor 3 DC block
19	$COMP_{IN}$	Compressor input
20	$NCAN_{OUT}$	Noise cancellation output

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage range	-0.3 to 6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC}+0.3)	V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Ambient operating temperature	-40 to +85	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +3.0V, 0dB = 77.5mV$_{RMS}$. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		2.7[4]	3.0	5.5	V
I_{CC}	Supply current	No signal Power down mode		3.1 125	4.0	mA µA
Z_L	Load impedance pins $NCAN_{OUT}$, EXP_{OUT}		50			kΩ
	$COMP_{OUT}$[1]		10			kΩ
Z_{IN}	Input impedance $COMP_{IN}$, MIC_{IN}		40	50	60	kΩ
	EXP_{IN}[2]		2.0			kΩ
	Noise cancellation current	Pin 6		25		µA
V_{OS}	DC offset $NCAN_{OUT}$[3]		-50	–3.0	50	mV

NOTES:

1. Compressor is tested in production with 50kΩ load.
2. Not tested in production.
3. Offset values are identical for both gain states of noise reduction circuit.
4. Operational down to V_{CC} = 2V.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +3.0V, 0dB level = 77.5mV$_{RMS}$. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	Preamplifier gain range		0		40	dB
	Preamplifier voltage gain 0dB	Pin 2 open	-1.0	0	1.0	dB
	Preamplifier voltage gain 40dB	Pin 2 AC ground	39.0	40	41.0	dB
	Preamplifier noise density	Pin 2 AC grounded RS = 50kΩ unweighted 20Hz-20kHz		7		nV/√Hz
		weighted CCIR DIN45405 20-20kHz		8		nV/√Hz
	Switch amplifier gain		9	10	11	dB
Compandor 1kHz, all tests[1]						
$COMP_{OUT}$	Compressor error at -21dB output level	Input level = -42dB	–1.0	–0.16	1.0	dB
$COMP_{OUT}$	Compressor error at -10dB output level	Input level = -20dB	-1.0	–0.11	1.0	dB
$COMP_{OUT}$	Compressor error at 0dB output level	Input level = 0dB	-1.5	+0.1	1.5	dB
$COMP_{OUT}$	Compressor error at +5dB output level	Input level = +10dB	-1.0	+0.04	1.0	dB
$COMP_{OUT}$	Compressor error at +10dB output level	Input level = +20dB	-1.0	+0.02	1.0	dB
EXP_{OUT}	Expandor error at -42dB output level	Input level = -21dB	–1.0	–0.12	1.0	dB
EXP_{OUT}	Expandor error at -21dB output level	Input level = -10.5dB	-1.0	+0.1	1.0	dB
EXP_{OUT}	Expandor error at -10dB output level	Input level = -5dB	-1.0	+0.03	1.0	dB

AC ELECTRICAL CHARACTERISTICS (Contineud)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
EXP_{OUT}	Expandor error at 0dB output level	Input level = 0dB	-1.5	–0.2	1.5	dB
EXP_{OUT}	Expandor error at +10dB output level	Input level = +5dB	-1.0	+0.03	1.0	dB
EXP_{OUT}	Expandor error at +20dB output level[2]	Input level = +10dB	-1.0	–0.1	1.0	dB
EXP_{OUT}	Expandor V_{OS}	No signal	-50.0	+3.0	50.0	mV
EXP_{OUT}	Expandor output DC shift	No signal to 0dB	-100	+2.0	100	mV
	Timing capacitors compandor			2200		nF
THD	Total harmonic distortion Compressor	1kHz, 0dB BW=300-3kHz		0.2	1	%
	Expandor	1kHz, 0dB BW=300-3kHz		0.1	1	%
	$NCAN_{OUT}$	1kHz. Pin 2 open output level = 0dB		0.02	1	%
		1kHz, Pin 2 open output level = +20dB		0.06	1	%
VOX_{OUT}	Sink current				0.5	mA
	Low level	Open collector I_L = 0.5mA			0.4	V
	High level			V_{CC}		V
VOX_{CTL}	Input current Low		-50	–6.6	0	µA
	High		-10	–0.02	+10	µA
	Input level Low		0		$0.3V_{CC}$	V
	High		$0.7V_{CC}$		V_{CC}	V
H_{PDN}	Input current Low		-10	–4.1	+10	µA
	High		-10	–0.2	+10	µA
	Input level Low		0		$0.3V_{CC}$	V
	High		$0.7V_{CC}$		V_{CC}	V
	Reference filter capacitor			10		µF

NOTE:
1. Measurements are relative to 0dB output.
2. Measurement is indicative of the output dynamic range capability.

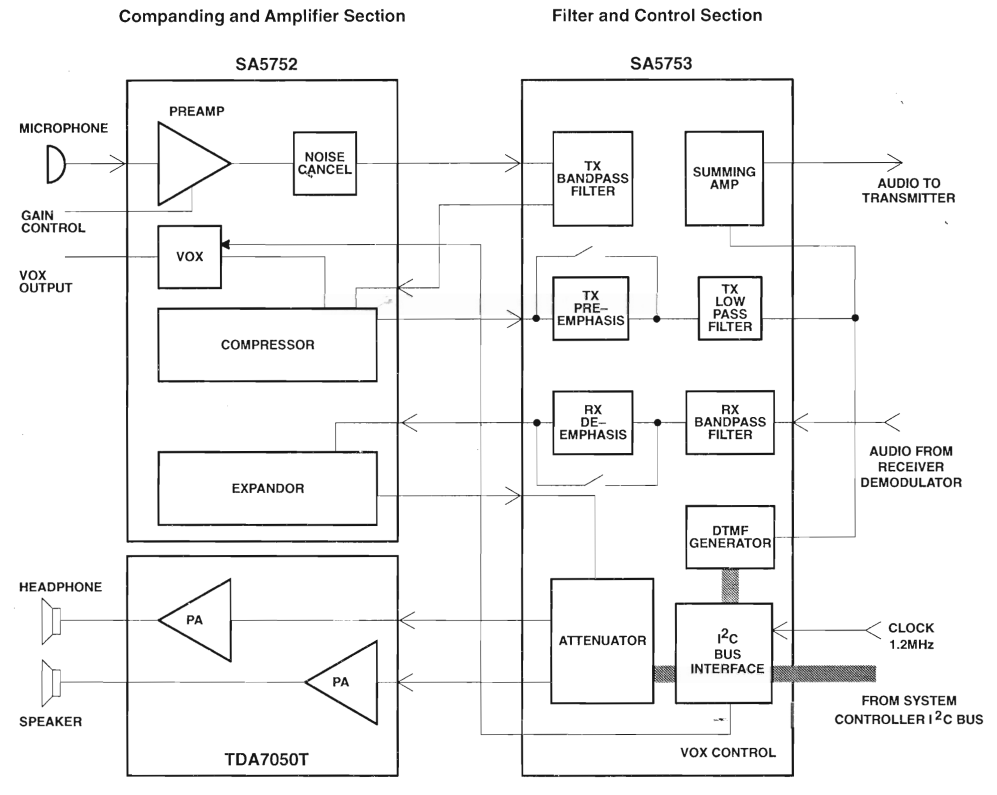


Figure 1. Typical Configuration of Audio Processor (APROC) System Chip Set

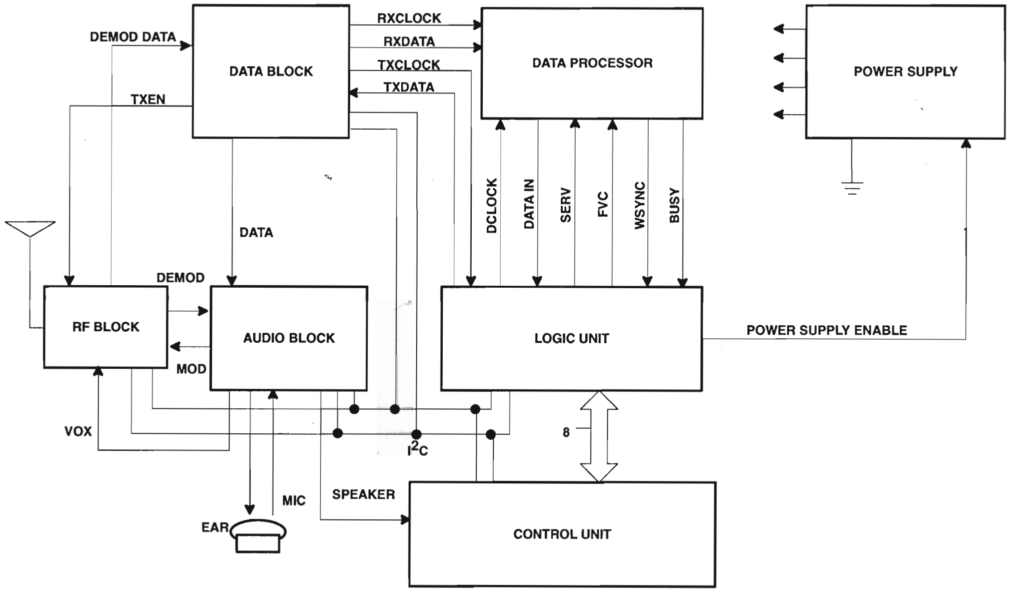


Figure 2. Cellular Radio System

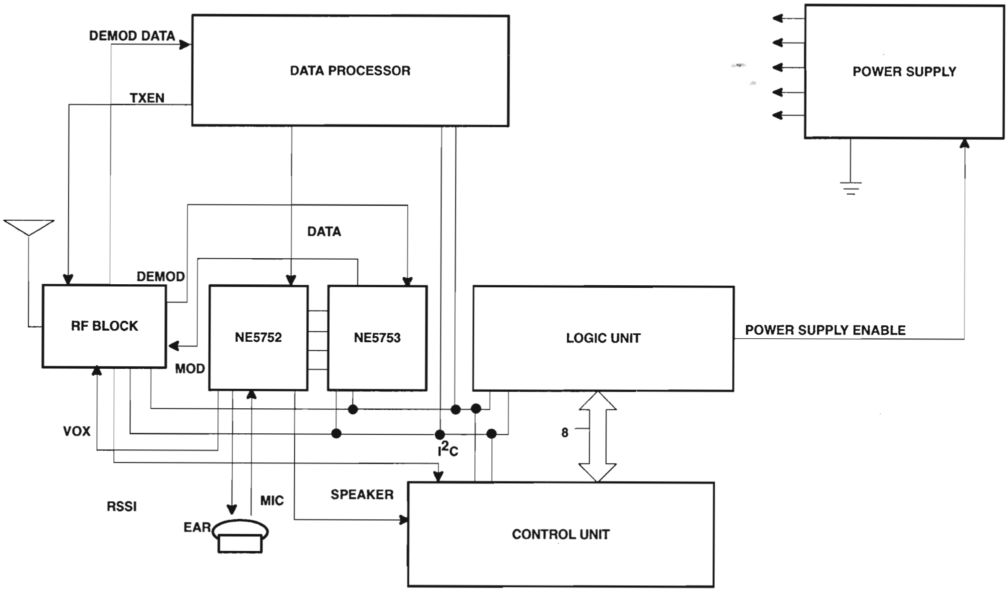


Figure 3. APROC Application Diagram

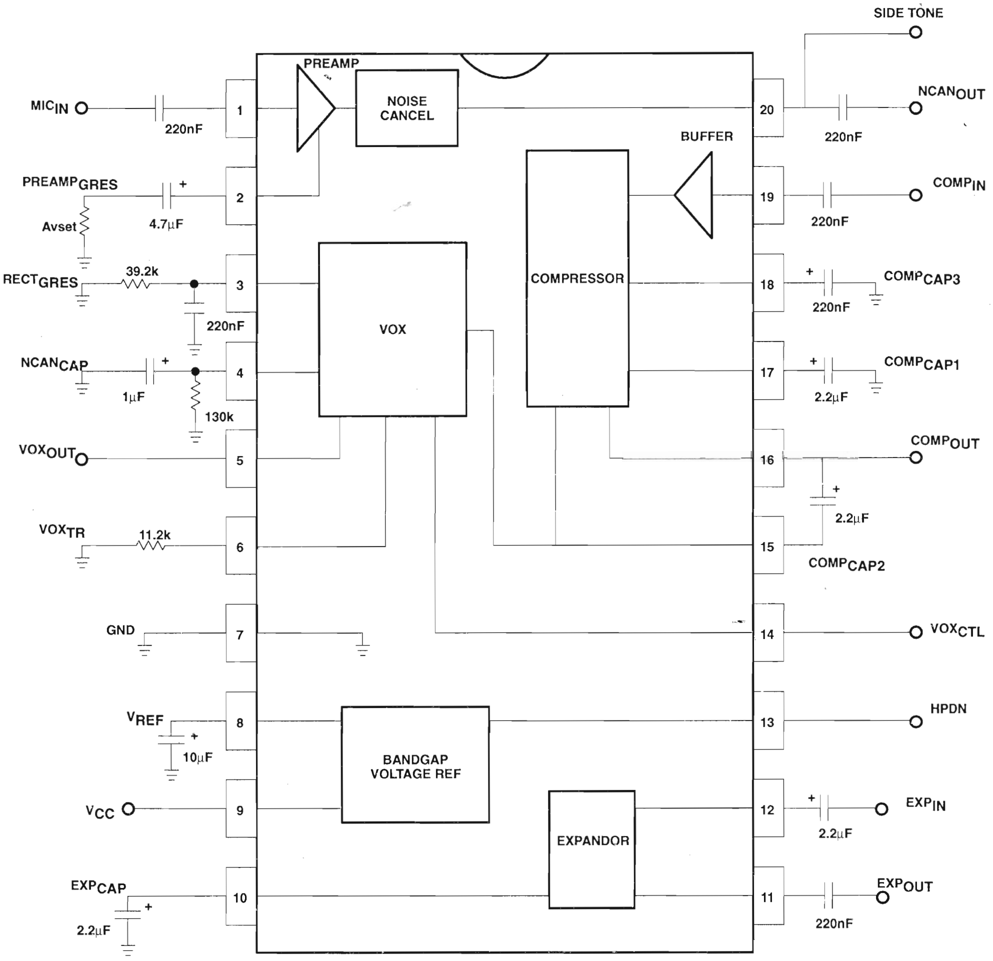


Figure 4. SA5752 Test and Application Circuit

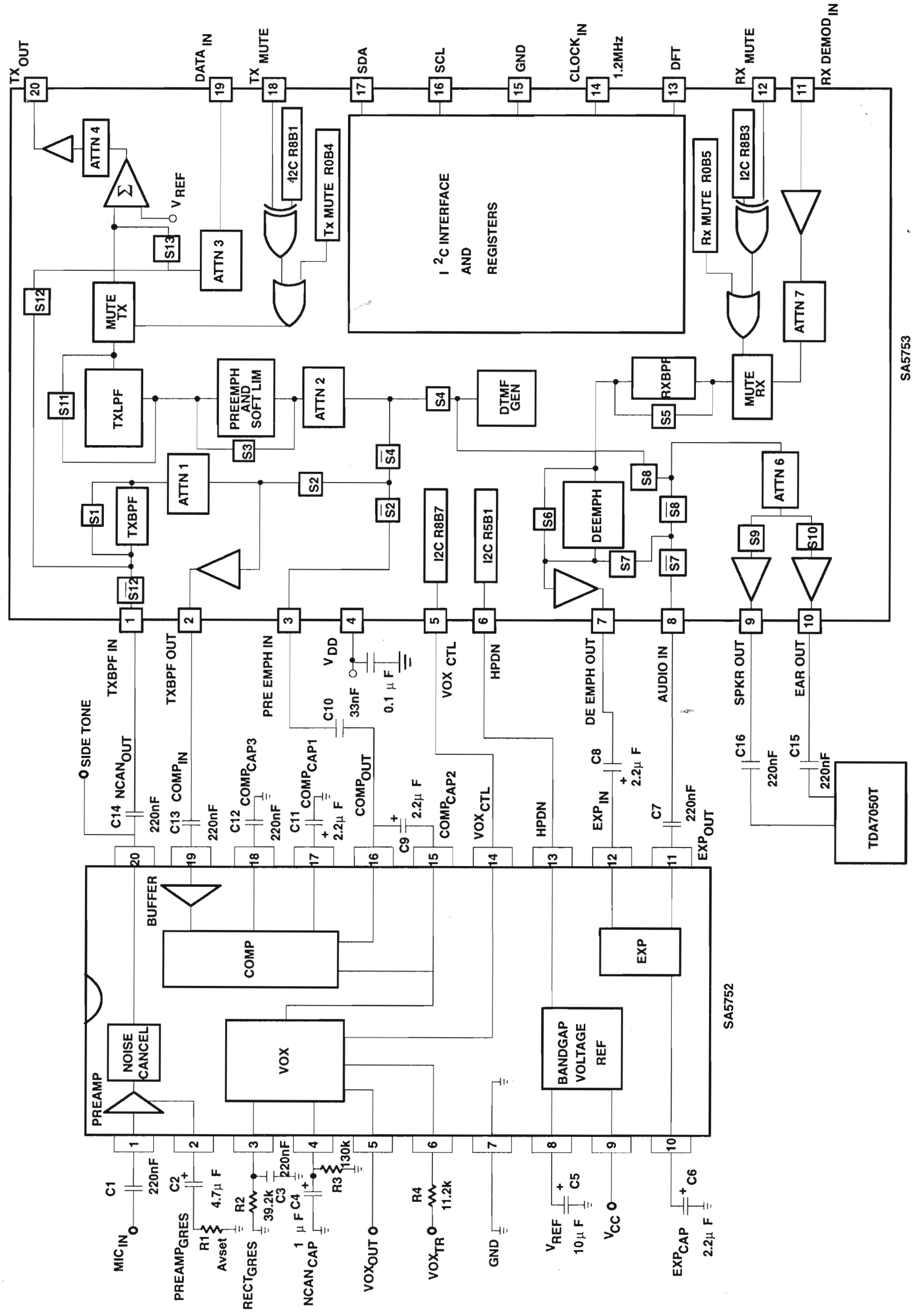
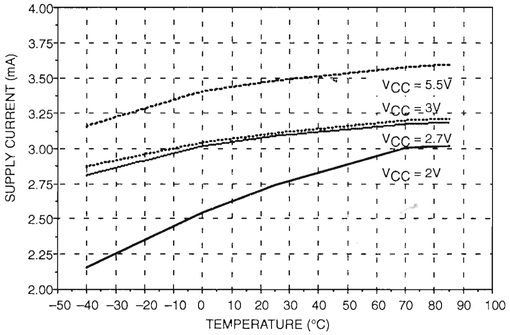


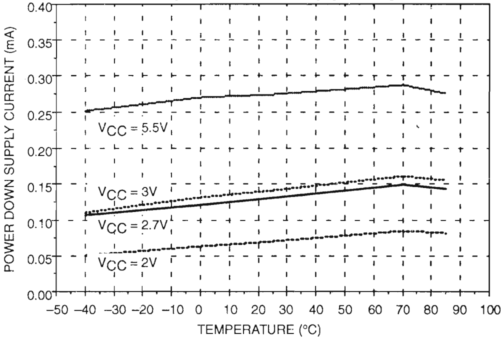
Figure 5. Application Diagram for the Audio Processor

TYPICAL PERFORMANCE CHARACTERISTICS

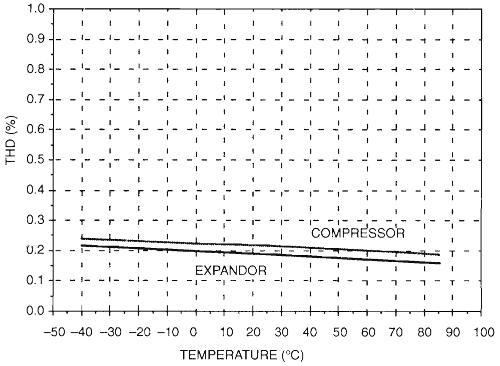
Supply Current vs Temperature and Supply Voltage



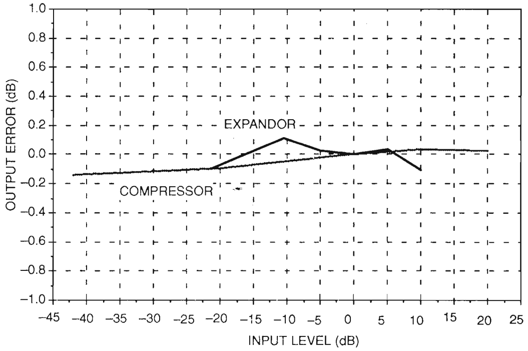
Power Down Supply Current vs Temperature and Supply Voltage



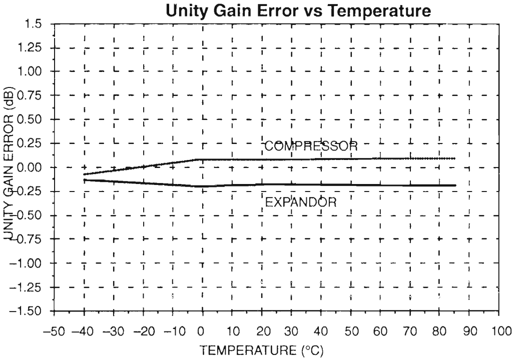
THD vs Temperature for 3V Supply



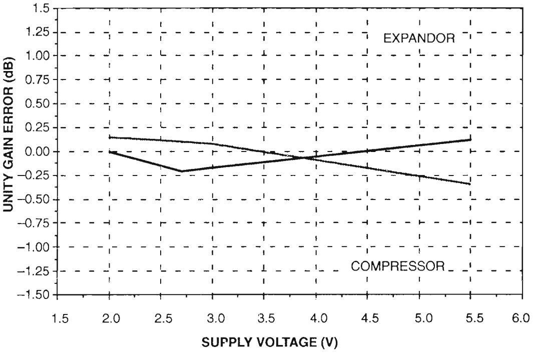
Compandor Tracking Error vs Input Level



Unity Gain Error vs Temperature



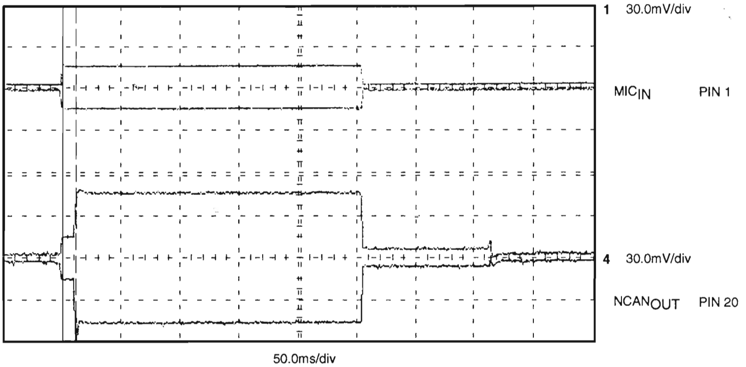
Unity Gain Error vs Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Noise Cancellation Switching Amplifier

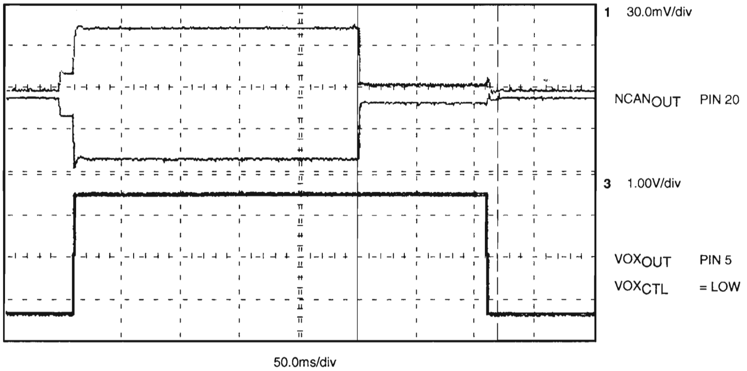
DYNAMIC RESPSONSE



STOP MARKER: 11.960 ms
START MARKER: 0.00000 s
Δt: 11.960 ms

Voice Activated Transmitter (VOX)

DYNAMIC RESPSONSE



STOP MARKER: 120.000 ms
START MARKER: 0.00000 s
Δt: 120.000 ms

Audio processor – filter and control section SA5753

DESCRIPTION

The SA5753 is a high performance low power CMOS audio signal processing system especially designed to meet the requirements for small size and low voltage operation of hand-held equipment. The SA5753 subsystem includes complementary transmit/receive voice band (300-3000Hz), switched capacitor bandpass filters with pre-emphasis and de-emphasis respectively, a transmit low pass filter, peak deviation limiter for transmit, digitally controlled attenuators for signal level and volume control, audio path mute switches, a programmable DTMF generator, power-down circuitry for low current standby, power-on reset capability, and an I^{2}C interface. When the SA5753 is used with an SA5752 (companding function), the complete audio processing system of an AMPS, TACS, NAMPS or NTACS cellular telephone is easily implemented.

The system also meets the requirements of the proposed NAMPS or NTACS specification, and can be used in cordless telephone applications.

The SA5753 can be operated without the I^{2}C bus interface by pulling DFT (Pin 13) HIGH.

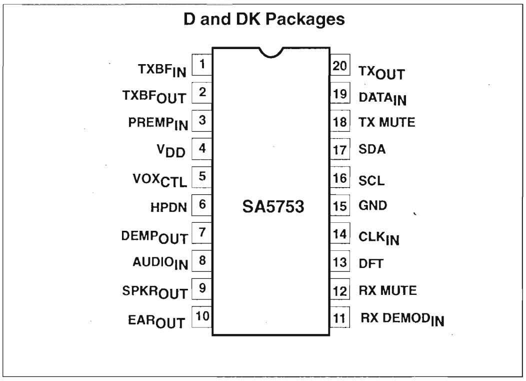
BENEFITS

- Very compact application
- Long battery life in portable equipment
- Complete cellular audio function with the SA5752

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

PIN CONFIGURATION



FEATURES

- Low 3V supply
- Miniature SSOP package
- Low power
- High performance
- Built-in programmable DTMF generator
- Built-in digitally controlled attenuators for modulation and volume control
- Built-in peak-deviation limiter
- I^{2}C Bus controlled
- Power-on reset
- Power down capability
- Programmable mute control
- Meets AMPS/TACS/NAMPS/NTACS requirements

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) Package	-40 to +85°C	SA5753D	0172D
20-Pin Plastic Shrink Small Outline Package (SSOP)	-40 to +85°C	SA5753DK	1563

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Power supply voltage range	-0.3 to 6	V
V_{IN}	Voltage applied to any other pin	-0.3 to V_{DD}+0.3	V
	Storage temperature	-65 to +150	°C
T_A	Ambient operating temperature	-40 to +85	°C

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	$TXBF_{IN}$	Transmit bandpass filter input
2	$TXBF_{OUT}$	Transmit bandpass filter output
3	$PREMP_{IN}$	Pre-emphasis input
4	V_{DD}	Positive supply
5	VOX_{CTL}	Vox control output
6	HPDN	Power-down I/O
7	$DEMP_{OUT}$	De-emphasis output
8	$AUDIO_{IN}$	Audio input
9	$SPKR_{OUT}$	Audio output to speaker
10	EAR_{OUT}	Audio output to earpiece
11	RX $DEMOD_{IN}$	Rx demodulated audio signal input
12	RX MUTE	RX audio signal mute input
13	DFT	Default input, non-I^2C or stand-alone operation
14	CLK_{IN}	Clock input (1.2MHz)
15	GND	Ground
16	SCL	I^2C serial clock line
17	SDA	I^2C serial data line
18	TX MUTE	Tx audio signal mute input
19	$DATA_{IN}$	Data input
20	TX_{OUT}	Transmit output

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +3.0V, unless otherwise specified. See test circuit, Figure 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{DD}	Power supply voltage		2.7	3.0	5.5[1]	V
I_{DD}	Supply current	Operating IDLE Power Down (PWDN)		2.7 600 200		mA μA μA
I_{IH}	Input current high TX MUTE, RX MUTE, HPDN DFT	$V_{IN} = V_{DD}$	–10 0	0 +10	+10 +30	μA μA
I_{IL}	Input current low TX MUTE, RX MUTE, HPDN, DFT	V_{IN} = GND	–30 –10	–10 0	0 +10	μA μA
V_{IH}	Input voltage high		$0.7V_{DD}$		V_{DD}	V
V_{IL}	Input voltage low		0		$0.3V_{DD}$	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +3.0V. See test circuit, Figure 1. Clock frequency = 1.2MHz; test level = 0dBV = $77.5mV_{RMS}$ = -20dBm, unless otherwise specified. All gain control blocks (Attenuators) = 0dB gain, NAMPS and VCO bits set to 0.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	RX BPF anti alias rejection			40		dB
	RX BPF input impedance	f= 1kHz		100		kΩ
	RX BPF gain with de-emphasis	f = 1kHz	-0.5	0	0.5	dB
	RX BPF gain with de-emphasis	f = 100Hz		-30		dBm0
	RX BPF gain with de-emphasis	f = 300Hz	9.0	9.6	11.0	dBm0
	RX BPF gain with de-emphasis	f = 3kHz	-11.0	-10.0	-9.0	dBm0
	RX BPF gain with de-emphasis	f = 5.9kHz		-58		dBm0
	RX BPF noise with de-emphasis	300Hz-3kHz		200		μV_{RMS}
	RX dynamic range	with deemphasis		80		dB
	$DEMP_{OUT}$ output impedance	f = 1kHz			40	Ω
	$DEMP_{OUT}$ output swing (1%)	2kΩ to $V_{DD/2}$; f = 1kHz		2.4		V_{P-P}
	$SPKR_{OUT}$ ouput swing (1%)	50kΩ to$V_{DD/2}$; f = 1kHz	V_{DD} -1	2.4		V_{P-P}
	EAR_{OUT} output swing (1%)	50kΩ to $V_{DD/2}$; f = 1kHz	V_{DD} -1	2.4		V_{P-P}
	$SPKR_{OUT}$ noise / EAR_{OUT} noise			200		μV_{RMS}
	CLK_{IN} high		2.1		3.0	V
	CLK_{IN} low		0		1.0	V
	TX BPF anti alias rejection	f > 50kHz		40		dB
	TX BPF input impedance	f = 3kHz		100		KΩ
	TX BPF noise	300 - 3000kHz		200		μV_{RMS}
	TX LPF gain	f = 5.9kHz		-39	-36	dBm0
	TX LPF gain with pre-emphasis	f = 1kHz, 0dBV		2.43		dB
	TX LPF gain with pre-emphasis	f = 100Hz		-19		dBm0
	TX LPF gain with pre-emphasis	f = 300Hz		-10.45		dBm0
	TX LPF gain with pre-emphasis	f = 3kHz		9.14		dBm0
	TX LPF gain with pre-emphasis	f = 5900Hz		-28		dBm0
	TX LPF gain with pre-emphasis	f = 9kHz		-48		dBm0
	TX overall gain	1kHz		2.43		dB
	TX overall gain	100Hz		-58	-45	dBm0
	TX overall gain	300Hz	-11	-10.4	-9	dBm0

NOTES:

1. Tx noise performance is optimized for operation with $V_{CC} \leq 4.2V$.

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	TX overall gain	3kHz	8	9	9.6	dBm0
	TX overall gain	5.9kHz		-52	-45	dBm0
	TX BPF dynamic range			TBD		dB
	$PREMP_{IN}$ input impedance	f = 3kHz		100		kΩ
	TX_{OUT} Slew rate Output impedance Output swing (limiting) Output swing (1% THD)	C_L = 15pF f = 3kHz 5kΩ load (25°C)		0.75 1.2 1.0	 40 	V/µs Ω V_{P-P} V_{P-P}
	Tx DTMF signal with TXLPF and pre-emphasis			0.45		V/kHz
	Rx DTMF sidetone		--0.8		5.2	dBm0
	Time delay to mute from RX MUTE or TX MUTE transition	$V_{IN} = V_{IL}$ to V_{IH} $V_{IN} = V_{IH}$ to V_{IL}		0.5 0.5		µs µs

Table 1. Gain Control Blocks (Bit 0 is Least Significant Bit)

SYMBOL	Bits	TYPICAL STEP (dB)	TYPICAL GAIN (dB)	
			MIN	MAX
A1	4	–0.8	–12.0	0
A2a	5	±0.25	–3.75	+3.75
A2b	2	–6, (–12 on first)	–24.0	0
A3	4	–1.0	–17.0	–2.0
A4	4	±0.5	–3.5	+3.5
A6	4	–2.0	–30.0	0
A7	4	±0.5	–3.5	+3.5
NAMPS	1		+1.9 in A2b –7.6 in A4	
VCO	1		+6.0 in A4	
For A2a, A4 and A7:		MSB sets the sign of the gain MSB = 0 for gain MSB = 1 for attenuation		
For all Gain Blocks:		All bits set to 0 = 0dB gain All bits set to 1 = maximum gain or attenuation		

FUNCTIONAL DESCRIPTION

The SA5753 is an audio signal processor designed to meet the requirements of compact low voltage radio telephone equipment. It includes transmit and receive bandpass filters for voiceband (300-3000Hz) with pre-emphasis and de-emphasis respectively, a transmit peak deviation limiter, voice channel mute switches and a data path which can be summed into the transmit channel. An I^2C interface is provided for software programmability of a DTMF generator, mute polarity, selection of different power down and operating modes and control of the gain in both the transmit and receive channels.

Software programmable gain control allows the device to be automatically optimized during equipment production and offers flexibility during normal operation.

Gain Blocks

The programmable gain blocks are shown in Table 1 and Figure 1. The purpose for each block is as follows:

a. A1 compensates for microphone gain variations in the transmit path.

b. A2a compensates for transmitter dynamic range variations due to manufacturing tolerances of the SA5753 and SA5752 compandor companion device. To meet AMPS requirements, the dynamic range between the zero crossing signal level of the compandor and the peak signal allowed by the deviation limiter is adjusted to 12.34dB.

c. A2b allows coarse attenuation to be inserted in the transmit path to eliminate positive feedback effects in hands-free speaker applications. First step is 12dB followed by two steps of 6dB.

d. A3 sets the gain between the $DATA_{IN}$ pin (Pin 19) and the TX_{OUT} pin (Pin 20) and should be adjusted after A2a and A4 have been previously optimized. The SA5753 will interface directly with the UMA1000T data processor (which produces a 2Vpk data signal). For NAMPS applications an additional 10 to 14dB resistive divider must be added at the $DATA_{IN}$ pin (Pin 19) for a 2V data signal.

e. A4 compensates for transmit gain variations due to manufacturing tolerances of the SA5753, SA5752 and VCO connected to TX_{OUT} (Pin 20). After A2a has been adjusted to set dynamic range then A4 is used to set the peak output voltage at TX_{OUT} (Pin 20) such that a nominal 10kHz/V VCO produces a peak deviation of 12kHz to meet AMPS specifications.

f. A6 is the volume control for both the $SPKR_{OUT}$ and EAR_{OUT}.

g. A7 compensates for manufacturing tolerances in the SA5753 and preceeding demodulator. For AMPS requirements, a 1kHz tone with 2.9kHz deviation should produce an output signal at $DEMP_{OUT}$ (Pin 7) corresponding to the zero crossing signal level of the expandor.

NAMPS and VCO Offsets

For NAMPS applications, a '1' programmed into R5B3 (register 5, bit 3) will offset the transmit gain for NAMPS applications. It is recommended that A2a and A4 be programmed after the NAMPS option is set to compensate for manufacturing tolerances in the NAMPS offset, itself.

When the VCO bit of R5B2 is a '1', an extra gain of 6dB is provided at TX_{OUT} for direct interface to VCOs with a nominal gain of 5kHz/V.

Operation Using the I^{2}C Communications Bus

The SA5753 includes on-chip gain blocks and options which can be programmed through an I^{2}C interface bus. To use this capability, the DFT pin (Pin 13) must be pulled LOW. In this mode, all signal level adjustments can be made through software with no external potentiometers required.

With DFT pulled LOW, the HPDN pin (Pin 6) is an OUTPUT having the same value as the program bit in register 5 bit 1 (R5B1) of the control register bit map. The value at the VOX_{CTL} output (Pin 5) is the same as the program bit in R8B7. The HPDN and VOX_{CTL} outputs can be used to control the state of the SA5752 companion device.

Power On Reset and Power Down Modes

In order to avoid undefined states of the SA5753 when power is initially applied, a power-on-reset circuit is incorporated which defaults RxP and TxP such that the receive and transmit paths are muted if a 'high' voltage is applied to RX MUTE and TX MUTE (Pins 12 and 18). RX MUTE and TX MUTE include on-chip pull up resistors so, during power up, the user may apply a logic '1' to these pins or leave them floating. After power up, the registers can be programmed and the mutes removed by a quick access write to R0.

Three software controlled low power modes are provided on the SA5753. These are POWER DOWN (PWDN), IDLE and DENA and can be selected by programming a '1' into R6B2, R6B1 or R6B0 as follows. In PWDN mode (R6B2=1) both the voice and data channels are powered down with the respective I/O pins at a high impedance. In DENA mode (R6B1=1) the voice channels are powered down, but the data channel (from $DATA_{IN}$ and TX_{OUT}) is fully active. In IDLE mode (R6B1=1, R6B0=1) both voice and data channels are powered down. (See Table on page 8.)

The difference between selecting IDLE and PWDN is that the former maintains the normal operational bias voltages at all voice and data I/O pins and provides a glitch-free transfer from power down to a fully active mode and vice-versa.

Although the POWER DOWN mode exhibits lower power consumption, glitches may occur when transferring to an active mode because of the previous high impedance of the I/O pins.

The VOX_{CTL} and HPDN pins (Pins 5 and 6) still have the same value as R8B7 and R5B1 in all low power modes.

Operation Without Using the I^{2}C Bus

The SA5753 can be operated in a default mode with the I^{2}C bus bypassed. To use this mode, the DFT pin (Pin 13) is pulled HIGH, then the I^{2}C bus is bypassed and the SA5753 operates as if all register bits in the I^{2}C address map table are set to '0' except R1B2 (S13), R0B0 (S10) and R0B1 (S9), which are set to '1' to enable the receiver output. R6B2 (PWDN), which is controlled by the state of the HPDN pin (Pin 6), which is an input in DEFAULT mode.

When HPDN is pulled HIGH, the R6B2 bit is set to '0' and the SA5753 is placed in it's normal operating mode with all Gain Control Blocks set to 0dB except A3, which is set to –2dB.

When HPDN is pulled LOW, the R6B2 bit is set to '1' and the SA5753 enters POWER DOWN.

There is no on-chip pull-up or pull-down structure on the HPDN pin and so it must not be allowed to float in DEFAULT mode since the operating mode of the SA5753 will then be undetermined.

The Tx MUTE and Rx MUTE pins must be pulled LOW to enable the transmit and receive paths, respectively.

The VOXCTL pin (Pin 5) will follow the value of the control bit stored in R8B7 prior to pulling DFT HIGH.

The DTMF is disabled in the DEFAULT mode.

Programming Without the I^{2}C Protocol

In the default mode, with DFT (Pin 13) and HPDN (Pin 6) pulled HIGH, the registers in the control register bit map are chained together so that bit 0 of a register is connected to bit 7 of the preceeding register with R0B6, R0B7, R1B6 and R1B7 bypassed, i.e., R0B5 is connected to R1B0, R1B5 is connected to R2B0, R2B7 is connected to R3B0, etc. Bits can then be loaded as a serial stream through the SDA pin of the I^{2}C bus by the negative edge of a shifting clock applied at the SCL pin of the I^{2}C bus. When a bit is loaded at SDA it will load first into R0B0 and then will be shifted to R8B7 after 68 clock edges.

A total of 68 clock pulses (applied at SCL) are therefore required to completely load the registers.

In this mode of operation the contents of the register map are also shifted out from the VOX_{CTL} pin since it takes the same value as R8B7. After power up there is no reset within the registers so the first 68 bits clock out at the VOX_{CTL} pin will have an indeterminate value.

Summary: To use this capability, the DFT pin and the HPDN pin must be pulled HIGH, the serial bit stream loaded through SCL synchronous with the negative clock edge applied at SCL for 68 clock pulses, and then the DFT pin pulled LOW.

Cordless Telephone Applications

For cordless telephone applications, a switch S12 is provided (R5B0) to route data through the complete transmit path while inhibiting the voice channel. In the receive path, a quick access mode is provided through the I^{2}C to disable both EAR_{OUT} and $SPKR_{OUT}$, by setting R0B0 and R0B1, when data is detected at the $DEMP_{OUT}$ pin (Pin 7).

I²C CHARACTERISTICS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL are bidirectional lines connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are HIGH. Data transfer may be initiated only when the bus is not busy (both lines HIGH).

The output devices, or stages, connected to the bus must have an open drain or open collector output in order to perform the wired-AND function.

Data at the I²C bus can be transferred at a rate up to 100kbits/s. The number of devices connected to the bus is solely dependent on the maximum allowed bus capacitance of 400pF.

For devices operating over a wide range of supply voltages, such as the SA5753, the following levels have been defined for a logical LOW and HIGH;

$V_{ILMAX} = 0.3V_{DD}$ (max. input LOW voltage)
$V_{IHMIN} = 0.7V_{DD}$ (min. input HIGH voltage)

Data Transfer

Data is transferred from a transmitting device to a receiving device with one data bit transferred during each clock pulse on the SCL line. The transmitter also generates the clock once arbitration has given it control of the SCL line. The data on the SDA line must remain stable during the HIGH period of the clock cycle, otherwise it may be interpreted as a control signal.

Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH to LOW transition of the data line while the clock line is HIGH is defined as a start condition. A LOW to HIGH transition of the data line while the clock is HIGH is defined as a stop condition.

Acknowledgement

Following each byte of data transfered, the receiver must acknowledge successful reception. To do this the transmitter releases the SDA line (allowing it to go HIGH) at the end of each transmitted byte, and it is pulled LOW by the receiver. If this condition is maintained during the next HIGH period of the clock pulse (called the acknowledge clock pulse) then data transfer is resumed. If the receiver does not pull the SDA line LOW, the transmitter will abort the transfer.

I²C Bus Data Configurations

The SA5753 is always a slave receiver in the I²C bus configuration). The slave address consists of eight bits in the serial mode and is internally fixed.

Control Registers

The control register bit map is shown below. Either a quick access or normal address mode can be used, determined by the two MSB bits in the first word following the SA5753 address word. If the quick access mode is used, the registers R0 or R1 can be updated by sending only two bytes of information (address plus update). If R0 or R1 are updated using the address mode, then B7 and B6 of the data word are ignored. In all access modes, incremental register addressing is supported with following words updating the next register until a 'stop' bit is sent.

High Tone DTMF Register

MSB							LSB
HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0

The eight bits determine the output frequency by the following formula.:

High Frequency = 1200kHz/6/HD
where HD is the value of the register.

Low Tone DTMF Register

MSB							LSB
LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0

The eight bits determine the output frequency by the following formula.:

Low Frequency = 1200kHz/14/LD
where LD is the value of the register.

The operation of the 96ms DTMF timer is initiated by the loading of the low tone DTMF register. This timer terminates transmission of the tones as the generated tones cross the reference level after 96ms. The on time of the tones can thus vary by up to one cycle of the tones.

Continuous tones can be obtained by again loading DTC = 1 in R1, bit 5.

Single tones can be obtained by loading 2 into the unused tone register to silence it.

Loading a value of 1 or 0 into the registers will default the register value to 257 or 256 for high tone or low tone, respectively.

Phase continuous frequency modulation can be produced by loading a new value into a DTMF register during continuous operation (DTC=1).

I^2C Address and Access

S	A7 A6 A5 A4 A3 A2 A1 A0	ACK	F7 F6 F5 F4 F3 F2 F1 F0	ACK	...	P

S = start, A0 = 0, ACK = acknowledge, P = stop, A7–0 = SA5753 address fixed internally at 1000000. Access mode is determined by F7, F6.

All access modes support incremental addressing.

Mode	F7	F6	Action
quick access	0	0	Load F5–F0 to R0B5 – R0B0
quick access	0	1	Load F5-F0 to R1B5 – R1B0
test mode	1	0	For test only. DO NOT USE.
address mode	1	1	F3–F0 point to register

Address Map

REG	Address				Register Bits							
	F3	F2	F1	F0	B7	B6	B5	B4	B3	B2	B1	B0
R0	0	0	0	0	Y	Y	RxM	TxM	A2bb1	A2bb0	S9	S10
R1	0	0	0	1	Y	Y	DTC	S4	S8	S13	S7	S2
R2	0	0	1	0	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0
R3	0	0	1	1	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0
R4	0	1	0	0	A1b3	A1b2	A1b1	A1b0	A4b3	A4b2	A4b1	A4b0
R5	0	1	0	1	A6b3	A6b2	A6b1	A6b0	NAMPS	VCO	HPDN	S12
R6	0	1	1	0	A2ab4	A2ab3	A2ab2	A2ab1	A2ab0	PWDN	IDLE 1	IDLE 0
R7	0	1	1	1	A3b3	A3b2	A3b1	A3b0	A7b3	A7b2	A7b1	A7b0
R8	1	0	0	0	VOX_{CTL}	S3	S5	S6	S11	RxP	TxP	S1

Y = ignored in address mode.
For all bits TRUE = '1'

A1b3–0 = program bits for gain block A1
A2ab4–0 = program bits for gain block A2a
A2bb1–0 = program bits for gain block A2b
A3b3–0 = program bits for gain block A3
A4b4–0 = program bits for gain block A4
A5b2–0 = program bits for gain block A5
A6b3–0 = program bits for gain block A6
A7b3–0 = program bits for gain block A7
HD7–0 = high tone DTMF
LD7–0 = low tone DTMF
NAMPS = program bit for NAMPS offset
VCO = 6dB higher TX_{OUT}
RxM = receive mute
TxM = transmit mute
RxP = receive mute polarity

TxP = transmit mute polarity
DTC = DTMF continuous
S1 = bypass TXBPF
S2 = bypass compressor in TX path, inhibit pre-emph input
S3 = bypass pre-emp and limiter in Tx path
S4 = enable DTMF to TX path and inhibit $PREMP_{IN}$ and S2.
S5 = bypass RXBPF
S6 = bypass de-emph in RX path
S7 = bypass expandor in RX path, inhibit audio input
S8 = enable DTMF to RX path and inhibit $AUDIO_{IN}$ and S7.
S9 = enable $SPKR_{OUT}$
S10 = enable EAR_{OUT}
S11 = bypass TXLPF
S12 = cordless data option established
S13 = enable data path

VOX_{CTL} = enable VOX of compandor/expander circuit. This bit appears at the VOX_{CTL} pin (Pin 5) of the SA5753.
HPDN = enable power down of compandor circuit. This bit appears at the HPDN pin (Pin 6) of the SA5753
PWDN, IDLE1, IDLE0 see Table below

Low Power Modes (R6B0 – R6B2)

PWDN	IDLE1	IDLE0	
1	X	X	(PWDN) Complete power down except I^2C, I/Os high impedance.
0	1	0	(DENA) Low power, I/Os at $V_{DD}/2$, $DATA_{IN}$ to TX_{OUT} enabled.
0	1	1	(IDLE) Low power, I/Os at $V_{DD}/2$, $DATA_{IN}$ to TX_{OUT} disabled.
0	0	0	Normal operation.
0	0	1	$DATA_{IN}$ to TX_{OUT} disabled.

X = don't care.

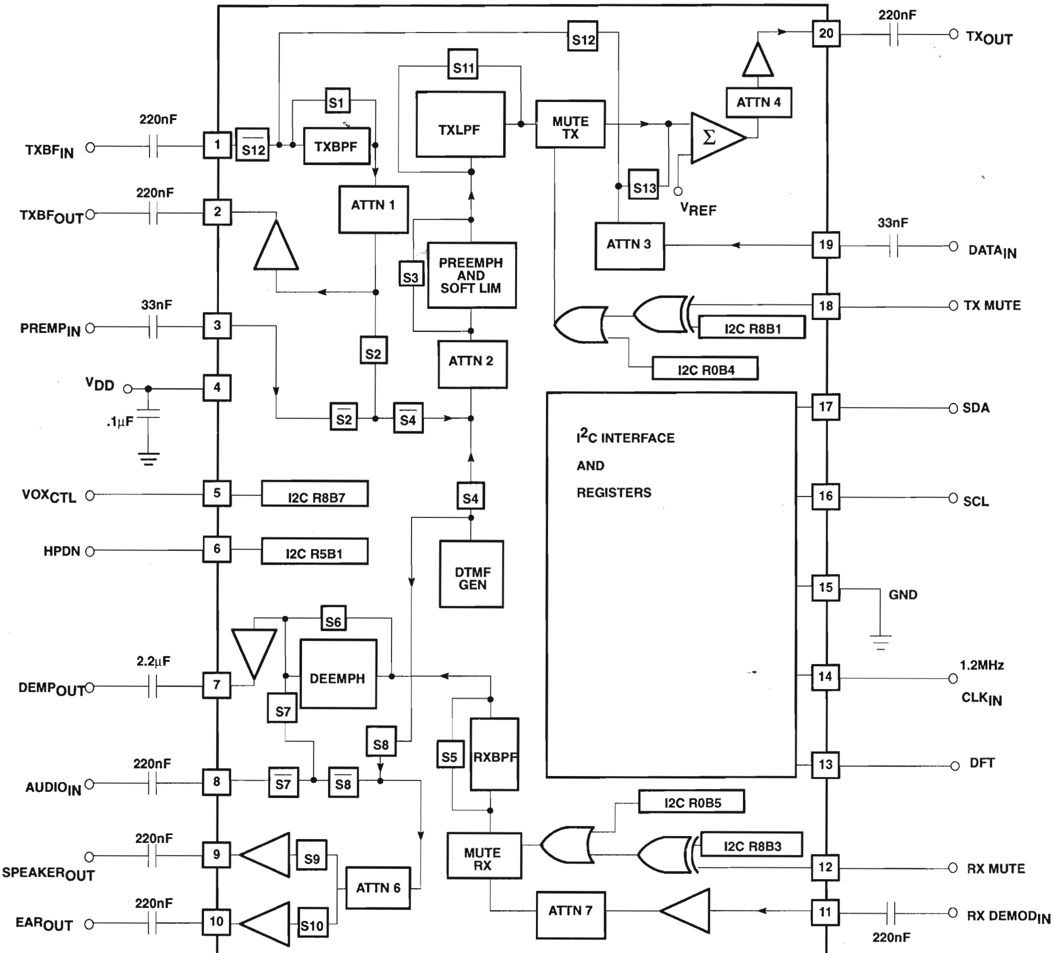


Figure 1. SA5753 Test and Application Circuit

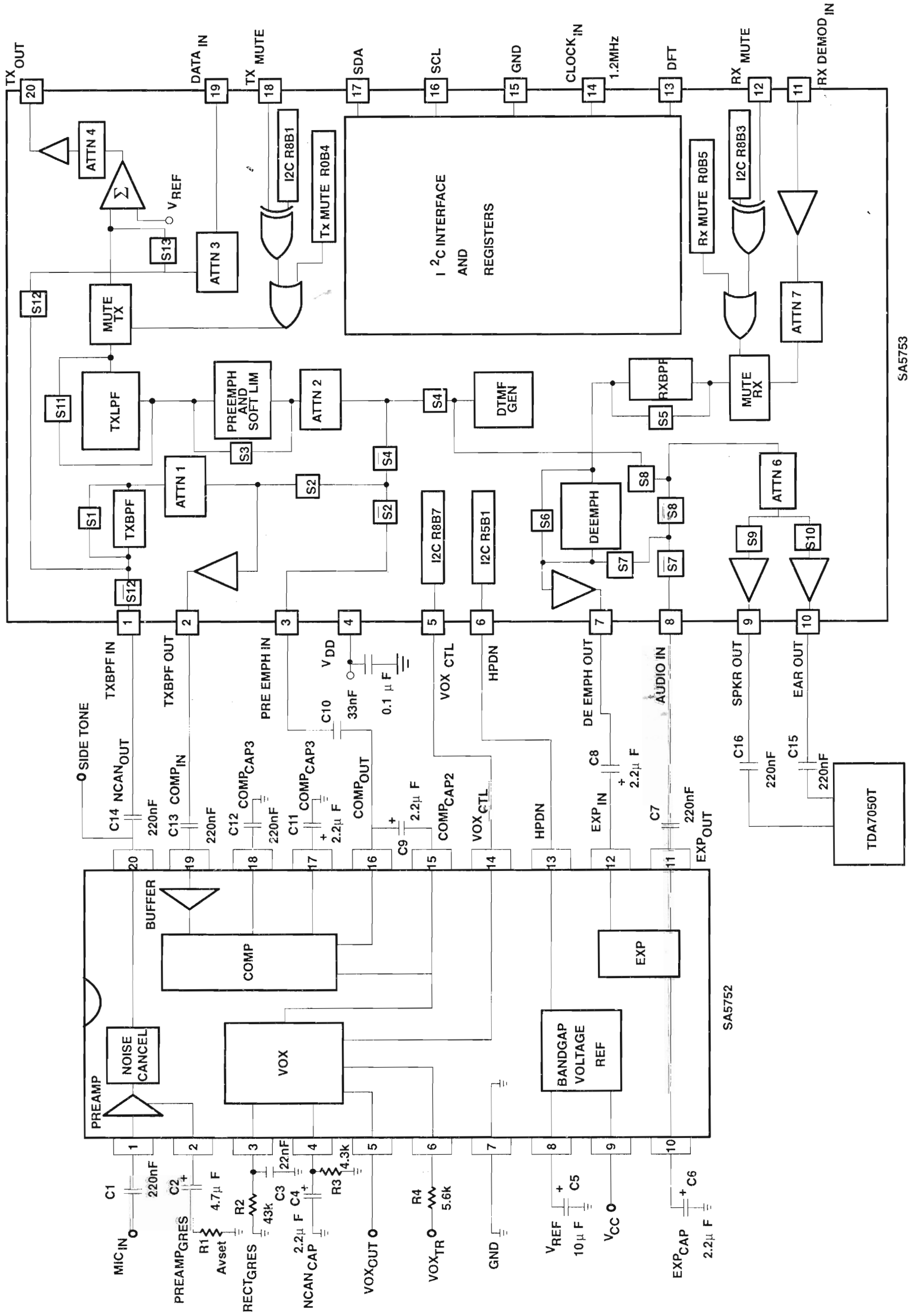


Figure 2. Application Diagram for the Audio Processor

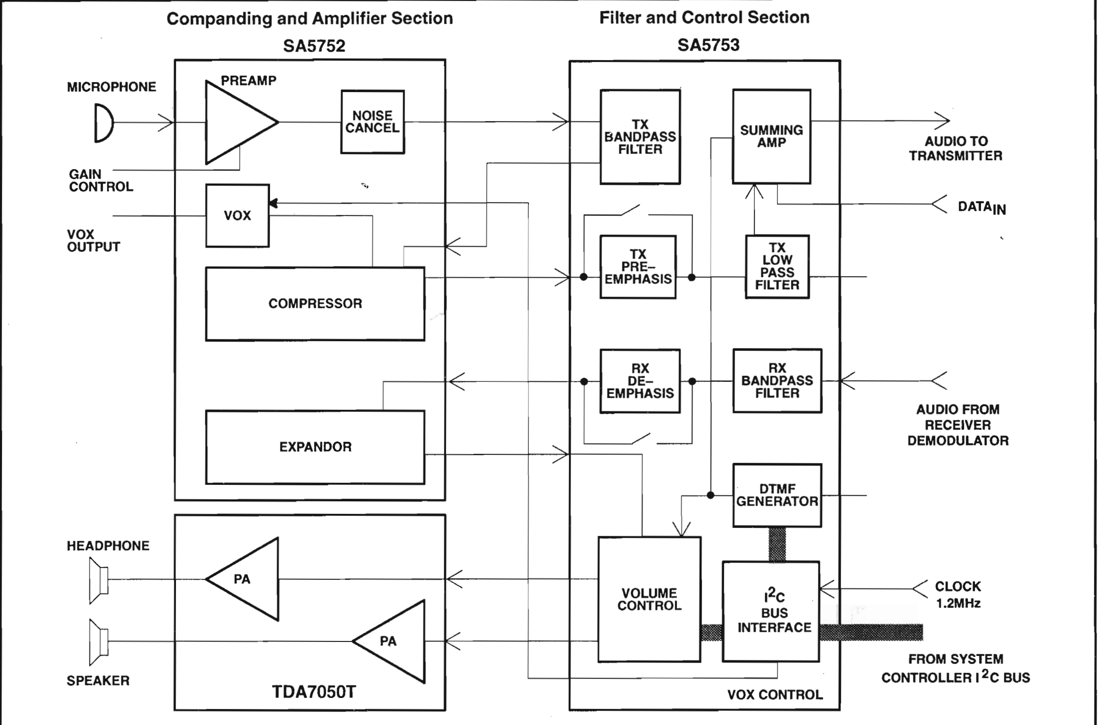


Figure 3. Typical Configuration of Audio Processor (APROC) System Chip Set

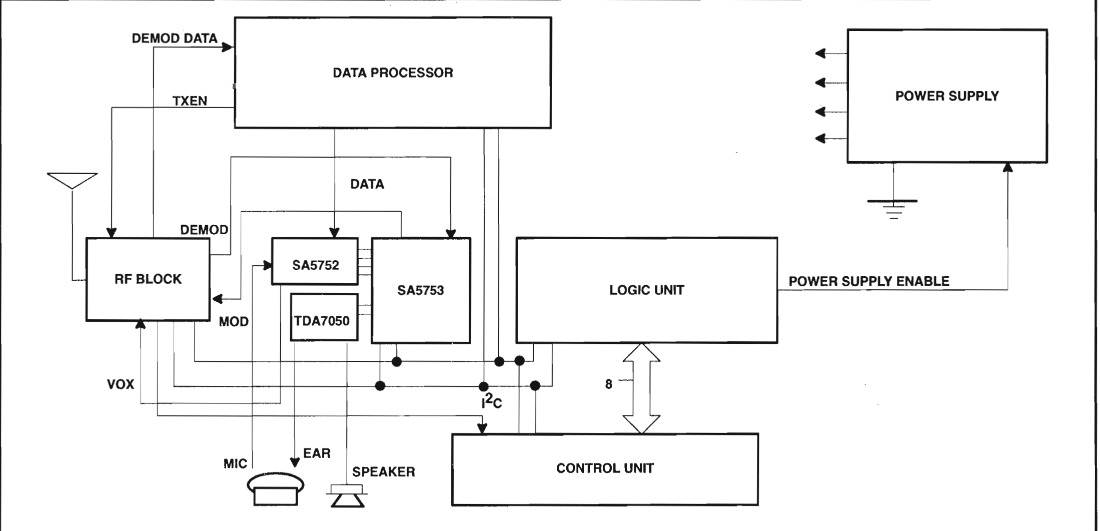
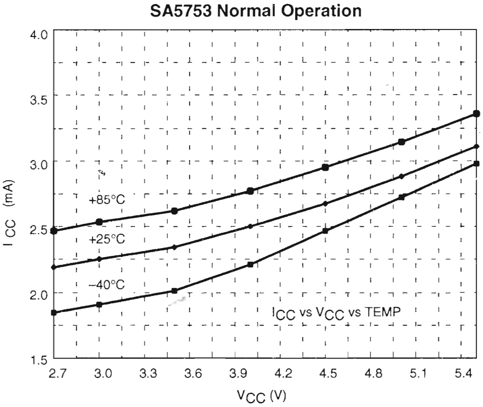
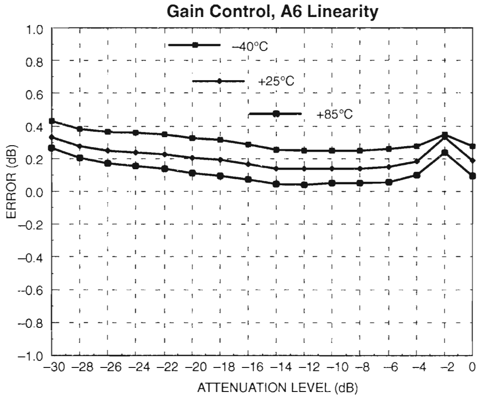
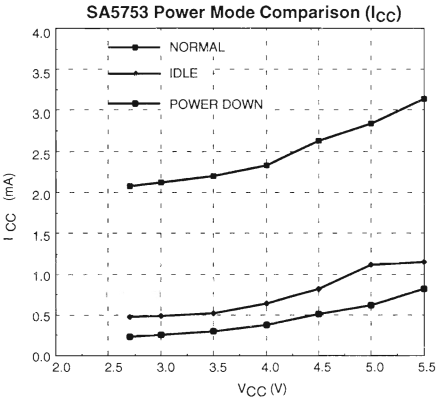


Figure 4. APROC Application Diagram


SA5753 Normal Operation
4.0
3.5
3.0
2.5
2.0
1.5
I CC (mA)
+85°C
+25°C
–40°C
I_CC vs V_CC vs TEMP
2.7
3.0
3.3
3.6
3.9
4.2
4.5
4.8
5.1
5.4
V_CC (V)


Gain Control, A6 Linearity
–40°C
+25°C
+85°C
1.0
0.8
0.6
0.4
0.2
0.0
–0.2
–0.4
–0.6
–0.8
–1.0
ERROR (dB)
–30
–28
–26
–24
–22
–20
–18
–16
–14
–12
–10
–8
–6
–4
–2
0
ATTENUATION LEVEL (dB)


SA5753 Power Mode Comparison (I_CC)
NORMAL
IDLE
POWER DOWN
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
I CC (mA)
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
V_CC (V)

Using the SA5752 and SA5753 for low voltage designs

AN1742

Author: *Alvin K. Wong*

INTRODUCTION

The SA5752 and the SA5753 are two audio processor chips that can be used in designs that require 3 volt operation. This chip set, known as the APROC II (SA5752 and SA5753), is functionally similar to the APROC I (SA5750 and SA5751), but with a number of enhancements which allow more design flexibility for the designer. Additionally, the APROC II offers the same high performance as the APROC I. The SA5752 is the low voltage version of the SA5750, and the SA5753 is the low voltage version of the SA5751. Figures 1 and 2 show the block diagrams of the APROC II and APROC I, respectively. Notice that the differences are subtle and pertain primarily to the amplifier section.

If a designer is not familiar with the APROC I chip set, he/she can refer to AN1741 which discusses the basics of audio processing and the key functions used to meet the strict requirements for cellular specifications. Additionally, it describes how to design with the chip set and how to measure attack and release times for the compandor section.

This application note should be used in conjunction with AN1741 to fully understand audio processing. Experience with the APROC I will help aid the designer in learning the APROC II, but this is not a necessity. This application note will focus on the main differences between the APROCs and highlight key areas of the APROC II.

I. KEY DIFFERENCES BETWEEN APROC I AND APROC II

- Comparing the SA5750 and SA5752
  - Packaging
  - External Amplifier
  - Power Consumption
- Comparing the SA5751 and SA5753
  - Packaging
  - Power Consumption
  - Programmable Gain Attenuators
  - Power Down
  - Programmable Transmit and Receive Mute Polarity Function
  - Non-I^{2}C Operation (Default Mode)
  - Cordless Application
  - VCO Mode
  - NAMPS Mode

II. SA5752

- Preamp
- VOX
- Noise Canceller
- Compressor
- Power Down

III. SA5753

- Non-I^{2}C Operation (Default Mode)
- Programming Without the I^{2}C Protocol
- DTMF
- The Limiter and All-Pass Circuit

IV. EVALUATION SOFTWARE AND DEMOBOARD

- DTMF

V. QUESTIONS AND ANSWERS

I. KEY DIFFERENCES BETWEEN APROC I AND APROC II

Table 2 shows the main differences between the APROC I and II. One noticeable difference is the power consumption and power down currents. Moreover, the SA5753 has three power down modes which will be discussed in detail in the Power Down Mode section of this application note.

Comparing the SA5750 and SA5752

The SA5750 and SA5752 differ in the following ways:

Packaging

There are minimal differences between the SA5750 and the SA5752. Instead of a 24 pin package, the SA5752 is offered in a 20 pin package. This change allows the SA5752 to come in the SSOP package. The SSOP package is smaller in dimension than the standard SO package which saves space.

External Amplifiers

Since many APROC I customers use their own external speaker and ear amplifiers, the SA5752 was designed without them (see Figures 1 and 2). However, the other key blocks are present, like the preamp, VOX, compressor, expandor, and noise canceller circuit.

Since the SA5752 does not supply the ear and speaker amplifiers internally, an external one can be used. The Philips TDA7050T is the recommended choice because of its low voltage operation and high performance capabilities.

Power Consumption

The current consumption and power down mode has been improved in the SA5752. For normal operation, the SA5752 only draws an I_{CC} of 3.1mA for a 3 volt supply compared to the SA5750, where I_{CC} = 8.4mA for V_{CC} = 5V. Additionally, in the power down mode, the SA5752 only draws 0.2mA of current, compared to 1.8mA for the SA5750. Recall that the power down mode is implemented when the chip is not being used to conserve battery life. The power down feature is preferred instead of completely turning off the power to the chip because the turn on time to normal operation is faster.

Comparing the SA5751 and SA5753

The SA5751 and SA5753 differ in the following ways:

Packaging

The SA5751 is available in a 24 pin DIP package or a 28 pin SO package.

Similar to the SA5752, the SA5753 is also offered in the 20 pin SSOP package. The combination of these packages allows all the audio processing functions to be done in a minimal amount of board space.

Power Consumption

The current and voltage specification has also improved for the SA5753. This chip draws 2.1mA at 3V compared to 2.7mA at 5V for the SA5751. There is also additional current economy from the three different power-down modes, PWDN, DENA and IDLE (see Power-Down section). These power-down currents are 0.2mA, 0.6mA and 0.7mA compared to 0.9 for the SA5751.

Programmable gain attenuators

The SA5753 has the same key block functions as the SA5751, but there are additional features. The SA5753 has nine programmable gain attenuators throughout the transmit and receive path. This allows the designer the flexibility to tailor the signal level at different ports. The SA5751 has only one programmable gain attenuator in the receive path which can be used as the volume control. Table 3 shows the programmable gain attenuators' range for the SA5753.

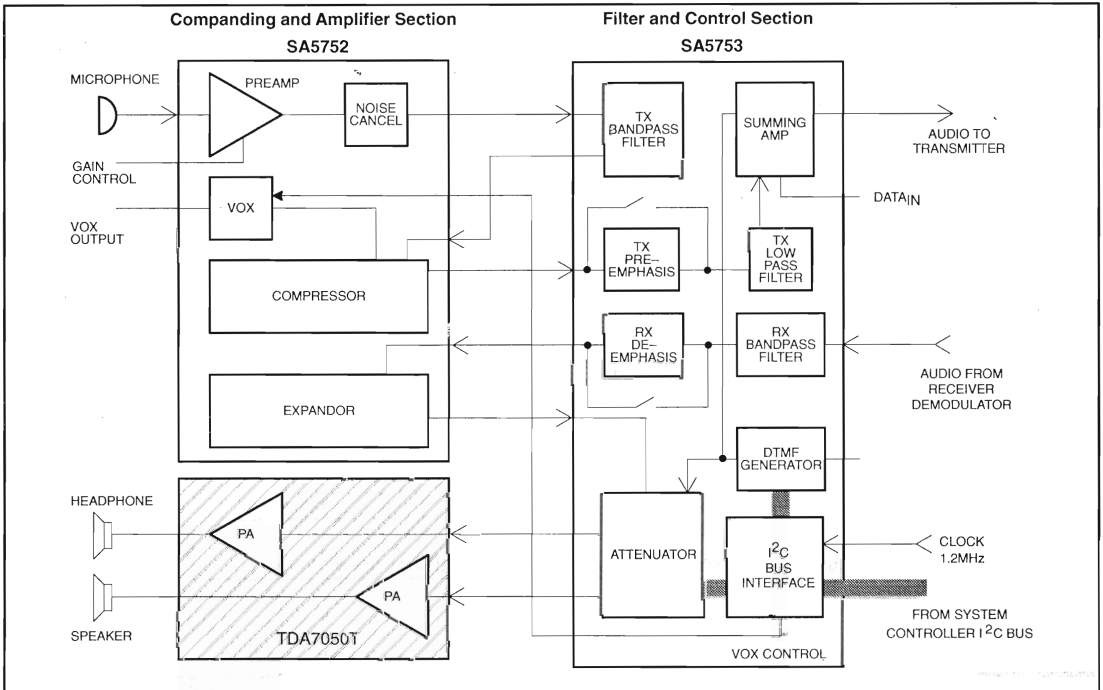


Figure 1. Block Diagram of Audio Processor (APROC II) System Chip Set

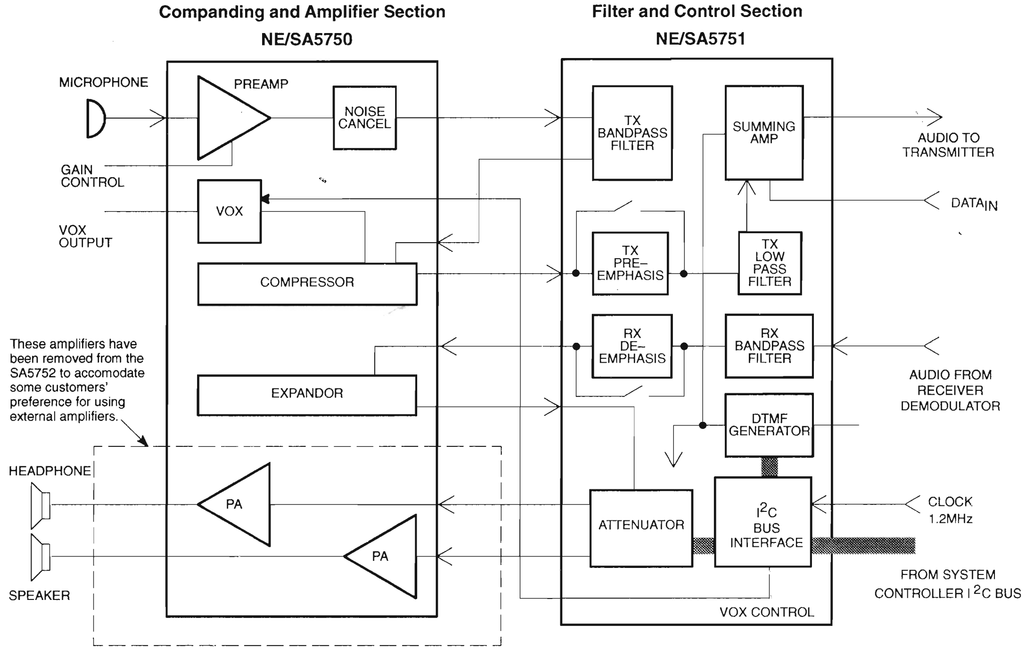


Figure 2. Block Diagram of Audio Processor (APROC I) System Chip Set

Table 2. Key Differences Between APROC I and APROC II (All values are Typical)

	APROC I		APROC II	
	SA5750	**SA5751**	**SA5752**	**SA5753**
V_{CC} (V)	4.5 – 5.5	4.5 – 5.5	2.7 – 5.5	2.7 – 5.5
I_{CC} (mA)	8.4 @ 5V	2.7 @ 5V	3.1 @ 3V	2.1 @ 3V
Total I_{CC} (mA)	11.10		5.4	
Power Down Modes	PWDN		PWDN, IDLE and DENA	
Power Down I_{CC} (mA)	1.8	0.9	0.2	PWDN 0.2 IDLE 0.6 DENA 0.7
Packages:				
NE: 0 to +70°C	NE5750N NE5750D	NE5751N NE5751D		
SA: –40 to +85°C	SA5750N SA5750D	SA5751N SA5751D	SA5752D SA5752DK	SA5753D SA5753DK
No. of Pins	24	24 or 28	20	20
Programmable Gain Attenuators	0	1	0	9
I^2C Protocol	Not required	Required	Not Required	Optional*

Package Codes:
N: Plastic Dual In-Line Package (DIP)
D: Plastic Small Outline (SO)
FE: Ceramic Dual In-Line Package
DK: Shrink Small Outline Package (SSOP)

*Operating the SA5753 without the I^2C protocol means DTMF generator and gain attenuators are no longer functional. See SA5753 section for more details.

Table 3. Attenuator Gain Blocks (SA5753)

SYMBOL	Bits	TYPICAL STEP (dB)	TYPICAL GAIN (dB)	
			MIN	MAX
A1	4	−0.8	−12.0	0
A2a	5	±0.25	−3.75	+3.75
A2b	2	−6, (−12 on first)	−24.0	0
A3	4	−1.0	−17.0	−2
A4	4	±0.5	−3.5	+3.5
A6	4	−2.0	−30	0
A7	4	−6, (−12 on first)	−24.0	+3.5
NAMPS	1		+1.9 in A2b −7.6 in A4	
VCO	1		+6.0 in A4	
For A2a, A4 and A7:		MSB sets the sign of the gain MSB = 0 for gain MSB = 1 for attenuation		
For all Gain Blocks:		All bits set to 0 = 0dB gain All bits set to 1 = maximum gain or attenuation		

Table 4. Power-Down Modes (SA5753)

PWDN	IDLE1	IDLE0	
1	X	X	(PWDN) Complete power down except I^2C, I/Os high impedance.
0	1	0	(DENA) Low power, I/Os at $V_{DD}/2$, $DATA_{IN}$ to TX_{OUT} enabled.
0	1	1	(IDLE) Low power, I/Os at $V_{DD}/2$, $DATA_{IN}$ to TX_{OUT} disabled.
0	0	0	Normal operation.
0	0	1	$DATA_{IN}$ to TX_{OUT} disabled.

X = don't care.

The benefit of having signal amplitude control throughout the signal path is that a designer will no longer have to add an external amplifier to boost signals. Additionally, external resistors are no longer needed to attenuate the signal. The SA5753 programmable gain attenuators make a design more flexible which saves cost and board space from external components.

Power Down

The SA5753 has three different power down modes compared to only one for the SA5751. The three power down modes are PWDN, IDLE, and DENA (see Table 4). All three power down modes have different current consumptions and provide different options to the designer.

In the PWDN mode, the voice and data channels are powered down. This allows for maximum power conservation. In the IDLE mode, both the voice and data channels are also powered down, but are glitch free when going from power down to power up.

The IDLE mode trades a higher standby current against glitch-free power-up. Hence, the IDLE mode is used for power conservation, whereas PWDN mode is mainly used for absolute maximum power conservation.

For the DENA mode, the voice channels are powered down, but the data channel is still fully active. This allows the chip set to transmit on reverse control channel without powering up the whole APROC II.

In the PWDN mode, the SA5753 transmit path from the Tx bandpass filter in to the Tx filter out pin has only 6dB of attenuation. This means that, if a signal is present and a designer does not want this signal through, he/she should use the IDLE (or DENA) mode.

Programmable Transmit and Receive Mute Polarity Function

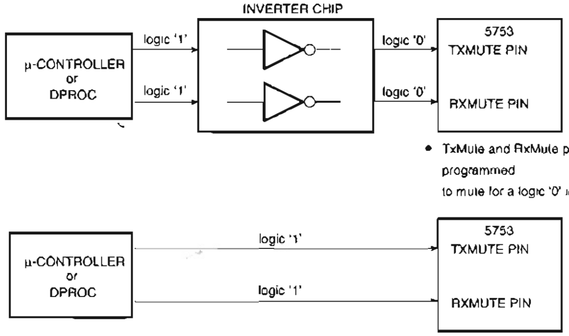
The SA5753 also has programmable transmit and receive mute polarity functions (TxP and RxP). A designer can mute the transmit or receive path with a logic '1' or '0' on the TxMute or RxMute pin depending on how the SA5753 is programmed by I^2C.

The benefit of having programmable transmit and receive mute polarity functions is that it eliminates the need for an inverter chip which saves on costs, power, and space. If the microcontroller or data processor (DPROC) can only provide a logic '1' to mute the Tx and Rx signal path, then to mute the chip-set the standard way, an inverter gate is needed because the logic '1' needs to be converted to a logic '0'. This logic '0' is then applied to the TxMute and RxMute pin. But with the SA5753, a logic '1' applied to the TxMute and RxMute pins will mute the Tx and Rx path if the SA5753 is programmed to mute for a logic '1'.

Figure 3 shows a diagram of how the inverter gate chip is eliminated. Additionally, a logic '0' applied to the TxMute or RxMute pin can mute the signal path if the SA5753 is programmed to mute when a logic '0' is applied to the TxMute and RxMute pins. Because of this feature the APROC II can now interface directly with the Philips Semiconductors UMA1000 DPROC.

Since the TxMute and RxMute pins are separate, the Tx and Rx path can also be muted separately. For example, if a user wants to mute his/her side of the conversation (such that the other party cannot hear), but still wants to hear the other party, the Tx path needs to be muted while the Rx path is left on. Therefore, a designer can provide a mute button on the keypad to provide this function to the user.

Since there are separate pins to mute the Tx and Rx paths, a designer is also given full flexibility in programming these pins separately. He/she can define a logic '1' to have the Tx path mute while programming a logic '0' to have the Rx path mute, or vice versa (see Figure 4). However, in most designs a logic '0' is programmed to have the Tx and Rx path muted.

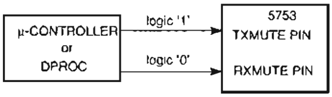


- TxMute and RxMute pins programmed to mute for a logic '0' input.

NOTE:
A 10k series resistor should be connected from the Logic signal to the TxMute/RxMute pin.
This allows the APROC II to operate at 3V, while safely accepting a 5V logic signal to these inputs.

- TxMute and RxMute pins programmed to mute for a logic '1' input
- Inverter chip eliminated

Figure 3. Benefit of Having Programmable Transmit and Receive Mute Pins



- TxMute pin programmed to mute for a logic '1' input.
- RxMute pin programmed to mute for a logic '0' input

NOTE:
A 10k series resistor should be connected from the Logic signal to the TxMute/RxMute pin. This allows the APROC II to operate at 3V, while safely accepting a 5V logic signal to these inputs.

Figure 4. Muting the Tx and Rx Path for Separate Programmable Inputs

Non–I^{2}C Operation (Default Mode)

The SA5753 can also be used without the I^{2}C protocol by pulling the DFT (default pin) and HPDN pin HIGH. This non-I^{2}C operation does not give the designer the flexibility to tailor the signal or use the internal DTMF generator. However, if the SA5753 is loaded serially, the SA5753 can be programmed. More information can be found in any I^{2}C documentation. See the SA5753 section for more detailed information.

Cordless Application

Unlike the SA5751, the SA5753 can be implemented more readily for cordless phone applications. The data path can be routed through the transmit path while inhibiting the voice channel. In the receive path, the EAR$_{OUT}$ and SPKR$_{OUT}$ can be disabled when the data is detected at the DEMP$_{OUT}$ pin.

To allow design flexibility, a designer can attenuate the data signal internally before it is passed through the TX$_{OUT}$ pin. This eliminates the need for external components and allows programmable attenuation steps

such that different data amplitude inputs can be tailored in real-time.

VCO Mode

If the VCO bit on the SA5753 is programmed correctly, the TX$_{OUT}$ provides an extra 6dB of gain through Attenuator 4. Therefore, the new range is 2.5dB to 9.5dB. Normally the TX$_{OUT}$ signal is connected to a VCO (Voltage Controlled Oscillator) with a slope of 10kHz/V. The designer can implement the VCO bit to get a stronger output from the SA5753 to match 5kHz/V VCOs.

NAMPS Mode

Another key difference between the SA5753 and the SA5751 is that the SA5753 can be programmed for NAMPS mode by tailoring the gain attenuator settings.

There are two attenuators that receive the modified gain adjustments. Attenuator 4 is reduced by –7.6dB and Attenuator 2B is boosted by 1.9dB. Therefore, the new ranges are –11.1dB to –4.1dB for Attenuator 4 and –22.1dB to 1.9dB for Attenuator 2B.

The reason the gain settings are reduced is because the signal amplitude needs to be reduced before going to the transmitter. Recall that for the NAMPS mode the frequency deviation is less, so less amplitude is required.

II. SA5752

Figure 5 shows the main blocks of the SA5752: preamp, noise canceller, VOX, compressor, and expandor. This part does not require any programming blocks and therefore, no I^{2}C is needed to operate this part. However, the SA5752 can be powered

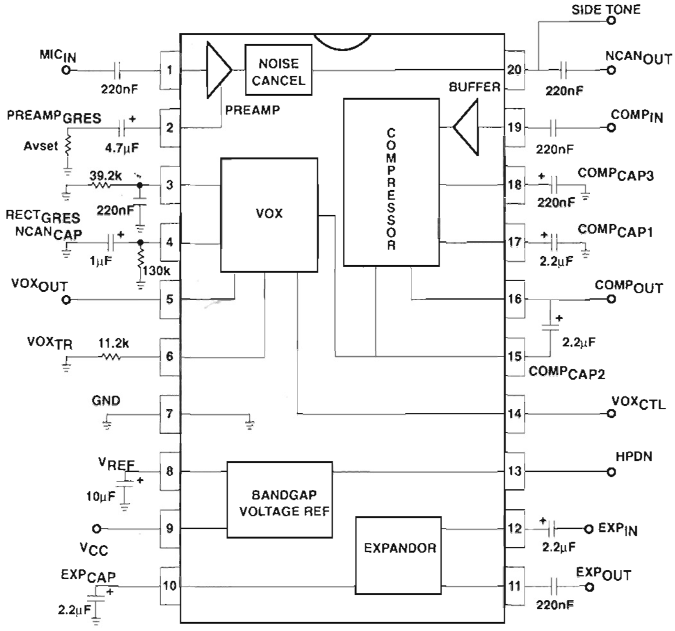


Figure 5. SA5752 Block Diagram

down via the SA5753 HPDN bit, which is under I^{2}C control.

Preamp

The SA5752 provides a preamp which has an adjustable gain range from 0 to 40dB. The gain may be adjusted with an external resistor which connects to Pin 2 (see Equation 1, below). Table 5 shows the resistor values needed to get the appropriate gain. If a designer wants to calculate for a different value, the equation below shows how to do so.

When a designer sets the preamp gain, be sure that the output signal does not clip due to the power supply rails. To prevent this, apply the predicted strongest signal to the preamp input and observe the output while setting the gain.

Additionally, if the VOX is implemented, be sure that the extra 10dB of gain is on from the noise canceller circuit (see VOX section for more details).

$$R1 = \left[\frac{50,000}{10^{\left(\frac{X(dB)}{20}\right)} - 1}\right] - 500 \quad \text{"X" in dB} \qquad (1)$$

where $0 < XdB < 40dB$

Table 5. Calculated R1 Values for Different Preamp Gains

X (dB)	R1
0	Leave Pin 2 open (∞)
5	64k
10	22k
15	10k
20	5.1k
25	2.5k
30	1.1k
35	405
40	Pin 2 AC grounded

The preamp input impedance is 50kΩ. The output of the preamp is connected to a noise canceller which can drive a minimum load impedance of 50kΩ.

When measuring the SA5752 preamp gain, be sure to measure the signal from Pin 20 to Pin 1. If the signal is measured from the SA5752 preamp input to the TX$_{OUT}$ of the SA5753, the signal's amplitude will not be the expected value due to the compressor, pre-emphasis, and attenuator settings. Therefore, remember to measure the preamp gain from the SA5752 preamp out to in.

Using the SA5752 and SA5753 for low voltage designs AN1742

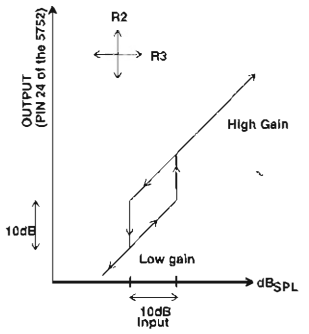


Figure 6. VOX Threshold Points

VOX

The SA5752 VOX circuitry operates like the SA5750 in that it works in conjunction with the noise canceller circuit. With the VOX activated, the noise canceller circuit will provide 10dB of gain when the input signal surpasses the "on" threshold point. When the input signal drops below the "off" threshold point, the noise canceller provides 0dB of gain. Figure 6 illustrates this function.

The VOX circuitry is useful for hands-free operation. This function is normally used in mobile conversation. Because there is road noise present in a moving vehicle, it is desirable to be able to prevent this noise from being heard. If the VOX threshold is set correctly, the noise canceller will provide 10dB of gain when the user speaks and a gain of 0dB when the user stops speaking. The other party will not hear the road noise in the background as loudly. Another feature of the VOX circuitry is that it can be used to save power. The transmitter can be switched off during non-speech periods if voice discontinuous mode (AMP) is enabled.

The VOX$_{OUT}$ and VOX$_{CTRL}$, Pins 5 and 14 respectively, can be used to determine the status of the noise canceller. Since the VOX$_{OUT}$ pin is an open collector output, a designer should connect a 10k pull up resistor to V$_{CC}$. This allows the output to read a high or low reading to determine the status of the noise canceller. Table 6 shows how Pins 5 and 14 can be used.

Having a logic '0' on Pin 14 (VOX$_{CTRL}$) is sufficient in most applications. When the voice is present, the noise canceller kicks on while the VOX$_{OUT}$ pin supplies a logic '1'. When voice is not present, VOX$_{OUT}$ pin supplies a logic '0'.

Supplying a logic '1' on Pin 14 would cause the VOX$_{OUT}$ pin to stay as a logic '1' regardless of any signal input to the preamp (Pin 1 of SA5752). However, the functionality of the noise canceller will still be signal dependent.

Table 6. VOX Truth Table

Inputs		Outputs	
Voice (Pin 1)	**VOX$_{CTRL}$ (Pin 14 of NE5752)**	**Noise Canceller Gain**	**VOX$_{OUT}$ (Pin 5 of NE5752)**
Not Present	logic '0'	0dB	logic '0'
Present	logic '0'	10dB	logic '1'
Not Present	logic '1'	0dB	logic '1'
Present	logic '1'	10dB	logic '1'

NOTE: If the NE5752 is used alone, be sure that the output of the noise canceller is AC coupled to the input of the compressor. Also, make sure that all of the components for the compressor are connected.

Pins 3, 4, 5, 6, and 14 all deal with the VOX's performance. Resistor R2 and capacitor C3 are connected to Pin 3. These components set the gain of the VOX. The values chosen here are for internal use only and should not be altered.

The following steps are the procedure for setting the VOX threshold. Remember that this setting can be set externally by the user using an external potentiometer or by a microprocessor which can sample the sound in the car and electronically set the "automatic environment VOX function" threshold. This can be done by implementing different resistor settings for different threshold points.

Step 1: Make sure:

a. Pin 6 is left open
b. The VOX attack and recovery components are in place at Pin 4.
c. R2 and C3 are connected to Pin 3.
d. If using the SA5752 alone, be sure to connect the preamp output (Pin 20) to the compressor input (Pin 19) with a DC blocking capacitor.
e. The preamp gain is already set (in this instance the preamp gain is 0dB)
f. Make sure that the compressor's components are also connected; compressor's attack time has to be functional.

Step 2. Apply a constant 1kHz sinewave signal to Pin 1 through a DC blocking cap (if the Philips evaluation board is used, apply the signal to the MIC input pin) with the desired threshold. In this case, 30mV$_{P-P}$.

Step 3. Measure the DC voltage on Pin 4: V4=275mV

Step 4. Calculate R5:

$$R5 = \frac{V4(V)}{25\mu A} = \frac{275mV}{25\mu A} = 11k \qquad (2)$$

Step 5. Connect R5 to Pin 6 and verify that VOX kicks on at the desired threshold. This set-up has the VOX kicking on at 30mV$_{P-P}$ and kicking off at 11mV$_{P-P}$ (for better accuracy use a 1% resistor value for R5).

Referring to the above example, if a preamp gain of 10dB was chosen before setting the threshold, the threshold will also change. So it is vital that the preamp gain be set before setting the VOX threshold.

Noise Canceller

The output of the preamp is connected to the input of the noise canceller circuit which is internal to the device. The function of the noise canceller is to automatically provide a set gain of either 0dB or 10dB when a voice is present or not present. The gain setting can be set by implementing the VOX functions.

Although the noise canceller circuit is really designed to be used with the VOX circuitry, it can be implemented without it. The noise canceller circuit can be set up to provide either 0dB or 10dB of gain at all times, regardless of the presence of a signal. Table 7 shows how to achieve either gain settings when the VOX function is bypassed.

Table 7. Setting Up the Gain of the Noise Canceller

Pin No.	Gain of Noise Canceller	
	0dB	10dB
3	Ground	Ground
4	Ground	V_{CC}
6	10k to GND	Ground

The output of the noise canceller is accessible to the designer at Pin 20.

Compressor

The SA5752 compandor operates with a unity gain level (0dB level) of $77.5mV_{RMS}$. It operates like the rest of the Philips Compandor family where any signal above the 0dB level in the compressor mode is half in dB, and any signal below the 0dB level is multiplied by 2 (assuming the unit is in dB)

As for the Expandor, the levels above and below the 0dB level are modified by the opposite of what the compressor does. This allows the signal to be restored to its original level with reduction of noise.

To determine the amplitude, the following formula is used.

$$XdB = 20\log\left(\frac{\text{AC level } mV_{RMS}}{77.5mV_{RMS}}\right) \qquad (3)$$

Example:

Determine the compressor's AC voltage output if a $200mV_{RMS}$ signal is applied to the compressor's input.

1. Convert $200mV_{RMS}$ to dB as in Equation 3

$$XdB = 20\log\left(\frac{200mV_{RMS}}{77.5mV_{RMS}}\right) = 8.23dB$$

2. Because 8.23dB is above the 0dB level, by definition of the compressor the signal is halved to 4.12dB
3. Now converting back to voltage using Equation 3 the output is $124.5mV_{RMS}$.

Figure 7 shows the diagram with other numbers for practice.

Power Down

The HPDN (Hardware Power Down) pin on the SA5752 can be left open or connected to V_{CC} for normal operation. For power down, a designer needs to ground this pin.

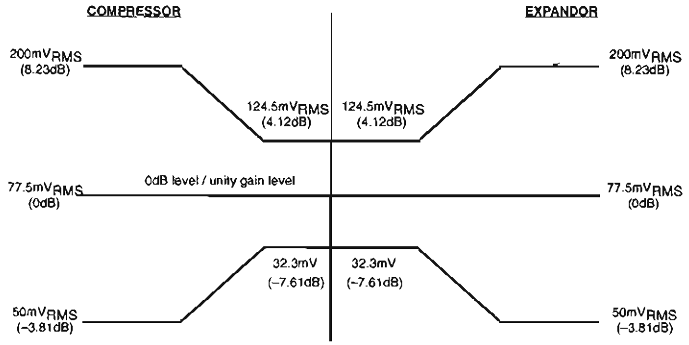


Figure 7. Determining the AC Signal Level Through a Compandor

Table 8. Programmable Divide Ratio Number

Decimal Value	Binary Value	HI DTMF Frequency	Lo DTMF Frequency
2	0000 0010	OFF	OFF
3	0000 0011	66.66kHz	28.57kHz
4	0000 0100	50kHz	21.43kHz
5	0000 0101	40kHz	17.14kHz
⋮	⋮	⋮	⋮
254	1111 1110	787.40Hz	337.46Hz
255	1111 1111	784.31Hz	336.13Hz
256	0000 0000	781.25Hz	334.82Hz
257	0000 0001	778.21Hz	333.52Hz

III. SA5753

Figure 8 shows the main blocks of the SA5753; the Transmit and Receive Bandpass filters, the Transmit Low Pass Filter. Pre-emphasis and De-emphasis, DTMF generator, attenuators and I^2C controls.

Non-I^2C Operation (Default Mode)

The SA5753 can be used without the I^2C protocol. To implement this feature, the DFT pin (default. Pin 13) and HPDN (Pin 6) must be connected to V_{CC}. In the default mode, a designer has less flexibility in programming the SA5753. The only way to program the SA5753 without the I2C protocol is to load the register serially (see next section).

If a designer decides not to program the SA5753 registers, they can no longer bypass key functions or attenuate/gain the signal. Additionally, they can no longer make use of the DTMF generator. The TxMute and RxMute pins are also no longer programmable, but are controllable externally.

A designer does not have a choice of programming the mute polarity pins. Muting the transmit and receive path now requires a designer to supply V_{CC} to the TxMute pin (Pin 18) and RxMute pin (Pin 12). To unmute the paths, a ground connection on these pins is required.

Pin 6 must be grounded for powering down the SA5753 in the default mode. For normal operations without the I^2C protocol, Pin 6 must be connected to V_{CC}. Although the SA5753 might be functional with Pin 6 left open, this is not advisable. This pin should either have V_{CC} or ground connected for a defined state. See the SA5753 data sheet for more information on non-I^2C operation.

The following is a list of features when the Default Mode is implemented:

1. All previous settings in the registers are ignored except for R8B7 (VOX_{CTL}).
2. VOX_{CTL} = the setting in R8B7 before DFT goes high.
3. All attenuators are set to 0dB.
4. HPDN is now an input, LOW=PWDN Mode.
5. DTMF = OFF
6. DEEMPH = ON
7. PREEMPH = ON
8. AMPS mode
9. Closed = S9. S10, S13
10. Open = S1, S2, S3, S4, S5, S6, S7, S8, S11, S12
11. RX is muted when RXMUTE = HI
12. TX is muted when TXMUTE = HI

NOTE: When the SA5753 is changed from DFT=HIGH (Default Mode) to DFT=LOW, the register settings will have an indeterminate value and all registers will need to be reloaded to avoid undefined states.

Programming Without the I^2C Protocol

In the default mode, with DFT (Pin 13) and HPDN (Pin 6) pulled HIGH, the registers in the control register bit map are chained together so that bit 0 of a register is connected to bit 7 of the preceding register with R0B6, R0B7, R1B6 and R1B7 bypassed, i.e., R0B5 is connected to R1B0, R1B5 is connected to R2B0, R2B7 is connected to R3B0, etc. Bits can then be loaded as a serial stream through the SDA pin of the I^2C bus by the negative edge of a shifting clock applied at the SCL pin of the I^2C bus. When a bit is loaded at SDA it will load first into R0B0 and then will be shifted to R8B7 after 68 clock edges.

A total of 68 clock pulses (applied at SCL) are, therefore, required to completely load the registers.

In this mode of operation the contents of the register map are also shifted out from the VOX_{CTL} pin since it takes the same value as R8B7. After power up there is no reset within the registers so the first 68 bits clock out at the VOX_{CTL} pin will have an indeterminate value. Once the registers are loaded, the DFT pin can be pulled low to enable the interface between the control registers and the program functions.

Summary: To use this capability, the DFT pin and the HPDN pin must be pulled HIGH, the serial bit stream loaded through SCL synchronous with the negative clock edge applied at SCL for 68 clock pulses, and then the DFT pin pulled LOW.

DTMF

The DTMF generator generates its tones by using the 1.2MHz I^2C clock and dividing it down to the desired frequency. There are high and low DTMF tones, so different divide ratios are used. To tailor the exact frequency, a programmable divide ratio number is provided to the designer. Figure 9 shows the basic scheme and the formulas to calculate the desired DTMF frequency.

The programmable divide ratio number ranges from 3 to 257 for both the high and low DTMF functions. This means that the high DTMF frequency range is from 778.21Hz to 66.66kHz. The low DTMF frequency range is from 333.52Hz to 28.57kHz.

The only caution in using the DTMF generator is when the programmable divide ratio decimal number is 256 or 257. For the SA5753, decimal values 256 and 257 are defined as a binary '0' and '1', respectively (see Table 8). The reason the decimal values 256 and 257 were defined this way is because of the actual length of their binary numbers.

Decimal 256 is binary 1 0000 0000 and decimal 257 is binary 1 0000 0001. These binary numbers exceed the 8-bit register, so 256 and 257 were replaced with a decimal '0' and '1' since these values were not previously used.

Other decimal divide ratio numbers can be converted directly to a binary number which is then loaded into the 8-bit register. To turn off the high or low DTMF generator, a decimal 2, converted to a binary 0000 0010, needs to be loaded into the register.

Below are two examples of loading the DTMF generator.

Step 1: Determine what frequency is desired for the High and Low frequencies.

Step 2: Use formulas in Figure 9 to calculate the programmable 'divide ratio number' for both High and Low tones.

Step 3: Convert the calculated 'divide ratio number' to a binary number and load into the proper register. NOTE: If the 'divide ratio number' is 256 or 257, load a binary 0000 0000 or 0000 0001, respectively. To turn off the high or low

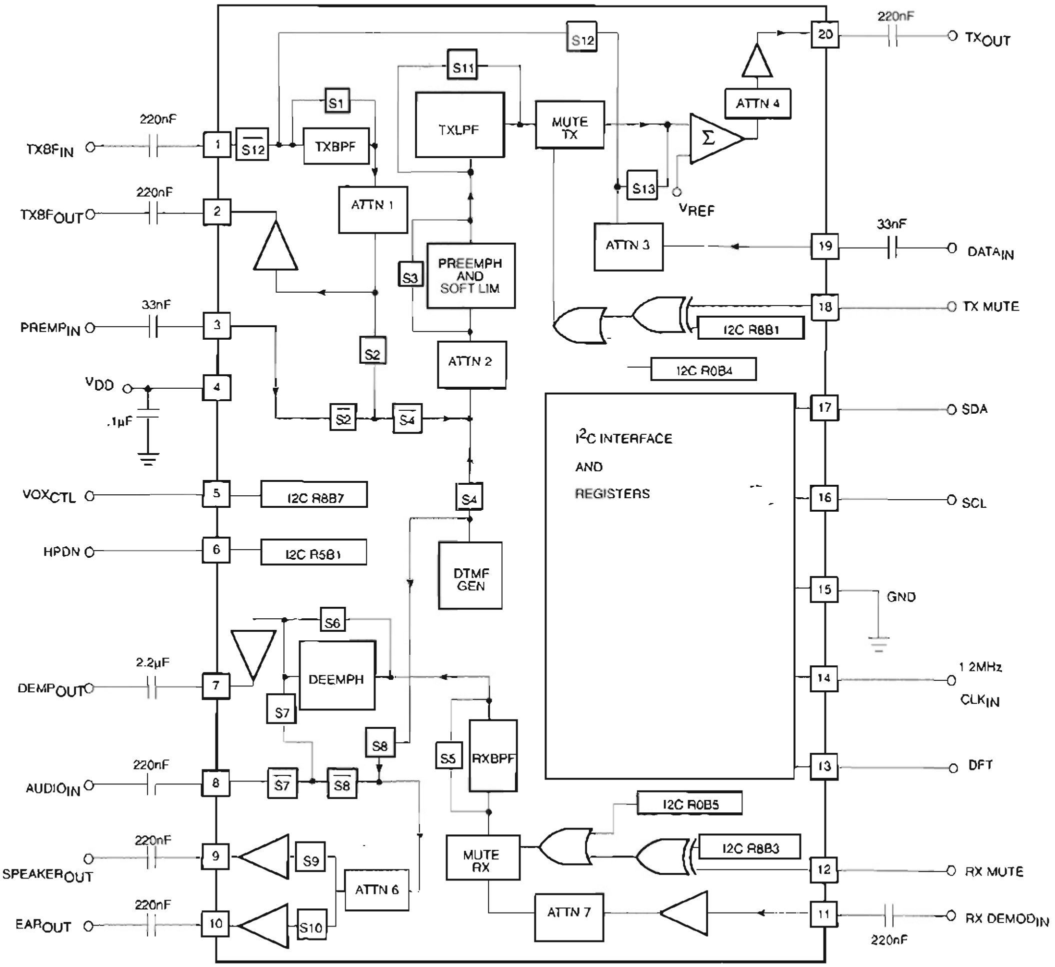


Figure 8. NE/SA5753 Test and Application Circuit

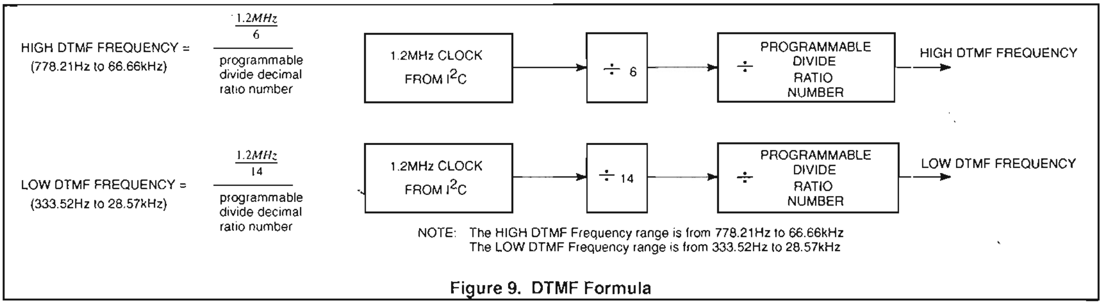

HIGH DTMF FREQUENCY =
(778.21Hz to 66.66kHz)
1.2MHz / 6
programmable divide decimal ratio number
1.2MHz CLOCK FROM I²C
÷ 6
PROGRAMMABLE ÷ DIVIDE RATIO NUMBER
HIGH DTMF FREQUENCY
LOW DTMF FREQUENCY =
(333.52Hz to 28.57kHz)
1.2MHz / 14
programmable divide decimal ratio number
1.2MHz CLOCK FROM I²C
÷ 14
PROGRAMMABLE ÷ DIVIDE RATIO NUMBER
LOW DTMF FREQUENCY
NOTE: The HIGH DTMF Frequency range is from 778.21Hz to 66.66kHz
The LOW DTMF Frequency range is from 333.52Hz to 28.57kHz

Figure 9. DTMF Formula

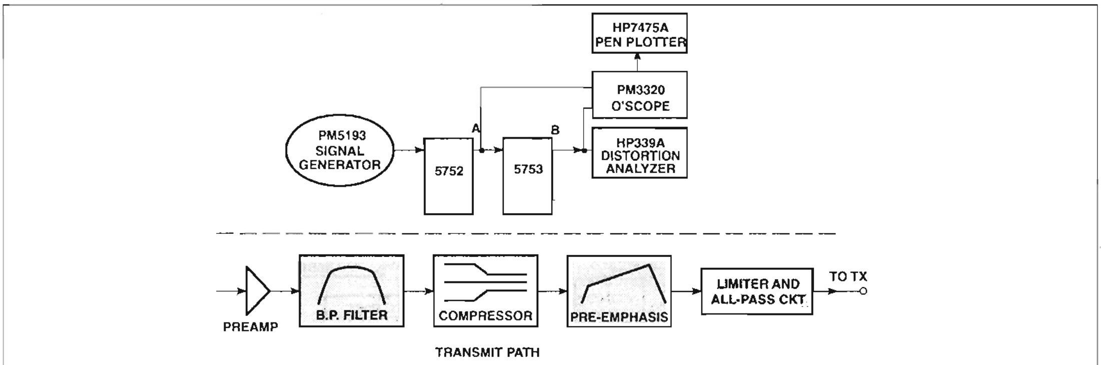


Figure 10. . Test Set-up and Tx Path of Signal

tone DTMF generator, load a binary 2 or 0000 0010 to the register.

Example 1

Program the SA5753 DTMF generator such that High DTMF = 4000Hz and Low DTMF = 3061.22Hz.

1. Using the formula in Figure 9,
   High DTMF 'divide ratio number' = 50
   Low DTMF 'divide ratio number' = 28
2. Convert 'divide ratio number' into a binary number
   High DTMF binary 'divide ratio number' = 0011 0010
   Low DTMF binary 'divide ratio number' = 0001 1100.
3. Load binary numbers into proper registers and observe on a spectrum analyzer.

Example 2

Program the SA5753 DTMF generator such that High DTMF = 778.21Hz and Low DTMF = OFF.

1. Calculate 'divide ratio number' using the formula in Figure 9,
   High DTMF 'divide ratio number' = 257
   Low DTMF 'divide ratio number' = 2, by definition for OFF see Table 8.
2. Converting 'divide ratio numbers'
   High DTMF binary 'divide ratio number' = 0000 0001 (remember the special case that applies here)
   Low DTMF binary 'divide ratio number' = 0000 0010.
3. Load binary numbers into proper registers and observe on a spectrum analyzer.

Programmable Transmit and Receive Mute Polarity Function

If a designer wants to operate the SA5753 at 3V and wants to mute the TxMute and RxMute pins with a 5V logic '1' signal, a series 10k resistor should be used. If the 10k resistor is not used, the SA5753 will draw more current. To eliminate the 10k resistor the designer should make sure that the logic '1' signal never exceeds V_{CC}.

The Limiter and All-Pass Circuit

An important aspect of the AMPS specification is concerned with the 12kHz maximum frequency deviation. The output of the APROC TX_{OUT} should be limited at a level which causes a maximum frequency deviation of 12kHz for the transmitter, regardless of the amplitude of the input signal. Figure 10 shows the equipment used for the test measurements and how the signal was processed. A 1kHz signal was applied to the input of the demo-board until a 5% distorted signal was measured at the limiter output. This waveform's peak-to-peak voltage was recorded as a reference. Then, at various chosen frequencies, the input of the demo-board was overdriven so we could record the distorted peak-to-peak waveform. (See Figure 11)

Formula 4 was used to calculate maximum frequency deviation from the waveforms shown in Figure 11.

$$\text{Max Freq Dev with All-Pass Ckt} = \left(\frac{BW_F}{BW_R}\right) 8\text{kHz} \qquad (4)$$

where

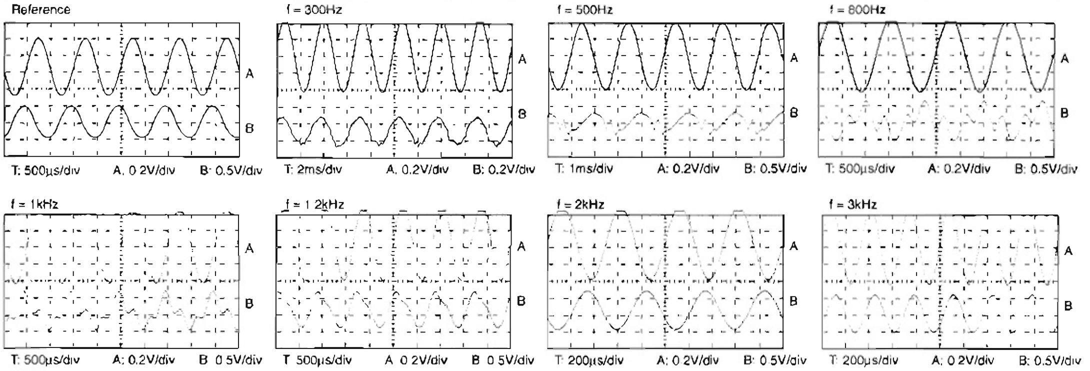
BW_F = the bottom waveform's peak-to-peak voltage from one of the observed figures.

BW_R = the bottom waveform's peak-to-peak voltage from the reference Figure 11.

for the 12kHz Test

Table 9. Maximum Frequency Deviation Results

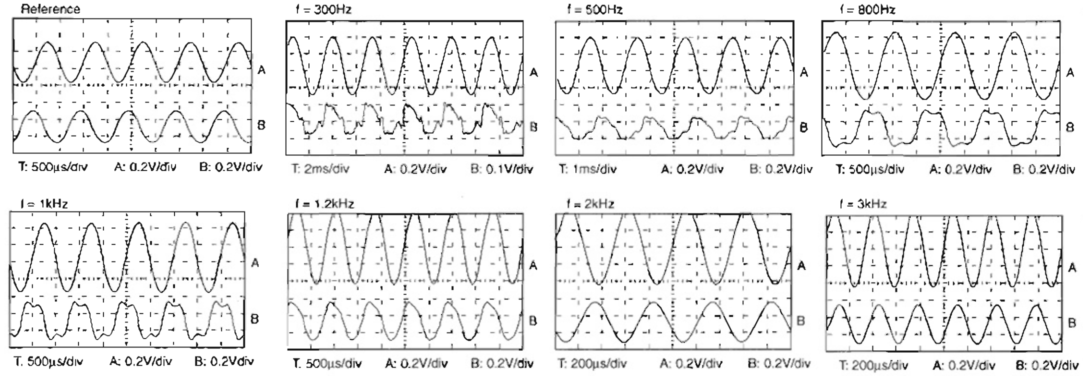
Frequency (Hz)	With All-Pass (kHz)
300	3.58
500	5.61
800	10.13
1000	10.01
1200	9.21
2000	10.01
3000	9.61



WAVEFORM A: INPUT TO SA5752 PREAMP

WAVEFORM B: OUTPUT TO SA5753 TX_{OUT} PIN

Figure 11. Results from the AMPS 12kHz Maximum Frequency Deviation Test



WAVEFORM A: INPUT TO SA5752 PREAMP

WAVEFORM B: OUTPUT TO SA5753 TX_{OUT} PIN

Figure 12. Results from the NAMPS 5kHz Maximum Frequency Deviation Test

Table 9 reveals the calculated results for maximum frequency deviation over the voice band. The test results show that the NE5752 and NE5753 will meet the 12kHz AMPS specification.

The same test set-up was used for the NAMPS measurements, however, the maximum frequency deviation formula changes. The following formula shows how to calculate the maximum frequency deviation for NAMPS:

Max Freq Dev with All-Pass Ckt =

$$\left(\frac{BW_F}{BW_R}\right) 2.9\text{kHz} \quad (5)$$

where

BW_F = the bottom waveform's peak-to-peak voltage from one of the observed figures.

BW_R = the bottom waveform's peak-to-peak voltage from the reference Figure 12.

Table 10. Maximum Frequency Deviation Results for the 5kHz Test

Frequency (Hz)	With All-Pass (kHz)
300	1.48
500	2.11
800	3.27
1000	3.46
1200	3.42
2000	3.65
3000	3.56

Formula 5 was used to calculate the maximum frequency deviation in Table 10 from the waveforms shown in Figure 12. These test results show that the APROC II will meet the 5kHz maximum frequency deviation for NAMPS.

IV. EVALUATION SOFTWARE AND DEMOBOARD

The APROC II demoboard and evaluation software are for evaluation purposes only. It can help a designer understand the hardware and software functionality. The APROC II schematic and layout can be seen in Figures 13 and 14, respectively. The function of each external component is briefly shown in Figure 13.

In this software package, the screen (see Figure 15) only shows the signal path for the SA5753. Recall that for the audio processing chip, the signal is routed between the SA5752 and SA5753. The appropriate pin numbers are labeled to show where the signal enters and leaves the SA5753.

The upper half of the screen is the Tx path and the lower half of the window is the Rx path. To complete the signal path, a designer can use the computer's arrow keys to get to the area of interest. The space bar is used to toggle on and off path switches and key functions (like NAMPS, VCO, HPDN, VOX_{CTRL} etc).

The 'greater than' (>) or 'less than' (<) symbol keys on the key board are used to vary the value of the gain attenuator blocks. The way the gain attenuator blocks are programmed does not follow the logical way where the 'greater than' symbol key means going up in gain and the 'less than' symbol means decreases gain. Instead, the set up is programmed logically by the bits. So a user should use the 'greater than' and 'less than' symbol keys to vary the value, but continue to use the keys until the values stop changing. (See Table 11.)

To power down the chip set the following steps should be taken:

1. To power down the SA5752, move the marker to HPDN and hit the space bar to implement this function.

2. To implement one of the SA5753 three power down modes move the marker to the Power = 000 Bin and program the appropriate mode.

- For PWDN, set Power=1xx Bin; X=don't care
- For IDLE, set Power = 011 Bin
- For the DENA mode, set Power= 010 Bin
- For normal operation, set Power= 000 Bin
- For $DATA_{IN}$ to TX_{OUT} disabled, set Power= 001 Bin. This can be used for cordless applications

To power up the chip set, a designer needs to set the Power=000 Bin (for the SA5753) and toggle the HPDN section (for the SA5752).

DTMF

To implement the DTMF tones, a user can program the high and low tones by typing in the frequencies or programming the I^2C bits.

The high decimal value is from 2 to 257 where the frequency range is from off to 778.21Hz–66.66kHz. The low decimal value is from 2 to 257 where the frequency range is from off to 333.52Hz up to 28.57kHz.

The difference between the SA5753 DTMF generator and the SA5751 is that when the cycle is completed, the DC voltage goes back to 0V, whereas the SA5751 might not return to 0V. Therefore, upon switching back to the Tx voice path, a glitch may be heard from the SA5751, but not from the SA5753.

V. QUESTIONS AND ANSWERS SECTION

Q: I connected your evaluation board and software program but I do not see any output signal on the Transmit path. My input signal is connected to the Mic input of the SA5752. What is the problem?

A: There are several issues to look at. Make sure that the TxMute and RxMute pins are defined. If the registers are programmed such that the TxMute and/or RxMute pins need to be grounded for a signal to flow, please be sure that those pins are grounded.

If the registers are defined such that the TxMute and RxMute pins need V_{CC} connected to them for a completed signal path, please connect V_{CC} to the pins. Although leaving these pins open may work, it defines an open state and is, therefore, not guaranteed.

Q: When I program a DTMF tone, it only stays on for 96ms. How can I make it stay on longer?

A: The DTMF generator is designed to stay on for only 96ms. If a longer tone is desired, the DTMF registers must be re-loaded before the 96ms expires or set DTC = 1. For the evaluation program, the DTMF register can be loaded up automatically to observe the DTMF tone. Just toggle the space bar on the "DTMF frequency DTC" section.

Q: On the evaluation program, there are ADD field and REG values. What are these?

A: These are the registers (ADD = Address field and REG = the register) that must be programmed when using the SA5753 in the I^2C mode. The address field defines which portion of the chip is being accessed (See SA5753 data sheet for a detail look). The register bits control the functions of the block.

If a designer toggles in/out functions, they can see the registers which control that function. The Evaluation software is meant as a learning tool to aid the designer in getting up to speed.

Q: The SA5753 seems to be consuming more current than usual. Is this part damaged?

A: One area to look at is the I^2C clock. If the I^2C clock goes below ground, the SA5753 will draw more current. Therefore, be sure that the I^{2}C clock is set at 1.2MHz square wave and it is from ground to V_{CC}.

Q: I have a Philips APROC II demoboard and a 5V I^{2}C interface board. At the present moment, I use two supplies to run the APROC II board at 3V and the interface board at 5V. Is there a 3V chip available that can be used for the interfacing between the computer's printer port to the I^{2}C section of the chip?

A: Yes, there is a 3V interface chip; the Philips PC74HC4049T. When a customer purchases an APROC II demoboard, he/she should receive an interface board. Most likely it will be the 3V version.

Q: The APROC II seems to draw more current than usual when I mute the TxMute and RxMute pins with a 5V logic '1' signal. The APROC II is operating at 3V. Is this normal, and if not, what can I do?

A: If you are going to operate the APROC II at 3V and apply 5V to the RxMute and TxMute pins, a series 10k resistor should be used to allow for this configuration.

If the logic '1' input is 3V and the APROC II is operating at 3V, the 10k resistor is not required. In general, it is safe to say that the logic '1' input should be no higher than V_{CC} if the 10k resistor is not used.

Q: I am evaluating your DTMF generator using the Philips evaluation program and demoboard. The frequency calculated and the frequency measured is correct but The evaluation screen, however, sometimes shows a different number, but the number shown is not too far off. Is there a bug in the program?

A: Yes, the program display is not correct. What you calculate and measure is fine. The program is incorrect at this time.

Q: I am evaluating the current consumption of the APROC II demoboard. I read a higher current than what is spec'd in the data sheet. What am I doing wrong?

A: Remember that the I^{2}C interface card will draw some current away from the APROC II board (if it's connected that way). To avoid this problem, operate the I^{2}C interface card with a separate power supply and then measure the APROC II current.

Q: I have your APROC II evaluation demoboard. I am applying an input signal of 1kHz at 100mV$_{RMS}$ to the MIC input and I am not getting any signal output on the TX$_{OUT}$ pin. Any suggestions?

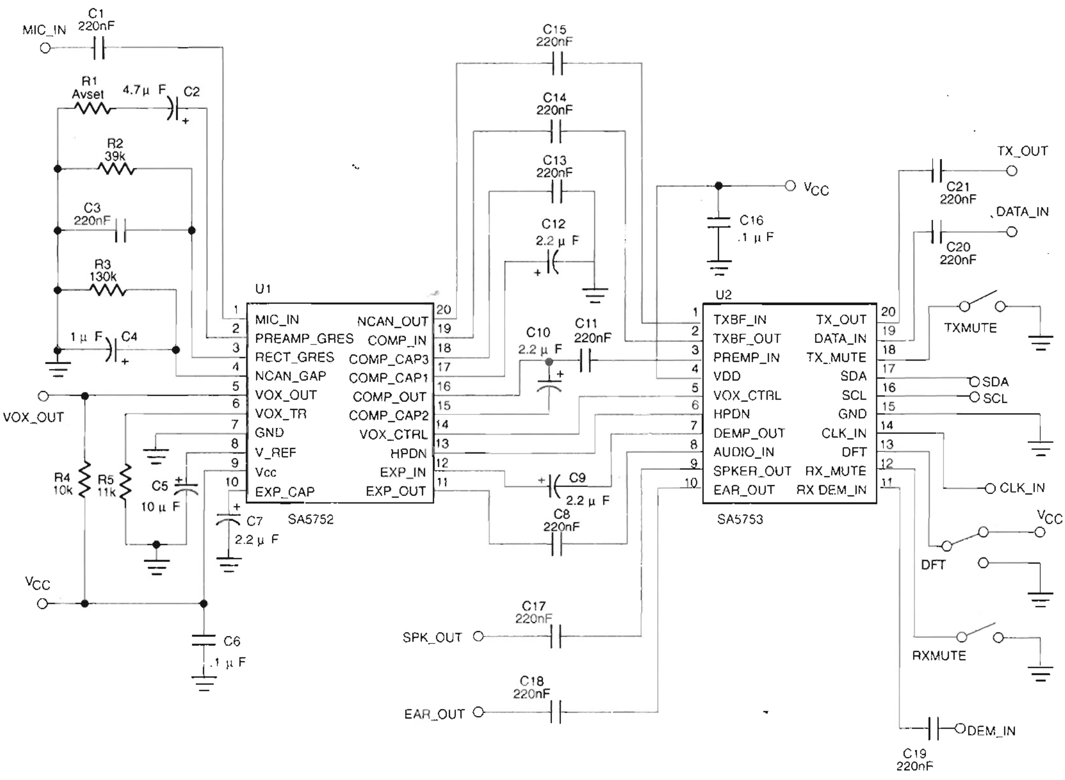
A: Your transmit path is probably open. To close the path you can do one of two things: either ground the TxP Mute pin (Pin 18) or redefine TxP to mute for a different input. You should also make sure that the SA5752 and SA5753 are in the power up state.

Q: I have a very unique situation using the SA5753. I would like to use the Default mode and I^{2}C mode in different situations. I know that the HPDN pin becomes an output when I^{2}C mode is implemented; and I know that the HPDN pin becomes an input when the Default mode is implemented. In my application I do not care about current consumption, therefore, the HPDN pin is not important to me. What can I do so that I don't leave the HPDN undefined, but at the same time, I allow myself to switch back and forth between the two modes?

A: For ease of use in the Default Mode without worrying about the function of the HPDN pin, the user can add an external pull-up resistor of 100kΩ between HPDN (Pin 6) and V_{DD}. This will put the SA5753 in Normal (active) Default operation when DFT (Pin 13) is pulled HIGH. For Power Down Mode the user will need to pull the HPDN pin LOW.

Using the SA5752 and SA5753 for low voltage designs

AN1742



Component Functions

C1	DC blocking capacitor for MIC IN pin
C2	DC blocking capacitor for Preamp gain
C3	Used for filtering, internal use only
C4	Used to set attack and release time of VOX
C5	V_{REF} filter capacitor
C6	V_{CC} bypass capacitor
C7	Sets attack and release time of expandor
C8	DC blocking cap for Expandor out
C9	DC blocking cap for De-emphasis out
C10	AC bypassing for compressor
C11	DC blocking cap for Pre-emphasis in
C12	Sets attack and release time for compressor
C13	Passes AC to GND
C14	DC blocking cap for compressor in
C15	DC blocking cap for TXBF in
C16	V_{CC} bypass cap
C17	DC blocking cap for SPKR OUT
C18	DC blocking cap for EAR OUT
C19	DC blocking for Demodulation in pin
C20	DC blocking for Data in pin
C21	DC blocking cap for Tx OUT
R1	Sets microphone preamp gain
R2	Sets gain of VOX, but for internal use only. Effects voltage on Pin 4.
R3	Used to set the release time of VOX
R4	Pull-up resistor to get logic level out
R5	Sets threshold level of VOX

Figure 13. APROC II Evaluation Board Schematic

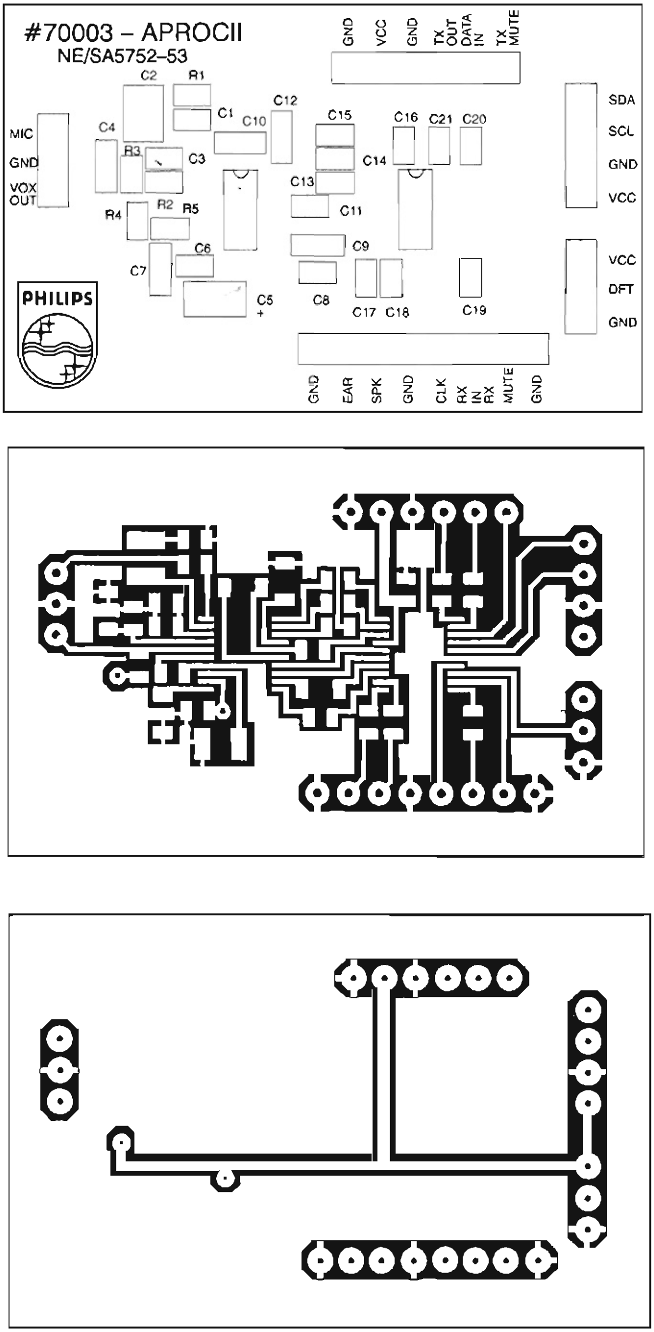


Figure 14. APROC II Evaluation Board Layouts

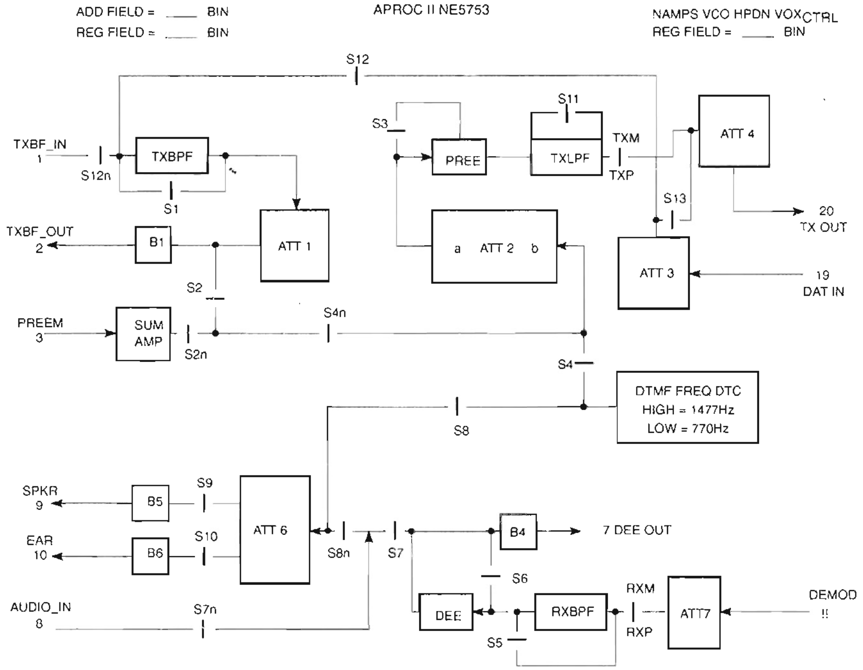


Figure 15. Graphical Display of SA5753 I^{2}C Evaluation Program

Table 11. Gain Attenuator Steps

SYMBOL	Sequence of Gain Attenuator Steps
A1	0, –0.8, –1.6, –2.4, –3.2, –4.0, –4.8, –5.6, –6.4, –7.2, –8.0, –8.8, –9.6, –10.4 –11.2, –12
A2a	0, 0.25, 0.50, 0.75, 1.00, 1.25, 1.50, 1.75, 2.00, 2.25, 2.50, 2.75, 3.00, 3.25, 3.50, 3.75, 0, –0.25, –0.50, –0.75, –1.00, –1.25, –1.50, –1.75, –2.00, –2.25, –2.50, –2.75, –3.00, –3.25, –3.50, –3.75
A2b	0, –12, –18, –24
A3	–2, –3, –4, –5, –6, –7, –8, –9, –10, –11, –12, –13, –14, –15, –16, –17
A4	0.5, 1.0, 1.5, 2.0, 2.5, 3.0, 3.5, 0, –0.5, –1.0, –1.5, –2.0, –2.5, –3.0, –3.5
A6	0, –2, –4, –6, –8, –10, –12, –14, –16, –18, –20, –22, –24, –26, –28, –30
A7	0, 0.5, 1, 1.5, 2, 2.5, 3, 3.5, 0, –0.5, –1, –1.5, –2, –2.5, –3, –3.5

Power amplifier controller for GSM systems PCA5075

FEATURES

.CMOS low power

.General purpose controller for Power Amplifier modules in GSM systems.

.High speed serial interface.

Power down mode.

.1 Mhz bandwidth suppresses AM-distortion of the power amplifier.

.On-Chip rampgenerator for all 16 GSM mobile station Power levels.

.Suitable for base station applications.

.On-chip detection for Quick-Restart. (base station applications only).

.Programmable analog output voltage limitation.

.Programmable integrator start condition.

.Ramp-up/timing related to the 13 Mhz GSM system frequency clock.

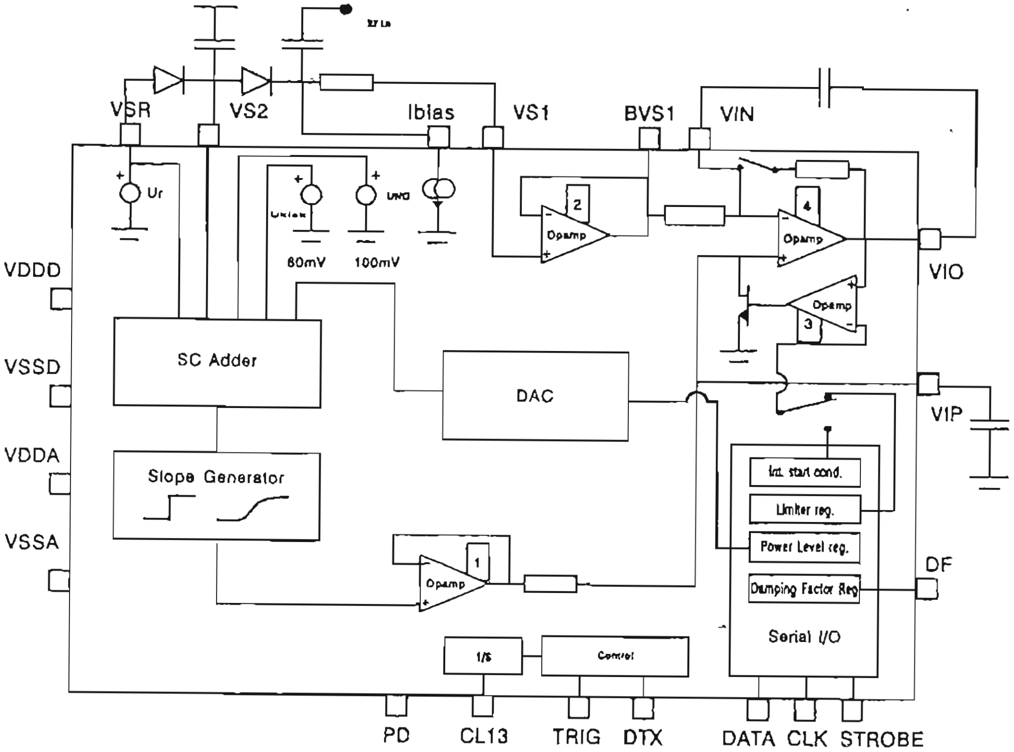
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VDD	supply voltage	2.9	5.0	6.0	V
IDD	supply current		8.5		mA
Tamb	ambient temp.	-40		+70	C

ORDERING INFORMATION

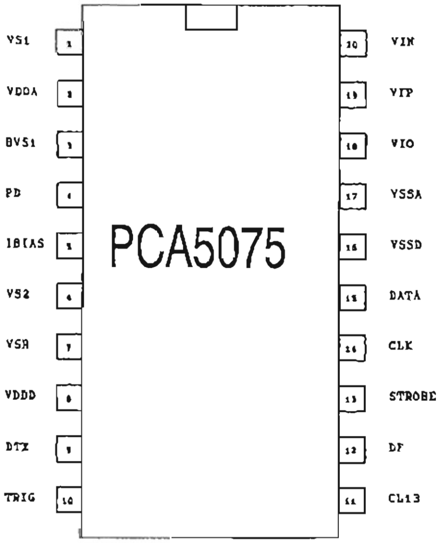
EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA5075	20	SSOP20	Plastic	SOT266

Figure 1. : Blockdiagram PCA5075



PIN CONFIGURATION.

SYMBOL	PIN	TYPE	DESCRIPTION
VS1	1	I	Sensor signal 1
VDDA	2	-	Analog positive supply
BVS1	3	O	Buffered sensor signal 1
PD	4	I	Power Down
IBIAS	5	I	Current reference for external rectifier
VS2	6	I	Sensor signal 2
VSR	7	O	Bias voltage for sensor
VDDD	8	-	Digital Supply
DTX	9	I	Disable speech transmission
TRIG	10	I	Trigger signal
CL13	11	I	13 Mhz GSM clock
DF	12	O	Damping switch control signal. (only for base-station applications).
STROBE	13	I	Serial bus strobe signal
CLK	14	I	Serial bus clock signal
DATA	15	I	Serial bus data signal
VSSD	16	-	Digital negative supply
VSSA	17	-	Analog negative supply.
VIO	18	O	Integrator Output voltage
VIP	19	I	Integrator positive input voltage
VIN	20	I	Integrator negative input voltage.



Functional description

This CMOS device integrates Opamps, a DA-Converter and a serial interface to implement an Integrating-Controller.
It is designed to control both the power level and the power up/down ramping of a GSM-transmitter.
All 16 GSM mobile station power up/down ramping curves (including sensor non-linearity) are generated on chip.
This device is also suitable for base stations. The extra base station ramp curves are generated by using an external damping network in front of the (external) rectifier and by decreasing the value of R1. This extra damping network and the additional resistor in parallel with R1, are activated when the signal DF is high. This DF signal again, is directly controlled by the Damping factor register.

The device operates on an internal clock frequency of 2.166 Mhz, (T_x=1/2.166 uS) that is generated on Chip by dividing the external 13 Mhz clock by six.

Generally the power amplifier is ramped up after a rising edge on TRIG and ramped down after a falling edge.
When a quick restart is detected (Base-station applications only), the integrating controller is not totally turned off. This enables the controller to ramp-up faster after a ramp-down.
A quick restart is executed when TRIG is low for only a very short period of T_{QRS}.
To detect a quick restart, all ramping is delayed wrt. TRIG by 2 * T_x.

To match the controller to different Power-amplifiers, the controller output VIO can be limited to 4 V, 4 V - V_{diode} or 4 V - 2 V_{diode}, depending on the contents of the limiter register.

The contents of the power level register determines which of the 16 ramp-curves is taken during ramp-up/down.

When the integrator is inactive, the controller output VIO will have a (programmable) voltage of 0.3 V , 0.3 V + V_{diode}, 2 V_{diode} - 0.05 V or 2 V_{diode} + 0.2 V, depending on the contents of the integrator start condition register.

When DTX becomes active during a ramp-up, ramping is immediately stopped and a down ramp is executed, turning the power amplifier off.

Separate power pins are provided to the analog and digital blocks.

The register information is written via a three wire serial bus.

The analog Integrating-Controller.

The analog Integrating controller consists out of four Opamps.
Opamp 1 and Opamp 2 are only used for buffering purposes.
Opamp 4 is used to make a differential integrator, whereas Opamp 3 is used to limit the integrator output voltage, and to set the integrator start condition ("homeposition") when the integrator is inactive.

A two-diode external rectifier is connected to pins VSR, VS2, Ibias and VS1.
The SC-Adder block, basically generates the voltage VSR - 2 U_d + U_{dac}.
The differential integrator the integrates the difference of this voltage and the voltage VSR - 2 U_d + U_{set} . The integrator output voltage is used to control the power amplifier module.

Ramp generation.

Ramp-up.

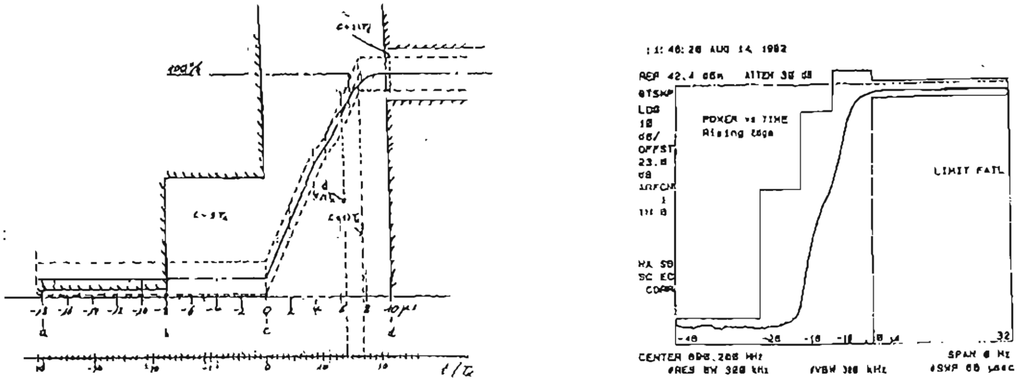


Fig 2a (left) and 2b (right).

Figure 2a shows the timing of a typical ramp-up curve. Figure 2b shows a measured ramp-up curve of a discrete controller implementation.

If no quick restart was detected during the last ramp-down, the controller was in "homeposition" before time B. The integrator output voltage is regulated to the value defined in the Integrator start condition register. The output of the adder and the slope generator is U_{kick} + VSR - $2U_d$. (U_{kick} is typically 60 mV).
The differential integrator input is U_{kick}.
On time B the integrator start condition circuitry is turned off. Due to the positive differential input voltage, the integrator output will start to rise.
If a quick restart was detected during the last ramp-down, the integrator start condition circuitry has already been turned off. In this case the output voltage of both adder and slope generator is VSR - $2U_d$.

On time C the DAC generates a new output voltage U_{dac}. The output of the adder block is now: VSR - $2U_d$ + U_{dac}. The slope generator will generate a "smooth" curve between the former and the newer output value of the adder block. The power amplifier is ramped up via the integrator.

On time D the new output value of the slope generator is reached.

Ramp-down.

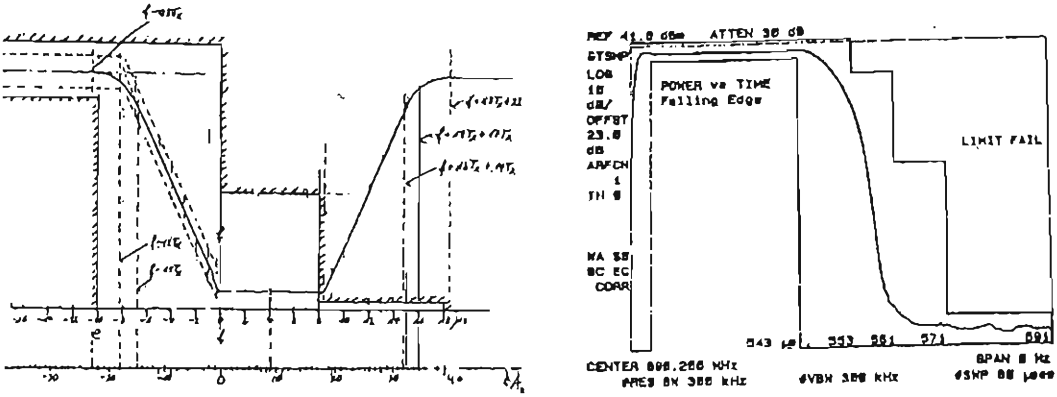


Figure 3a (left) and Figure 3b (right).

In Figure 3a, the timing of a typical ramp-down curve is shown, Figure 3b shows again measurements on a discrete implementation of this controller.

On time E the ramp-down is started.
If a quick restart was detected the adder output voltage after time E will be: VSR - $2U_d$
If not, the adder output voltage after time E will be: VSR - $2U_d$ - U_{NO}, with U_{NO} typically 100mV.
The slope generator again generates a "smooth" curve between the new adder output voltage and the old adder output voltage.

On time F the output of the slope generator has reached its final value.

If a quick restart was detected, a ramp up will be executed.
The adder output voltage will be VSR - $2U_d$ + U_{dac}.

If, however, no quick restart was detected, the integrator will be turned into its "homeposition". The integrator output voltage will be regulated again to the value defined in the integrator start condition register. Also the adder output voltage will be VSR - 2 U_d + U_{kick}.

Serial Programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 wires are: *Data Clk and Strobe*. The data sent to the device are loaded in bursts framed by Strobe. Programming clock edges and their appropriate data bits are ignored until Strobe goes active low. The programmed information is loaded into the addressed latch when *Strobe* returns inactive high. Only the last 18 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. If *Strobe* returns high wile *Clk* is still low, the extra clock edge produced causes data shift. The fully static CMOS design uses virtually no current when the bus is inactive.

Data Format

Data is entered with the most significant bit first. The leading bits make up the data field, whilst the trailing four bits are an address field. The PCA5075 uses only 1 of the available addresses. The format is shown below; the first entered bit is p1, the last one p18.

PROGRAMMING REGISTER BIT USAGE									
p18	p17	p16	p15	p14	p13	p12	pxx	p2	p1
add0	add1	add2	add3	data0	data1	data2	datax	data12	data13
Latch address				LSB		data			MSB

The trailing address bits are decoded upon the inactive *Strobe* edge. This produces an internal load pulse to store the data in one of the addressed latches. To avoid erroneous circuit operation, the pulse is not allowed during data reads by the rest of the circuit. This condition is guarantee by respecting a minimum *Strobe* pulse width after data transfer.
The correspondence between data fields and addresses is provided in the following table:

REGISTER BIT ALLOCATIONS																	
p 1	p 2	p 3	p 4	p 5	p 6	p 7	p 8	p 9	p 10	p 11	p 12	p 13	p 14	p 15	p 16	p 17	p 18
d13	d12	data field												address			
Power Level								DF1	DF0	L1	L0	IS1	IS0	1	0	1	0

DF = Damping Factor.

DF0 = data on DF output
DF1 = enable of this output.

L = Limiter voltage.

L1	L0	Limiter voltage
1	1	4 - 2 Vd
1	0	4 - Vd
0	X	4

IS = Initial start condition.

IS1	IS0	Initial value of VIO
0	0	0.3 V
0	1	0.3 V + Vd
1	0	-0.05 V + 2 Vd
1	1	0.2 V + 2 Vd

Specifications of Opamp4.

Tamb= -40 to 70 C , VDD = VDDA = VDDD unless otherwise specified.

SPEC	MIN.	TYP	MAX	UNIT	CONDITION
VDD	2.9		6.0	V	
additional peaking in integrator amplitude characteristic.			3	dB	Integrator Loop closed. R2=8.2 Kohm, C1=180 pF F=7 Mhz
additional phase shift in integrator application			30	deg.	Integrator Loop closed. R2=8.2 KOhm, C1=180pF F= 7 Mhz.
CMMR	?			dB	
PSRR+	?			dB	
PSRR-	?			dB	
SR+	1			V/uS	
SR-	1			V/uS	
Dynamic range common mode input signal	4.2			V	Vdd = 5V
VIO Output voltage	0.3		4	V	Vdd = 5V
Rin	?			Ohm	
Rout	?			Ohm	

Specifications of Opamp 1 and 2.

Tamb= -40 to 70 C , VDD = VDDA = VDDD = 5V unless otherwise specified.

SPEC	MIN.	TYP	MAX	UNIT	CONDITION
VDD	2.9		6.0	V	
3-Db point	4			Mhz.	Z1= 1/(s*62pF)+8.2Kohm
Gain peaking			3.0	dB	"
Dyn. ranges comm.mode	4.2			V	"
SR+, SR-	1/3			V/uS	"

Specifications of DAC8.

Tamb= -40 to 70 C , VDD = VDDA = VDDD=5V unless otherwise specified.

SPEC	MIN.	TYP	MAX	UNIT	CONDITION
INL			+/- 1	LSB	
DNL			+/- 1	LSB	
Fs	2.5			Mhz	Load = 4pF
Output range	Ur			V	Reference=Ur

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)
VDD = VDDD = VDDA, VSS = VSSA = VSSD

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
VDD	Supply voltage	.5	6.0	V
Vi	DC input voltage on all pins	-0.5	VDD	V
IDD	Supply current	-	11.5	mA
Ptot	Total power dissipation		tbf	mW
Tstg	Storage temperature range	-65	150	C
Tamb	Operating ambient temperature	-40	70	C

DC CHARACTERISTICS

Tamb= -40 to 70 C , VDD = VDDA = VDDD, VSS = VSSA = VSSD, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VDD	Supply voltage range		2.9	5.0	6.0	V
IDD	Total operating current	CLK13= 13 MHz		8.5		mA
IDDq	Total quiescent current	PD = High			10	uA
Logic inputs ; Pin nrs. 5,8-13						
VIL	Input voltage low		0.3*VDD			V
VIH	Input voltage high				0.7*VDD	V
IL	Input leakage current		-5		5	uA
Cin	Input capacitance			10		pF

Analog Inputs

Tamb= -40 to 70 C, VDD = VDDA = VDDD = 5 V, VSS = VSSA = VSSD = 0 V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VS1	Sensor signal 1		0.8		4.2	V
VS2	Sensor signal 2				VSR	V
IL	Input leakage current		-5		5	uA
Cin	Input capacitance				10	pF

Controller timing characteristics.

VDD = VDDA = VDDD = 5 V, VSS = VSSA = VSSD, T= -40 to 70 C unless otherwise specified.
For signal explanation see Fig. 2 and 3. TX = 6/13 uS.

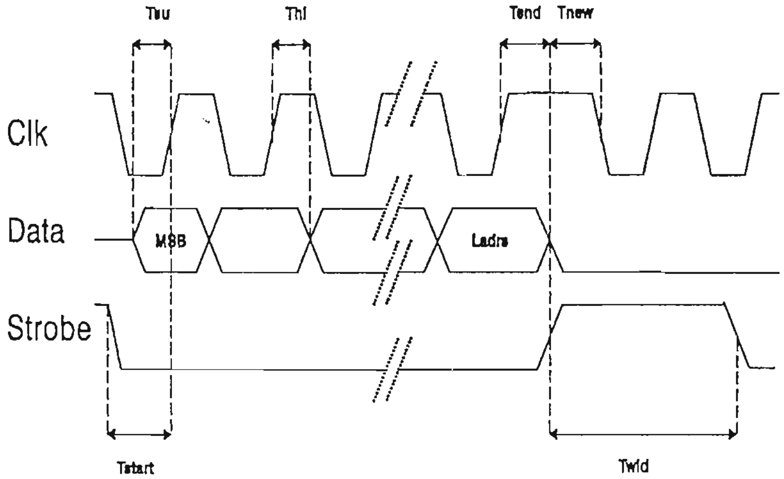
SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNIT.
TQRS	Negative pulse width on TRIG for quick restart recognition.	TX/3		2*TX	S
TB	Delay from positive TRIG edge to point B. (See Fig. 2)		2TX		S
TC	Delay from positive TRIG edge to point C. (See Fig. 2)		TB+18TX		S
TD	Delay from positive TRIG edge to point D. (See Fig. 2)		TC+22TX		S
TF no qrs	Delay from negative TRIG edge to point F. (See Fig. 3)		2TX +22TX		S
TF w. qrs	Delay from negative TRIG edge		3TX +22TX		S

Analog Output

Tamb= 25 C, VDD = VDDA = VDDD = 5 V, VSS = VSSA = VSSD = 0 V, unless otherwise specified.

SYMBOL	PARAMETER	TC	MIN.	TYP.	MAX.	UNIT
VSR	Bandgap +/- 4%	-0.175 mv/C	1.2	1.25	1.3	V

Serial Bus Timing characteristics.

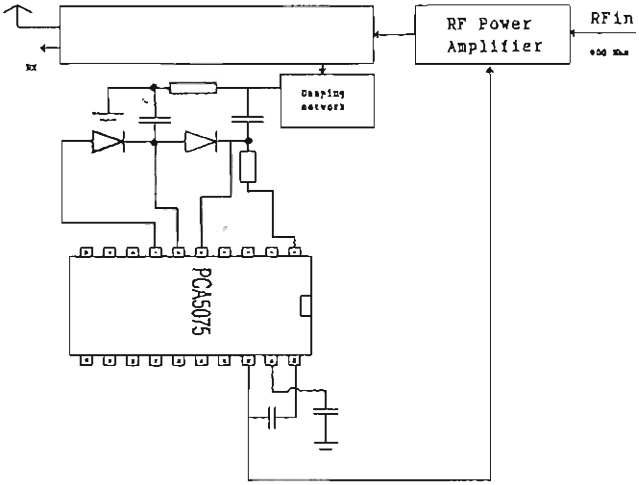


VDD = VDDA = VDDD = 5 V, VSS = VSSA = VSSD = 0 V, T = -40 to 70 C unless otherwise specified.

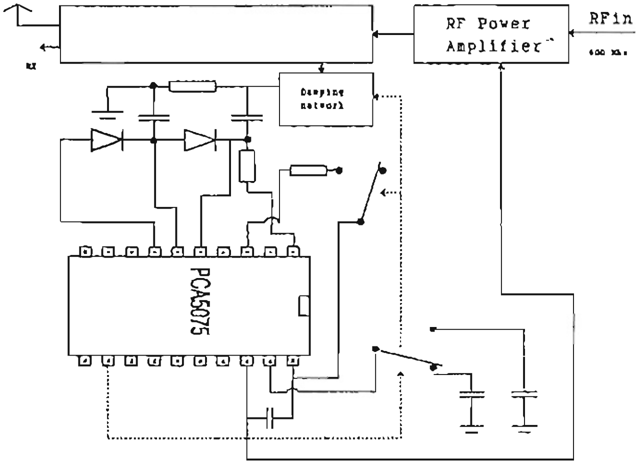
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial programming Clock (Pin CLK)						
Tr,Tf	Input rise and fall times			10	40	ns
Tcyc	Clock period		100			ns
Enable programming (Pin Strobe)						
Tstart	Delay to rising clock edge		40			ns
Tend	Delay from last clock edge		10			ns
Twid	Minimum inactive pulse width		100			ns
Tnew	Delay from TRIG inactive to new data		200			ns
Register serial input data (pin Data)						
Tsu	Input data to CLK setup time		20			ns
Thl	Input data to CLK hold time		20			ns

* NOTE: After rising edge of STROBE one more CLK low period completes the transfer.

Application Diagram



Application diagram Mobile Station



Application Diagram Base Station.

Advanced POCSAG paging decoder

PCD5003

FEATURES

- Wide operating supply voltage range: 1.5 to 6.0 V
- Low operating current: 50 μA typ. (ON), 25 μA typ. (OFF)
- Temperature range: –25 to +70 °C
- *"CCIR Radio paging Code No. 1"* (POCSAG) compatible
- 512, 1200 and 2400 bits/s data rates using 76.8 kHz crystal
- Built-in data filter (16-times oversampling) and bit clock recovery
- Advanced ACCESS synchronization algorithm
- 2-bit random and (optional) 4-bit burst address error correction
- Up to 6 user addresses (RICs), each with 4 functions/alert cadences
- Up to 6 user address frames, independently programmable
- Standard POCSAG sync word, plus up to 4 user programmable sync words
- Received data inversion (optional)
- Call alert via beeper, vibrator or LED
- 2-level acoustic alert using single external transistor
- Alert control: automatic (POCSAG), via cadence register or alert input pin
- Separate power control of receiver and RF-oscillator for battery economy
- Synthesizer set-up and control interface (3-line serial)
- On-chip EEPROM for storage of user addresses (RICs), pager configuration and synthesizer data
- On-chip SRAM buffer for message data
- Slave I^2C-bus interface to microcontroller for transfer of message data, status/control and EEPROM programming
- Wake-up interrupt for microcontroller, programmable polarity
- Direct and I^2C-bus control of operating status (ON/OFF)
- Battery-low indication (external detector)
- Out-of-range condition indication
- Real time clock reference output
- On-chip voltage doubler.

APPLICATIONS

- Display pagers, basic alert-only pagers
- Information services
- Personal organizers
- Telepoint
- Telemetry/data transmission.

GENERAL DESCRIPTION

The PCD5003 is a very low power POCSAG decoder and pager controller. It supports data rates of 512, 1200 and 2400 bits/s using a single 76.8 kHz crystal. On-chip EEPROM is programmable at 2.5 V minimum supply. The PCD5003 is Fast I^2C-bus compatible (maximum 400 kbits/s).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5003H	TQFP32	plastic thin quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1
PCD5003U/10	–	film-frame carrier (naked die) 32 pads	

BLOCK DIAGRAM

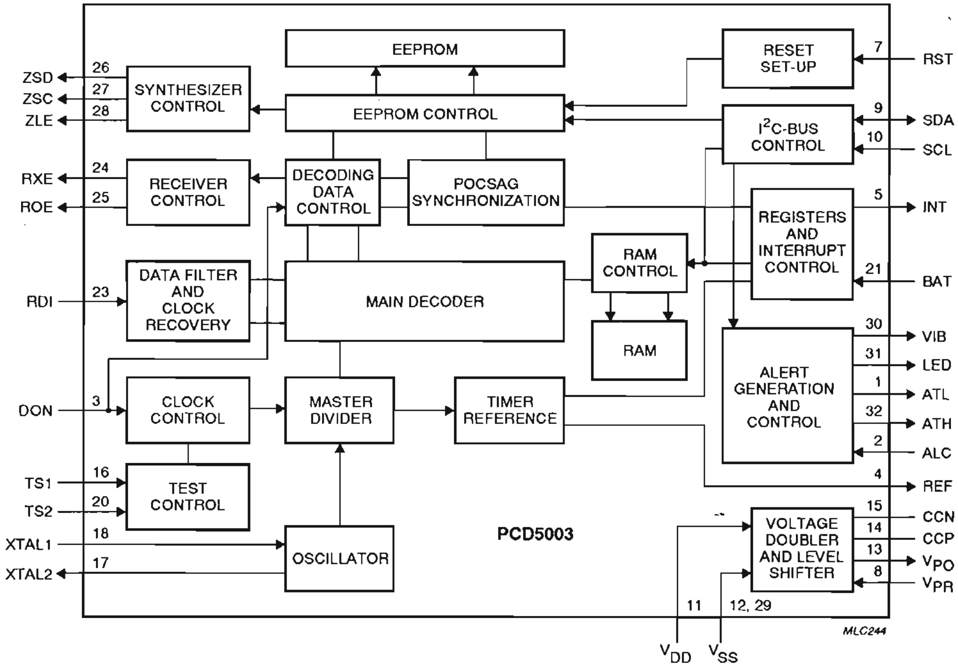


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
ATL	1	alert LOW-Level output
ALC	2	alert control input (normally LOW by internal pull-down)
DON	3	direct ON/OFF input (normally LOW by internal pull-down)
REF	4	real time clock frequency reference output
INT	5	interrupt output
n.c.	6	not connected
RST	7	reset input (normally LOW by internal pull-down)
V_{PR}	8	external positive voltage reference input
SDA	9	I^{2}C-bus serial data input/output
SCL	10	I^{2}C-bus serial clock input
V_{DD}	11	main positive supply voltage
V_{SS}	12	main negative supply voltage
V_{PO}	13	voltage converter positive output
CCP	14	voltage converter shunt capacitor (positive side)
CCN	15	voltage converter shunt capacitor (negative side)
TS1	16	test input 1 (normally LOW by internal pull-down)
XTAL2	17	decoder crystal oscillator output
XTAL1	18	decoder crystal oscillator input
n.c.	19	not connected
TS2	20	test input 2 (normally LOW by internal pull-down)
BAT	21	battery sense input
n.c.	22	not connected
RDI	23	received POCSAG data input
RXE	24	receiver circuit enable output
ROE	25	receiver oscillator enable output
ZSD	26	synthesizer serial data output
ZSC	27	synthesizer serial clock output
ZLE	28	synthesizer latch enable output
V_{SS}	29	main negative supply voltage
VIB	30	vibrator motor drive output
LED	31	LED drive output
ATH	32	alert HIGH-level output

The PCD5003 is available in a TQFP32 package and as naked die. The pinning for TQFP32 package is shown in Fig.2.

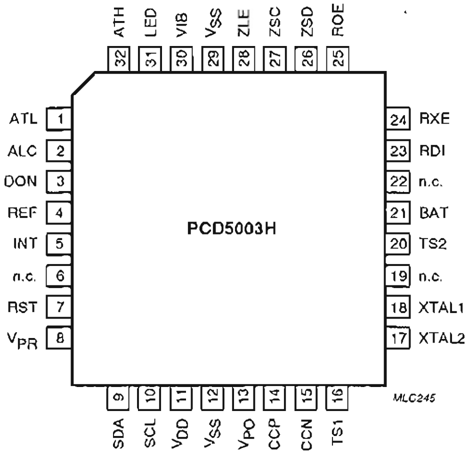


Fig.2 Pin configuration for SOT358-1 (TQFP32).

FUNCTIONAL DESCRIPTION

Introduction

The PCD5003 is a very low power decoder and pager controller specifically designed for use in new generation radio pagers. The architecture of the PCD5003 allows for flexible application in a wide variety of radio pager designs.

The PCD5003 is fully compatible with *"CCIR Radio paging Code No. 1"* (also known as the POCSAG code) operating at data rates of 512, 1200 and 2400 bits/s using a single oscillator crystal of 76.8 kHz.

In addition to the standard POCSAG sync word the PCD5003 is also capable of recognizing up to 4 User Programmable Sync Words (UPSWs). This permits the reception of both private services and POCSAG transmissions via the same radio channel.

Used together with the Philips UAA2080 Paging Receiver, the PCD5003 offers a highly sophisticated, miniature solution for the radiopaging market. Control of an RF synthesizer circuit is also provided to ease alignment and channel selection.

On-chip EEPROM provides storage for user addresses (Receiver Identity Codes or RICs) and Special Programmed Functions (SPFs), which eliminates the need for external storage devices and interconnection. The low EEPROM programming voltage makes the PCD5003 well-suited for 'over-the-air' programming/reprogramming.

On request from an external controlling device or automatically (by SPF programming), the PCD5003 will provide standard POCSAG alert cadences by driving a standard acoustic 'beeper'. Non-standard alert cadences may be generated via a cadence register or a dedicated control input.

Via external bipolar transistors the PCD5003 can also produce a HIGH-level acoustic alert as well as drive an LED indicator and a vibrator motor.

The PCD5003 contains a low-power, high-efficiency voltage converter (doubler) designed to provide a higher voltage supply to LCD drivers or microcontrollers. In addition, an independent level shifted interface is provided allowing communication to a microcontroller operating at a higher voltage than the PCD5003.

Interface to such an external device is provided by an I^2C-bus which allows received call identity and message data, data for the programming of the internal EEPROM, alert control and pager status information to be transferred between the devices. Pager status includes features provided by the PCD5003 such as battery-low and out-of-range indications.

A selectable low frequency timing reference is provided for use in real time clock functions.

Data synchronization is achieved by the Philips patented ACCESS® algorithm ensuring that maximum advantage is made of the POCSAG code structure particularly in fading radio signal conditions. The algorithm allows for data synchronization without preamble detection whilst minimizing battery power consumption.

Random and (optional) burst error correction techniques are applied to the received data to optimize on call success rate without deteriorating falsing rate beyond specified POCSAG levels.

When the PCD5003 is used in combination with a microcontroller, communication takes place via an I^2C-bus interface. A dedicated interrupt line minimizes the required microcontroller activity.

The POCSAG paging code

A transmission using the *"CCIR Radio paging Code No. 1"* (POCSAG code) is constructed in accordance with the following rules (see Fig.3).

The transmission is started by sending a **preamble**, consisting of at least 576 continuously alternating bits (10101010...). The preamble is followed by an arbitrary number of batch blocks. Only complete batches are transmitted.

Each **batch** comprises 17 codewords of 32 bits each. The first codeword is a synchronization codeword with a fixed pattern. The **sync** word is followed by 8 frames (0 to 7) of 2 codewords each, containing message information. A codeword in a frame can either be an address, message or idle codeword.

Idle codewords also have a fixed pattern and are used to fill empty frames or separate messages.

Address codewords are identified by an MSB of logic 0 and are coded as shown in Fig.3. A user address or RIC consists of 21 bits. Only the upper 18 bits are encoded in the address codeword (bits 2 to 19). The lower 3 bits designate the frame number in which the address is transmitted.

Four different **call types** can be distinguished on each user address. The call type is determined by two function bits in the address codeword (bits 20 and 21), as shown in Table 1.

Alert-only calls only consist of a single address codeword. Numeric and alphanumeric calls have message codewords following the address.

Message codewords are identified by an MSB of logic 1 and are coded as shown in Fig.3. The message information is stored in a 20-bit field (bits 2 to 21). The data format is determined by the call type: 4 bits per digit for numeric messages and 7 bits per (ASCII) character for alphanumeric messages.

Each codeword is protected against transmission errors by 10 CRC check bits (bits 22 to 31) and an even-parity bit (bit 32). This permits correction of maximum 2 random errors or up to 3 errors in a burst of 4 bits (a 4-bit burst error) per codeword.

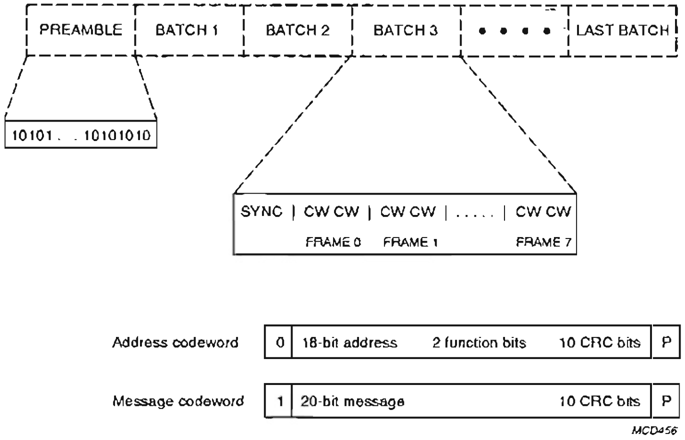


Fig.3 POCSAG code structure.

Table 1 POCSAG call types

BIT 20 (MSB)	BIT 21 (LSB)	CALL TYPE	DATA FORMAT
0	0	numeric	4-bits per digit
0	1	alert-only	–
1	0	alert-only	–
1	1	alphanumeric	7-bits per ASCII character

Error correction

In the PCD5003 error correction methods have been implemented as shown in Table 2.

Random error correction is default for both address and message codewords. In addition, burst error correction can be enabled by SPF programming. Up to 3 erroneous bits in a 4-bit burst can be corrected.

The error correction method used is identified in the message data output to the microcontroller, allowing rejection of calls with too many errors.

Table 2 Error correction

ITEM	DESCRIPTION
Preamble	4 random errors in 31 bits
Synchronization codeword	2 random errors in 32 bits
Address codeword	2 random errors, plus: 4-bit burst errors (optional)
Message codeword	2-bit-random errors, plus: 4-bit burst errors (optional)

Operating states

The PCD5003 has 2 operating states:

- ON status
- OFF status.

The operating state is determined by a Direct Control input (DON) and bit D4 in the control register (see Table 3).

Table 3 Truth table for decoder operating status

DON INPUT	CONTROL BIT D4	OPERATING STATUS
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

ON STATUS

In ON status the decoder pulses the receiver and oscillator enable outputs (respectively RXE and ROE) according to the code structure and the synchronization algorithm. Data received serially at the data input (RDI) is processed for call receipt. Reception of a valid paging call is signalled to the microcontroller by means of an interrupt signal. The received address and message data can then be read via the I^2C-bus interface.

OFF STATUS

In OFF status the decoder will neither activate the receiver or oscillator enable outputs, nor process any data at the data input. The crystal oscillator remains active to permit communication with the microcontroller.

In both operating states an accurate timing reference is available via the REF output. By SPF programming the signal periodicity may be selected as: 32.768 kHz, 50 Hz, 2 Hz or $\frac{1}{60}$ Hz.

Current consumption is reduced by switching off internal decoder sections whenever the receiver is not enabled.

Reset

The decoder can be reset by applying a positive pulse on input pin RST. A power-on reset circuit consisting of an RC network can be connected to this input as well. Conditions during and after a reset are described in Chapter "Operating instructions".

Bit rates

The PCD5003 can be configured for data rates of 512, 1200 or 2400 bit/s by SPF programming. These data rates are derived from a single 76.8 kHz oscillator frequency.

Oscillator

The oscillator circuit is designed to operate at 76.8 kHz. Typically, a tuning fork crystal will be used as a frequency source. Alternatively, an external clock source can be connected to pin XTAL1 only, but a slightly higher oscillator current is consumed.

To allow easy oscillator adjustment (e.g. by means of a variable capacitor) a 32.768 kHz reference frequency can be selected at output REF by SPF programming.

Input data processing

Data input is binary and fully asynchronous. Input bit rates of 512, 1200 and 2400 bits/s are supported. As a programmable option, the polarity of the received data can be inverted before further processing.

The input data is noise filtered by means of a digital filter. Data is sampled at 16 times the data rate and averaged by majority decision.

The filtered data is used to synchronize an internal clock generator by monitoring transitions. The recovered clock phase can be adjusted in steps of $\frac{1}{8}$ or $\frac{1}{32}$ bit period per received bit.

The larger step size is used when bit synchronization has not been achieved, the smaller when a valid data sequence has been detected (e.g. preamble or sync word).

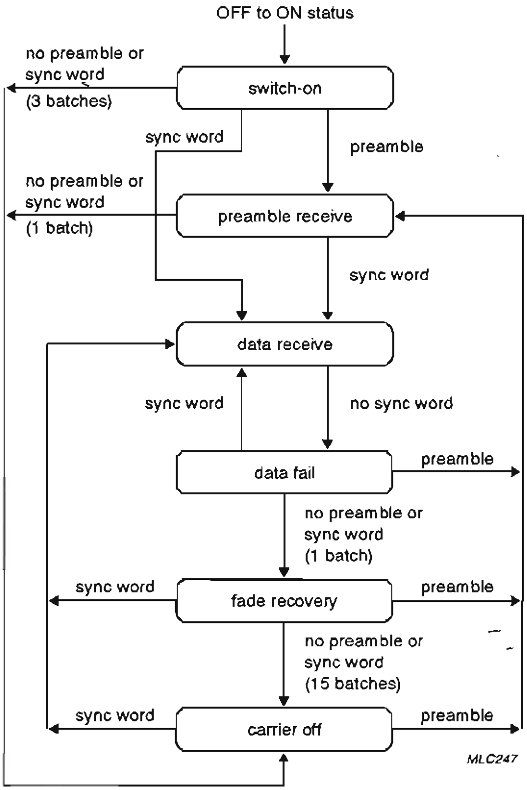


Fig.4 ACCESS® synchronization algorithm.

Synchronization strategy

In ON status the PCD5003 synchronizes to the POCSAG data stream by means of the Philips ACCESS® algorithm. A flow diagram is shown in Fig.4. Where 'sync word' is used, this implies both the standard POCSAG sync word and any enabled User Programmable Sync Word (UPSW).

Several modes of operation can be distinguished depending on the synchronization state. Each mode uses a different method to obtain data synchronization. The Receiver and Oscillator Enable outputs (respectively RXE and ROE) are switched accordingly, with the appropriate establishment times (respectively t_{RXON} and t_{ROON}).

Before comparing received data with preamble, an enabled sync word or programmed user addresses, the appropriate error correction is applied.

Initially, after switching to ON status, the decoder is in **Switch-on** mode. Here the receiver will be enabled for a period up to 3 batches, testing for preamble and sync word. Failure to detect preamble or sync word will cause switching to Carrier Off mode.

Detection of preamble switches to **Preamble Receive** mode, in which sync word is looked for. The receiver will remain enabled while preamble is detected. When neither sync word nor preamble is found within 1 batch duration Carrier Off mode is entered.

Upon detection of a sync word **Data Receive** mode is entered. The receiver is activated only during enabled user address frames and sync word periods. When an enabled user address has been detected, the receiver will be kept enabled for message codeword reception until the call termination criteria are met.

During call reception data bytes are stored in an internal SRAM buffer, capable of storing 2 batches of message data.

Messages are transmitted contiguously, only interrupted by sync words at the beginning of each batch. When a message extends beyond the end of a batch, no testing for sync takes place. Instead, a message data transfer will be initiated by an interrupt to the external controller. Data reception continues normally after a period corresponding to the sync word duration.

If any message codeword is found to be uncorrectable, Data Fail mode is entered and no data transfer will be attempted at the next sync word position. Instead, a test for sync word will be carried out.

In **Data Fail** mode message reception continues normally for 1 batch duration. Upon detection of sync word at the expected position the decoder returns to Data Receive mode. If sync word again fails to appear, batch synchronization is deemed lost. Call reception is then terminated and Fade Recovery mode is entered.

Fade Recovery mode is intended to scan for sync word and preamble over an extended window (nominal position ±8 bits). This is done for a period of up to 15 batches, allowing recovery of synchronization from long fades in the radio signal. Detection of preamble switches to Preamble Receive mode, while sync word detection switches to Data Receive mode. When neither is found within a period of 15 batches, the radio signal is considered lost and Carrier Off mode is entered.

The purpose of **Carrier Off** mode is to detect a valid radio transmission and synchronize to it quickly and efficiently. Because transmissions may start at random, the decoder enables the receiver for 1 codeword in every 18 codewords looking for preamble and sync word. By using a buffer containing 32 bits (n bits from the current scan, 32 – n from the previous scan) effectively every batch bit position can be tested within a continuous transmission of at least 18 batches. Detection of preamble switches to Preamble Receive mode, while sync word detection switches to Data Receive mode.

Call termination

Call reception is terminated:

- Upon reception of any address codeword (including Idle codeword) requiring no more than single bit error correction
- In Data Fail mode, when a sync word is not found at the expected batch position
- When a forced call termination command is received from an external controller.

The latter method permits an external controller to stop call reception depending on the number and type of errors which occurred in a codeword. After a forced call termination the decoder will enter Data Fail mode.

The type of error correction as well as the call termination conditions are indicated by status bits in the message data output.

Following call termination, transfer of the data received since the previous sync word period is initiated by means of an interrupt to the external controller.

Call data output format

POCSAG call information is stored in the decoder SRAM in blocks of 3 bytes per codeword. Each stored call consists of a Call Header, followed by Message Data blocks and concluded by a Call Terminator. In the event of concatenated messages the Call Terminator is replaced with the Call Header of the next message. An alert-only call only has a Call Header and a Call Terminator.

The formats of a Call Header, a Message Data block and a Call Terminator are shown in Tables 4, 6 and 8.

A **Call Header** contains information on the last sync word received, the RIC which began call reception and the type of error correction performed on the address codeword.

A **Message Data** block contains the data bits from a message codeword plus the type of error correction performed. No deformatting is done on the data bits: numeric data appear as 4-bit groups per digit, alphanumeric data have a 7-bit ASCII representation.

The **Call Terminator** contains information on the last sync word received, information on the way the call was terminated (Forced Call Termination command, loss of sync word in Data Fail mode) and the type of error correction performed on the terminating codeword.

Sync word indication

The sync word recognized by the PCD5003 is shown in the Call Header (bits S3 to S1). The decimal value represents the identifier number in the EEPROM of the UPSW in question. A value of 7 indicates the standard POCSAG sync word.

Error type indication

Table 10 shows how the different types of detected errors are encoded in the call data output format.

A message codeword containing more than a single bit error (bit E3 = 1) may appear as an address codeword (bit M1 = 0) after error correction. In this event the codeword is processed as message data and does not cause call termination.

Data transfer

Data transfer is initiated either during sync word periods or as soon as the receiver is disabled after call termination. If the SRAM buffer is full, data transfer is initiated immediately during the next codeword.

When the PCD5003 is ready to transfer received call data an external interrupt will be generated via output INT. Any message data can be read by accessing the RAM output register via the I^{2}C-bus interface. Bytes will be output starting from the position indicated by the RAM read pointer.

Table 4 Call Header format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	0	S3	S2	S1	R3	R2	R1	DF
2	0	S3	S2	S1	R3	R2	R1	0
3	X	X	F0	F1	E3	E2	E1	0

Table 5 Call Header bit identification

BITS (MSB to LSB)	IDENTIFICATION
S3 to S1	identifier number of sync word for current batch (7 = standard POCSAG)
R3 to R1	identifier number of user address (RIC)
DF	Data Fail mode indication (1 = Data Fail Mode); note 1
F0, F1	function bits of received address codeword (bits 20, 21)
E3 to E1	detected error type; see Table 10; E3 = 0 in a concatenated call header

Note

1. The DF bit in the Call Header is set:
   a) When the sync word of the batch in which the (beginning of the) call was received, did not match the standard POCSAG or a user-programmed sync word. The sync word identifier (bits S3 to S1) will then be made 0.
   b) When any codeword of a previous call received in the same batch was uncorrectable.

Table 6 Message Data format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	M2	M3	M4	M5	M6	M7	M8	M9
2	M10	M11	M12	M13	M14	M15	M16	M17
3	M18	M19	M20	M21	E3	E2	E1	M1

Table 7 Message Data bit identification

BITS (MSB to LSB)	IDENTIFICATION
M2 to M21	Message codeword data bits
E3 to E1	Detected error type; see Table 10
M1	Message codeword flag

Table 8 Call Terminator format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	FT	S3	S2	S1	0	0	0	DF
2	FT	S3	S2	S1	0	0	0	X
3	X	X	F0	F1	E3	E2	E1	0

Table 9 Call Terminator bit identification

BITS (MSB to LSB)	IDENTIFICATION
FT	Forced Call Termination (1 = yes)
S3 to S1	identifier number of last sync word
R3 to R1	identifier number of user address (RIC)
DF	Data Fail mode indication (1 = Data Fail mode); note 1
F0, F1	function bits of received address codeword (bits 20, 21)
E3 to E1	detected error type; see Table 10; E3 = 0 in a call terminator

Note

1. The DF bit in the Call Terminator is set:
   a) When any call data codeword in the terminating batch was uncorrectable, while in Data Receive mode.
   b) When the sync word at the start of the terminating batch did not match the standard POCSAG or a user-programmed sync word, while in Data Fail mode.

Successful call termination occurs by reception of a valid address codeword with less than 2 bit errors. Unsuccessful termination occurs when sync word is not detected while in Data Fail mode.

It is generally possible to distinguish these two conditions using the sync word identifier number (bits S3 to S1); the identifier number will be non-zero for correct termination, and zero for sync word failure.

Only when a call is received in Data Fail mode and the call is terminated before the end of the batch, is it not possible to distinguish unsuccessful from correct termination.

Reception of message data can be terminated at any time by transmitting a Forced Call Termination command to the Control register via the I^2C-bus. Any call received will then be terminated immediately and Data Fail mode will be entered.

Table 10 Error type identification

E3	E2	E1	ERROR TYPE	NUMBER OF ERRORS
0	0	0	no errors - correct codeword	0
0	0	1	parity bit in error	1
0	1	0	single bit error	1 + parity
0	1	1	single bit error and parity error	1
1	0	0	not used	
1	0	1	4-bit burst error and parity error	3 (e.g.1101)
1	1	0	2-bit random error	2
1	1	1	uncorrectable codeword	3 or more

Receiver and oscillator control

A paging receiver and an RF oscillator circuit can be controlled independently via enable outputs RXE and ROE respectively. Their operating periods are optimized according to the synchronization mode of the decoder. Each enable signal has its own programmable establishment time (see Table 11).

External receiver control and monitoring

An external controller may enable the receiver control outputs continuously via an I^{2}C-bus command, overruling the normal enable pattern. Data reception continues normally. This mode can be left by means of a Reset or an I^{2}C-bus command.

External monitoring of the receiver control output RXE is possible via bit D6 in the Status register, when enabled via the Control register (D2 = 1). Each change of state of output RXE will generate an external interrupt at output INT.

Battery condition input

A logic signal from an external sense circuit signalling battery condition can be applied to the BAT input. This input is sampled each time the receiver is disabled (RXE ↓ 0).

When enabled via the Control register (D2 = 0), the condition of input BAT is reflected in bit D6 of the Status register. Each change of state of bit D6 causes an external interrupt at output INT.

When using the UAA2080 pager receiver a Battery-Low condition corresponds to a logic HIGH-level. With a different sense circuit the reverse polarity can be used as well, because every change of state is signalled to an external controller.

After a reset the initial condition of the Battery-Low indicator in the Status register is zero.

Table 11 Receiver and oscillator establishment times (note 1)

CONTROL OUTPUT	ESTABLISHMENT TIME				UNIT
RXE	5	10	15	30	ms
ROE	20	30	40	50	ms

Note

1. The exact values may differ slightly from the above values, depending on the bit rate (see Table 22).

Synthesizer control

Control of an external frequency synthesizer is possible via a dedicated 3-line serial interface (outputs ZSD, ZSC and ZLE). This interface is common to a number of available synthesizers. The synthesizer is enabled using the oscillator enable output ROE.

The frequency parameters must be programmed in EEPROM. Two blocks of maximum 24 bits each can be stored. Any unused bits must be programmed at the beginning of a block: only the last bits are used by the synthesizer.

Data is transferred to the synthesizer each time the PCD5003 is switched from OFF to ON status. Transfer takes place serially in two blocks, starting with bit 0 (MSB) of block 1 (see Table 25).

Data bits on ZSD change on the falling flanks of ZSC. After clocking all bits into the synthesizer, a latch enable pulse copies the data to the internal divider registers. A timing diagram is given in Fig.5.

The data output timing is synchronous, but has a pause in the bit stream of each block. This pause occurs in the 13th bit while ZSC is LOW. The nominal pause duration t_p depends on the bit rate and is shown in Table 12. The total duration of the 13th bit is given by $t_{ZCL} + t_p$.

A similar pause occurs between the first and the second data block. The delay between the first latch enable pulse and the second data block is given by $t_{ZDL2} + t_p$. The complete start-up timing of the synthesizer interface is given in Fig.12.

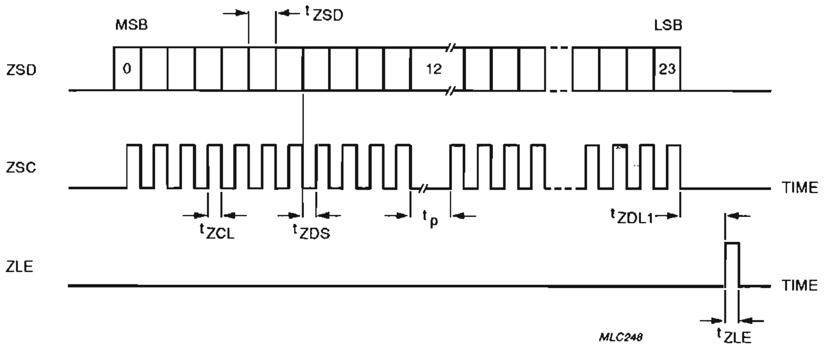


Fig.5 Synthesizer interface timing.

Table 12 Synthesizer programming pause

BIT RATE (bit/s)	t_p (clocks)	t_p (μs)
512	119	1549
1200	33	430
2400	1	13

Serial microcontroller interface

The PCD5003 has an I²C-bus serial microcontroller interface capable of operating at 400 kbits/s. The PCD5003 is a slave transceiver with I²C-bus address 39 Dec (bits A6 to A0 = 0100111).

Data transmission requires 2 lines: SDA (data) and SCL (clock), each with an external pull-up resistor. The clock signal (SCL) for any data transmission must be generated by the external controlling device.

A transmission is initiated by a start condition (S: SCL = 1, SDA = ↓) and terminated by a stop condition (P: SCL = 1, SDA = ↑).

Data bits must be stable when SCL is HIGH. If there are multiple transmissions, the stop condition can be replaced with a new start condition.

Data is transferred on a byte basis, starting with a device address and a read/write indicator. Each transmitted byte must be followed by an Acknowledge bit (ACK: active LOW). If a receiving device is not ready to accept the next complete byte, it can force a bus wait state by holding SCL LOW.

The general I²C-bus transmission format is shown in Fig.6. Formats for master/slave communication are shown in Fig.7.

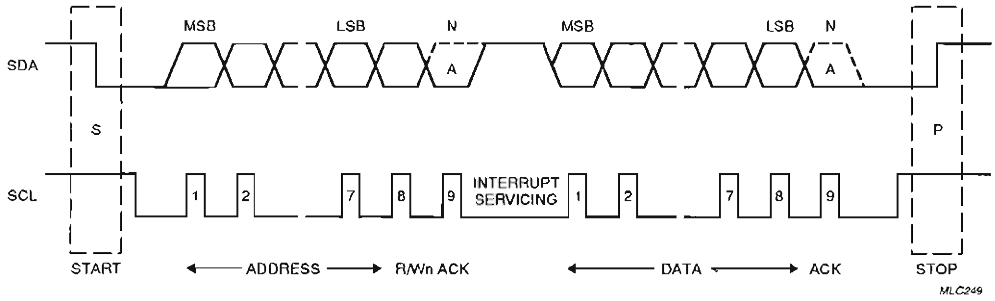


Fig.6 I²C-bus message format.

Decoder I²C-bus access

All internal access to the PCD5003 takes place via I²C-bus interface. For this purpose the internal registers, SRAM and EEPROM have been memory mapped and are accessed via an **index register**. Table 13 shows the index addresses of all internal blocks.

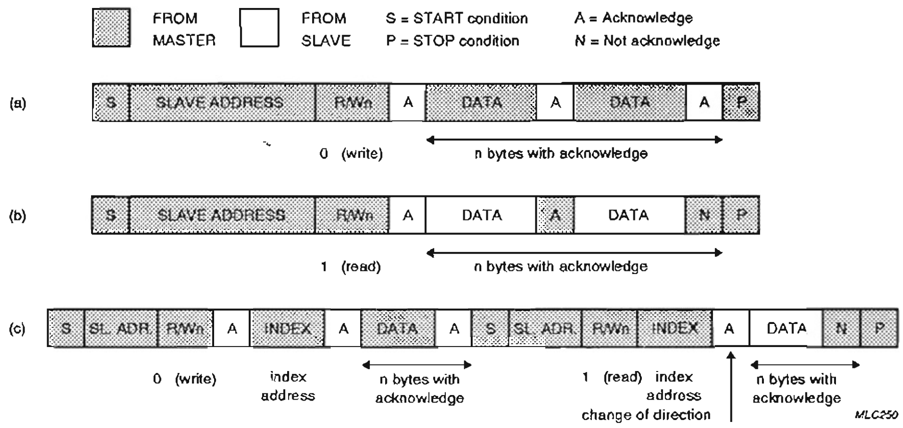
Registers are addressed directly, while RAM and EEPROM are addressed indirectly via address pointers and I/O registers.

Remark: The EEPROM memory map is non-contiguous and organized as a matrix. The EEPROM address pointer contains both row and column indicators.

Data written to read-only bits will be ignored. Values read from write-only bits are undefined and must be ignored.

Each I²C-bus message to the PCD5003 must start with its slave address, followed by the index address of the memory element to be accessed. The different I²C-bus message types are shown in Fig.7.

As a slave the PCD5003 cannot initiate bus transfers by itself. To prevent an external controller from having to monitor the operating status of the decoder, all important events generate an external interrupt on output INT.



(a) Master writes to slave.
(b) Master reads from slave.
(c) Combined format (shown: write plus read).

Fig.7 Message types.

Table 13 Index register

ADDRESS[1]	REGISTER FUNCTION	ACCESS
00 Hex	Status	R
00	Control	W
01	Real Time Clock: seconds	R/W
02	Real Time Clock: $\frac{1}{100}$ second	R/W
03	Alert Cadence	W
04	Alert Setup	W
05	Periodic Interrupt Modulus	W
05	Periodic Interrupt Counter	R
06	RAM Write Address pointer	R
07	EEPROM Address pointer	R/W
08	RAM Read Address pointer	R/W
09	RAM Data Output	R
0A	EEPROM Data Input/Output	R/W
0B to 0F	unused	note 2

Notes

1. The index register only uses the least significant nibble, the upper 4 bits are ignored.
2. Writing to registers 0B to 0F has no effect, reading produces meaningless data.

External interrupt

The PCD5003 can signal events to an external controller via an interrupt signal on output INT. The interrupt polarity is programmable via SPF programming. The interrupt source is shown in the status register.

Interrupts are generated by the following events (more than one event possible):

- Call data available for output (bit D2)
- SRAM pointers becoming equal (bit D3)
- Expiry of periodic time-out (bit D7)
- Expiry of alert time-out (bit D4)
- Change of state in Out-of-Range indicator (bit D5)
- Change of state in Battery-Low indicator or in receiver control output RXE (bit D6).

Immediate interrupts are generated by status bits D3, D4, D6 (RXE monitoring) and D7. Bits D2, D5 and D6 (BAT monitoring) generate interrupts as soon as the receiver is disabled (RXE = 0).

When call data is available (D2 = 1) but the receiver remains switched on, an interrupt is generated at the next sync word position.

The interrupt output INT is reset after completion of a status read operation.

Status/Control register

The Status/Control register consists of two independent registers, one for reading (Status) and one for writing (Control).

The Status register shows the current operating condition of the decoder and the cause(s) of an external interrupt. The Control register activates/deactivates certain functions. Tables 14 and 15 show the bit allocations of both registers.

All status bits will be reset after a status read operation except for the Out-of-Range, Battery-Low and Receiver Enable indicator bits (see note 1 to Table 14).

Table 14 Status register (00 Hex, read)

BIT [1]	VALUE	DESCRIPTION
D1, D0	0 0	no new call data
	0 1	call data available
	1 0	reserved for future use
	1 1	reserved for future use
D3, D2	0 0	no data to be read (default after reset)
	0 1	RAM read/write pointers different: data to be read
	1 0	RAM read/write pointers equal: no more data to read
	1 1	RAM buffer full or overflow
D4	1	alert time-out expired
D5	1	Out-of-Range
D6	1	BAT input HIGH or RXE output active (selected by Control bit D2)
D7	1	periodic timer Interrupt

Note

1. After a status read operation bits D3, D4 and D7 are always reset, bits D1 and D0 only when no second call is pending. D2 is reset when the RAM is empty (read and write pointers equal).

Table 15 Control register (00 Hex, write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	1	forced call termination (automatically reset after termination)
D1	1	EEPROM programming enable
D2	0	BAT input selected for monitoring (Status bit D6)
	1	RXE output selected for monitoring (Status bit D6)
D3	1	receiver continuously enabled (RXE = 1, ROE = 1)
D4	0	decoder in OFF status (while DON = 0)
	1	decoder in ON status
D5 to D7	X	not used: ignored when written

Pending interrupts

A secondary Status register is used for storing status bits of pending interrupts. This occurs:

- When a new call is received while the previous one was not yet acknowledged by reading the Status register
- When an interrupt occurs during a status read operation.

After completion of the status read the primary register is loaded with the contents of the secondary register, which is then reset. Next, an immediate interrupt is generated, output INT becoming active 1 decoder clock cycle after it was reset following the status read.

Remark: In the event of multiple pending calls only the status bits of the last call are retained.

Out-of-Range Indication

The Out-of-Range condition occurs when entering Fade Recovery or Carrier Off mode. This condition is reflected in bit D5 of the Status register. The Out-of-Range condition is left when entering Data Receive mode.

The Out-of-Range bit (D5) in the Status register is updated each time the receiver is disabled (RXE ↓ 0). Every change of state in bit D5 generates an interrupt.

Real time clock

The PCD5003 provides a periodic reference pulse at output REF. The frequency of this signal can be selected by SPF programming:

- 32768 Hz
- 50 Hz (square-wave)
- 2 Hz
- $\frac{1}{60}$ Hz.

The 32768 Hz signal does not have a fixed period: it consists of 32 pulses evenly distributed over 75 main oscillator cycles at 76.8 kHz. The timing is shown in Fig.13.

When programmed for $\frac{1}{60}$ Hz (1 pulse per minute) the pulse at output REF is held off while the receiver is enabled.

Except for the 50 Hz frequency the pulse width t_{RFP} is equal to one decoder clock period.

The real time clock counter runs continuously irrespective of the operating condition of the PCD5003. It contains a **seconds register** (maximum 59) and a **$\frac{1}{100}$ second register** (maximum 99), which can be read or written via the I^{2}C-bus. The bit allocation of both registers is shown in Tables 16 and 17.

Table 16 Real time clock: seconds register (01 Hex, read/write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	–	1 second
D1	–	2 seconds
D2	–	4 seconds
D3	–	8 seconds
D4	–	16 seconds
D5	–	32 seconds
D6	X	not used: ignored when written, undetermined when read
D7	X	not used: ignored when written, undetermined when read

Table 17 Real time clock: $\frac{1}{100}$ second register (02 Hex, read/write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	–	0 01 second
D1	–	0.02 second
D2	–	0.04 second
D3	–	0.08 second
D4	–	0.16 second
D5	–	0.32 second
D6	–	0.64 second
D7	X	not used: ignored when written, undetermined when read

Periodic interrupt

A periodic interrupt can be realised with the Periodic Interrupt Counter. This 8-bit counter is incremented every $\frac{1}{100}$ second and produces an interrupt when it reaches the value stored in the Periodic Interrupt Modulus register. The Counter register is then reset and counting continues.

Operation is started by writing a non-zero value to the Modulus register. Writing a zero will stop interrupt generation immediately and will halt the Periodic Interrupt Counter after 2.55 seconds.

The Modulus register is write-only, the Counter register can only be read. Both registers have the same index address (05 Hex).

Received call delay

Call reception causes both the Periodic Interrupt Modulus and the Counter register to be reset.

Since the Periodic Interrupt Counter runs for another 2.55 seconds after a reset, the received call delay (in $\frac{1}{100}$ second units) can be determined by reading the Counter register.

Alert generation

The PCD5003 is capable of controlling 3 different alert transducers: acoustic beeper (HIGH- and LOW-level), LED and vibrator motor. The associated outputs are ATH/ATL, LED and VIB respectively. ATL is an open drain output capable of directly driving an acoustic alerter via a resistor. The other outputs require external transistors.

Each alert output can be individually enabled via the Alert Setup register. Alert level and warble can be separately selected. The alert pattern can either be standard POCSAG or determined via the Alert Cadence register. Direct alert control is possible via Input ALC.

The Alert Setup register is shown in Table 18.

Standard POCSAG alerts can be selected by setting bit D0 in the Alert Setup register, bits D6 and D7 determining the alert pattern used.

Automatic generation via all alert outputs of the POCSAG alert pattern matching the received call type can be enabled by SPF programming (SPF byte 03, bit D2).

Table 18 Alert setup register (04 Hex, write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	0	call alert via Cadence Register
	1	POCSAG call alert (pattern selected by D7, D6)
D1	0	LOW-level acoustic alert (ATL), pulsed vibrator alert (25 Hz)
	1	HIGH-level acoustic alert (ATL + ATH), continuous vibrator alert
D2	0	normal alerts (acoustic and LED)
	1	warbled alerts: 16 Hz (LED: on/off, ATL/ATH: alternate f_{AWH}, f_{AWL})
D3	1	acoustic alerts enable (ATL, ATH)
D4	1	vibrator alert enabled (VIB)
D5	1	LED alert enabled (LED)
D7, D6(1)	0 0	POCSAG alert pattern FC = 00, see Fig.8(a)
	0 1	POCSAG alert pattern FC = 01, see Fig.8(b)
	1 0	POCSAG alert pattern FC = 10, see Fig.8(c)
	1 1	POCSAG alert pattern FC = 11, see Fig.8(d)

Note

1. Bits D7 and D6 correspond to function bits 20 and 21 respectively in the address codeword, which designate the POCSAG call type as shown in Table 1.

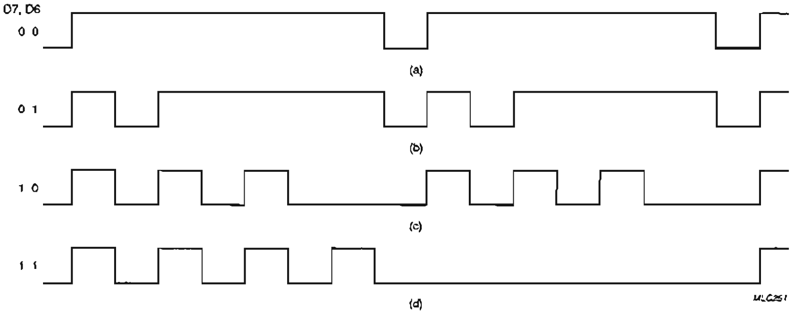


Fig.8 POCSAG alert patterns.

ALERT CADENCE REGISTER (03 HEX, WRITE)

When not programmed for POCSAG alerts (Alert Setup register bit D0 = 0), the 8-bit Alert Cadence register determines the alert pattern. Each bit represents a 62.5 ms time slot, a logic 1 activating the enabled alert transducers. The bit pattern is rotated with the MSB (bit D7) being output first and the LSB (bit D0) last.

When the last time slot (bit D0) is started an interrupt is generated to allow loading of a new pattern. When the pattern is not changed it will be repeated. Writing a zero to the Alert Cadence register will halt alert generation.

ACOUSTIC ALERT

Acoustic alerts are generated via outputs ATL and ATH. For LOW-level alerts only ATL is active, while for HIGH-level alerts ATH is also active. ATL is driven in counter phase with ATH.

The alert level is controlled by bit D1 of the Alert Setup register.

When D1 is reset for standard POCSAG alerts (D0 = 1), a LOW-level acoustic alert is generated during the first 4 seconds (ATL), followed by 12 seconds at HIGH-level (ATL + ATH). When D1 is set, the full 16 seconds are at HIGH-level. An interrupt is generated upon expiry of the full alert time.

When using the Alert Cadence register, D1 would normally be updated by external control when the alert time-out interrupt occurs at the start of the 8th cadence time slot. Since D1 acts immediately on the alert level, it is advised to reset the last bit of the previous pattern to prevent unwanted audible level changes.

LED ALERT

The LED output pattern corresponds either to the selected POCSAG alert or to the contents of the Alert Cadence register. No equivalent exists for high/low-level alerts.

VIBRATOR ALERT

The vibrator output (VIB) is activated continuously during a standard POCSAG alert or whenever the Alert Cadence register is non-zero.

Two alert levels are supported: low-level (25 Hz square-wave) and high-level (continuous). The vibrator level is controlled by bit D1 in the Alert Setup register.

WARBLED ALERT

When enabled by setting bit D2 in the Alert Setup register, the signals on outputs ATL, ATH and LED are warbled with a 16 Hz modulation frequency. Output LED is switched on and off at the modulation rate, while outputs ATL and ATH switch between f_{AWH} and f_{AWL} alerter frequencies.

DIRECT ALERT CONTROL

A direct Alert Control input (ALC) is available for generating user alarm signals (e.g. Battery-Low warning). A HIGH-level on input ALC activates all enabled alert outputs, overruling any ongoing alert patterns.

ALERT PRIORITY

Generation of a standard POCSAG alert (D0 = 1) overrides any alert pattern in the Alert Cadence register. After completion of the standard alert, the original cadence is restarted from the position it was left at. The Alert Setup register will now contain the settings for the standard alert.

The highest priority has been assigned to the Alert Control input (ALC). All enabled alert outputs will be activated while ALC is set. Outputs are activated/deactivated synchronous with the decoder clock. Activation requires an extra delay of 1 clock when no alerts are being generated.

When input ALC is reset, acoustic alerting does not cease until the current output-frequency cycle has been completed.

AUTOMATIC POCSAG ALERTS

Standard alert patterns have been defined for each POCSAG call type, as indicated by the function bits in the address codeword (see Table 1). The timing of these alert patterns is shown in Fig.9.

When enabled by SPF programming (SPF byte 03, bit D2) standard POCSAG alerts will automatically be generated on outputs ATL, ATH, LED and VIB upon call reception. The alert pattern matches the call type as indicated by the function bits in the received address codeword.

The original settings of the Alert Setup register will be lost. Bit D0 is reset after completion of the alert.

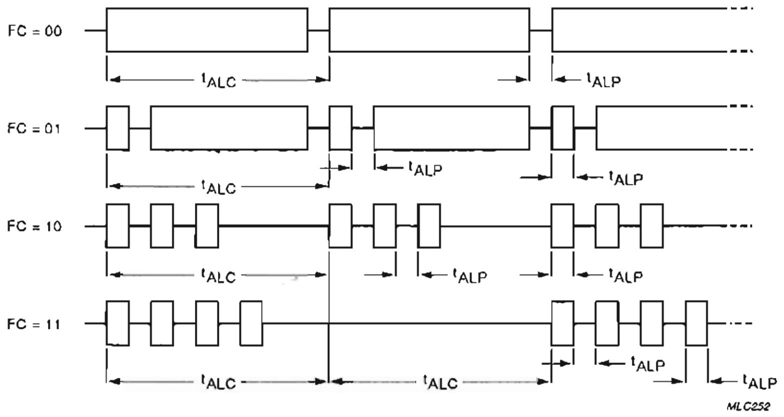


Fig.9 POCSAG alert timing.

RAM organization

SRAM ACCESS

The on-chip SRAM can hold up to 96 bytes of call data. Each call consists of a Call Header (3 bytes), Message Data blocks (3 bytes per codeword) and a Call Terminator (3 bytes).

The RAM is filled by the decoder and can be read via the I²C-bus interface. The RAM is accessed indirectly by means of a read address pointer and a data output register. A write address pointer indicates the position of the last message byte stored.

Status register bit D2 is set when the read and write pointers are different. It is reset only when the SRAM pointers become equal during reading, i.e. when the RAM becomes empty.

Status bit D3 is set when the read and write pointers become equal. This can be due to a RAM empty or a RAM full condition. It is reset after a status read operation.

Interrupts are generated as follows:

- When Status bit D2 is set and the receiver is disabled (RXE = 0): data is available for reading
- Immediately when Status bit D3 is set: RAM is either empty (Status bit D2 = 0) or full (Status bit D2 = 1).

To avoid loss of data due to RAM overflow at least 3 bytes of data must be read during reception of the codeword following the 'RAM full' interrupt.

RAM WRITE ADDRESS POINTER (06 HEX, READ)

The RAM write address pointer is automatically incremented during call reception, as the decoder writes each data byte to RAM. The RAM write address pointer can only be read. Values range from 0 to 5F Hex.
Bit D7 (MSB) is not used and its value is undefined when read.

RAM READ ADDRESS POINTER (08 HEX, READ/WRITE)

The RAM read address pointer is automatically incremented after reading a data byte via the RAM output register.

It can be accessed for writing as well as reading.

The values range from 0 to 5F Hex. When at 5F Hex a read operation will cause wrapping around to 00 Hex.
Bit D7 (MSB) is not used; it is ignored when written and undefined when read.

RAM DATA OUTPUT REGISTER (09 HEX, READ)

The RAM data output register contains the byte addressed by the RAM read address pointer. It can only be read, each read operation causing an increment of the RAM read address pointer.

EEPROM organization

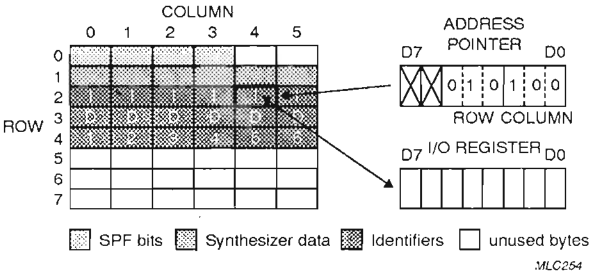


Fig.10 EEPROM organization and access.

EEPROM ACCESS

The EEPROM is intended for storage of user addresses (RICs), sync words and Special Programmed Function (SPF) bits representing the decoder configuration.

The EEPROM can store 48 bytes of information and is organized as a matrix of 8 rows by 6 columns. The EEPROM is accessed indirectly via an address pointer and a data I/O register.

The EEPROM is protected against inadvertent writing by means of the Programming Enable bit in the Control register (bit D1).

The EEPROM memory map is non-contiguous as can be seen in Fig.10, which shows both the EEPROM organization and the access method.

Identifier locations contain RICs or sync words. A total of 20 unassigned bytes is available for general purpose storage.

EEPROM ADDRESS POINTER (07 HEX, READ/WRITE)

An EEPROM location is addressed via the EEPROM address pointer. It is incremented automatically each time a byte is read or written via the EEPROM data I/O register.

The EEPROM address pointer contains two counters, for the row and the column number. Bits D2 to D0 contain the column number (0 to 5) and bits D5 to D3 the row number (0 to 7). Bits D7 and D6 of the address pointer are not used. Data written to these bits will be ignored, while their values are undefined when read.

The column and row counters are connected in series. Upon overflow of the column counter (column = 5) the row counter is automatically incremented and the column counter wraps to 0. On overflow the row counter wraps from 7 to 0.

EEPROM DATA I/O REGISTER (0A HEX, READ/WRITE)

The byte addressed by the EEPROM address pointer can be written or read via the EEPROM Data I/O register. Each access automatically increments the EEPROM address pointer.

EEPROM ACCESS LIMITATIONS

Since the EEPROM address pointer is used during data decoding, the EEPROM may not be accessed while the receiver is active (RXE = 1). It is advised to switch to OFF state before accessing the EEPROM.

The EEPROM cannot be written unless the EEPROM Programming Enable bit (bit D1) in the Control register is set.

For writing a minimum supply voltage V_{PG} is required (2.5 V typ.). The supply current needed during writing (I_{PG}) will be ~500 μA.

EEPROM READ OPERATION

EEPROM read operations must start at a valid address in the non-contiguous memory map. Single-byte or block reads are permitted.

EEPROM WRITE OPERATION

EEPROM write operations must always take place in blocks of 6 bytes, starting at the beginning of a row. Programming a single byte will reset the other bytes in the same row. Modifying a single byte in a row requires re-writing the unchanged bytes with their old contents.

After writing each block a pause of maximum 7.5 ms is required to complete the programming operation internally. During this time the external microcontroller may generate an I²C-bus Stop condition. If another I²C-bus transfer is started the decoder will pull SCL LOW during this pause.

After writing the EEPROM Programming Enable bit (D1) in the Control register must be reset.

INVALID WRITE ADDRESS

When an invalid write address is used, the column counter bits (D2 to D0) are forced to zero before being loaded into the address pointer. The row counter bits are used normally.

INCOMPLETE PROGRAMMING SEQUENCE

A programming sequence may be aborted by an I²C-bus Stop condition. Next, the EEPROM Programming Enable bit (D1) in the Control register must be reset.

Any bytes received of the last 6-byte block will be ignored and the contents of this (incomplete) EEPROM block will remain unchanged.

UNUSED EEPROM LOCATIONS

A total of 20 EEPROM bytes is available for general purpose storage (see Table 19).

Table 19 Unused EEPROM addresses

ROW	HEX
0	04, 05(1)
5	28 to 2D
6	30 to 35
7	38 to 3D

Note

1. When using bytes 04 and 05 Hex, care must be taken to preserve the SPF information stored in bytes 00 to 03 Hex.

SPECIAL PROGRAMMED FUNCTION ALLOCATION

The SPF bit allocation in the EEPROM is shown in Tables 20 to 24. The SPF bits are located in row 0 of the EEPROM and occupy 4 bytes.

Bytes 04 and 05 Hex are not used and are available for general purpose storage.

Table 20 Special Programmed Functions (00 Hex)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	X	reserved for future use; logic 0 when read
D1	X	reserved for future use
D2	X	reserved for future use
D3	X	reserved for future use
D4	X	reserved for future use
D5	X	reserved for future use
D6	X	reserved for future use; logic 0 when read
D7	1	received data inversion enabled

Table 21 Special Programmed Functions (01 Hex)

BIT (MSB: D7)	VALUE	DESCRIPTION
D1, D0	0 0	5 ms receiver establishment time (nominal); note 1
	0 1	10 ms
	1 0	15 ms
	1 1	30 ms
D3, D2	0 0	20 ms oscillator establishment time (nominal); note 1
	0 1	30 ms
	1 0	40 ms
	1 1	50 ms
D5, D4	0 0	512 bits/s received bit rate
	0 1	1024 bits/s (not used in POCSAG)
	1 0	1200 bits/s
	1 1	2400 bits/s
D6	1	synthesizer interface enabled (programming at switch-on)
D7	1	voltage converter enabled

Note

1. Since the exact establishment time is related to the programmed bit rate, Table 22 shows the values for the various bit rates.

Table 22 Establishment time as a function of bit rate

NOMINAL ESTABLISHMENT TIME	ACTUAL ESTABLISHMENT TIME (bits)			
	512 bits/s	1024 bits/s	1200 bits/s	2400 bits/s
5 ms	5.9 ms (3)	5.9 ms (6)	5.0 ms (6)	5.0 ms (12)
10 ms	11.7 ms (6)	11.7 ms (12)	10.0 ms (12)	10.0 ms (24)
15 ms	15.6 ms (8)	15.6 ms (16)	16.7 ms (20)	16.7 ms (40)
20 ms	23.4 ms (12)	23.4 ms (24)	20.0 ms (24)	20.0 ms (48)
30 ms	31.2 ms (16)	31.2 ms (32)	26.7 ms (32)	26.7 ms (64)
40 ms	39.1 ms (20)	39.1 ms (40)	40.0 ms (48)	40.0 ms (96)
50 ms	46.9 ms (24)	46.9 ms (48)	53.3 ms (64)	53.3 ms (128)

Table 23 Special Programmed Functions (02 Hex)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	X	not used
D1	X	not used
D3, D2	0 0	32768 Hz Real Time Clock reference
	0 1	50 Hz square-wave
	1 0	2 Hz
	1 1	$\frac{1}{60}$ Hz
D4	1	Signal test mode enabled (REF and INT outputs)
D5	0	Burst error correction enabled
D7, D6	X X	reserved for future use

Table 24 Special Programmed Functions (03 Hex)

BIT (MSB: D7)	VALUE	DESCRIPTION
D1, D0	0 0	2048 Hz Acoustic alerter frequency
	0 1	2731 Hz
	1 0	4096 Hz
	1 1	3200 Hz
D2	1	Automatic POCSAG alert generation enabled
D3	X	not used
D4	X	not used
D5	X	not used
D6	0	INT output polarity: active LOW
	1	INT output polarity: active HIGH
D7	X	not used

SYNTHESIZER PROGRAMMING DATA

Data for programming a PLL synthesizer via pins ZSD, ZSC and ZLE can be stored in row 1 of the EEPROM. Six bytes are available starting from address 08 Hex.

Data is transferred in two serial blocks of 24 bits each, starting with bit 0 (MSB) of block 1. Any unused bits must be programmed at the beginning of a block.

Table 25 Synthesizer programming data (08 to 0D Hex)

ADDRESS (HEX)	BIT (MSB: D7)	DESCRIPTION
08	D7 to D0	bits 0 to 7 of data block 1 (bit 0 is MSB)
09	D7 to D0	bits 8 to 15
0A	D7 to D0	bits 16 to 23
0B	D7 to D0	bits 0 to 7 of data block 2 (bit 0 is MSB)
0C	D7 to D0	bits 8 to 15
0D	D7 to D0	bits 16 to 23

IDENTIFIER STORAGE ALLOCATION

Up to 6 different identifiers can be stored in EEPROM for matching with incoming data. The PCD5003 can distinguish two types of identifiers:

- User addresses (RIC)
- User Programmable Sync Words (UPSW).

Identifiers are stored in EEPROM rows 2, 3 and 4. Each identifier location consists of 3 bytes in the same column. The identifier number is equal to the column number + 1.

Only the last 4 identifiers (numbers 3 to 6) can be programmed as a UPSW. Identifiers 1 and 2 always represent RICs. A UPSW represents an unused address and must differ by more than 6 bits from preamble to guarantee detection.

The standard POCSAG sync word is always enabled and has identifier number 7.

Table 26 shows the memory locations of the 6 identifiers. The bit allocation per identifier is given in Table 27.

Table 26 Identifier storage allocation (10 to 25 Hex)

ADDRESS (HEX)	BYTE	DESCRIPTION
10 to 15	1	identifier number 1 to 6
18 to 1D	2	identifier number 1 to 6
20 to 25	3	identifier number 1 to 6

Table 27 Identifier bit allocation

BYTE	BIT (MSB: D7)	DESCRIPTION
1	D7 to D0	bits 2 to 9 of POCSAG codeword (RIC or UPSW); notes 1 and 2
2	D7 to D0	bits 10 to 17
3	D7, D6	bits 18, 19
	D5	frame number bit FR3 (RIC); note 3
	D4	frame number bit FR2 (RIC)
	D3	frame number bit FR1 (RIC)
	D2	identifier type selection (0 = UPSW, 1 = RIC); note 4
	D1	identifier enable (1 = enabled)
	D0	reserved for future use, logic 0 when read

Notes

1. The bit numbering corresponds with the numbering in a POCSAG codeword: bit **1** is the flag bit (0 = address, 1 = message).
2. A UPSW needs 18 bits to be matched for successful identification. Bit 1 (MSB) must be logic 0; bits 2 to 19 contain the identifier bit pattern; they are followed by 2 predetermined random (function) bits and the UPSW is completed by 10 CRC error correction bits and an even-parity bit.
3. Bits FR3 to FR1 (MSB: FR3) contain the 3 least significant bits of the 21-bit RIC.
4. Identifiers 1 and 2 (RIC only) will be disabled by programming bit D2 as logic 0.

Voltage doubler

An on-chip voltage doubler provides an unregulated DC output for supplying an LCD or a low power microcontroller on output V_{PO}. An external ceramic capacitor of typical 100 nF is required between pins CCN and CCP. The voltage doubler is enabled via SPF programming.

Level-shifted interface

All interface lines are suited for communication with a microcontroller operating from a higher supply voltage. The external device must have a common reference at V_{SS} of the PCD5003.

The reference voltage for the level-shifted interface must be applied to input V_{PR}. This could be the on-chip voltage doubler output V_{PO} if required. When the microcontroller has a separate (regulated) supply this separate supply voltage should be connected to V_{PR}.

The level-shifted interface lines are: RST, DON, ALC, REF, INT.

The I^{2}C-bus interface lines SDA and SCL can be level-shifted independently of V_{PR} by means of the standard external pull-up resistors.

Signal test mode

A special Signal test mode is available for monitoring the performance of a receiver circuit together with the front-end of the PCD5003.

For this purpose the output of the digital noise filter and the recovered bit clock are made available at outputs REF and INT respectively. All synchronization and decoding functions are normally active.

Signal test mode is activated/deactivated by SPF programming.

OPERATING INSTRUCTIONS

Reset conditions

When the PCD5003 is reset by applying a HIGH-level on input RST, the condition of the decoder is as follows:

- OFF status (irrespective of DON input level)
- REF output frequency 32768 Hz
- All internal counters reset
- Status/Control register reset
- INT output at LOW-level
- No alert transducers selected
- LED, VIB and ATH outputs at LOW-level
- ATL output high-impedance
- SDA, SCL inputs high-impedance
- Voltage converter disabled.

Within t_{RSU} after release of the reset condition (RST LOW) the programmed functions are activated. The settings affecting the external operation of the PCD5003 are as follows:

- REF output frequency
- Voltage converter
- INT output polarity
- Signal test mode.

When input DON is HIGH, the decoder starts operating in ON status immediately following t_{RSU}.

Power-on reset circuit

Input RST has an internal high-ohmic pull-down resistor (nom. 2 MΩ at 2.5 V supply). This can be used together with an external capacitor to V_{PR} to make a power-on reset signal.

Since this pull-down varies considerably with processing and supply voltage, a more accurate reset duration can be realised with an additional external resistor to V_{SS}.

Reset timing

The start-up time for the crystal oscillator may exceed 1 second (typ. 800 ms). It is advised to apply a reset condition at least during the first part of this period. The minimum reset pulse duration t_{RST} is 50 μs.

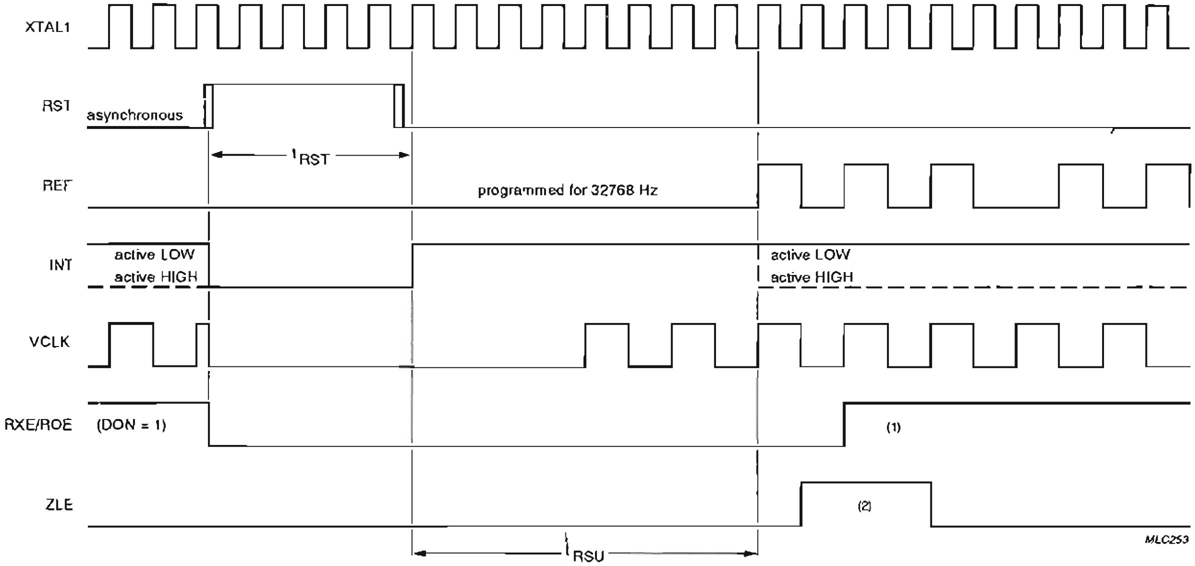
During reset the oscillator is active, but clock signals are inhibited internally. Once the reset condition is released the end of the oscillator start-up period can be detected by a rising edge on output INT.

During a reset the voltage converter clock (VCLK) is held at zero. The resulting output voltage drop may cause problems when the external resetting device is powered by the internal voltage doubler. A sufficiently large buffer capacitor between output V_{PO} and V_{SS} must be provided to supply the microcontroller during reset. The voltage at V_{PO} will not drop below $V_{DD} - 0.7$ V.

Immediately after a reset all programmable internal functions will start operating according to a programmed value of 0. During the first 8 full clock cycles (t_{RSU}) all programmed values are loaded from EEPROM.

After reset the receiver outputs RXE and ROE become active immediately, if DON is HIGH and the synthesizer is disabled. When the synthesizer is enabled, RXE and ROE will only become active after the second pulse on ZLE completes the loading of synthesizer data.

The full reset timing is shown in Fig.11. The start-up timing including synthesizer programming is given in Fig.12.



(1) The RXE/ROE output signals are shown for disabled synthesizer. When the synthesizer is enabled RXE/ROE are held off until after the second pulse on ZLE (programming complete).

(2) The ZLE output signal is shown for enabled synthesizer and DON = 1. When DON = 0 output ZLE remains HIGH until ON state is entered (DON = 1 or control register bit D4 = 1).

Fig.11 Reset timing.

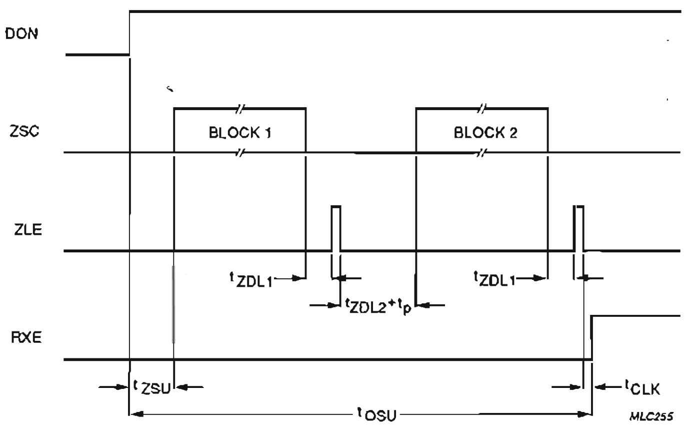


Fig.12 Start-up timing including synthesizer programming.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7.0	V
V_n	input voltage any pin	V_{SS} − 0.8	V_{DD} + 0.8	V
P_{tot}	total power dissipation	−	250	mW
P_O	power dissipation per output	−	100	mW
T_{amb}	operating ambient temperature	−25	+70	°C
T_{stg}	storage temperature	−55	+125	°C

DC CHARACTERISTICS

V_{DD} = 2.7 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		1.5	2.7	6.0	V
I_{DD0}	supply current (OFF)	note 1	–	25.0	40.0	µA
I_{DD1}	supply current (ON)	note 1; DON = V_{DD}	–	50.0	80.0	µA
V_{PG}	programming supply voltage		2.5	–	–	V
I_{PG}	programming supply current		–	–	800	µA
Inputs						
V_{IL}	LOW level input voltage					
	RDI, BAT XTAL1		–	–	$0.3V_{DD}$	V
	DON, ALC, RST		–	–	$0.3V_{PR}$	V
	SDA, SCL		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage					
	RDI, BAT XTAL1		$0.7V_{DD}$	–	–	V
	DON, ALC, RST		$0.7V_{PR}$	–	–	V
	SDA, SCL		$0.7V_{DD}$	–	–	V
I_{IL}	LOW level input current	T_{amb} = 25 °C				
	RDI, BAT,TS1, TS2	$V_I = V_{SS}$	0	–	−0.5	µA
	DON, ALC, RST	$V_I = V_{SS}$	0	–	−0.5	µA
I_{IH}	HIGH level input current	T_{amb} = 25 °C				
	TS1, TS2	$V_I = V_{DD}$	6	–	20	µA
	RDI, BAT	$V_I = V_{DD}$; RXE = 0	6	–	20	µA
	RDI, BAT	$V_I = V_{DD}$; RXE = 1	0	–	0.5	µA
	DON, ALC, RST	$V_I = V_{DD}$	250	500	850	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
I_{OL}	LOW level output current	T_{amb} = 25 °C				
	VIB, LED	V_{OL} = 0.3 V	80	–	–	μA
	ATH	V_{OL} = 0.3 V	250	–	–	μA
	INT, REF	V_{OL} = 0.3 V	80	–	–	μA
	ZSD, ZSC, ZLE	V_{OL} = 0.3 V	70	–	–	μA
	ATL	V_{OL} = 1.2 V; note 2	13	27	55	mA
	ROE, RXE	V_{OL} = 0.3 V	80	–	–	μA
I_{OH}	HIGH level output current	T_{amb} = 25 °C				
	VIB, LED	V_{OH} = 0.7 V	–0.6	–	–2.4	mA
	ATH	V_{OH} = 0.7 V	–3.0	–	–11.0	mA
	INT, REF	V_{OH} = 2.4 V	–80	–	–	μA
	ZSD, ZSC, ZLE	V_{OH} = 2.4 V	–60	–	–	μA
	ATL	ATL high-impedance	–	–	–0.5	μA
	ROE, RXE	V_{OH} = 2.4 V	–600	–	–	μA

Notes

1. All inputs = V_{SS}; all outputs open-circuit; SDA, SCL pulled up to V_{DD}; clock signal at XTAL1: f_{OSC} = 76800 Hz, amplitude: V_{SS} to V_{DD}; outputs RXE and ROE logic 0; REF output: f_{ref} = $\frac{1}{60}$ Hz.
2. Maximum output current is subject to absolute maximum ratings per output (see Chapter "Limiting values").

DC CHARACTERISTICS (WITH VOLTAGE CONVERTER)

V_{DD} = 2.7 V; V_{SS} = 0 V; V_{PR} = V_{PO}; T_{amb} = –25 to +70 °C; C_s = 100 nF; voltage converter enabled.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		1.5	–	3.0	V
$V_{PO(0)}$	output voltage; no load	V_{DD} = 2.7; I_{PO} = 0	–	5.4	–	V
V_{PO}	output voltage	V_{DD} = 2.0 V; I_{PO} = –250 μA	3.0	3.5	–	V
I_{PO}	output current	V_{DD} = 2.0 V; V_{PO} = 2.7 V	–400	–650	–	μA
		V_{DD} = 3.0 V; V_{PO} = 4.5 V	–650	–900	–	μA

OSCILLATOR CHARACTERISTICS

Quartz crystal type: MX-1V or equivalent.

Quartz crystal parameters: f = 76800 Hz; $R_{S(max)}$ = 35 kΩ; C_L = 8 pF; C_0 = 1.4 pF; C_1 = 1.5 fF; TC = –35 × 10^{-6}/K.

Maximum overall tolerance: ±200 × 10^{-6} (includes: cutting, temperature, aging).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{XO}	output capacitance XTAL2		–	10	–	pF
g_m	oscillator transconductance	V_{DD} = 1.5 V	6	12	–	μS

AC CHARACTERISTICS

V_{DD} = 2.7 V; V_{SS} = 0 V; T_{amb} = 25 °C;. f_{OSC} = 76800 Hz.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock						
T_{CLK}	system clock period	f_{OSC} = 76800 Hz	–	13.02	–	µs
Call alert frequencies						
f_{AL}	alert frequency	SPF byte 03 Hex; bits:				
		D1, D0 = 0 0	–	2048	–	Hz
		D1, D0 = 0 1	–	2731	–	Hz
		D1, D0 = 1 0	–	3200	–	Hz
		D1, D0 = 1 1	–	4096	–	Hz
f_{AW}	warbled alert; modulation frequency	alert setup bit D2 = 1; outputs ATL, ATH, LED	–	16	–	Hz
f_{AWH}	warbled alert; high acoustic alert frequency	alert setup bit D2 = 1; outputs ATL, ATH	–	f_{AL}	–	Hz
f_{AWL}	warbled alert; low acoustic alert frequency	alert setup bit D2 = 1; outputs ATL, ATH	–	$\frac{1}{2}f_{AL}$	–	Hz
f_{VBP}	pulsed vibrator frequency (square-wave)	low-level alert	–	25	–	Hz
Call alert duration						
t_{ALT}	alert time-out period		–	16	–	s
t_{ALL}	ATL output time-out period	low level alert	–	4	–	s
t_{ALH}	ATH output time-out period	high level alert	–	12	–	s
t_{VBL}	VIB output time-out period	low level alert	–	4	–	s
t_{VBH}	VIB output time-out period	high level alert	–	12	–	s
t_{ALC}	alert cycle period		–	1	–	s
t_{ALP}	alert pulse duration		–	125	–	ms
Real time clock reference						
f_{ref}	real time clock reference frequency	SPF byte 02 Hex; bits:				
		D3, D2 = 0 0; note 1	–	32768	–	Hz
		D3, D2 = 0 1; note 2	–	50	–	Hz
		D3, D2 = 1 0	–	2	–	Hz
		D3, D2 = 1 1	–	$\frac{1}{60}$	–	Hz
t_{RFP}	real time clock reference pulse duration	all reference frequencies except 50 Hz (square-wave)	–	13.02	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiver control						
t_{RXT}	RXE, ROE transition time	C_L = 5 pF	–	100	–	ns
t_{RXON}	RXE establishment time (nominal values: actual duration is bit rate dependent, see Table 22)	SPF byte 01 Hex; bits:				
		D1, D0 = 0 0	–	5	–	ms
		D1, D0 = 0 1	–	10	–	ms
		D1, D0 = 1 0	–	15	–	ms
		D1, D0 = 1 1	–	30	–	ms
t_{ROON}	ROE establishment time (nominal values: actual duration is bit rate dependent, see Table 22)	SPF byte 01 Hex; bits:				
		D3, D2 = 0 0	–	20	–	ms
		D3, D2 = 0 1	–	30	–	ms
		D3, D2 = 1 0	–	40	–	ms
		D3, D2 = 1 1	–	50	–	ms
I^2C-bus interface						
f_{SCL}	SCL clock frequency		0	–	400	kHz
t_{LOW}	SCL clock low period		1.3	–	–	µs
t_{HIGH}	SCL clock HIGH period		0.6	–	–	µs
t_{SUDAT}	data set-up time		100	–	–	ns
t_{HDDAT}	data hold time		0	–	–	ns
t_r	SDA, SCL rise time		–	–	300	ns
t_f	SDA, SCL fall time		–(3)	–	300	ns
C_B	capacitive bus line load		–	–	400	pF
t_{SUSTA}	start condition set-up time		0.6	–	–	µs
t_{HDSTA}	start condition hold time		0.6	–	–	µs
t_{SUSTO}	stop condition set-up time		0.6	–	–	µs
Reset						
t_{RST}	external reset duration		50	–	–	µs
t_{RSU}	set-up time after reset	oscillator running	–	–	105	µs
t_{OSU}	set-up time after switch-on	oscillator running	–	–	4	ms
Data input						
t_{TDI}	data input transition time		–	–	100	µs
t_{DI1}	data input logic 1 duration		infinite			
t_{DI0}	data input logic 0 duration		infinite			
POCSAG data timing (512 bits/s)						
f_{DI}	data input rate	SPF byte 01 Hex; bits D5, D4 = 0 0	–	512	–	bits/s
t_{BIT}	bit duration		–	1.9531	–	ms
t_{CW}	codeword duration		–	62.5	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{PA}	preamble duration		1125	–	–	ms
t_{BAT}	batch duration		–	1062.5	–	ms
POCSAG data timing (1200 bits/s)						
f_{DI}	data input rate	SPF byte 01 Hex; bits D5, D4 = 1 0	–	1200	–	bits/s
t_{BIT}	bit duration		–	833.3	–	µs
t_{CW}	codeword duration		–	26.7	–	ms
t_{PA}	preamble duration		480	–	–	ms
t_{BAT}	batch duration		–	453.3	–	ms
POCSAG data timing (2400 bits/s)						
f_{DI}	data input rate	SPF byte 01 Hex; bits D5, D4 = 1 1	–	2400	–	bits/s
t_{BIT}	bit duration		–	416.6	–	µs
t_{CW}	codeword duration		–	13.3	–	ms
t_{PA}	preamble duration		240	–	–	ms
t_{BAT}	batch duration		–	226.6	–	ms
Synthesizer control						
t_{ZSU}	synthesizer set-up duration	oscillator running; note 4	1	–	2	bits
f_{ZSC}	output clock frequency	note 5	–	38400	–	Hz
t_{ZCL}	clock pulse duration		–	13.02	–	µs
t_{ZSD}	data bit duration	note 5	–	26.04	–	µs
t_{ZDS}	data bit set-up time		–	13.02	–	µs
t_{ZDL1}	data load enable delay		–	91.15	–	µs
t_{ZLE}	load enable pulse duration		–	13.02	–	µs
t_{ZDL2}	inter block delay		–	117.19	–	µs

Notes

1. 32768 Hz reference signal: 32 pulses per 75 clock cycles, alternately separated by 1 or 2 pulse periods (pulse duration: t_{RFP}). The timing is shown in Fig.13.
2. 50 Hz reference signal: square-wave.
3. Fall time may be faster than prescribed in the I^2C-bus specification. This does not influence the functionality but may cause more interference.
4. Duration depends on programmed bit rate; after reset t_{ZSU} = 1.5 bits.
5. Nominal values; pause in 12th data bit (see Table 12).

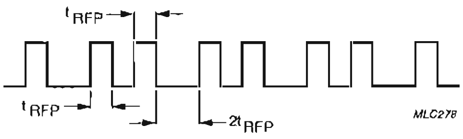
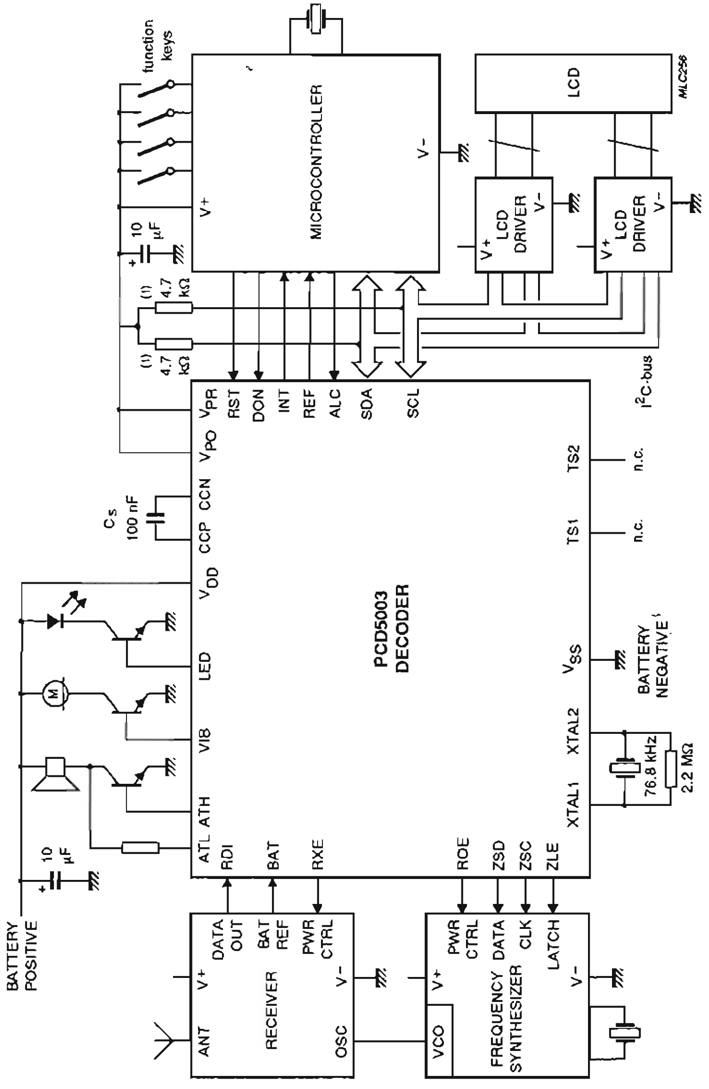


Fig.13 Timing of the 32768 Hz reference signal.

APPLICATION INFORMATION



(1) Value depends on number of devices attached.

Fig.14 Typical application example (display pager).

ADPCM CODEC for Digital Cordless Telephone

The PCD5032 is a CMOS device designed for use in Digital European Cordless Telephone systems (DECT) but it is also suited for other cordless telephony applications (e.g. CT2). The PCD5032 performs A/D and D/A conversion, ADPCM encoding and decoding compliant to CCITT recommendation G.721 (blue book 1988). The PCD5032 allows direct connection to external microphone and earpiece. The device can be used in both handset and base-station designs.

This objective specification contains advance information and is subject to change without notice.

Featuress

- G.721 compliant ADPCM encoding and decoding
- 'Bitstream' A/D and D/A conversion
- On-chip receive and transmit filter
- On-chip ringer and tone generator
- Programmable gain of receive and transmit path
- Serial ADPCM interface with independent timing for maximum flexibility
- Linear PCM data accessible for digital echo cancelling
- Programmable via I²C interface
- Fast receiver mute input via pin
- On-chip voltage reference
- On-chip symmetrical supply for electret microphone
- Few external components; direct connection to microphone and earpiece
- Low power consumption in standby mode
- Low supply voltage (single supply 2.7 V up to 5.5 V)
- CMOS technology
- Minimized EMC on digital outputs

Applications

- Digital European Cordless Telephony (DECT)
- CT2 cordless
- Speech compression

Package Outline

SO28 (SOT136A)
QFP44S14 (SOT205AG)

1.0 Block Diagram

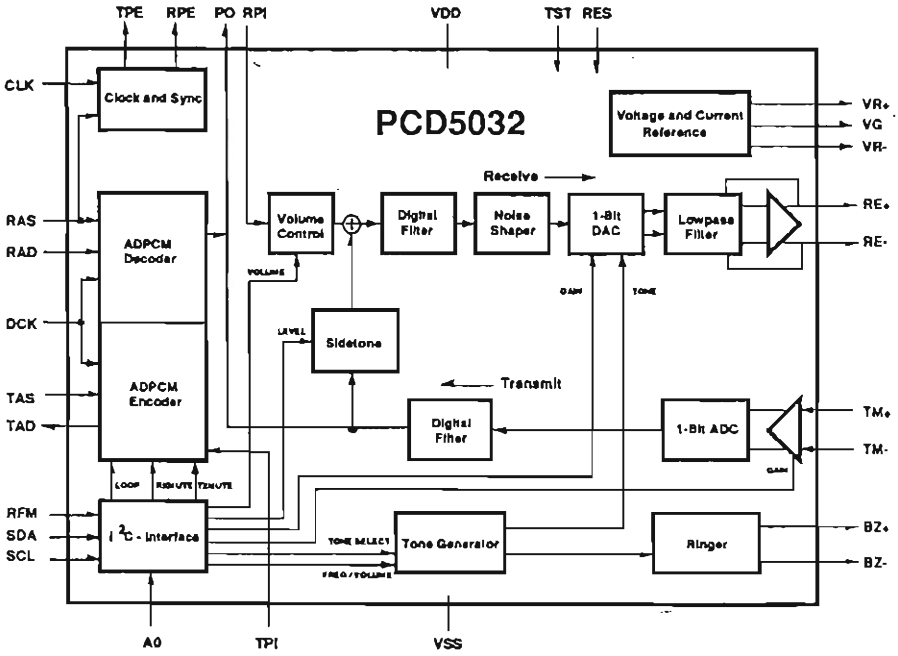
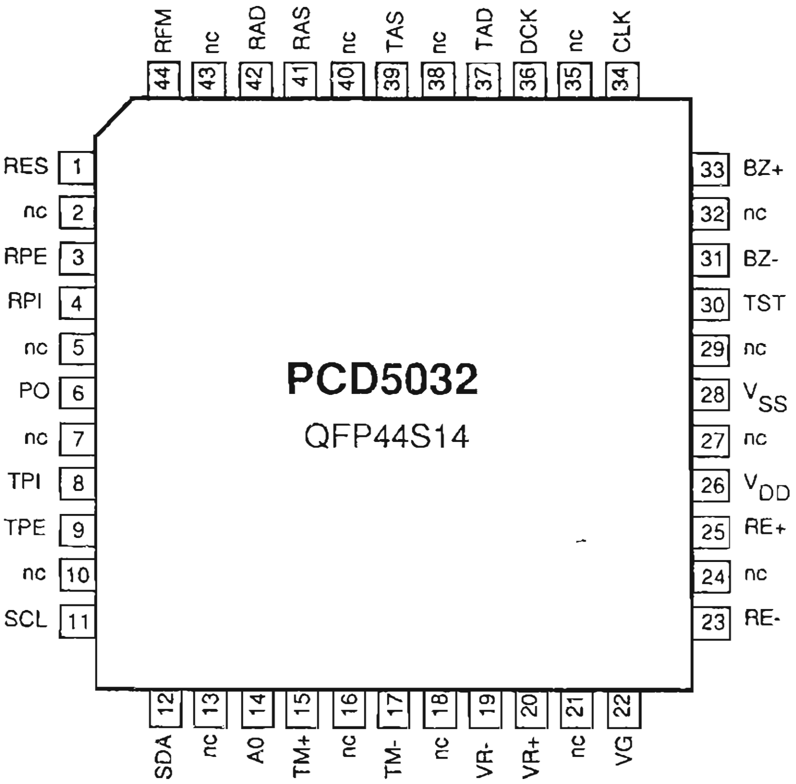


Fig. 1 Block diagram.

2.0 Pinning



nc = not connected

Fig. 2a Pinning diagram PCD5032 QFP44S14

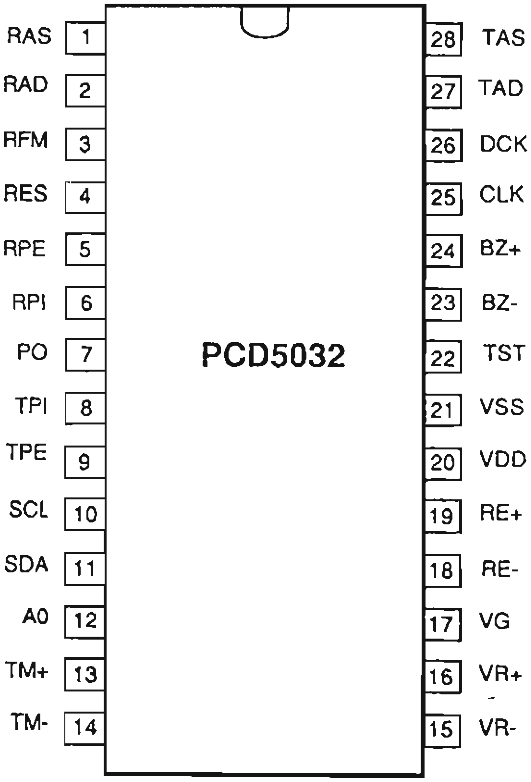


Fig. 2b Pinning diagram PCD5032 SO28

2.1 Pin Description

Pin	Name	I/O	Description	
General				
26	V_{DD}	-	Positive power supply (2.7V - 5.5V)	
28	V_{SS}	-	Negative power supply (0V)	
22	VG	O	Analog signal ground	
20	VR+	O	Positive reference voltage	(1)
19	VR-	O	Negative reference voltage	(1)
Digital				
34	CLK	I	Clock input	
36	DCK	I	Data clock (ADPCM)	
41	RAS	I	Receiver ADPCM sync	(2)
42	RAD	I	Receiver ADPCM data input	(2)
4	RPI	I	Receiver PCM input	(2)
3	RPE	O	Receiver PCM output enable	(2)
44	RFM	I	Receiver fast mute	(2)
39	TAS	I	Transmitter ADPCM sync	(2)
37	TAD	O	Transmitter ADPCM data output	(2)
8	TPI	I	Transmitter PCM input	(2)
9	TPE	O	Transmitter PCM output enable	(2)
6	PO	O	PCM data output	
12	SDA	I/O	I^2C serial data input / acknowledge	
11	SCL	I	I^2C clock input	
14	A0	I	I^2C address select pin	
1	RES	I	Reset input (active high)	
30	TST	I	Test mode	(3)
Analog				
33	BZ+	O	Ringer output	
31	BZ-	O	Ringer output	
15	TM+	I	Transmitter audio input (microphone)	
17	TM-	I	Transmitter audio input (microphone)	
25	RE+	O	Receiver audio output (earpiece)	
23	RE-	O	Receiver audio output (earpiece)	

(1) Internally generated, Intended for electret microphone supply.
(2) Definition: Receiver = direction from ADPCM interface to earpiece;
Transmitter = direction from microphone to ADPCM interface.
(3) To be connected to V_{SS} in normal application.

3.0 Functional description

3.1 Digital interfaces (see Fig.1 Block diagram)

3.1.1 ADPCM interface

The ADPCM interface pins (RAD, TAD) carry 4 bits of serial data. Transmit and receiver data both are controlled by separate synchronisation pins (RAS, TAS).

Upon detection of a high RAS signal (with rising DCK edge), the receiver will read 4 ADPCM bits on the next 4 high-to-low transitions of the DCK data clock. Likewise, upon reception of a high TAS signal, the transmitter will output 4 ADPCM bits on the next 4 low-to-high transitions of DCK. Figure 5 shows the timing diagram. During the time that the ADPCM data output (TAD) is not activated, it will be in a high impedance state, enabling a bus structure to be used in multi-line base stations. Input RAD has an internal pull-down resistor.

The minimum frequency on the DCK input is f_{CLK} / 54, the maximum value equals the clock frequency, and any frequency in between may be chosen. The RAS signal controls the start of each conversion in a frame at an 8 kHz rate. The master clock 'CLK' must be locked to the frequency of 'RAS', with a ratio $f_{CLK} = 432 \times f_{RAS}$.

3.1.2 PCM interface

To enable additional data processing in a base station both transmit and receive linear PCM data paths are accessible.

For the receive direction the PCM data is output on pin PO and read from pin RPI. For the transmit direction the PCM data is output on pin PO and read from pin TPI. To enable bus structures to be used in base stations the PCM output PO is in high impedance state when not active. Inputs TPI/RPI have internal pull-down.

In a typical (handset) application pin PO is directly connected to RPI and TPI.If additional data processing is required (e.g. echo cancellation in a base-station), then a data processing unit may be placed between PO and RPI or PO and TPI.

The data format is serial, 2's complement, MSB first. PO outputs 16 bits(14 data bits followed by 2 zeroes). TPI/RPI read 14 data bits.The bit frequency is 3456 kHz (CLK). Data output PO changes on the falling edge of CLK. Data inputs TPI/RPI are read on the rising edge of CLK (Figures 7,8).

For interfacing to digital signal processors signals TPE and RPE (both active low) mark the position of the transmit and receive pcm data on pin PO (Figure 6).
TPE/RPE change on the rising edge of CLK.

Outputs RPE and TPE have low impedance only from half a CLK cycle before to half a CLK cycle after the active state. The rest of the time they are in high impedance state.
Thus a wired-OR configuration can be made when only one DSP serial input port is used for reading both transmit and receive data. An external pull-up is required.

3.1.3 I^{2}C interface

The Philips I^{2}C interface is used for programming gain and mode of operation.

0	0	1	1	0	0	A0	0

(Write-only)

Fig. 3 I^{2}C address

With the address select pin A0 it is possible to have 2 independently programmed ADPCM codecs in a base station (2 outside lines). If more codecs are used in one base station then the address pin can be used as a 'select' signal. For timing of the I^{2}C bus, see Philips Semiconductors' brochure "The I^{2}C-bus and How to Use It" dated January 1992, ordering code 9398 393 40011.

Each function can be accessed by writing one 8-bit data word to the ADPCM codec. For this reason the 8-bit word is divided into 2 fields:

bit7, bit6 : function
bit5 to bit0 : value/setting.

Table 1: Overview of the I^{2}C programming possibilities.

Function	b7	b6	b5	b4	b3	b2	b1	b0
OPERATION MODE	0	0	-	-	TONE	PON	T1	T0
RECEIVER CONTROL	0	1	RV2	RV1	RV0	RG2	RG1	RG0
TRANSMITTER CONTROL	1	0	ST1	ST0	MUTE	TG2	TG1	TG0
RINGER	1	1	BF2	BF1	BF0	BV2	BV1	BV0

Definitions:

TONE : 'tone/ringer' selection for tone generator output;
tones can be sent to ringer or receiver DAC.
PON : power on (active)
T1 - T0 : test loops
RG2 - RG0 : receiver gain
TG2 - TG0 : transmitter gain
RV2 - RV0 : receiver volume
BV2 - BV0 : tone volume
BF2 - BF0 : tone frequency
ST1 - ST0 : sidetone level

Programming the ADPCM codec is possible in active mode as well as in standby mode. A reset clears all I^{2}C registers.

3.1.4 Fast mute

The RFM (Receiver Fast Mute) pin enables fast muting of the received signal if erroneous data is present on the ADPCM interface.

Muting is done in the same manner as the receiver mute via I^{2}C bus.The input data of the ADPCM decoder is blanked, so that the ADPCM decoder output signal goes to zero. To ensure immediate silence on the analog outputs RE+/RE-, the linear PCM input data of the receive filter is set to zero as well.

If the mute signal is switched off again, then the ADPCM decoder output settles gradually from zero to the appropriate PCM signal level. No audible clicks will occur.

The sidetone level is not affected by the mute function.

3.2 Analog parts and I²C programming

3.2.1 Input/Output

The analog input pins (TM+, TM-) can be connected directly to a microphone. For electret microphones capacitive coupling is required (Figure 11). The earpiece must be a low ohmic device (>100Ω differential).

The microphone and earpiece amplifiers have the possibility of gain control via the I²C interface. Further the sending and receiving direction can be muted separately. Analog gain control for the receive path can be set in steps of 1 dB. Digital volume control can be set in 6 dB steps. The following table gives an overview of the programming possibilities.

Table 2: Overview of gain control options

Function	**I²C-code**	**description**	**note**
Receiver gain (relative)	01xxx101	- 3 dB	
	01xxx110	- 2 dB	
	01xxx111	- 1 dB	
	01xxx000	0 dB	default
	01xxx001	+ 1 dB	
	01xxx010	+ 2 dB	
	01xxx011	+ 3 dB	
	01xxx100	+ 4 dB	
Receiver volume	01000xxx	0 dB	defaults
	01001xxx	- 6 dB	
	01010xxx	-12 dB	
	01011xxx	-18 dB	
	01100xxx	-24 dB	
	01101xxx	-30 dB	
	01110xxx	-36 dB	
	01111xxx	RX MUTE	
Transmitter gain (relative)	10xxx101	- 3 dB	
	10xxx110	- 2 dB	
	10xxx111	- 1 dB	
	10xxx000	0 dB	default
	10xxx001	+ 1 dB	
	10xxx010	+ 2 dB	
	10xxx011	+ 3 dB	
	10xxx100	+ 4 dB	
Transmitter mute	10xx1xxx	TX MUTE	default off

3.2.2 Sidetone

With the I^{2}C interface the (local) sidetone level can be set to -12, -18, -24 dB, or switched off. See table 3. The sidetone level is independent of the receiver volume control setting.

Table 3: Sidetone level options

Function	**I^{2}C-code**	**description**	**note**
Sidetone	1000xxxx	no local sidetone	default
	1001xxxx	level = -12 dB	
	1010xxxx	level = -18 dB	
	1011xxxx	level = -24 dB	

3.2.3 Tone generator and Ringer

The PCD5032 contains a programmable tone generator which can be used for generating ringer tones (BZ+, BZ-) or local information tones in the receive path (RE+, RE-).

By setting the TONE bit (b3) in the operation mode register the tone output will be directed to the receiver DAC, otherwise the tones will be sent to the ringer output stage. Table 4 shows the possible frequency and volume settings.

Table 4: Tone output frequency / volume options

Function	**I^{2}C-code**	**description**	**note**
Volume (rel)	11xxx000	signal off	default
	11xxx001	-29 dB	sine wave
	11xxx010	-23 dB	sine wave
	11xxx011	-17 dB	sine wave
	11xxx100	-11 dB	sine wave
	11xxx101	- 5 dB	sine wave
	11xxx110	0 dB	sine wave
	11xxx111	+4 dB	squarewave
Frequency	11000xxx	400 Hz	
	11001xxx	421 Hz	
	11010xxx	444 Hz	
	11011xxx	800 Hz	
	11100xxx	1000 Hz	
	11101xxx	1067 Hz	
	11110xxx	1333 Hz	
	11111xxx	2000 Hz	

The ringer output (BZ) is differential and is intended for low ohmic devices. If the ringer is switched off then both outputs are low. The output signal is a pulse density modulated block wave (on a 32 kHz basic pulse rate) to generate a sinewave-like output signal, see figure 4. Volume is controlled by changing the pulse width of each pulse. In the square wave mode a full square wave is generated and results in the maximum volume. The volume settings (in dB) are given for the first harmonic signal component.

One period of a 1 kHz signal (0 dB) looks like this (V(BZ+) - V(BZ-)):

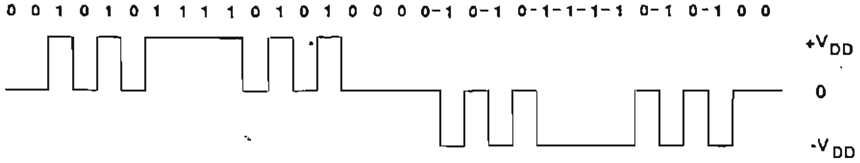


Fig. 4 Tone output example

3.3 Modes of operation

The ADPCM codec has three modes of operation, a normal mode and two loop modes. See the table below for details on setting these modes. Also the standby and active mode are set via the I^{2}C bus.

Table 5: Modes of operation.

Function	**I^{2}C-code**	**description**	**note**
Standby mode	00xxx0xx	power down	default
active mode	00xxx1xx	active	
set Normal mode	00xxxx00	normal operation	default
set Loop 1	00xxxx01	loopback on ADPCM side and on PCM side without using ADPCM transcoder.	
set Loop 2	00xxxx10	loopback of TM+/TM- to RE+/RE- through ADPCM transcoder.	

3.3.1 Standby mode

After a reset the ADPCM codec will by default be in standby mode. All I^{2}C settings will be cleared. PON=0 sets the codec in standby mode. In standby mode all circuits are switched off, except for the I^{2}C interface. Before going to standby mode the PCD5032 performs a reset of the ADPCM transcoder, digital filters and auxiliary logic functions. The I^{2}C interface registers are not cleared.

3.3.2 Active mode

PON=1 in the operation mode register sets the codec in active mode.
In active mode the ADPCM codec can be operated either in normal mode or one of the two test loops may be selected.

3.3.3 Test loops

Both test loops can be used for test or evaluation purposes.

Loop 1 is intended for testing the audio path and A/D, D/A converters, the ADPCM transcoder is not addressed in this mode.
The ADPCM data is directly looped back towards the radio interface. The PCM data is looped from transmit filter output to receive filter input.

Loop 2 is intended for testing the complete audio path including ADPCM encoding and decoding.

3.3.4 Reset (input RES)

After an external reset pulse the circuit will perform an internal reset procedure. The reset pulse must be active during at least 10 CLK cycles. 125 us (one 8kHz period) after RES has gone low, the internal reset is completed and the PCD5032 goes into standby mode.
At that moment the ADPCM codec is ready to be programmed.

A reset clears all I2C registers and resets the ADPCM transcoder, digital filters and auxiliary logic functions.

4.0 Characteristics

4.1 Maximum Ratings

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	min	max	unit
Supply voltage V_{DD} - V_{SS}	-0.5	+6,5	V
Voltage at any pin except V_{DD}	V_{SS} - 0.5	V_{DD} + 0.5	V
DC current through pin:			
V_{DD}, V_{SS}	-	150	mA
BZ+, BZ-	-	150	mA
RE+, RE-	-	50	mA
other pins	-	10	mA
Total power dissipation	-	500	mW
Operating ambient temperature	-25	+70	°C
Storage temperature	-65	+150	°C

Handling

Inputs and outputs are protected against electrostatic discharge in normal handling. ESD protection according to Human Body Model is guaranteed up to 800 V. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

4.2 Electrical Characteristics

Conditions: V_{DD} = 3.0 V, CLK = 3456 kHz

Parameter	min.	typ.	max.	unit	note
GENERAL					
Operating temperature	-25	25	70	°C	
Supply voltage	2.7	3.0	5.5	V	
Supply current					T_{amb} = 25 °C
-active (no load)	-	7	14	mA	note 0
-standby	-	20	100	µA	note 0
Leakage current inputs	-	-	1	µA	
Analog ground	0.48	0.5	0.52	x V_{DD}	
Reference voltage VR+	0.8	1.0	1.2	V	note 1
Reference voltage VR-	-0.8	-1.0	-1.2	V	note 1
DIGITAL I/O					
V_{IH}	0.7	-	1.0	x V_{DD}	note 2
V_{IL}	0	-	0.3	x V_{DD}	note 2
V_{OL}	-	-	0.4	V	note 2
V_{OH}	V_{DD} - 0.4	-	V_{DD}	V	note 2
Pull-down resistor	-	150	-	kΩ	note 2
DCK frequency	f_{CLK} / 54=64	-	f_{CLK}	kHz	note 3
RAS,TAS frequency	-	8	-	kHz	note 3

Electrical Characteristics (con't)

parameter	**min**	**typ**	**max**	**unit**	
I²C Bus Timing					
SCL clock frequency	-	-	100	kHz	
Tolerable spike width	-	-	50	ns	
Bus free time	4.7	-	-	µs	
Start condition set-up time	4.7	-	-	µs	
Start condition hold time	4.0	-	-	µs	
SCL LOW time	4.7	-	-	µs	
SCL HIGH time	4.0	-	-	µs	
SCL and SDA rise time	-	-	1.0	µs	
SCL and SDA fall time	-	-	0.3	µs	
Data set-up time	250	-	-	ns	
Data hold time	0	-	-	ns	
Stop condition set-up time	4.0	-	-	µs	
ANALOG INPUTS					note 4
TM+ / TM- input impedance	-	125	-	kΩ	note 5
Nominal input level	-	12	-	mV_{rms}	note 6
Maximum input signal	-	56	-	mV_{rms}	note 7
Min. voltage gain	-4	-3	-2	dB	
Max. voltage gain	+3	+4	+5	dB	
Stepsize voltage gain	-	1	-	dB	
TX harmonic distortion	-	-	-40	dB	note 8
ANALOG OUTPUTS					
Receiver audio output:					
- output impedance		10		Ω	note 5
- signal level at 0 dBm_0		550		mV_{rms}	note 9
- signal level at 3.14 dBm_0		1250		mV_{rms}	note 10
- min. gain	-4	-3	-2	dB	
- max. gain	+3	+4	+5	dB	
- gain step size	-	1	-	dB	
- volume control range	-36	-	0	dB	
- volume stepsize	-	6.0	-	dB	
- RX harmonic distortion	-	-	-40	dB	note 11

Electrical Characteristics (con't)

Parameter	min.	typ.	max.	unit	note
Ringer output:					note 4,12
-output impedance	-	14	29	Ω	
-volume control range	-29	-	+4	dB	
FILTER CHARACTERISTICS				dB	
Transmitter:					
-Passband ripple			0.5	dB	300 - 3000 Hz
-Frequency response					
f = 50 Hz	-35			dB	
f = 3400 Hz			-2	dB	
f = 4600 Hz	-35			dB	
f = 8000 Hz	-55			dB	
Receiver:					
- Passband ripple			0.5	dB	300 - 3000 Hz
- Frequency response:					
f = 50 Hz	-35			dB	
f = 3400 Hz			-2	dB	
f = 4600 Hz	-35			dB	
f = 8000 Hz	-60			dB	
ANALOG TO DIGITAL CONVERTER					
Signal to noise ratio (Fig. 12)		35		dB	note 5,13
DIGITAL TO ANALOG CONVERTER					
Signal to noise ratio (Fig. 12)		35		dB	note 5,13
GROUP DELAY					
Transmitter			400	µs	note 14
Receiver			525	µs	note 14
GROUP DELAY DISTORTION					
See Fig. 9					

Notes to the characteristics:

General:
- +3.14 dBm0 is the maximum signal level on the PCM interface.
- Specifications are valid in active mode (except standby current).

0. I_{DD} active measured with all inputs to V_{SS}, except CLK, DCK connected to 3.456 MHz, and RAS, TAS connected to 8 KHz. I_{DD} standby measured with all inputs connected to V_{SS}, except TMP, TMM left open. All outputs left open for both cases.
1. The ref. voltage is available on VR+ and VR- and is measured with respect to VG. The voltage outputs are intended for electret microphone supply, and can deliver 400 µA.
2. Digital inputs and outputs are CMOS-levels compatible. The outputs can sink or source 1 mA. Pull-down resistors are present at pins RPI, TPI, TST, RAD.
3. Any frequency between min and max is allowed for DCK. The signals CLK and RAS/TAS must be frequency-locked, and will have a ratio $f_{CLK} / f_{RAS} = 432$.
4. All analog input/output voltages and impedances are measured differentially. The circuit is designed for use with an electret microphone.
5. Frequency band is 300 Hz - 3400 Hz. Maximum load capacitance = 100 pF differentially, or 200 pF each pin.
6. Nominal signal level gives -10 dBm0 on the PCM interface (G.711/G.712). Value given for TX gain setting 0 dB.
7. Maximum signal level gives +3.14 dBm0 on the PCM interface, with larger input signals the digital output signal will be saturated. Value given for TX gain setting 0dB.
8. TX gain setting = 0 dB and input signal level 40 mVrms (will generate 0 dBm0 signal level on PCM interface according to G.711).
9. PCM signal level is 0 dBm0 and RX gain setting 0 dB. With a load of 300 Ω between RE+ and RE- the given signal level results in an output power of 1 mW. The maximum output current is 10 mA.
10. PCM signal level is +3.14 dBm0 and RX gain setting +4 dB. The maximum output current is 10 mA.
11. PCM signal level is 0dBm0 (G.711).
12. For maximum output power the load resistance should equal the typical output impedance (specified at $I_{load} = 20$ mA). The minimum load resistance is limited by the "Maximum Ratings".
13. Measured with psophometric filter (CCITT G.223).
    Only fulfilled at V_{DD} noise level smaller than 40 mVp (0 - 20 kHz).
    Measured on sample basis at $V_{DD} = 3.0$ V, temperature = 25 °C, compliant with G.712.
    Signal level is -40 dBm0 on PCM interface (0.4 mVrms on analog input).
    Gain setting is 0 dB.
14. Group delay includes ADPCM / PCM conversion; signal frequency = 1.5 kHz.
    Figure is given for RAS/TAS signals at the same moment.

5.0 Timing Diagrams

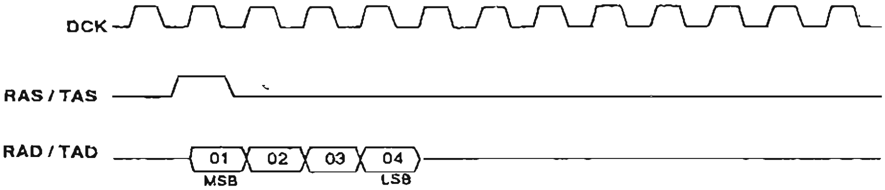


Fig. 5 ADPCM timing

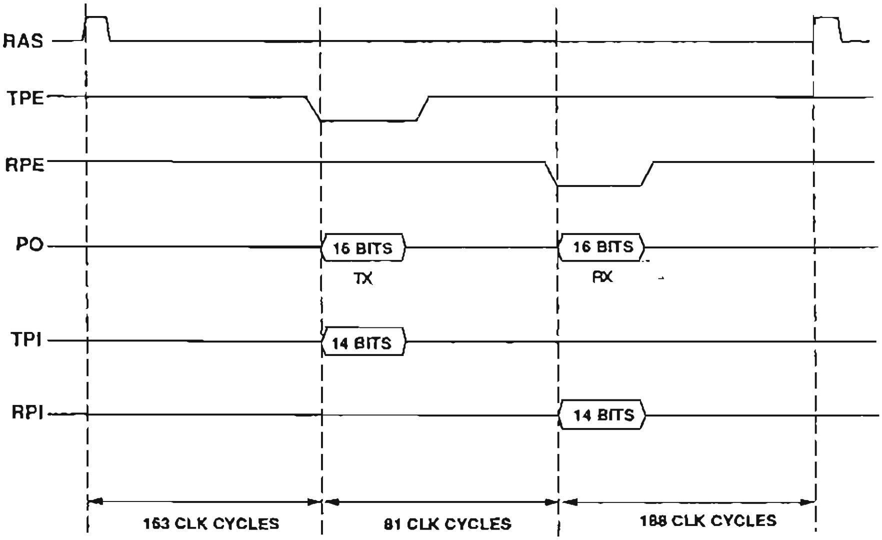


Fig. 6 PCM timing

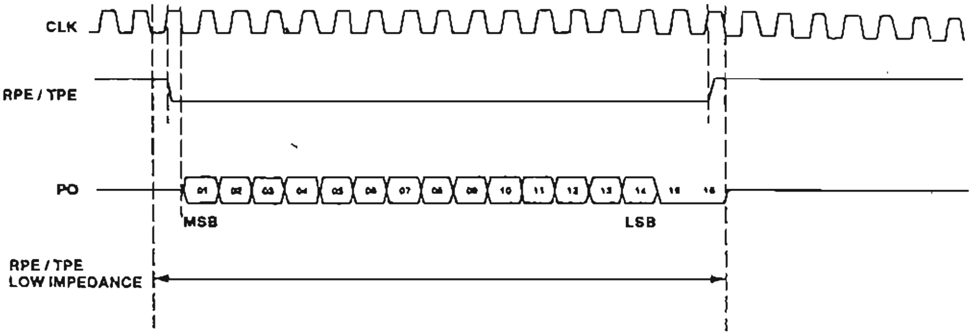


Fig. 7 PCM output timing

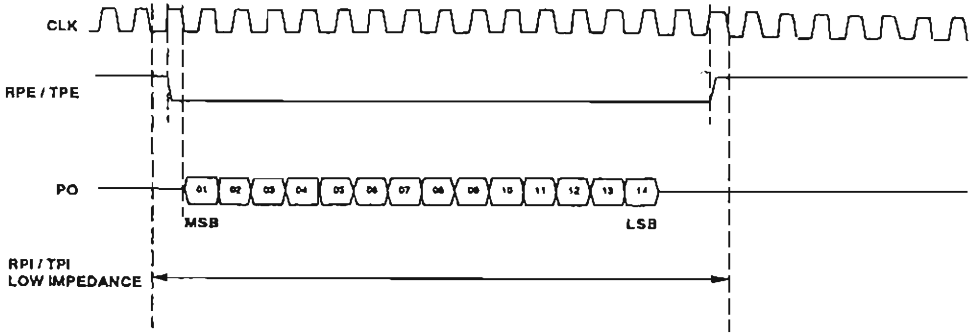


Fig. 8 PCM input timing

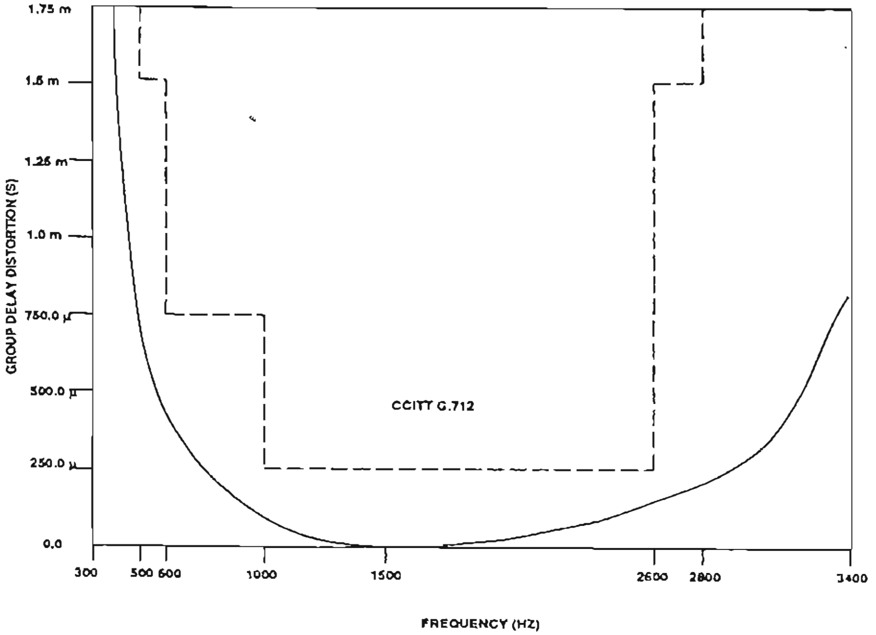


Fig. 9 Group delay distortion transmit + receive (loop measurement)

6.0 Application Information

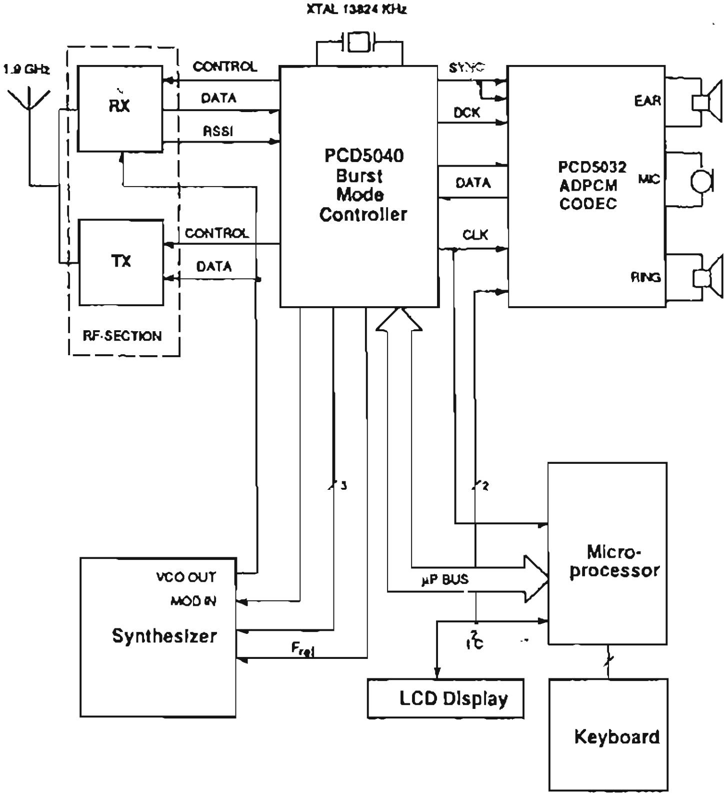


Fig. 10 Typical block diagram for a DECT handset.

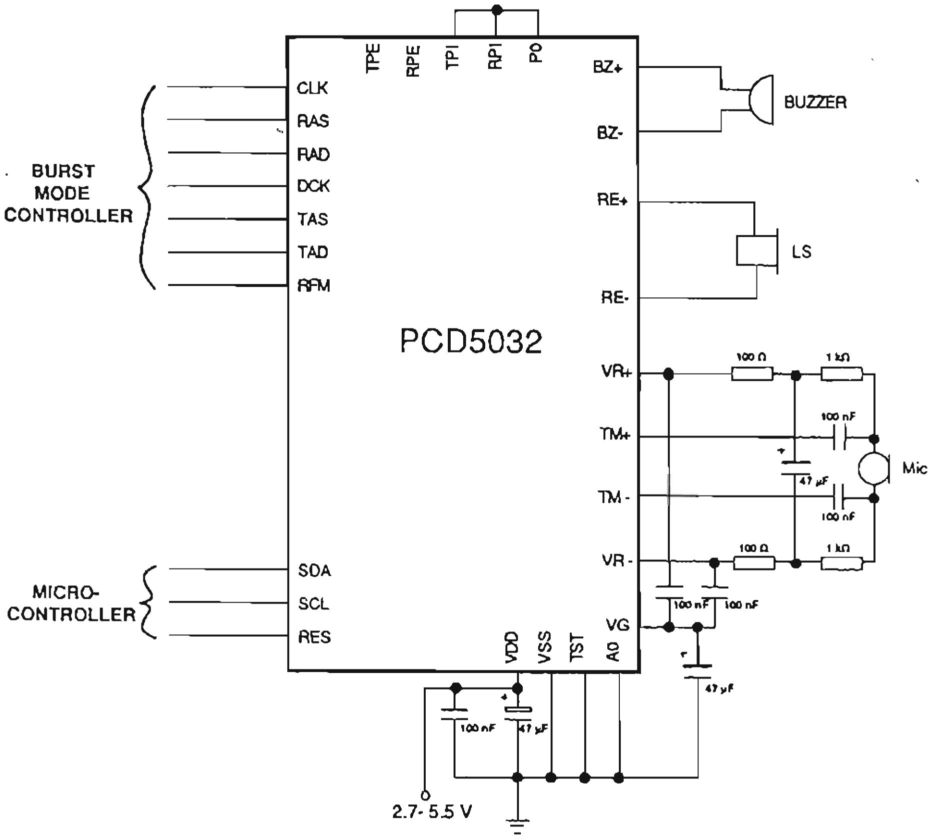


Fig. 11 Typical handset application diagram for the PCD5032.

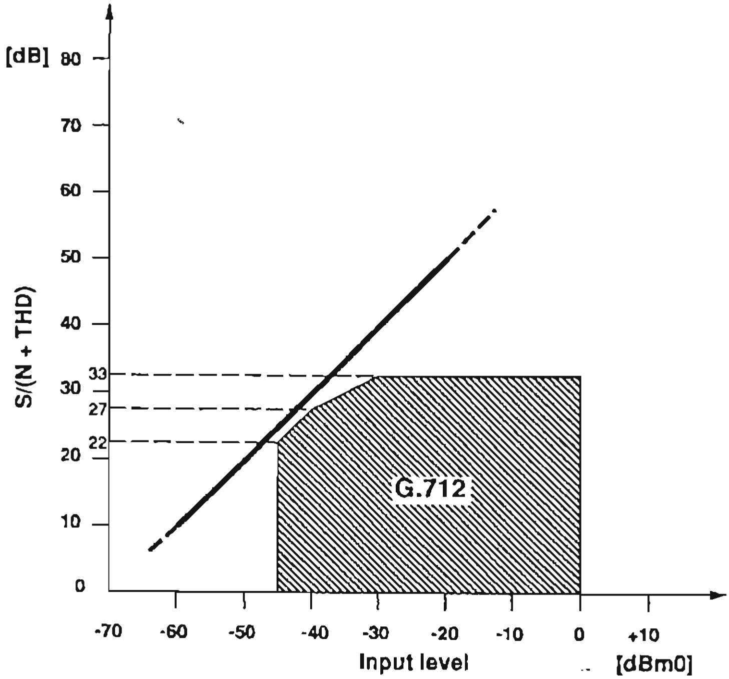


Figure 12 Typical performance of AD & DA in cascade (Loop 1)

DECT burst mode controller PCD5040

The PCD5040 DECT Burst Mode Controller (BMC) is a custom IC that performs the DECT Physical Layer and Medium Access Control Layer (MAC) time critical functions for application in DECT handset and base station products which comply to the following standards (+ updates):

- DECT CI part 2: Physical layer (DE/RES 3001-2)
- DECT CI part 3: Medium Access Control layer (DE/RES 3001-3)
- DECT CI part 7: Security features for DECT (DE/RES 3001-7)
- DECT CI part 9: Public Access Profile (DE/RES 3001-9)

The BMC is designed to be connected to a ADPCM codec (PCD5032) and a 8051-type microcontroller without glue logic. Other codec's and microcontrollers (e.g. 68000-family) are also supported. Four versions of the BMC will become available. The PCD5040 will have a RAM memory containing the BMC firmware, while the PCD5041, 5042, 5043 have a ROM instead. All versions have the same pinning. ROM versions will also be available in SQFP-80.

Features

- An embedded RISC controller (PCC) with 4 kbyte (RAM / ROM) program memory for implementation of Traffic Bearer Control (TBC), MAC message handling, scanning, and the general control of the BMC hardware.
- PP & FP modes.
- TDMA frame (de)multiplexing.
- Encryption.
- Scrambling.
- CRC generation and checking.
- Beacon transmission control (P00 packets).
- Switches up to12 simultaneous active speech channels from speech interface to 1152 kb/s. radio interface, and vice versa.
- RSSI measurement with on-chip peak/hold detector and 6-bit A/D converter.
- Local call switching for up to 6 internal calls on RF side / local call switching on speech side.
- Quality control report.
- Digital Phase Locked Loop.
- Synchronisation (handset to active bearer, base station to cluster of RFP's).
- Seamless handover procedure.
- Fast (hardware) and slow (software) mute function.
- 1 kbyte extended RAM memory for the handset mode.
- On-chip crystal oscillator (13.824 MHz).
- Programmable microcontroller clock frequency.
- Programmable interrupts.
- Watchdog with two programmable timeouts
- Low power consumption in standby mode.
- Low supply voltage (2.7V-6V).
- SACMOS technology.

Interfaces to:

- Up to 2 ADPCM codec's in a simple base station (with up to 2 analogue lines) and in the handset mode.
- 2048 kb/s highway interface for systems requiring more than 2 connections to the network.
- A fully decoded radio interface including power down signals.
- 80C51-type microcontroller, or a 68000-type microcontroller.

1.0 BLOCK DIAGRAM

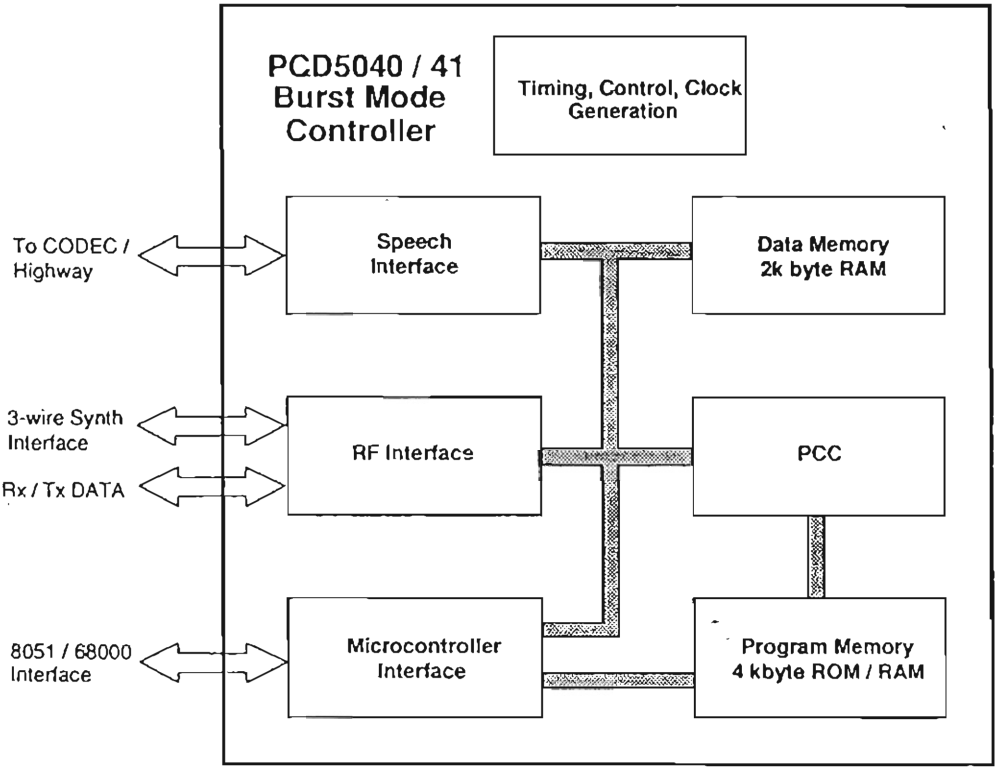


Fig. 1: Block diagram PCD5040 / 41 DECT Burst Mode Controller

2.0 PINNING

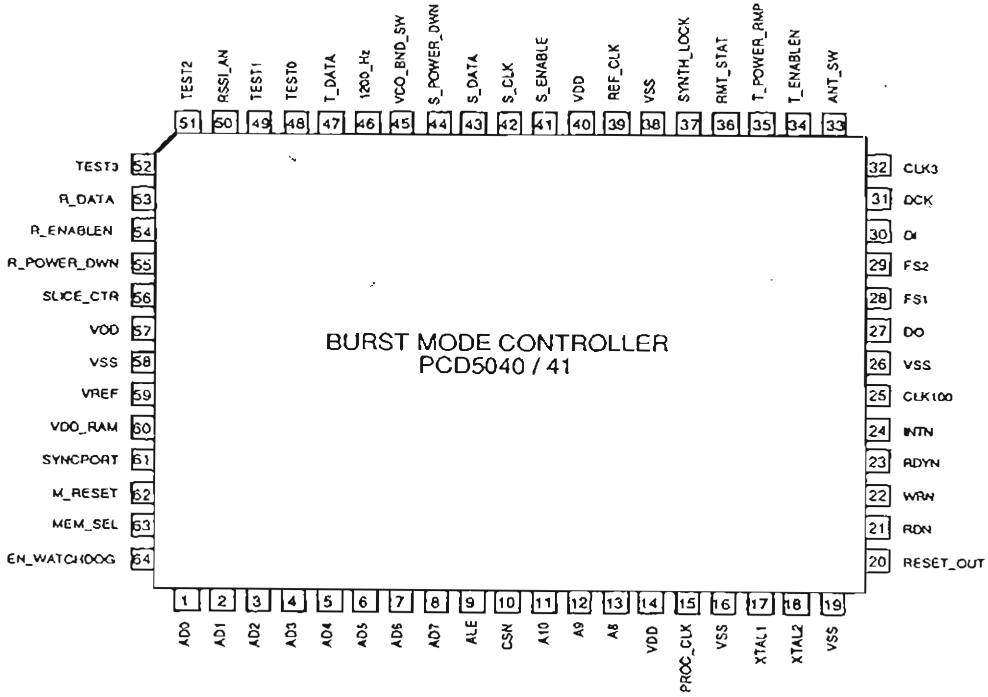


Fig 2: Pinning : QFP64REC (SOT319)

PIN	NAME	I/O	DESCRIPTION
14,40,57	V_{DD}	-	•
16,19,26,38,58	VSS	-	•
60	VDD_RAM	-	Power supply data RAM
48,49,51,52	TEST0..3	I	selects various test modes. Normal operation set to 0.
17	XTAL1	I	crystal oscillator input
18	XTAL2	O	crystal oscillator output
32	CLK3	O	3.456 MHz clock (nominal value, used to adjust system timing)
31	DCK	I/O	simple base + handset; 1152 kHz data clock (output), otherwise 2048 kHz data clock (input) signal
28	FS1	I/O	8 kHz framing signal to ADPCM codec 1 output, for simple base + handset, otherwise 8 kHz framing input.
29	FS2	O	8 kHz framing signal to ADPCM codec 2 in the base station mode.
27	DO	O	tri-state data output on the speech interface
30	DI	I	data input on the speech interface
15	PROC_CLK	O	microcontroller clock. Programmable from Fclk/64..Fclk, where Fclk is the crystal oscillator frequency.
63	MEM_SEL	I	Selects PCC program memory at microcontroller interface
9	ALE	I	address latch enable
21	RDN	I	read (active low)

PIN	NAME	I/O	DESCRIPTION
22	WRN	I	write (active low)
1..8	AD0..7	I/O	Address/Data bus
13..11	A8..10	I	Address bus
10	CSN	I	Chip Select (active low)
24	INTN	O	Interrupt (active low)
23	RDYN	O	Ready signal (active low), to initiate wait states in the microcontroller
54	R_ENABLEN	O	Receiver Enable (active low)
55	R_POWER_DWN	O	Receiver Power Down
56	SLICE_CTR	O	Slice Time Constant control
53	R_DATA	I	Receive Data
34	T_ENABLEN	O	Transmitter Enable (active low)
35	T_POWER_RMP	O	Transmitter Power Ramp control
47	T_DATA	O	Serial output data to transmitter
33	ANT_SW	O	Selects one of two antennas
44	S_POWER_DWN	O	Synthesizer Power Down control
46	1200_HZ	O	Control signal for dual synthesizer schemes
45	VCO_BND_SW	O	VCO bandswitch control signal
43	S_DATA	O	serial data to the synthesizer
42	S_CLK	O	clock signal, to be used with S_DATA.
41	S_ENABLE	O	Synthesizer enable
37	SYNTH_LOCK	I	Lock indication from synthesizer
39	REF_CLK	O	Reference Frequency for the synthesizer, ie. the crystal oscillator clock Fclk.
50	RSSI_IN	I	Analog signal (for basic DECT systems), peak signal strength measured after a low_pass filter.
36	RMT_STAT	I	Serial 8 bit data can be read in for each slot. REMote radio STATus
59	VREF	I	Reference input for the A/D converter
25	CLK100	O	100 Hz frame timer output
61	SYNCPORT	I/O	In the base station the signal is the SYNCPORT input/output. It is an output in a master base station, input in a slave base station, according to annex C, DECT CI specification part 2. The SYNCPORT signal is not active in the handset.
62	M_RESET	I	BMC master reset signal
64	EN_WATCHDOG	I	Enable watchdog input. When HI, the watchdog timer of the BMC is enabled
20	RESET_OUT	O	Watchdog timer output; intended to reset the external microcontroller when expired.

NOTE : ALL signals, which are input or I/O, and which can be floating, need to be pulled-up/down, in order to protect the BMC against cross-current. Exception are VREF and RSSI_AN, which do not have to be protected.

3.0 INTRODUCTION

The DECT Burst Mode Controller (BMC) is a custom IC, that performs the DECT Physical Layer and Medium Access Control Layer (MAC) time critical functions, for application in DECT handset and base station products, that comply to the following standards (+ updates):

- DECT CI part 2: Physical layer (DE/RES 3001-2)
- DECT CI part 3: Medium Access Control layer (DE/RES 3001-3)
- DECT CI part 7: Security features for DECT (DE/RES 3001-7)
- DECT CI part 9: Public Access Profile (DE/RES 3001-9)

The BMC is designed to be connected to the ADPCM codec (PCD5032) and a 8051-type microcontroller without glue logic. Also other codec's and microcontrollers (e.g. 68000-family) are supported.

Two versions of the BMC will become available. The PCD5040 will have a RAM memory, containing the BMC firmware, while the PCD504x have a ROM instead. All versions will have the same pinning. The firmware is used by the internal RISC processor, and is a part of the product. The product is described in two parts:

Part1:	DECT Burst Mode Controller hardware (this document)
Part2:	DECT Burst Mode Controller firmware

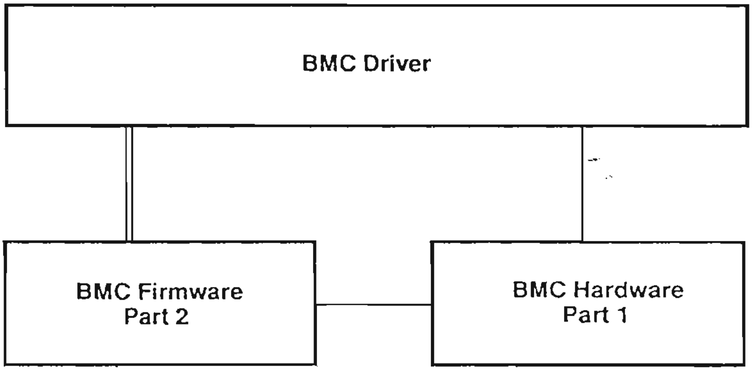


Figure 3: BMC document description

NOTE: This specification contains advance information and is subject to change without notice. Furthermore, this specification is valid for BMC versions from PCD5040-2 on.

4.0 FUNCTIONAL DESCRIPTION

The basic philosophy around the BMC implementation is to have a few dedicated hardware blocks containing logic for time critical functions (with bit/byte time accuracy); all other functions (with slot time accuracy) are contained in a small programmable core, the Programmable Communication Controller (PCC). This approach offers maximums flexibility during prototyping.

The block diagram of the BMC is shown below. In the following sections, the functional blocks and the internal bus are described.

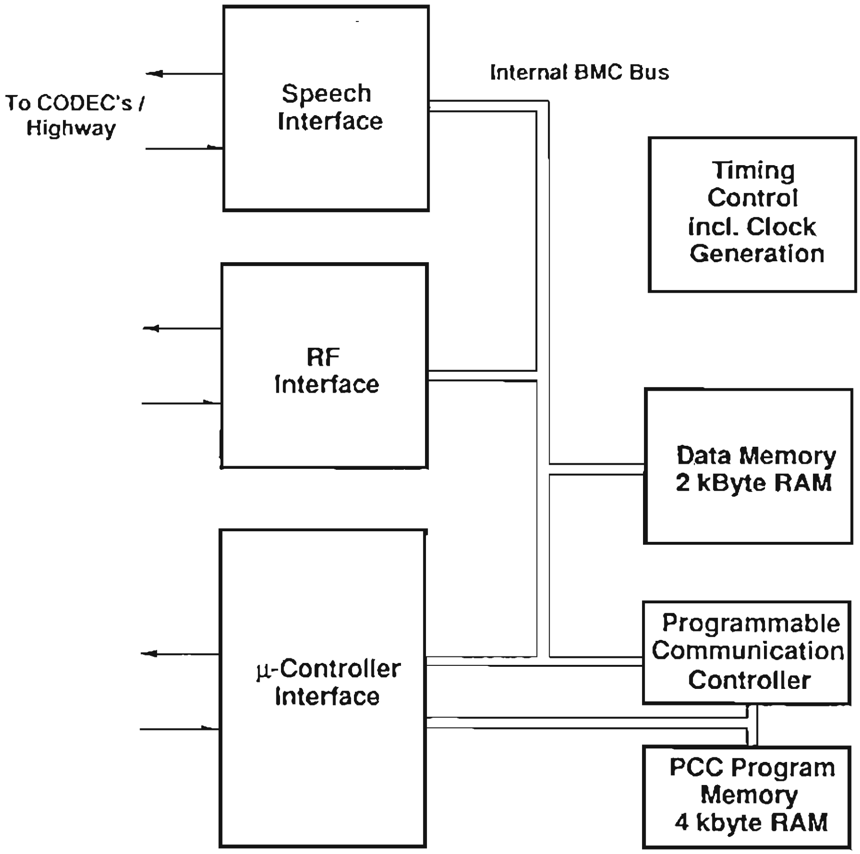


Figure 4.1: Internal Bus with main Functional Blocks

4.1. Internal Bus

4.1.1. Function of the Internal Bus

The function of the Internal Bus is:

- to provide access for all functional blocks to the common Data Memory,
- to provide access for the µC-Interface block and the Communication Controller (PCC) to all other functional blocks.

All functional blocks (speech, RF, cipher, µ-Controller, PCC) can autonomously use the internal bus to communicate with the common data memory.

A bus controller is used to handle the bus priority mechanism. When several blocks request access simultaneously, the request with the highest priority is handled first.

4.1.2. Data Memory

A large part of the data memory is used for the bit rate adaptation between the DECT radio interface and the speech interface.

In a handset, the BMC uses only 1 kbyte of the common data memory. The remainder (1 kbyte) can be used by the µ-controller as an extended data memory for the higher layer software. The µ-controller is not aware of the fact, that it is sharing the memory with the BMC; the µ-controller interface plus the common data memory behave as a standard RAM device, from the µ-controller point of view. In the base station, the BMC will use the full common data memory.

The data memory is also acting as the main communication interface between external micro-processor and PCC. The format of data structure is described in part 2 : 'DECT Burst Mode Controller Firmware'.

4.2. Clock Generation and Correction

The BMC has an on-chip 13.824 MHz crystal oscillator. From this source, a few frequencies are derived for internal and external use. Frequencies generated for external use are:

- 13.824 MHz	for the synthesizer reference (pin REF_CLK), which is only running if the synthesizer is not in power down mode (pin S_POWER_DWN).
- 0.144-13.824 MHz	for the µ-controller clock (pin PROC_CLK).
- 3.456 MHz	for the ADPCM codec (pin CLK3)
- 1200 Hz	for dual synthesizer switching
- 100 Hz	indicates start of frame

Nominally, the frequency on pin CLK3 is 3.456 Mhz. This frequency is divided from the crystal (divide-by-4). But sometimes, it will be divided by 3 or by 5, to synchronise the combination of the ADPCM codec and the BMC to an external source. Applications in which the BMC can be synchronised are:

- handset :	the incoming radio channel, using the 'slot synchronisation' event of one active channel, so the handset is locked to one base station.
- master base station :	The master base station is providing a 100 Hz signal to slave base stations on pin SYNCPORT. If the BMC is connected to a digital interface (32-slot mode speech interface), the external synchronisation will be done on the incoming 8 kHz signal. If it is connected to an analog line (12-slot mode speech interface), it will use its own crystal oscillator as reference.
- slave base station :	The slave base station will use the incoming SYNCPORT signal as synchronisation reference.

Each of these three application area's define their own 'sync' event for adjusting the internal timing of the BMC (see section 5.5)

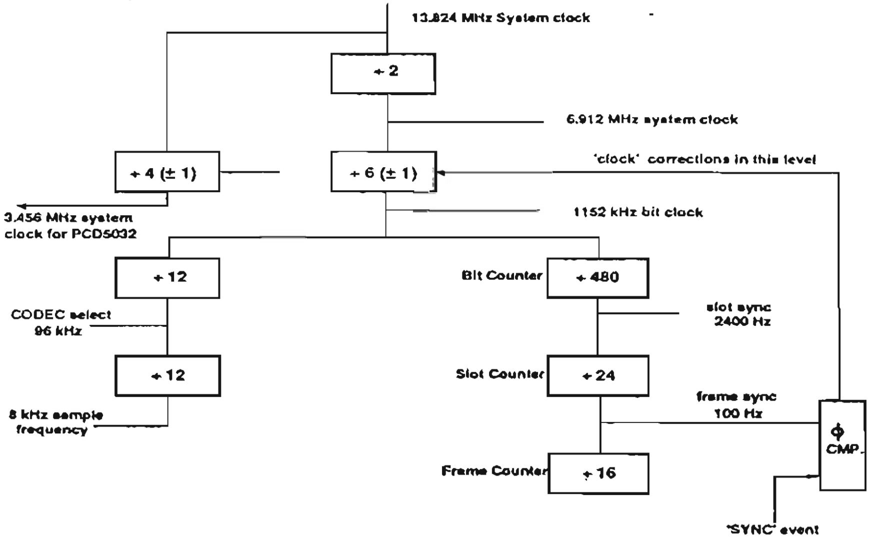


Figure 4.2: internal clocking scheme of the BMC

4.3. Programmable Communication Controller + Program Memory

4.3.1.PCC

The PCC is a RISC type controller and is used to control BMC functions, which are slot time accurate. It is well suited for bit manipulation, and runs at a clock frequency of 6.912 MHz (3.4 Mips). After having finished execution of a task, it switches to a power saving state, from which it returns after a pre-programmed time.

4.3.2.Program memory (PCD5040 only)

The PCC will fetch its program from a RAM memory, which is downloaded by the microcontroller during initialisation of the BMC, to allow maximum flexibility, with respect to:

- application area of DECT,
- parts of the MAC specification which are still to be evaluated,
- future radio architectures (zero-IF),
- flexibility to control different synthesizers,

To start the download procedure, the µ-Controller selects one of the two PCC program banks by writing the µC Interface Mode register. When MEM_SEL (pin 63) is made high, a memory bank is connected to the external address bus. The microcontroller will use the 2 kbyte BMC addressing range, to fill a Program Memory bank. Hereafter, MEM_SEL is made low, so the microcontroller can have normal access to the internal bus again. The same procedure is repeated for the second bank. The MEM_SEL pin must be kept HI during an internal bus transfer, because it is not latched internally.

Memory organisation

PCC program memory is 4 kbytes, organised as 2 blocks of each 2kbyte. The PCC can read them in parallel; in this way it reads one word at a time with the LO byte coming from Bank 0 and the HI byte coming from Bank 1. The µC-interface can read and write only in bytes. If Bank 0 is selected, the least significant bytes are addressed. If Bank 1 is selected, the most significant bytes are selected. See figure 4.3.

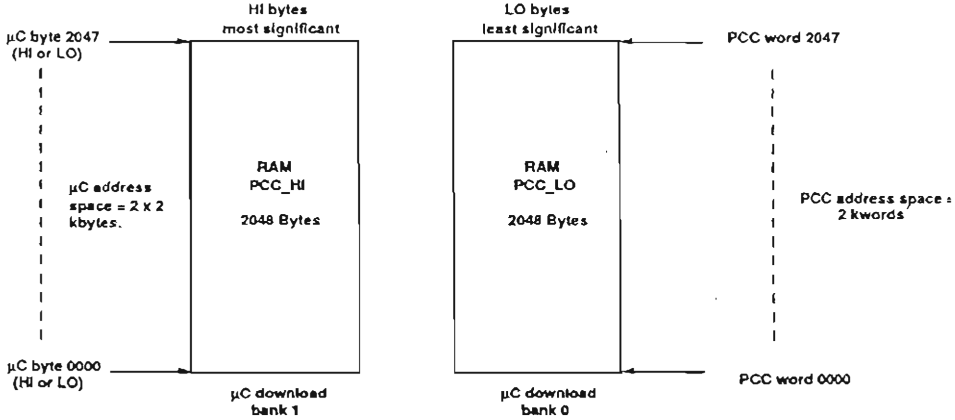


Figure 4.3: organisation of the PCC memory

4.3.3.PCC functions

Most important functions of the PCC are to:

- perform the appropriate actions on received messages, such as: identity checks, N_T-check procedure, TBC-handling, and thus also to;
- prepare A-field messages for transmission,
- prepare the RF-interface for the coming slot,
- perform the procedures for RSSI and set-up scan, maintaining scan counters and timers, assembling the RSSI field in the common data memory.
- filter events, and indicate them to the microcontroller (interrupt).

A complete description of the functional behaviour of the PCC program can be found in part 2 : DECT Burst Mode Controller Firmware.

4.4. Speech Interface

4.4.1. 12-Slot Mode

The 12-slot mode is selected, if 1 or 2 ADPCM codec(s) are connected to the BMC, where the BMC is the master of these codec's. In the handset, this is always the case. Also in simple base stations, which are connected with 1 or 2 analogue lines to the public network. Each codec is connected with a separate framing reference signal (FS1,FS2) to the BMC. Only two framing signals of the 12 are decoded externally. No interface logic is needed when using the PCD5032 ADPCM codec.

An indirection table is used, to determine (for reception and transmission) where to store/fetch speech data. The hardware speech-interface is capable to address the right speech buffer for the relevant speech slot, and will maintain a counter, carrying the offset to the fetched address.

4.4.2. 32-Slot Mode

The 32-slot mode is used to connect the BMC to a digital interface, with a 2Mb/sec interface. Up to 12 of the possible 32 slots on this interface can be used. The same indirection table, which is used in the 12-slot mode, is used for the 32-slot mode.

4.4.3. Muting

Due to various reasons the quality of the incoming speech data may be degraded significantly. By muting the speech data, these disturbances are not (or less) audible to the user. Two types of muting are distinguished by the BMC:

- fast muting
- slow muting

Fast muting, which is performed by the BMC automatically, is nothing more than a repetition of the previously received frame (80 speech samples) to the ADPCM codec. It is issued if no Sync word was detected.

Slow muting is issued by the µ-controller, after having detected a degradation of quality. A slow mute is implemented as a continuous `0000' nibble transmission to the ADPCM codec, until slow mute is released.

4.4.4. local call

A local call option is implemented, in order to loopback data from one codec to another codec, and vice versa, as illustrated below.

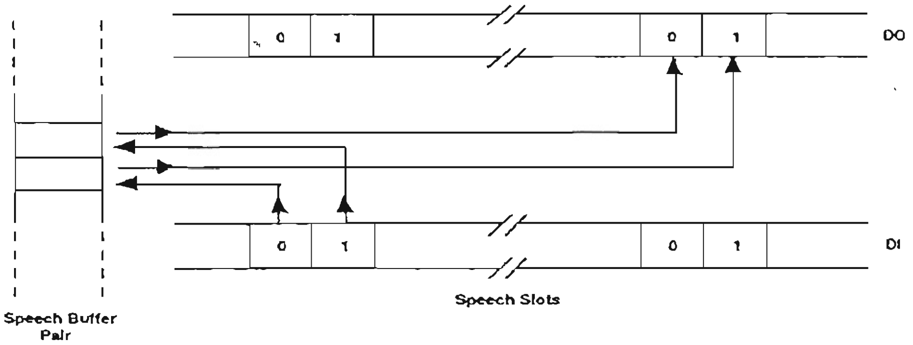


Figure 4.4 Local call switching on the speech-interface

4.5. RF Interface

Most of the functions, performed by the RF interface, are under control of the PCC. Especially the processing of non-speech data, programming of functions and registers, is done via the PCC.

4.5.1. Serial Receiver

The serial receiver processes the data, which comes from the radio head, and which is already filtered by the synchronisation part. The data is latched, using the recovered data clock.

The serial receiver will collect the complete A-field and B-field, and store it in the common data memory. Before the A-field is received, the A-field start address is programmed by the PCC. Upon reception of A-field nibbles, the address is updated by the serial receiver. Meanwhile, the PCC will program the B-field start address.

In figure 4.5 the data flow in the serial receiver is shown. The state machine, controlling the events and the data flow is not shown. Note that almost no decoding of messages is required. Only the header of the A-field needs to be decoded to check if a Cs message is received or transmitted, which requires the ciphering to be switched on also in the A-field

4.5.2. Serial Transmitter

The serial transmitter structure performs the reverse functions, compared to the receiver. Several blocks, used in the receiver, are also used in the transmitter. Amongst these are the CRC-generators, the scrambler, and the address registers. Figure 4.6 shows the serial transmitter structure

By transmitting the X-CRC twice, the Z-field is transmitted. The handling of the address registers is the same for the transmitter. Transmission of the synchronisation sequence (S-field) is done using the same method as the A-field and B-field. The S-field is stored in the common data memory, and will be fetched by the transmitter, just before transmission.

Not shown in the diagram, is that in the handset the data in the serial transmitter may be advanced by a programmable number of bit periods. This is done to compensate for the delay in the radio head.

Furthermore, the transmitted data can be inverted (using a switch in the BMC mode register), in order to connect the BMC to VCO's requiring a negative modulation.

4.5.3. Seamless Handover

Seamless handover guarantees that when the transfer of the speech information changes from one slot to an other, no speech samples are lost, added or displaced. Seamless handover is guaranteed by the following measures in the design of the Rx and Tx blocks in the RF interface:

- By using a lookup table, containing the correct start addresses of the B-fields in the data memory.
- The RF receive and transmit blocks will move and fetch data to/from the data memory block in 4-bit nibbles.

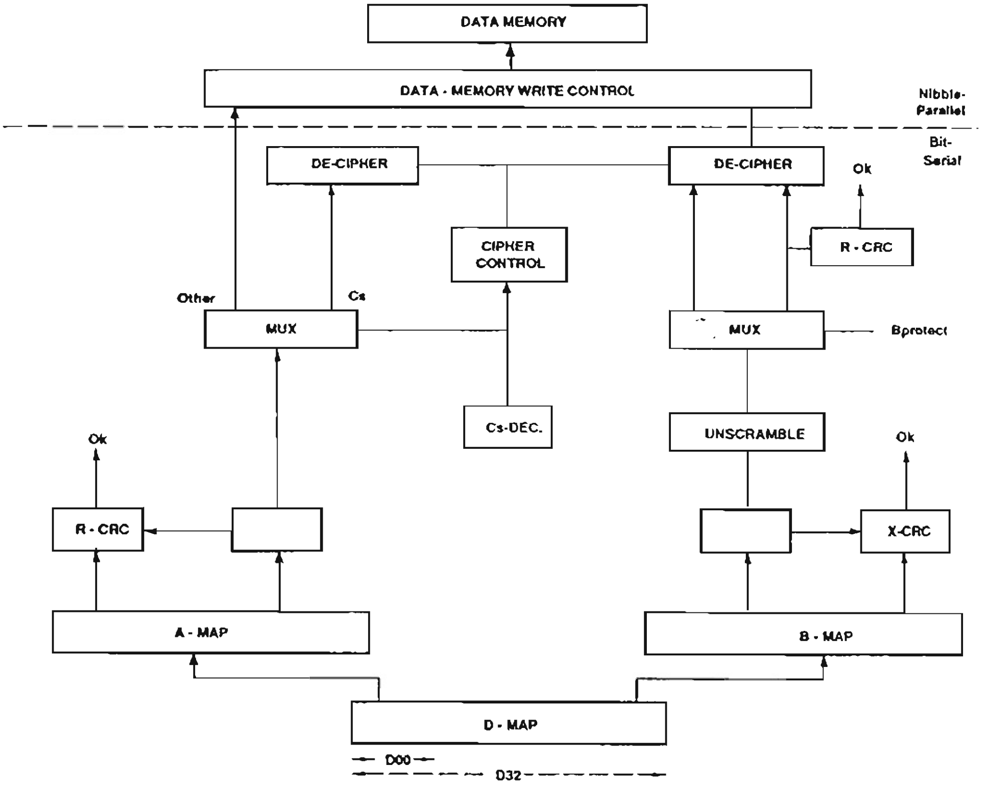


Figure 4.5 serial receiver structure

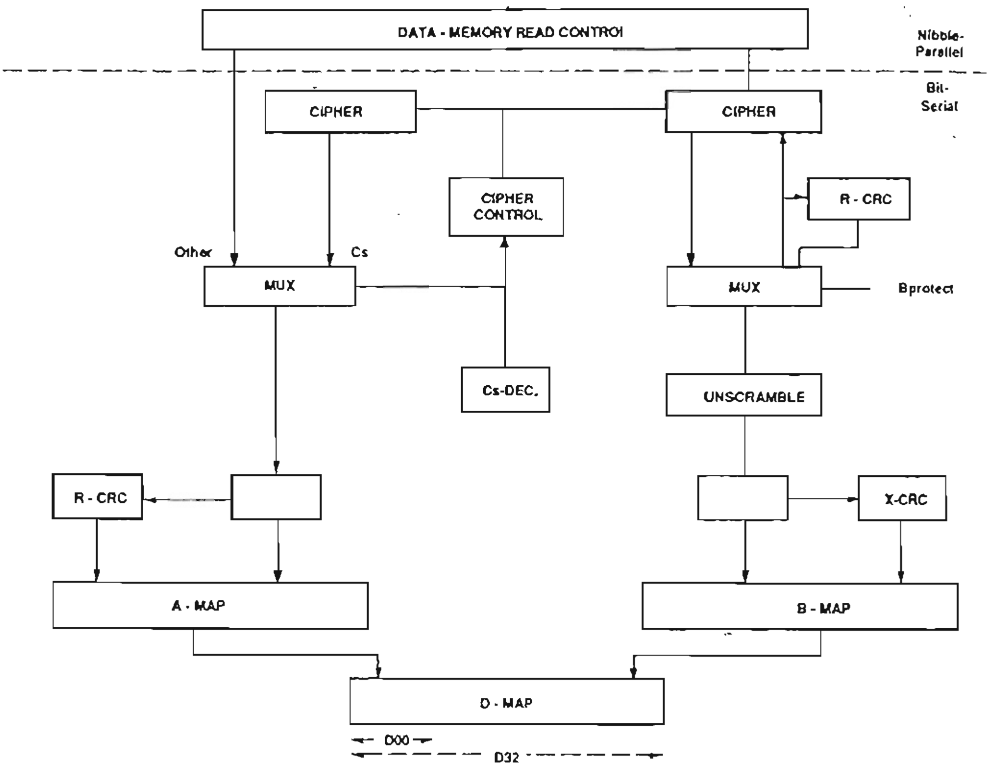


Figure 4.6 serial transmitter structure

4.5.4. RF Control Signals

The timing of the control signals to the radio head is fixed, but such that an RF delay between 1.5 and 7 µs can be tolerated (see section 5.3.2 for details). Only the transmitter ramp signal and the synthesizer enable are programmable within certain limits.

4.5.5. Synthesizer Programming

To program a synthesizer, a 3-wire serial interface is used. The signals on this interface are:

- S_ENABLE (enable)
- S_CLK (clock)
- S_DATA (data)

To program various types of synthesizers, a 3-byte shift register is present. Three data formats are supported: 8,16 or 24 bit words can be selected. The transfer of data from a frequency table in the common data memory to the shift register is under control of the PCC.

4.5.6. RSSI Measurement

The RSSI measurement in the BMC RF-interface block is done in 3 parts: a peak/hold detector, a 6-bit A/D converter, and an RSSI control block, which controls the peak/hold detector and the A/D converter. Once per slot time, a sample is fetched by the PCC, and saved in the appropriate area of the common data memory.

If the radio receiver is active in a particular time slot, the RSSI value will automatically be measured in that slot. Adjustment to the RSSI_AN input level can be made with VREF.

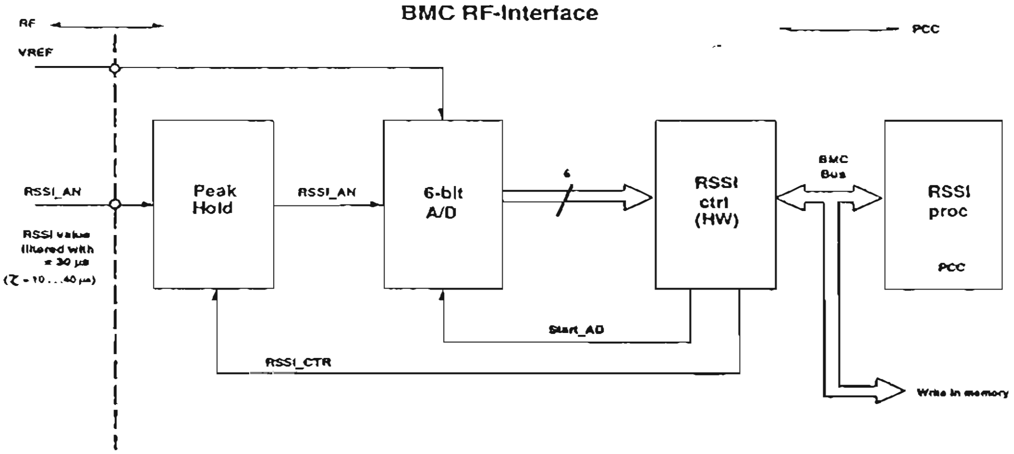


Figure 4.7 RSSI measurement path

4.5.7. Local call switching

The BMC provides a local call switching function in the base station. It will store incoming speech nibbles in the common data memory, in the area reserved for that particular receive slot. Then, during the transmit phase, it will pass to the transmit block, the start pointer of the same data memory area. Thus, the speech data is echoed to the other user (see illustration below). To handle quality degradation during local calls, a mute can be performed at the RF side of the speech buffer.

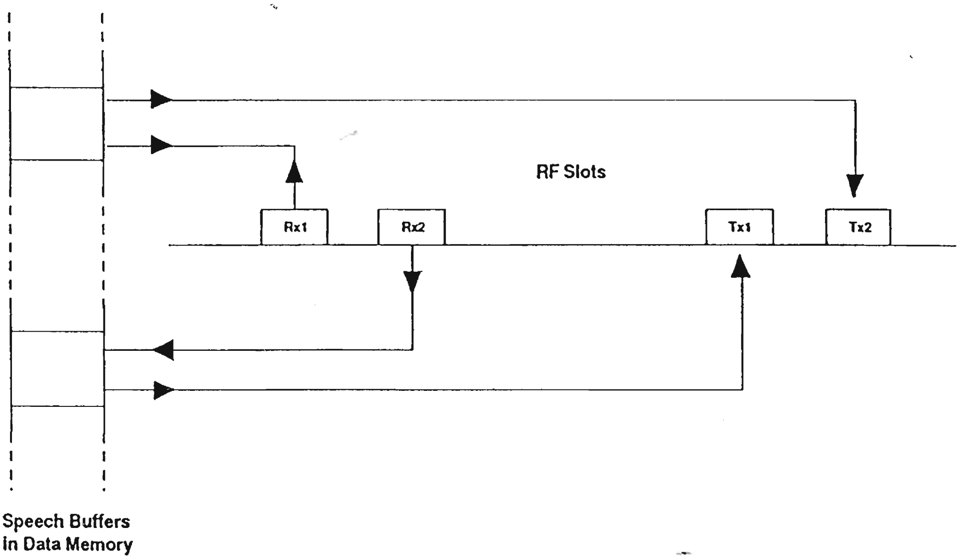


Figure 4.8: Local call switching on the RF-side

4.5.8. Data synchronisation

The data synchronisation is done in 2 phases:
- bit synchronisation
- sync word detection

Bit synchronisation is done using a Digital PLL (DPLL), with an oversampling factor of 12, i.e. the DPLL is running on a frequency, which is 12 times the data rate.

Sync word detection is achieved by checking the incoming data pattern with the expected synchronisation field pattern, using a correlator. The correlator has a programmable threshold, so it can accept bit errors in the sync field pattern up to the threshold level. Furthermore, the correlator window is programmable. This means, that only during a certain period (the time window), a `SlotSync' can be detected, indicating the slot synchronisation event.

The flow of the signals in the synchronisation part is shown in figure 4.9. Note, that in the base station the inverted data bits are shifted into the register. This is done, because the synchronisation field pattern is inverted for the base station, compared to the handset.

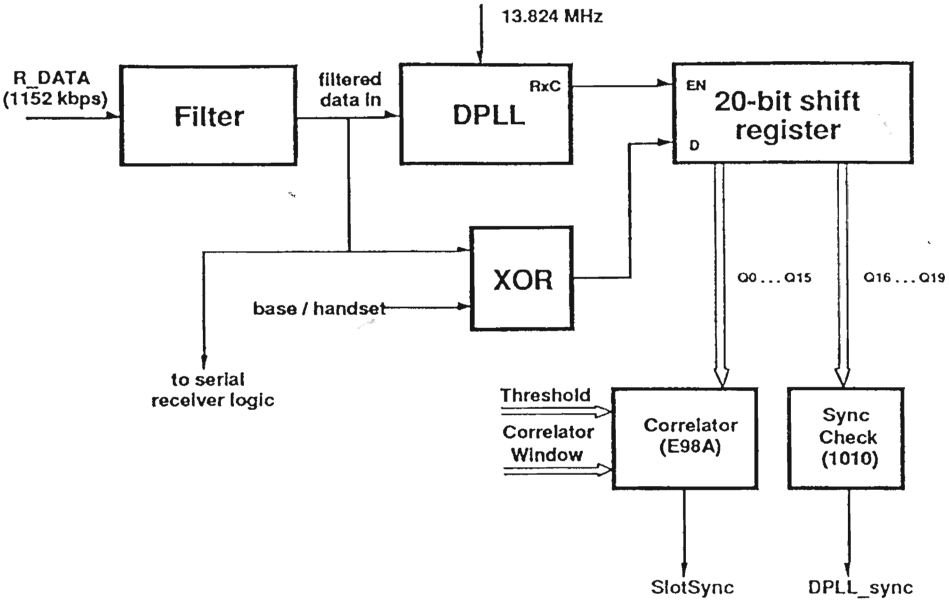


Figure 4.9: schematic of the receiver synchronisation part

The 'DPLL_sync' indication should only be used, when 'SlotSync' is active. It indicates that the last 4 bits of the preamble field (the training sequence) are received correctly, and thus indicates that the DPLL was in lock (synchronised) in time. If the 'SlotSync' is active, and the 'DPLL_sync' is not, then a sliding interferer might have been detected.

If 'SlotSync' is not detected, effectively no data is received in that slot. This implies a "fast mute" because speech data received in the previous frame is not destroyed.

4.5.9. Ciphering Machine

The description of the cipher machine is subject to confidentiality. The specification of its algorithms are delivered by ETSI after a Non Disclosure Agreement.

The cipher machine is under control of the TBC, which is implemented in the PCC. The cipher machine generates 2 fields of ciphering bits:
- A_cipher (40 bits) for A-field messages (Cs tail ONLY !!)
- B_cipher (320 bits) for speech in B-field

The transmitted ciphered bits are then:
- A_ciphered := A XOR A_cipher
- B_ciphered := B XOR B_cipher

On reception by the peered endpoint, deciphering consists of the same operation thanks to the synchronous generation of A_cipher and B_cipher.

The cipher machine is time-multiplexed on a slot basis. Initially, the Initialisation Vector (IV) and the key must be loaded into the cipher machine. Transfer of the IV and key from the common data area to the cipher machine is done automatically by the cipher machine. The contents of the memory space where IV and key are found, are the responsibility of the PCC, and the external µC.

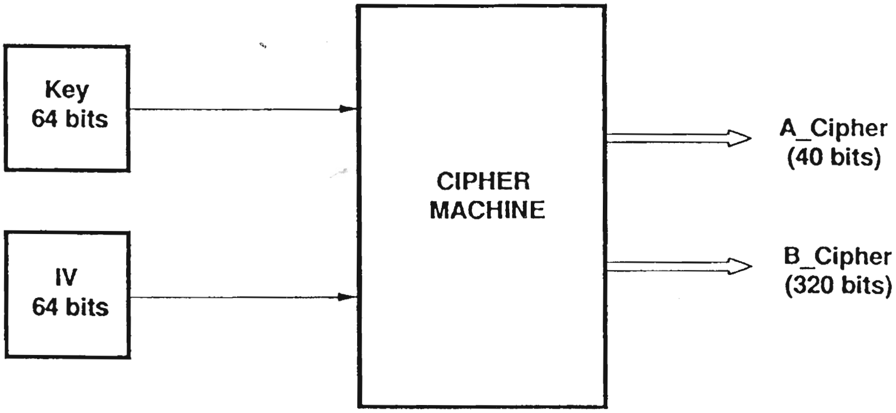


Figure 4.10: Cipher machine plus its sources

4.6. Microcontroller Interface

4.6.1. Function of the Microcontroller Interface.

The microcontroller Interface will provide the following services.

- Direct interface to processors which have an INTEL-8051 compatible interface.
- General interface to processors that can handle `wait states' e.g. 68000-family. In this case glue logic is required.
- Processor clock signal of which the frequency is programmable in order to adjust instantaneously processor performance to processor work load.
- A programmable interrupt register
- A watchdog timer with timeout periods of 1.25 or 82 seconds, depending on the programming.

The µC can address the BMC as any other RAM memory connected to the µC bus. By writing the `Interface-Mode Register', the µC can select the interface mode and it's own clock frequency.

4.6.2. Microcontroller Interrupts.

The function of µC Interrupts is to make optimal use of the µ-controllers processing power, and to achieve optimal cooperation between time-critical tasks and less time-critical tasks both executed in software. Three registers are available to handle interrupts. These are:

- Interrupt Event Register
- Interrupt Enable Register
- Interrupt Reset Register

These registers are to be regarded together. Corresponding bits in these registers relate to one and the same event. Bits in the Interrupt Event Register are set by the PCC and are to be reset by the external processor by writing '1's in the correponding bits in the Interrupt Reset Register. The mask in the Interrupt Enable Register enables the interrupt if corresponding events do occur.

4.6.3. Watchdog

The BMC is equipped with a watchdog timer, which generates a reset towards an external device (e.g. a µC) after timeout. Two (fixed) timeout periods can be programmed; 1.25 sec and 82 sec. The watchdog function can be disabled by using the EN_WATCHDOG input pin.

4.7. Power Down

The PCC may switch off the 6.912 MHz internal clock, to enter a power saving mode. All blocks, running on this clock are then switched off (i.e. RF-interface, cipher block, speech interface, PCC). This is called the power down state, and is only used in the handset mode.

The 13.824 MHz clock is never switched off. The Timing Control, µC interface, and Bus Controller keep running, in order to remain synchronous with a base station, and to keep the wake-up circuitry active. During power down the external µC has still access to the common data area.

GSM baseband interface

PCD5071

General Information

The baseband interface circuit pcd5071 is a fully CMOS IC. The baseband interface modulates the incoming data bits at a rate of 270.833 kb/s to Gaussian shaped Minimum Phase Shift Keying (GMSK), In phase (I) and Quadrature (Q) components. The I and Q components are derived using a digital filter. The filter uses four symbols and 8 times over-sampling of each symbol. Two 10 bit DAC's and analog filters complete the signal path. A symmetrical buffer driver allows direct connection of the differential I and Q outputs to a mixer converter in the RF part, converting the generated I/Q baseband signals directly to 900Mc frequency without additional filtering.

In the receiver part this pcd5071 demodulates the incoming 10.70 Mc IF data into 7 bits I and Q components. Sampling the incoming IF frequency in phase and with a 90 degrees phase shift makes it possible to regenerate digitally the I and Q components. The receive clock is derived from the 13 Mc master clock input by a PLL, which is partly integrated on chip. Optionally, the sampling scheme also allows to select between additional processing of I and Q, i.e. derotate on minus 90 degrees phase shift per symbol, derotate on plus 90 degrees phase shift per symbol or no derotate . When using derotate on it can be shown that the I and Q output components are approximated by amplitude modulated signals, which eases the DSP equalizer tasks.

Features

o GSM GMSK baseband modulator / demodulator
o Single interface circuit between Radio frontend and Baseband DSP
o Full CMOS, single 5 V supply
o Dissipation during active call in average less than 40 mW
o Power down mode
o Demodulates and derotates from a standard IF frequency; 10.70Mc
o Programmable derotate function
o Auto-adjusting DC-offset to control carrier suppression
o Auxillary 10 bit DAC for VCXO control

Quick reference data

Parameter	min	typ	max	unit
Vdd DC power supply	4.5V	5V	5.5	V
Idd max total power			38	mA
Transmitter			7.0	mA
Receiver			30	mA
Standby mode			4	mA
Power down mode			10	uA
Tamb ambient temperature	-25		+70	C
I/Q symmetrical outputs		1		Vpp
RFIN input frequency			10.70	MHz

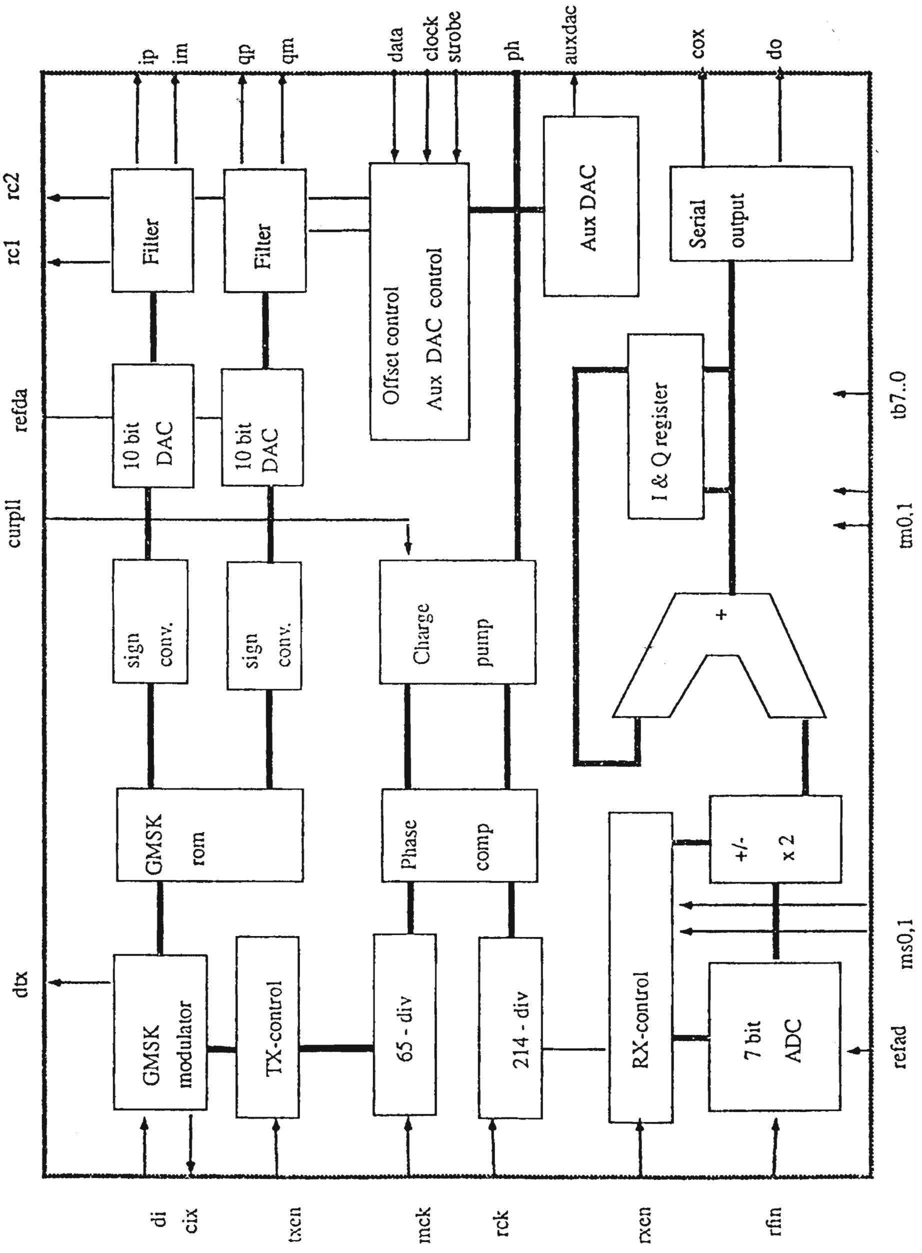
Ordering and package information

typenr	pins	package	material	code
pcd5071	44	QFP44SL	plastic	SOT307B.4

Application information

o Interface circuit between baseband processor and GSM RF frontend.

pcd5071 Block Diagram



pcd5071 Block Diagram

Clocks The transmit section (upper section in the block diagram) uses a 13/6 Mhz clock. The receive section uses a 43 Mhz and a 4.3 Mhz clock. A PLL, part of which is implemented on the chip generates the 43 Mhz clock from the 13 Mhz system clock.An external loop-filter and VCO are needed to complete the PLL.

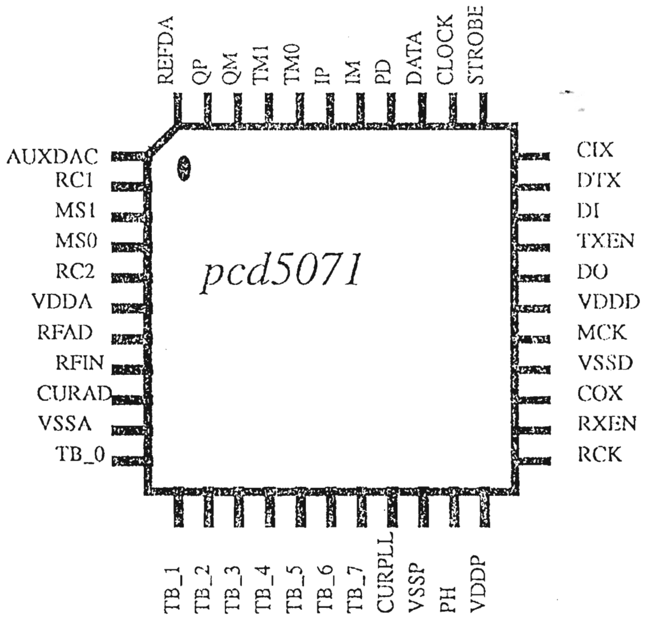
Transmit Blocks GMSK-mod and GMSK-rom generate digitally a GMSK modulation scheme with BT=0.3, as specified in the GSM recommendations 5.04. The differential encoding of the data-bits is also included in this block. The codes from the ROM are converted in two 10bit DAC's and filtered in two 3rd order equiripple delay filters. Both I and Q values have differential outputs.

Receiver The IF-signal is sampled by a 7 bit analog to digital converter. The output values are then processed in a decimating filter consisting of a sign-converter, a 12 bit full adder and two 12 bit registers. The resulting values for I and Q are serially transmitted to the outside world. Exact timing for ADC sampling, very important for the demodulation function, is supplied by the RX-cntrl block.

Offset control A three-wire serial bus is used to clock in two offset correction values, which will be fed into two 6 bits DAC's. The DAC's signal is fed into the filter to obtain a zero-offset output signal.

Auxdac The same serial bus is used to feed a 10bit DAC with its value. This analog signal is used to control the system's main 13 Mhz reference clock.

pcd5071 Pinning diagram:



All ground pins (Vss, Vssa & Vssp) are connected on chip.

Package: OFP44SL (SOT307B 4), 44-pin small quad flat pack

pcd5071 Pin description

1- AUXDAC	Voltage output of auxiliary dac.
2- RC1	External calibrating resistor for filter tuning. Nominally 20K ohms.
3- MS1	Derotation mode select input.
4- MS0	Derotation mode select input.
5- RC2	Filter calibrating resistor: connect between RC1 and RC2.
6- VDDA	Analog power supply.
7- REFAD	ADC reference output, 2.5 V. Connect a 100nF capacitor between REFAD and VSSA.
8- RFIN	Receiver input, connected to the IF output from the frontend.
9- CURAD	ADC Bias control input, nominally 100uA. Use a 27K pullup to VDDA.
10-VSSA	Analog ground.
11-TB_0	Bidirectional testbus. Used in scan, DAC and ADC tests.
12-TB_1	Bidirectional testbus.
13-TB_2	Bidirectional testbus.
14-TB_3	Bidirectional testbus.
15-TB_4	Bidirectional testbus.
16-TB_5	Bidirectional testbus.
17-TB_6	Bidirectional testbus.
18-TB_7	Bidirectional testbus.
19-CURPLL	Current control input for PLL, nominally 16 uA. Use a 190K pullup to VDDP.
20-VSSP	PLL chargepump ground.
21-PH	PLL chargepump output.
22-VDDP	PLL chargepump power supply.
23-RCK	43 Mhz clock input, reduced swing.
24-RXEN	Receive burst enable, active low.
25-COX	Clock output for received data. (f = MCK/3)
26-VSSD	Digital ground.
27-MCK	13 Mhz clock input, reduced swing.
28-VDDD	Digital power supply.
29-DO	Receiver data word output.
30-TXEN	Transmit burst enable. Active low.
31-DI	Transmitter data input.
32-DTX	Power amplifier control output. Used to suppress transmitting during speech pauses.
33-CIX	Clock output for transmitted data. This is a 271 kHz signal to the DSP.
34-STROBE	Serial interface strobe, active low.
35-CLOCK	Serial interface clock, positive edge triggered.
36-DATA	Serial interface data input.
37-PD	Power down input. When high, chip will enter power-down state.
38-IM	In phase component of transmitted signal (differential)
39-IP	In phase component of transmitted signal.
40-TM0	Test mode selection pin.
41-TM1	Test mode selection pin. Connect both to ground for normal operation.
42-QM	Quadrature component of transmitted signal (differential)
43-QP	Quadrature component of transmitted signal.
44-REFDA	DAC reference output, 2.35 V. Connect a 100nF capacitor between REFDA and VSSA.

All ground pins (Vss, Vssa & Vssp) are connected on chip.

Device operational modes.

Table 1: pcd5071 operation modes

tm1	tm0	pd	txen	rxen	ms0	ms1	Functionality
x	x	1	x	x	x	x	Power down state
0	0	0	1	1	x	x	Standby state
0	0	0	0	1	x	x	Transmitter active
0	0	0	0	0	0	0	Xmit & receive, derot forward
0	0	0	0	0	0	1	Xmit & receive, derot backward
0	0	0	0	0	1	0	Xmit & receive, equidistant sampling
0	0	0	1	0	0	0	Receiver, derotate forward
0	0	0	1	0	0	1	Receive, derotate backward
For testing purposes only:							
0	1	0	1	0	0	0	ADC test mode, derotate forward
0	1	0	1	0	0	1	ADC test mode, derotate backward
0	1	0	1	0	1	1	ADC test mode, equidistant
0	1	0	0	1	x	x	Dac test mode
1	0	0	x	x	x	x	Scan test, normal mode
1	1	0	x	x	x	x	Scan test, scan input

This table lists all relevant modes of the pcd5071. All modes will be explained in some more detail in the following pages.

A) Power down mode.

On a PD input equals high the pcd5071 will enter the powerdown state. In the this state all the clocks are switched off together with the power to the different opamps and resistor ladders. The PLL in the pcd5071 will also be powered down. Current consumption in powerdown mode will be less then 10 uA.
Power up time after PD goes low again is a function of the PLL loopfilter and VCO characteristics.

B) Standby mode.

In the standby mode neither the transmitter nor the receiver are activated. The PLL is active, thus generating the 43 Mhz secondary clock. This mode should also be used to initiate an offset auto-zeroing cycle on the filter & output circuitry. ADC and DAC circuits are powered down in standby mode. State of the auxiliary DAC is controlled via the serial bus.

C) Transmit mode.

A TXEN transition from high-to-low in standby mode initiates the transmit active mode. In this mode the pcd5071 accepts a 270Khz bitstream from the GSM DSP and converts them into modulation data for the GSM mixer. The first bit of each transmission burst will be latched and put onto the DTX pin, which in turns controls the power output module. This enables a rapid suppression of a transmit burst should the speechcoder have detected a speech pause.The GMSK modulated datastream has a 2.2 Mhz rate due to the 8-fold oversampling that is used. On a Low to

High transition of the TXEN pin the pcd5071 reenters the standby mode. Transmission of the current bit will be finished.

D) Receive modes.

A RXEN transition from high-to-low in standby mode initiates the receiver active mode. In this mode the receiver samples the 10.70 MHz IF frequency delivered by the frontend to obtain 9 I and 8 Q samples for each bitperiod. These 7-bit samples will be averaged and transmitted serially to the DSP. Exact timing of the sampling moments is required to perform the derotation function. Three possible derotation functions are implemented. Selection takes place with theMS0 & MS1 pins:

Table 2: Derotation modes

ms1	ms2	Derotation mode
0	0	Derotate forward
1	0	Derotate backward
1	1	Equidistant sampling

The equidistant sample mode is for testing purposes only and should not be used in normal operation.
A low-to-high transition of the RXEN pin will terminate the receive-active mode and the device will reenter the standby mode. Transmission of the last bit will NOT be completed, i.e. the DSP will receive an incomplete word for the last bit. Duration of the RXEN active period should be calculated so that no useful bits will be lost.

E) DAC test mode.

The DAC test mode is used to access the DAC's directly. In this mode, the testbus is connected to the input of both DAC's and to the auxiliary DAC. Since the DAC's are 10 bits wide and the testbus is only 8 bits wide, 2 extra signals are needed for a fully parallel access: derotation select signals MS1 and MS0 will serve as inputs to bits 9 and 8 of the DAC resp. Data are latched into an internal buffer before being passed on to the main DAC's. No buffer is present for the auxiliary DAC. Offset adjust circuitry is active in this mode and herefore must be initialized before meaningful measurements can take place.

F) ADC test mode.

The ADC test mode is used to access the ADC directly. In this mode, the testbus is connected to the output of the ADC. The derotation mode is also active, so derotation select signals MS1 and MS0 must be used to ensure predictable operation. To facilitate ADC testing, the equidistant sampling mode (MS1=1, MS0=1) should be used. In this mode he ADC will generate one sample for each nine periods of the 43 MHz secondary clock i.e. 4.7 megasamples per second.

G) Scan test normal mode.

Scan test normal mode is used to exercise the digital circuitry according to the ATPG patterns.

H) Scan test shift mode.

Scan test shift mode is used to shift in the testpatterns generated by ATPG programs. The same mode is used to shift out the results of the scan test normal mode.

DSP interface

The interface to the DSP uses TTL level I/O's. The interface to the DSP can be split in a receive section and a transmit section where the transmit section comprises three lines:

o TXEN: transmit enable input which is low active
o CIX: Transmit clock output
o DI: Data input

When TXEN is low the first bit on DI is clocked in on a positive edge of CIX. CIX will change from high to low after TXEN is low. Cix will have an average period of 3.69 micro seconds. To power up the DAC's the first positive transition of Cix is delayed with half a bit period. The first I/Q samples are generated one bit period after TXEN becomes low. To send N bits, the TXEN signal must be active for N symbol periods. N+1 bits are read from the DSP processor, of which the last one will be discarded.

The receive section also comprises three lines:

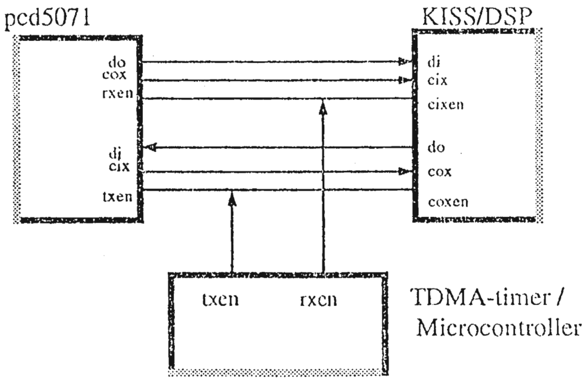
o RXEN: Receive enable input which is low active
o COX: Receive clock output
o DO: Data output

Whenever RXEN changes from high to low the receive section will be activated. At the first transition of the COX clock from high to low the first bit is put on Do output. The format is shown below:

I7 I6 I5 I4 I3 I2 I1 I0 Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0.

Where the MSB (I7) is transmitted first and the digital word is coded in two's complement notation.
To power up the ADC and to fill the pipeline registers with enough data, the first negative transition of Cox clock is delayed with approx. one symbol period. Duration of RXEN is therefore N + 1 symbol periods. RXEN synchronizes the sampling scheme to the TDMA frame and the symbol timing.

DSP interface



DC adjustments / serial bus.

To adjust carrier suppression a DC offset adjustment is foreseen in the pcd5071. This adjustment is either automatic or fixed by the GSM system microcontroller. The offset adjustment block is controlled via the GSM chipset's fast three wire serial bus. Instructions are send via this bus to several devices in the GSM chipset. These instructions are all 16 bits wide, with the four most significant bits being the device code. The device code for the pcd5071 is '1001', decimal 9. The remaining 12 bits can be interpreted at will by the various devices. In case of the pcd5071, the 12 bits are formed by a 6 bit instruction and a 6 bit data word.

Serial Programming bus

A simple 3-line unidirectional serial bus is used to program the automatic offset-adjusting loop. The 3 wires are: data, clk and strobe. The data sent to the device are loaded in bursts framed by strobe. Data bits are clocked in on a positive going edge of the clock, if the enable is low. The programmed information is loaded into the pcd5071 on the first positive edge of the clock after enable went high. Only the last 16 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. Signals necessary to maintain proper operation of the serial bus are described in the AC characteristics section of this datasheet.

Table 1: Programming register bit usage

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
i1	i0	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	a3	a2	a1	a0
2 b instr.		10 bit data field										1	0	0	1
INSTRUCTION						DATA						I.D. CODE			

Data Format

Data is entered with the most significant bit first. The leading bits make up the data field, whilst the trailing four bits are an address field. The pcd5071 uses only 1 of the available addresses.
The trailing address bits are decoded upon the inactive strobe edge. This produces an internal load pulse to store the data in one of the addressed latches. To avoid erroneous circuit operation, the pulse is not allowed during data reads by the rest of the circuit. This condition is guaranteed by respecting a minimum strobe pulse width after data transfer
The offset-adjust values at initial powerup are undefined, therefore an auto-adjust cycle should be started on both I & Q channels should be performed before start of the first transmission burst. Offset adjust values are maintained during powerdown and standby states.

In order to obtain proper operation of the device , at least three instructions must be carried out after device initialisation :

Firstly an instruction to define auxillary DAC and comperator status, then a load 100000 on both I and Q offset DAC's, or an auto-adjust cycle on both I & Q. Lastly, a value for the AUXDAC should be entered in order to obtain a clearly defined value at the auxdac output

Normal operation would be

instr.1) 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 : AUX. DAC powered up, normal comperator operation
instr 2) 0 0 0 1 1 1 0 0 0 0 0 0 1 0 0 1 : Perform autoadjust on I and Q
instr 3) 1 1 1 0 0 0 0 0 0 0 0 0 1 0 0 1 : Put AUX DAC at middle value

Table 2: pcd5071 Instructions

15	14	13	12	11	10	Function
I1	I0	D9	D8	D7	D6	
0	0	0	0	0	1	Load I offsetregister
0	0	0	0	1	0	Load Q offsetregister
0	0	0	0	1	1	Load I and Q register
0	0	0	1	0	1	Autoadjust I-section offset
0	0	0	1	1	0	Autoadjust Q-section offset
0	0	0	1	1	1	Autoadjust I and Q sections
0	1	Identical to above				Filter inputs remain shortcircuited after instruction.*
1	0	1	x	x	x	Auxiliary DAC powered down
1	0	0	x	x	x	Auxiliary DAC active
1	0	x	1	x	x	Invert operation of comperators
1	0	x	0	x	x	Normal operation of comparators
1	1	d9	d8	d7	d6	Load Auxiliary DAC with a 10b value

*) Use any other instruction to revert to normal operation.

Transmit mixer interface.

A symmetrical buffer driver, driving 1Vpp into a load impedance of typically 50kohm//10pF, in both I and Q outputs, with a common mode DC offset of nominal 2.35 V which allows direct connection to the transmitter mixer circuit.

Receiver interface.

Maximum input is 1.8 Vpp input swing and frequency is typically 10.70 Mc; The input impedance is less than 20 pF and more than 10 kohm. Normally the RFIN input is AC coupled to the 10.70 Mc RF output. The DC level is maintained to 1 Volt with the aid of two resistors.

Auxiliary DAC interface.

A 10-bit DAC followed with a x 2 buffer is used to generate a voltage with range from 0.4 V to 4.5V. This is used to control the system's main 13 Mhz clock . Output impedance is less than 25K Ohms.

Maximum ratings

Limiting values in accordance with the Absolute Maximum System (IEC134)

Parameter	Symbol	Min	Max	unit
Supply voltage VDDD, VDDA, VDDP		-0.5	+6.5	Volts
Maximum supply voltage offset			0.5	Volts
All input voltages		Vi -0.5	Vdd+0.5	Volts
DC current into any input or output Ii,Io			5	mA
Total power dissipation	Ptot		tbf	mW
Storage temperature range	Tstg	-65	150	C
Operating ambient temperature range	Tamb	-25	70	C
Operating junction temperature	Tj		85	C

Operating currents

VDD D= VDDA = VDDP = 5V +/-10%, Vss = 0V, ambient temp = -25/70 C

	min	typ	max	unit	conditions
into Vddd					
TX_active			5.0	mA	PD=0, TXEN=0, RXEN=1
RC_active			5.1	mA	PD=0, TXEN=1, RXEN=0
Standby			3.0	mA	PD=0, TXEN=1, RXEN=1
powerdown			3	uA	PD=1, TXEN=x, RXEN=x
into Vdda (= DAC + ADC + filters + auxdac)					
TX_active			13.0	mA	PD=0, TXEN=0, RXEN=1
RC_active			26	mA	PD=0, TXEN=1, RXEN=0
Standby			3.0	uA	PD=0, TXEN=1, RXEN=1
powerdown			3.0	uA	PD=1, TXEN=x, RXEN=x
Auxillary DAC alone		0.7	1.0	mA	Only AUX DAC active
into Vddp (= PLL supply voltage)					
Standby		0.35	0.9	mA	PD=0
powerdown			3.0	uA	PD=1

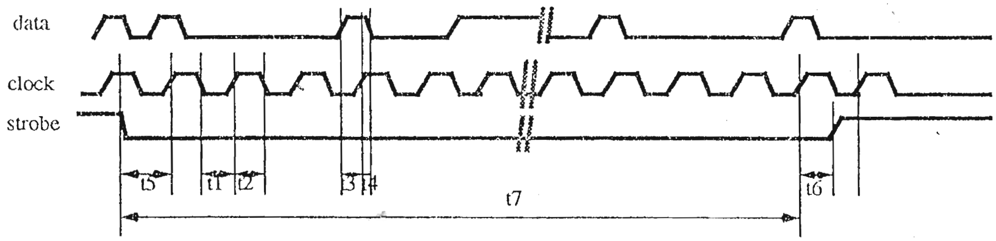
DC characteristics

Digital interfaces:	min	typ	max	unit	conditions
inputs : (MS0, MS1, DI, TXEN, RXEN, PD, DATA, STROBE, CLOCK)					
input level low			0.8	V	(= TTL level)
input level high	2			V	(= TTL level)
outputs : (COX, CIX, DO, DTX)					
output level low			0.4	V	@ 1.6 mA
output level high	2.4			V	(= TTL level)

Unit	Min.	Nom.	Max	Units	Remarks
Transmitter specification					
Dac resolution		10		bits	
Integral nonlinearity			+/- 1	LSB	
Differential nonlinearity			+/- 1	LSB	
Unadjusted offset voltage			+/- 30	mV	
Offset compensation range		64		mV	-32 to + 32 mV
Output spectrum mask			-1	dB	0 - 100 kHz
	30			dB	200 kHz
	33			dB	250 kHz
	60			dB	400 kHz
	70			dB	600kHz
	70			dB	2 Mhz
Matching I vs. Q amplitude			0.25	dB	at 67.5 kHz
			tbd	dB	at 250 kHz
Matching Group delay		30		ns	
Group delay ripple		10		ns	
PSRR		60		dB	
IP - IM and QP- QM differential output swing	0.9	1	1.1	V-	into 10kohm diff //10pF
Dc offset		2.35		V	
Group delay analog part	1.4	1.5	1.6	usec	DAC + Filter
REF_DAC DAC reference voltage		2.35		V	With Cd=100nF
MCK					
Input level		600		mVpp	Vdd/2 offset voltage
impedance		5		kohm	at 13MHz,

Unit	Min.	Nom.	Max	Units	Remarks
Receiver specification					
ADC resolution	7			bits	DC to 4.75 MHz
Differential non lin.			+/-1	LSB	
Integral non lin.			+/-1	LSB	
Group delay		3.69		us	RXEN to DO
RFIN					
input voltage range	0		2.0	V	AC coupled
DC offset		1		V	
frequency		10.70		MHz	
input impedance		60		kohm	at Fs=4.75 MHz
		15		pF	
REF_AD					
Reference voltage output		2.0		V	With C d= 100 nF
CUR_AD					
Bias current control input		tbf		uA	Use a 27k pullup
RCK					
Input level		600		mVpp	Vdd/2 offset voltage
impedance		5		kohm	at 43 MHz.
PLL charge pump specification					
CURPLL					
Pll current control input		16		uA	Use a 190K pullup
PH					
Absolute output current	400	512	600	uA	Positive or negative
Leakage current			100	nA	
Phase detector gain Kd		81.5		uA/rad	
Auxiliary DAC specification					
Dac resolution		10		bits	
Integral nonlinearity			+/- 4	LSB	
Differential nonlinearity			+/- 1	LSB	
Useful output voltage range	0.4		4.5	V	
LSB		4.5/1024		V	

Serial interface timing diagram



Timing parameter		min	max	units	remarks
clock period L	t1	50		ns	
clock period H	t2	50		ns	
data setup time	t3	tbd		ns	
data hold time	t4			ns	
strobe setup time	t5	tbd		ns	
stobe hold time	t6	tbd		ns	
Minimal strobe active time	t7	1.85		us	

POCSAG paging decoder PCF5001

FEATURES

- Wide operating supply voltage range (1.5 to 6.0 V)
- Extended temperature range: –40 to +85 °C (between –40 to –10 °C, minimum supply voltage restricted to 1.8 V), see Chapter “Limiting values”
- Very low supply current (60 µA typ. with 76.8 kHz crystal)
- Decodes CCIR radio paging Code No. 1 (POCSAG-code)
- Programmable call termination conditions
- 512 and 1 200 bits/s data rates (2400 bits/s with some restrictions), see Section “Decoding of the POCSAG data stream”
- Improved ACCESS synchronization algorithm
- Supports 4 user addresses (RICs) in two independent frames
- Eight different alert cadences
- Directly drives magnetic or piezo ceramic beeper
- High level alert requires only a single external transistor
- Optional vibrator type alerting
- Silent call storage, up to eight different calls
- Repeat alarm facility
- Programmable duplicate call suppression
- Interfaces directly to UAA2033T, UAA2050T and UAA2080 digital paging receivers
- Programmable receiver power control for battery economy
- On-chip non-volatile EEPROM storage
- On-chip voltage converter with improved drive capability
- Serial microcontroller interface for display pager applications
- Optional visual indication of received call data using a modified RS232 format
- Level shifted microcontroller interface signals
- Alert on low battery
- Optional out-of-range indication.

APPLICATIONS

- Alert-only pagers, display pagers
- Telepoint
- Telemetry/data receivers.

GENERAL DESCRIPTION

The PCF5001 is a fully integrated low-power decoder and pager controller. It decodes the CCIR radio paging Code No.1 (POCSAG-Code) at 512 and 1 200 bits/s data rates. The PCF5001 is fabricated in SACMOS technology to ensure low power consumption at low supply voltages.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF5001T	28	SO28L	plastic	SOT136-1
PCF5001H	32	TQFP32(1)	plastic	SOT358-1

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *“Quality Reference Pocketbook”* (order number 9398 510 34011) are followed.

BLOCK DIAGRAMS

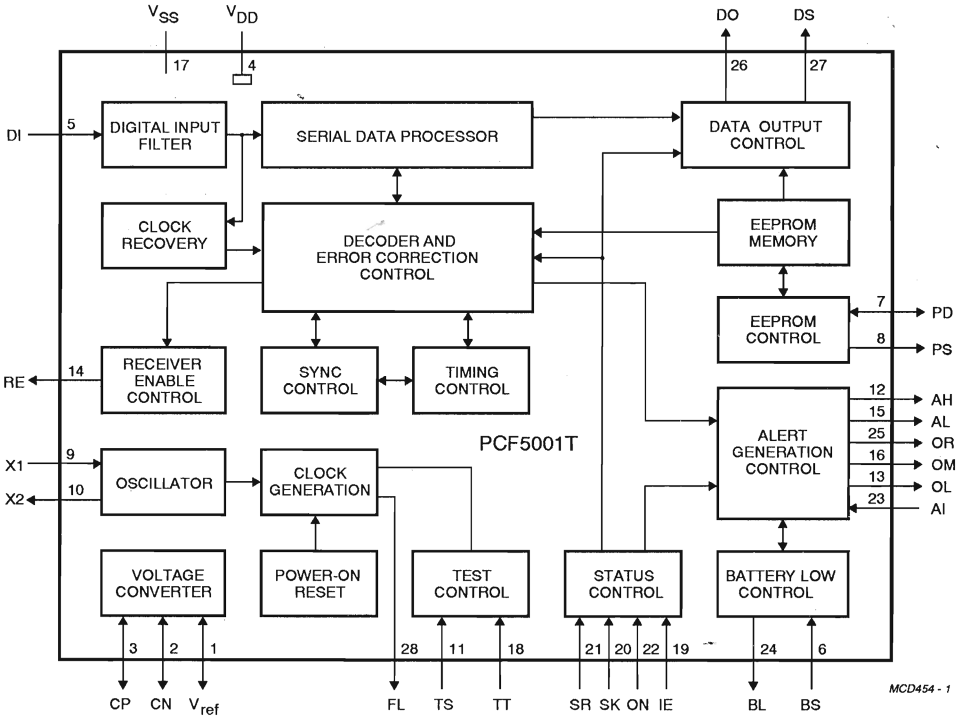


Fig.1 Block diagram (SO28L; SOT136-1).

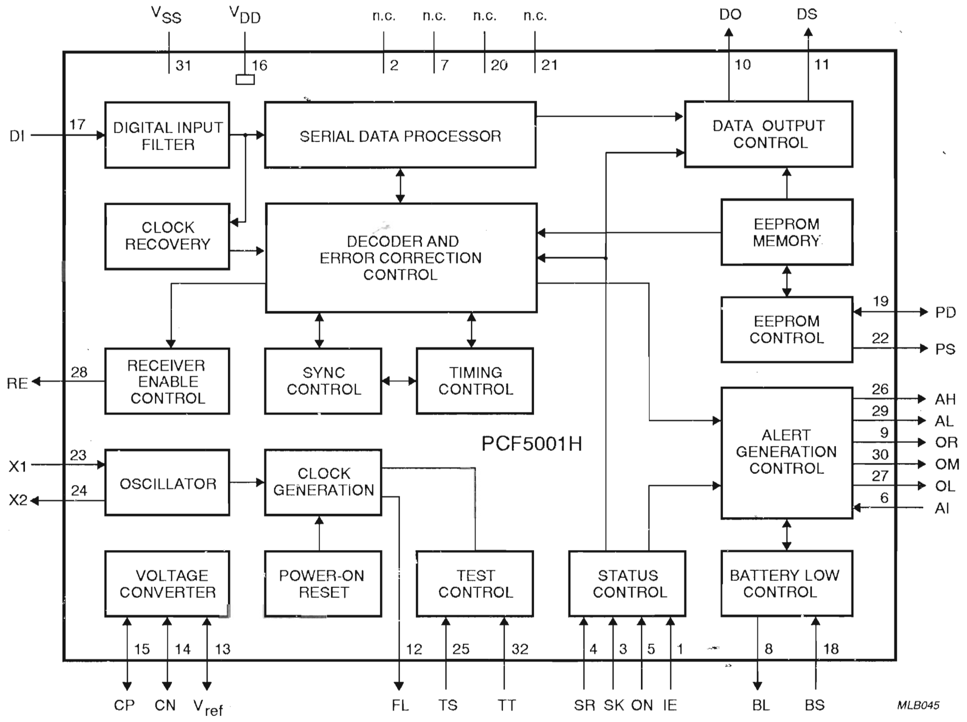


Fig.2 Block diagram (TQFP32; SOT358-1).

PINNING

SYMBOL	PIN		DESCRIPTION
	SO28L SOT136-1	TQFP32 SOT358-1	
V_{ref}	1	13	Microcontroller interface reference voltage output. The LOW level of pins FL, DS, DO, OR, BL, AI, ON, SK, SR and IE is related to the voltage on V_{ref}. May be driven from an external negative voltage source or must be connected to V_{SS}, if pins CN and CP are left open-circuit. When the on-chip voltage converter is used, this pin provides a negative output voltage.
CN	2	14	Voltage converter external shunt capacitance, negative side. Connect the negative side of the shunt capacitor to this pin, if the on-chip voltage converter function is used.
CP	3	15	Voltage converter external shunt capacitor, positive side. Connect the positive side of the shunt capacitor to this pin, if the on-chip voltage converter function is used.
V_{DD}	4	16	Main positive power supply. This pin is common to all supply voltages and is referred to as 0 V (common).
DI	5	17	Serial data input (POCSAG code). The serial data signal train applied to this pin is processed by the decoder. Pulled LOW by an on-chip pull-down when the receiver is disabled (RE = LOW).
BS	6	18	Battery-low indication input. The decoder samples this input during synchronization scan, when it is in ON or SILENT status and the receiver is enabled (RE = HIGH). A battery-low condition is assumed, if the decoder detects four consecutive samples HIGH. An audible battery-low indication is made by the decoder, when operating in ON status. Normally LOW by the operation of an on-chip pull-down.
PD	7	19	EEPROM programming data input and output. Normally HIGH by the operation of an on-chip pull-up. During programming of the on-chip EEPROM, PD is a bidirectional data and control signal.
PS	8	22	EEPROM programming strobe input. Normally LOW by the operation of an on-chip pull-down. During programming of the on-chip EEPROM, PS is a unidirectional control input.
X1	9	23	Crystal oscillator input. Connect a 32768 Hz or 76800 Hz crystal and a biasing resistor between this pin and X2. In addition, provide a load capacitance to V_{DD}, which may also be used for frequency tuning.
X2	10	24	Crystal oscillator output. Return connection for the external crystal and resistor at X1.
TS	11	25	Scan test mode enable input. Always LOW by operation of an on-chip pull-down.
AH	12	26	Alert HIGH-level output. This output can directly drive an external bipolar transistor to control HIGH-level alerting in conjunction with AL, by means of an alerter or beeper.
OL	13	27	LED indication output. This output can directly drive an external bipolar transistor to control the visual alert function by means of an LED. It may also be used for visual indication of received call data during call reception.

SYMBOL	PIN		DESCRIPTION
	SO28L SOT136-1	**TQFP32 SOT358-1**	
RE	14	28	Receiver enable output. May be used to control the paging receiver power control input, to minimize power consumption. The decoder provides a HIGH-level at this pin, when receiver operation is requested. Each time the decoder does not require any input data at DI the receiver enable output is LOW.
AL	15	29	Alert LOW-level output. Open drain alert output in anti-phase to AH, to provide LOW-level alerting. HIGH-level alerting is generated in conjunction with AH.
OM	16	30	Vibrator output. This output can directly drive an external bipolar transistor to control a vibrator type alerter.
V_{SS}	17	31	Main negative supply voltage.
TT	18	32	Test mode enable input. Always LOW by operation of an on-chip pull-down.
IE	19	1	Interface enable input. While the interface enable input is active HIGH, operation of the ON, SK, SR, AI, BL and OR inputs and outputs is possible. When IE is LOW the inputs do not respond to applied signals and the outputs are made high-impedance. In alert only pager mode the interface enable input does not have any effect on the operation of inputs ON, SK and SR, but IE must be referenced to LOW or HIGH.
SK	20	3	Silent state control input. The silent control input selects the decoder ON status (LOW-level) or SILENT status (HIGH-level), if the ON input is active HIGH. An on-chip pull-up is provided, if the decoder has been programmed for alert-only pager mode, whereby the pull-up is disabled for display pager mode. In display pager mode status change is possible provided the interface enable input (IE) is HIGH and the status is latched on the falling edge of IE.
SR	21	4	Status request and reset input. A HIGH-going pulse on this input causes (a) status indication cadence to be generated, if the decoder is not alerting or (b) resetting of a call alert, repeated call alert or battery-low alert, if active or (c) triggers the call store re-alert facility, if repeat mode is active. In display pager mode operation of SR is possible only, if the interface control input is active. Normally LOW by the operation of an on-chip pull-down.
ON	22	5	On/off control input. The on/off control input selects the decoder ON status (HIGH-level) or OFF status (LOW-level). An on-chip pull-up resistor is provided, if the decoder has been programmed for alert-only pager mode, but the pull-up resistor is disabled for display pager mode. In display pager mode status change is possible provided the interface enable input (IE) is HIGH and the status is latched on the falling edge of IE.
AI	23	6	Alarm input. A HIGH-level on this input causes generation of a continuous HIGH-level alert via AH and AL outputs, if the decoder operates in ON status or OFF status. In addition, the LED output is active independent from the decoder status, but in accordance with AI. Pulsing the input may be used to modulate the alert and LED indication. Normally LOW in alert-only pager mode by operation of an on-chip pull-down.

SYMBOL	PIN		DESCRIPTION
	SO28L SOT136-1	TQFP32 SOT358-1	
BL	24	8	Battery-low indication output. If the decoder encounters a battery-low condition a battery-low output latch is set HIGH. The battery-low output latch may be tested for a battery-low condition, whenever the interface enable input (IE) is active (HIGH), otherwise the battery-low output is made high-impedance. The battery-low output latch is reset only, by switching the decoder to OFF status.
OR	25	9	Out-of-range indication output. Whenever the decoder detects an out-of-range condition an out-of-range output latch is set HIGH after expiry of the programmed out-of-range hold-off time selected by means of special programming (SPF06 and SPF07) of the EEPROM. The out-of-range latch may be tested for an out-of-range condition, whenever the interface enable input (IE) is active (HIGH), otherwise the out-of-range output is made high-impedance. The out-of- range output is reset by detection of a valid data transmission or by switching the decoder to OFF status.
DO	26	10	Serial interface data output. During normal decoder operation, accepted calls and possibly subsequent message data are serially output via this pin in conjunction with the data strobe output (DS). This pin is also used to output the EEPROM contents upon special command, if the decoder is programmed for display pager.
DS	27	11	Serial interface data strobe output. Provides a clock signal for the received call data and EEPROM data appearing at the data output (DO). Each time this output is LOW the data at DO is valid. Additional start and stop conditions allow easy identification of data sequence start and end.
FL	28	12	Frequency reference output. When programmed for display pager mode, this output provides a clock reference with 16384 or 32768 Hz per second, selected by SPF32. See Chapter “Functional description” .
n.c.	–	2, 7, 20, 21	Not connected.

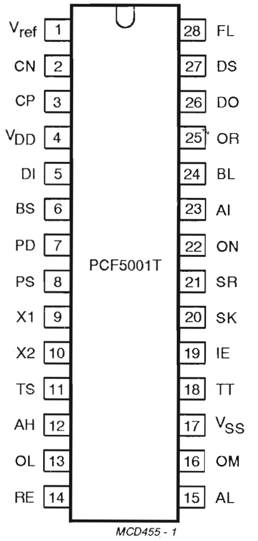


Fig.3 Pin configuration (SO28L; SOT136-1).

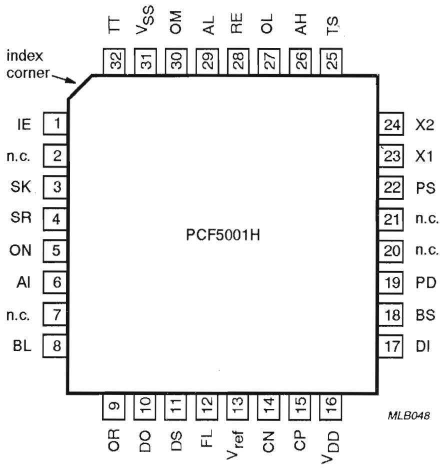


Fig.4 Pin configuration (TQFP32; SOT358-1).

FUNCTIONAL DESCRIPTION

The PCF5001 is a very low power Decoder and Pager Controller specifically designed for use in new generation radio pagers. The architecture of the PCF5001 allows for flexible application in a wide variety of radio pager designs.

The PCF5001 is fully compatible with *"CCIR radio paging Code Number 1"* (also known as the POCSAG code) operating at the originally specified 512 bits/s data rate, and also at the newly specified 1200 bits/s data rate (2400 bits/s operation is also possible). The PCF5001 also offers features which extend the basic flexibility and efficiency of this code standard.

The PCF5001 supports two basic modes of operation

In Alert-Only-Pager mode only a minimum number of external components are required to build a complete tone-only pager. Selection of operating states ON, OFF or SILENT is achieved using a slider switch interface.

In Display-Pager mode the state input logic is switched to a bus interface structure. Received calls and messages are transferred to an external microcontroller via the serial microcontroller interface. A built-in voltage converter with increased drive capabilities can supply doubled supply voltage output, and appropriate logic level shifting on microcontroller interface signals is provided.

Upon reception of valid calls one of eight different call cadences is generated; upon status interrogation status indication tones make the current status of the decoder available to the user.

On-chip non-volatile 114-bit EEPROM storage is provided to hold up to four user addresses, two frame numbers and the programmed decoder configuration.

Synchronization to the input data stream is achieved using the improved ACCESS algorithm, which allows for data synchronization and re-synchronization without preamble detection while minimizing battery power consumption by receiver power control. One of four error correction algorithms is applied to the received data to optimize the call success rate.

The POCSAG paging code

A transmission using the CCIR radio paging Code No.1 (POCSAG code) is constructed in accordance with the following rules (see Fig.5).

The transmission is started by sending a preamble, which is a sequence of at least 576 continually alternating bits (10101010...). The preamble precedes a number of batch blocks. The transmission is terminated after the last batch.

Each batch comprises a synchronization codeword with a fixed 32-bit pattern followed by eight frames (numbered 0 to 7). Only complete batches are transmitted.

A frame consists of two codewords, each 32-bits long. A codeword is either an address or a message or an idle codeword. Idle codewords are transmitted to fill empty batches or to separate messages.

An address codeword is coded as shown in Fig.5. The upper 18-bits of the 21-bit digital user address (or RIC = Receiver Identification Code) are coded in the codeword itself (bits 2 to 19), which is protected against transmission errors by a number of CRC check bits (bits 22 to 31). Bit 32 is a simple overall even-parity bit. The lower three bits of the digital user address are coded in the number of the frame, in which the address codeword is transmitted. Two function bits (bits 20 and 21) allow distinguishing of four different calls to one user address.

In a message codeword 20-bits of any display information can be put into the message bits, which are protected again by additional check bits.

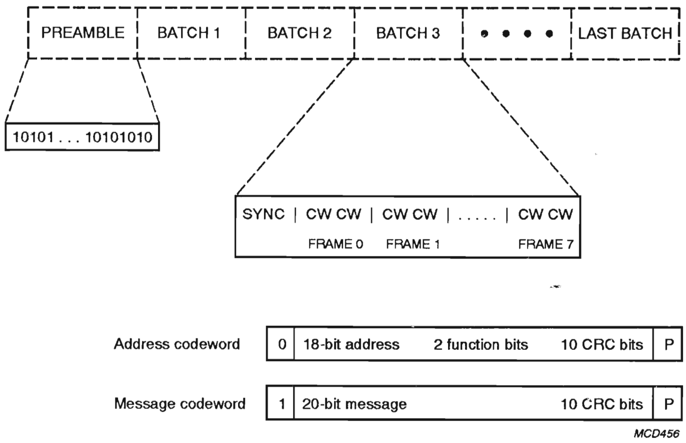


Fig.5 POCSAG code structure.

Modes and states of the decoder

The PCF5001 supports two basic operating modes:

- Alert-only pager
- Display pager mode.

Two further modes, the Programming mode and the Test mode, are implemented to program and verify the EEPROM contents and to support pager production and approval tests, respectively.

In Alert-only pager mode no external microcontroller is required, see Fig.21. A three position slider switch interface is provided to select the internal state of the decoder. The decoder performs regular scanning of the switch inputs to detect a status change. A push-button interface is provided on the SR input, which is used as input for user acknowledgment actions and status interrogation. Upon reception of valid calls, tone alert cadences are generated. A call storage is provided to store calls received while operating in Silent status and to recall cadences upon repeat mode operation. The voltage doubler and the frequency reference output are disabled in this mode.

In Display pager mode the PCF5001 operates as decoder and pager controller in combination with an external microcontroller, see Fig.22. The internal states of the decoder are determined by appropriate logic levels on the status inputs. A bus type interface structure is used to interface the decoder to the microcontroller. The decoder's on-chip voltage converter provides doubled supply voltage output to provide a higher supply voltage to the microcontroller and any additional hardware. The logic levels of the interface's input and output signals are level shifted to allow for direct coupling between microcontroller and the decoder. Upon detection of a valid call, address and message information are transferred to the external microcontroller using the serial microcontroller interface. In addition, appropriate call alert cadences are generated.

If the decoder is in one of the two operating modes, it is always in one of the following three internal states:

- OFF status. This is the power saving, inactive status of the PCF5001. The paging receiver is disabled, no decoding of input data takes place. However, the crystal oscillator is kept running to ensure that scanning of the status inputs/status switch is maintained to allow changing into one of the following two active states.
- ON status. This is the normal active status of the decoder. Incoming calls are compared with the user addresses stored in the internal EEPROM. Upon detection of valid calls, alert cadences and LED indication are generated and data is shifted out at the serial microcontroller interface.
- SILENT status. The Silent status is the same as the On status with the exception that valid calls no longer cause generation of call alert cadences. Instead, if programmed as alert-only pager, the decoder stores up to eight different calls and generates appropriate alert cadences after the decoder has been put back into the On status. However, special silent override calls will cause generation of alert cadences, if enabled.

The decoder operating status is selected as indicated in Table 1.

When programmed for alert-only pager a switch debounce period is applied to the status inputs. For status change and status interrogation in display pager mode, see Figs 6 and 7.

Table 1 Truth table for decoder operating status.

ON INPUT	SK INPUT	OPERATING STATUS
0	0	OFF
0	1	OFF (EEPROM transfer mode; note 1)
1	0	ON
1	1	SILENT

Note

1. The EEPROM transfer mode applies to display pager mode only.

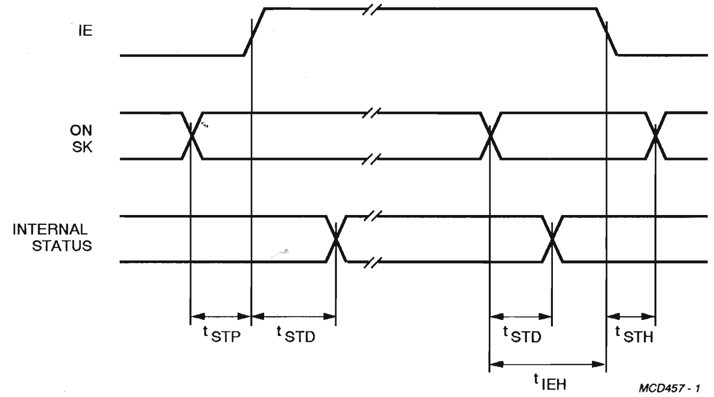


Fig.6 Status change in display pager mode.

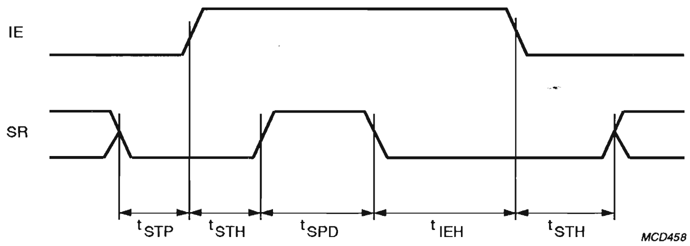


Fig.7 Status interrogation in display pager mode.

Decoding of the POCSAG data stream

The POCSAG coded input data stream is first noise filtered by a digital filter. From the filtered data a sampling clock synchronous to the data rate is derived. The PCF5001 supports 512 bits/s and 1200 bits/s data rates. This results in a 512 Hz or 1200 Hz sampling clock frequency, respectively. Synchronization on the POCSAG code structure is performed using the improved Philips ACCESS algorithm, which employs a state machine with six internal states.

A data rate of 2400 bits/s is possible if an external clock generator of 153.6 kHz is connected to X1. The minimum supply voltage is then −1.8 V.

The receiver enable output is activated a period equal to t_{RXON} before the input data is actually needed. The decoder has first to achieve bit and word synchronization before it can receive calls. The algorithm searches first for the preamble and then for synchronization codeword patterns. This is carried out for the duration of 3 batches in Power-on mode or 1 batch (=preamble duration) in Preamble Receive mode. Error correction algorithms are applied to the data before it is compared with preamble and synchronization codeword patterns. The synchronization process is terminated and thus Data Receive mode entered as soon as synchronization codewords are seen at the beginning of each batch.

The decoder handles loss of synchronization in three steps:

1. If the decoder fails to detect the synchronization pattern at the beginning of the current batch it continues data reception as normal. This Data Fail mode is signalled in the message output when an address codeword was received, as shown in Table 4.
2. If also at the beginning of the next batch no synchronization codeword can be detected, the algorithm assumes a small bit shift in the Fade Recovery mode and performs more synchronization codeword checks around the expected position for the following 15 batches. Call reception is suspended.
3. If it fails to re-synchronize in the Fade Recovery mode, the Carrier Off mode is selected, in which the decoder attempts to regain synchronization by bit-wise shifting its synchronization scan window. Using this technique re-synchronization is obtained within a continuous data stream of at least 18 batches without preamble detection.

In Data Receive mode, the input data stream is sampled at the synchronization codeword position and the programmed frame positions. The received codewords are error corrected and then, if address codewords, compared with the stored user addresses related to that frame. On detection of a valid call, the decoder performs the following three operations:

1. Set a store for call alert cadence generation according to the combination of the function bits in the accepted address codeword. The call alert cadence will not be generated before the call has been terminated.
2. Keep the receiver enable output (RE) active and receive subsequent message codewords, until any of the call termination criteria are fulfilled.
3. Trigger the serial message transfer by sending a start condition and transfer deformatted message codewords as attached to the address codeword via the serial microcontroller interface to an external microcontroller, followed by a stop condition.

Normally call termination is assumed, when a valid idle or address codeword is received. On reception of uncorrectable codewords, call termination takes place in accordance with conditions shown in Table 2.

Generation of output signals

The PCF5001 provides output indications for call alert, repeat mode alert, out of range alert, battery-low alert, status indication alert and start-up alert. Some of the alert functions may be freely configured by programming of SPF bits within the EEPROM. Table 3shows the outputs which are used for special output indications, if the decoder operates in ON status.

Remark: reception of special silent override calls causes the decoder to generate call alert indication via AL and AH even if it operates in SILENT status.

Table 2 Call termination on error.

SPF12	SPF13	CALL TERMINATION EVENT
0	X(1)	Any two consecutive codewords or the codeword directly following the address codeword uncorrectable.
1	0	Any single codeword uncorrectable.
1	1	Any two consecutive codewords uncorrectable.

Note

1. X = don't care.

Table 3 Output signals.

ALERT FUNCTION	OUTPUT ACTIVE(1)					
	AL	AH	OL	OM	OR	BL
Start-up	(yes)	–	yes	yes	–	–
Status indication	yes	–	–	–	–	–
Call reception	(yes)	(yes)	yes	SPF11	–	–
Repeat mode	(SPF16)	(SPF16)	SPF16	–	–	–
Out-of-range	–	–	SPF15	–	yes	–
Battery-low	(yes)	(yes)	–	–	–	yes
Alarm input	(yes)	(yes)	yes	–	–	–

Note

1. Entries in parenthesis are not valid, if the decoder operates in SILENT status.

Alerter

The PCF5001 provides the AL and AH outputs for acoustical LOW-level and HIGH-level signalling. LOW-level alerting is provided by the AL output only. For HIGH-level alerting both, AL and AH are active in anti-phase. The square-wave output signals produce tone alert cadences by means of a magnetic or piezo ceramic beeper. The alert frequency, 2048 Hz or 2731 Hz square-wave, is selected by programming of SPF31.

When valid calls are received while operating in ON status, the PCF5001 generates call alert cadences. The first four seconds are generated at LOW-level, a further twelve seconds are generated at HIGH-level. Alert tone generation and LED indication automatically terminate after sixteen seconds unless terminated by pulsing the status request and reset input (SR). Call alert generation is inhibited until completion of message codeword reception and the termination word is sent by the decoder. Call alert generation commences after an alert delay period, t_{ALD}, at the earliest, see Fig.8. Call alert deletion is possible during the alert delay period.

The call alert cadence is modulated according to the two function bits (FC) in the received address codeword, see Fig.9.

Valid calls received on RIC B or RIC D cause the alerter frequency to be warbled by means of an additional 16 Hz and 1 024 Hz signal (respective 1365 Hz for SPF31 = 1) as opposed to RIC A and RIC C where no alert frequency warble takes place. Thus, eight different call cadences are distinguishable.

On status interrogation by the status request and reset input (SR) the PCF5001 generates a status cadence at LOW-level, in accordance with the present internal decoder status (see Fig.10).

When detecting a battery-low condition the PCF5001 provides a battery-low indication. Operating in ON status causes generation of a battery-low alert at HIGH-level for sixteen seconds or until terminated by pulsing SR. Operating in SILENT status or repeat mode the battery-low alert is stored and inhibited until switching to ON status.

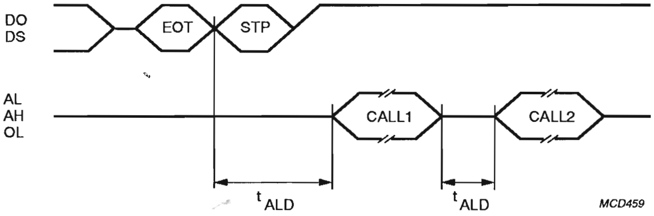


Fig.8 Call alert delay.

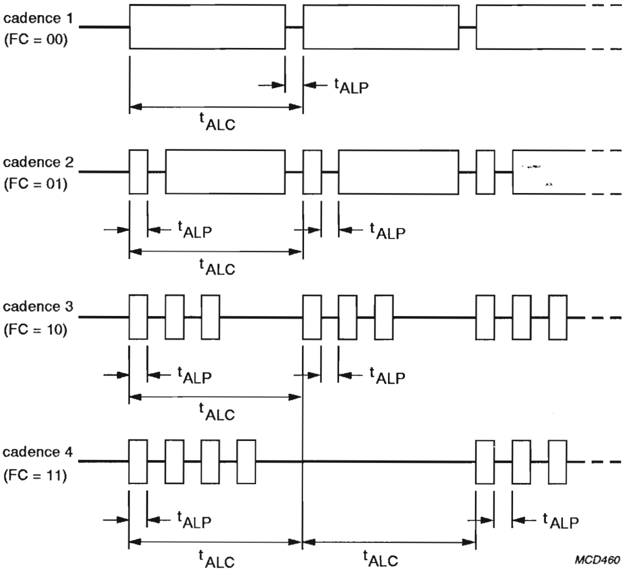


Fig.9 Call alert cadences.

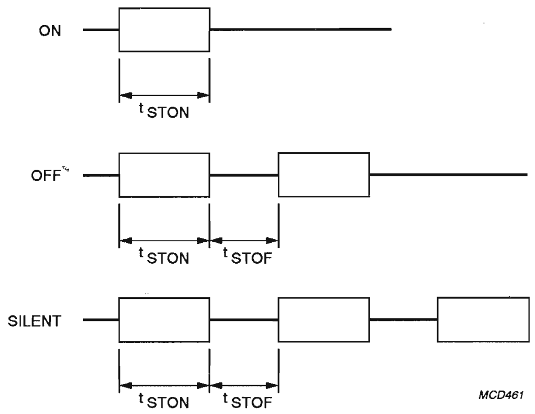


Fig.10 Status indication cadences.

Silent call storage and Repeat mode

When programmed for alert only pager the PCF5001 provides a call alert storage for storing of call alerts received during SILENT status or for call alerts which caused the decoder to enter Repeat mode. Call alert is not stored, when call indication is terminated by action of the status request and reset input (SR).

Allowing the call indication to time-out by expiration of a sixteen second alert operation causes the Repeat mode to be entered, while operating in ON status or SILENT status. Such call alerts are stored for later repeated call alert on interrogation by the user. When Repeat mode has been entered and the decoder operates in ON status, the repeat call store is interrogated by pulsing the status request and reset input (SR) or on switching to ON status if the decoder operates in SILENT status. When silent override calls are received, which entered the Repeat mode, interrogation of repeat call store operates as in decoder ON status. After interrogation of repeat call store and subsequent generation of all stored call alerts the call store is cleared and the Repeat mode is terminated.

When programmed by means of SPF16, a repeat alert cadence is generated periodically, whenever Repeat mode has been entered. Operating in ON status causes the repeat alert cadence to be generated at HIGH-level and warbled by means of an additional 16 Hz and 1 024 Hz signal (respective 1365 Hz for SPF31 = 1) as shown in Fig.11. The LED output indicates the same alert cadence and alert warble. In SILENT status only the LED output is active.

No call alert storage occurs when the decoder is programmed for display pager mode.

Duplicate Call Suppression

The PCF5001 provides a Duplicate Call Suppression with time-out facility, to identify duplicate call reception. When selected by programming of SPF14, the PCF5001 inhibits any duplicate call alert in alert-only pager mode. In display pager mode, duplicate call indication is achieved only via the serial microcontroller interface. A call is assumed to be duplicate if its address and function bit setting is equal to the latest received call, which initialized the call address and function bit reference. The Duplicate Call Suppression time-out is selectable by programming of SPF06 and SPF07.

LED indicator

The PCF5001 provides for visual signalling using a LED via output OL.

Call alert indication is provided by the LED with the same cadence and warble modulation as for the alerter outputs AL and AH. Call alert indication occurs in ON and SILENT status and automatically terminates after sixteen seconds time-out unless terminated by pulsing the status request and reset input (SR).

When detecting an out-of-range condition and enabled by programming of SPF15, the LED output provides an out-of-range indication as shown in Fig.12.

The LED output can be made to provide message data by programming SPF17. Alert signals are inhibited during message data transfer.

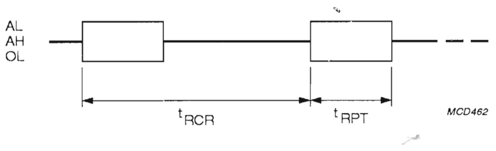


Fig.11 Repeat alert cadence.

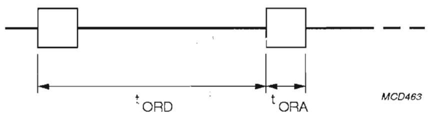


Fig.12 Out-of-range indication.

Vibrator output

The PCF5001 provides the OM output for activating a vibrator-type alerter for call alert indication. The vibrator output is enabled by programming of SPF11.

Calls received while operating in SILENT status cause activation of the vibrator output for the normal call alert cadence or until terminated by operation of the status request and reset input (SR). Silent override calls, calls received in decoder ON status and repeated call alerts are alerted normally by the AL and AH outputs.

Start-up alert

To indicate the establishment of operational condition whenever the decoder status has been changed from OFF to ON or SILENT status, the PCF5001 provides a start-up alert indication. Switching from OFF to ON status causes generation of a start-up alert cadence at LOW-level and on the LED output OL (see Fig.13).

When changing from OFF to SILENT status, the start-up alert will be indicated on the LED output and the vibrator output OM.

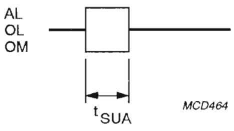


Fig.13 Start-up alert.

Serial communication interface

To transmit any call message data received to an external microcontroller for post-processing, a serial communication interface has been provided by a serial data output signal DO and a data strobe signal DS as shown in Fig.14.

Upon interrogation the PCF5001 is also able to transfer EEPROM contents via the serial communication interface, see Section “Read-back operation via Microcontroller Interface”.

Message data transfer

The transfer of message data via DO and DS is organized in 8-bit words providing additional start and stop conditions as shown in Fig.15.

On reception of a valid call address the PCF5001 generates a start condition and outputs an address word as shown in Fig.15 a.

The address word indicates call address, function bit setting and decoder flags as shown in Table 4.

Message codewords received and concatenated to a valid call address are transferred after completion of the address word. The message bits received in the message codewords are split into blocks and are converted to obtain the message words. The message words comprise an error flag to indicate message words, which are derived from uncorrectable message codewords as shown in Table 5.

Message data is output at a rate of 2048 bits/s with a minimum delay of 2 bits between consecutive message words.

Termination of call reception causes a termination word to be transferred, which indicates successful or unsuccessful call termination as shown in Table 6.

Serial data transfer for a received call ends with a stop condition as shown in Fig.15 c.

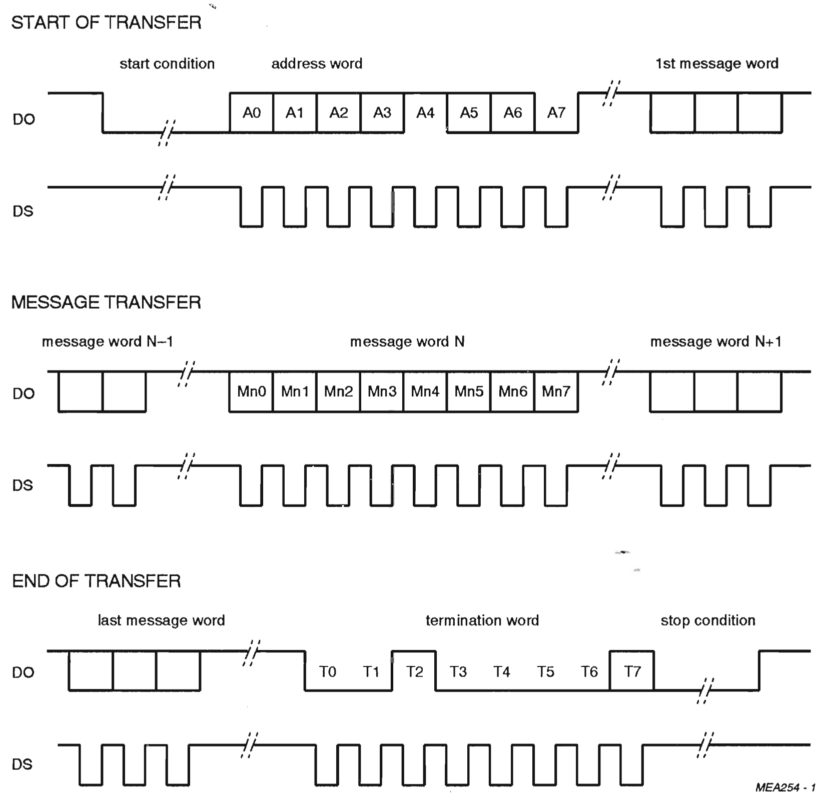
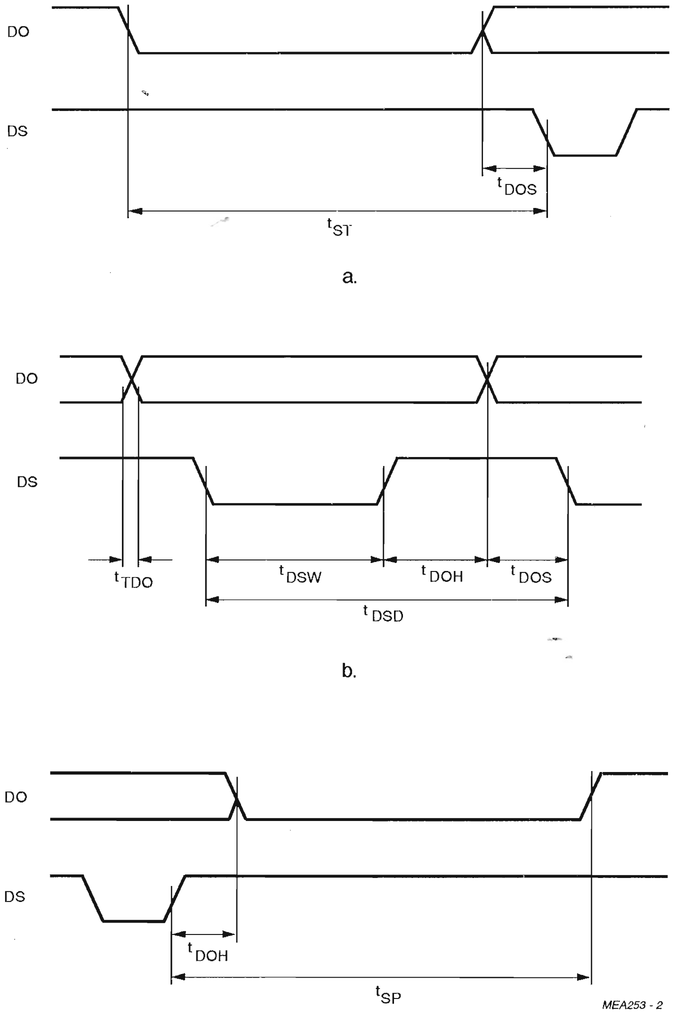


Fig.14 Call data transfer on the serial communication interface.



a. Start condition.
b. Data bit.
c. Stop condition.

Fig.15 Serial communication interface timing.

Call Data output on LED

When enabled by programming of SPF17 = 1, message data will appear on the LED output OL. The data format and timing are equal to the signal on DO, except that the start/stop conditions are replaced with start/stop bits (respectively 1 and 0). The data format is shown in Fig.16. No alert signals will appear on OL during message data transfer. Consecutive message words have a minimum separation of 1 start bit and 1 stop bit.

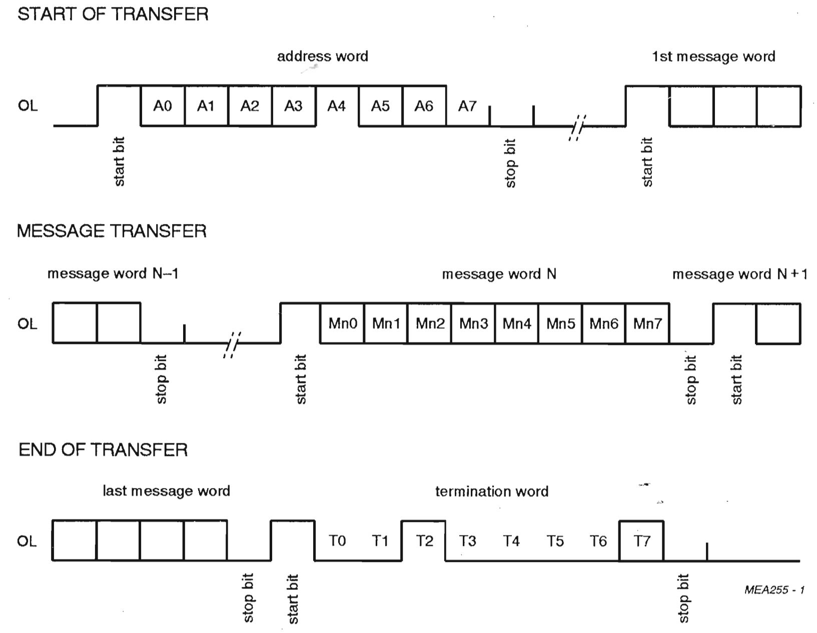


Fig.16 Call data transfer on the LED output.

Serial communication call data format

Table 4 Address word format.

FUNCTION CODE		CALL ADDRESS			BIT 4	SYNC STATUS	DUPLEX CALL	BIT 7
BIT 0 (LSB)	BIT 1 (MSB)	BIT 2	BIT 3	RIC		BIT 5	BIT 6	
Bit 21 of address codeword	bit 20 of address codeword	0	0	A	1	0 = Data Receive; 1 = Data fail	1 = Duplex Call time-out active	0
		0	1	B				
		1	0	C				
		1	1	D				

Table 5 Message word format.

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7(1)
LSB			message bits			MSB	error flag

Note

1. Bit 7 = 1, if message codeword could not be corrected.

Table 6 Termination word format.

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7(1)
0	0	1	0	0	0	0	error flag

Note

1. Bit 7 = 1, if call termination on error.

Data conversion

The PCF5001 automatically converts message codewords received in numeric or alphanumeric format into ASCII format. Depending on SPF13 and the function bit setting in the received address codeword a conversion takes place as shown in Table 7.

When a conversion from alphanumeric format to ASCII takes place, the received message codewords are split into message blocks, seven bits in length. After adding the error flag they are transferred as message words.

When a conversion from numeric format to ASCII takes place, the received message codewords are split into blocks, four bits in length. Each four bit block is converted to a seven bit block as shown in Table 8. After adding the error flag they are transferred as message words.

Table 7 Message data conversion.

SPF13	FUNCTION BITS		MESSAGE FORMAT
	BIT 20 (MSB)	BIT 21 (LSB)	
0	X(1)	X(1)	numeric
1	0	0	numeric
1	X(1)	1	alphanumeric
1	1	X(1)	alphanumeric

Note

1. X = don’t care.

Table 8 Numeric format to ASCII conversion.

4-BIT BLOCK				CHARACTER	7-BIT BLOCK						
LSB			MSB		LSB						MSB
0	0	0	0	‘0’	0	0	0	0	1	1	0
1	0	0	0	‘1’	1	0	0	0	1	1	0
0	1	0	0	‘2’	0	1	0	0	1	1	0
1	1	0	0	‘3’	1	1	0	0	1	1	0
0	0	1	0	‘4’	0	0	1	0	1	1	0
1	0	1	0	‘5’	1	0	1	0	1	1	0
0	1	1	0	‘6’	0	1	1	0	1	1	0
1	1	1	0	‘7’	1	1	1	0	1	1	0
0	0	0	1	‘8’	0	0	0	1	1	1	0
1	0	0	1	‘9’	1	0	0	1	1	1	0
0	1	0	1	‘*’	0	1	0	1	0	1	0
1	1	0	1	‘U’	1	0	1	0	1	0	1
0	0	1	1	‘ ’	0	0	0	0	0	1	0
1	0	1	1	‘–’	1	0	1	1	0	1	0
0	1	1	1	‘]’	1	0	1	1	1	0	1
1	1	1	1	‘[’	1	1	0	1	1	0	0

Memory Organization

The PCF5001 POCSAG decoder contains non-volatile EEPROM memory to store four user addresses, two frame numbers and specially programmed function bits (SPF01 to SPF32) for decoder application configuration. The EEPROM is organized as three arrays of 38 bits each as shown in Fig.17.

A user address (or RIC) in POCSAG code comprises of 21 bits, but the three least significant bits are coded in the frame number and therefore not explicitly transmitted. In the PCF5001, addresses A/B and C/D must share the same frame number: addresses A and B reside in frame FR1 (FR10, FR11 and FR12), addresses C and D reside in frame FR2 (FR20, FR21 and FR22). Figure 18 shows an example of decimal address to EEPROM content conversion. Each address must be explicitly enabled by resetting of the associated enable bit.

EEPROM ARRAY 1

BIT18	BIT17	BIT16	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00	$\overline{\text{ENA}}$

BIT37	BIT36	BIT35	BIT34	BIT33	BIT32	BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19
B17	B16	B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00	$\overline{\text{ENB}}$

EEPROM ARRAY 2

BIT18	BIT17	BIT16	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
C17	C16	C15	C14	C13	C12	C11	C10	C09	C08	C07	C06	C05	C04	C03	C02	C01	C00	$\overline{\text{ENC}}$

BIT37	BIT36	BIT35	BIT34	BIT33	BIT32	BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19
D17	D16	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	$\overline{\text{END}}$

EEPROM ARRAY 3

BIT18	BIT17	BIT16	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SPF13	SPF12	SPF11	SPF10	SPF09	SPF08	SPF07	SPF06	SPF05	SPF04	SPF03	SPF02	SPF01	FR20	FR21	FR22	FR10	FR11	FR12

BIT37	BIT36	BIT35	BIT34	BIT33	BIT32	BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19
SPF32	SPF31	SPF30	SPF29	SPF28	SPF27	SPF26	SPF25	SPF24	SPF23	SPF22	SPF21	SPF20	SPF19	SPF18	SPF17	SPF16	SPF15	SPF14

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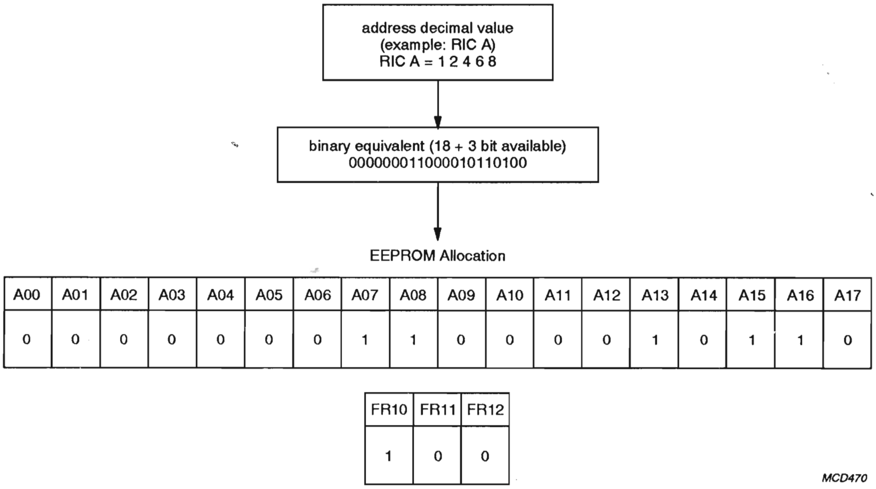
A00 represents the MSB of RIC A, B00 is the MSB of RIC C, etc.
FR10 represents the MSB of Frame 1 (valid for RICs A and B), FR20 is the MSB of Frame 2 (RICs C and D).

Fig.17 EEPROM memory organization.



A00	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16	A17
0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	1	0

FR10	FR11	FR12
1	0	0

A00 is the MSB of RIC A, FR10 is the MSB of Frame 1.

Fig.18 Decimal address to memory contents conversion example.

Description of the Special Programmed Function (SPF) bits

The following features can be selected by appropriate programming of the special programmed function bits as shown in Table 9.

Table 9 Special Programmed Function (SPF) bits.

SPF	BIT	FUNCTION
SPF01	0	Alert-only mode.
	1	Display pager mode.
SPF02	0	512 bits/s data rate.
	1	1200 bits/s data rate, possible with 76.8 kHz crystal only.
SPF03	0	32768 Hz crystal configuration.
	1	76800 Hz crystal configuration.
SPF04, SPF05		Receiver establishment time (depending on data rate).
	00	7.8 ms/512 bits/s; 53.3 ms/1200 bits/s.
	01	15.6 ms/512 bits/s; 6.7 ms/1200 bits/s.
	10	31.3 ms/512 bits/s; 13.3 ms/1200 bits/s.
	11	62.5 ms/512 bits/s; 26.7 ms/1200 bits/s.

SPF	BIT	FUNCTION
SPF06, SPF07		Duplicate call suppression time-out and out-of-range hold-off time-out.
	00	30 s.
	01	60 s.
	10	120 s.
	11	240 s.
SPF08	0	Voltage converter disabled, if SPF01 = 1 (Display pager mode).
	1	Voltage converter enabled, if SPF01 = 1 (Display pager mode).
SPF09	0	Silent override on address C disabled.
	1	Silent override on address C enabled.
SPF10	0	Silent override on address D disabled.
	1	Silent override on address D enabled.
SPF11	0	Vibrator output disabled.
	1	Vibrator output enabled.
SPF12	0	Call termination criteria combination method (note 1).
	1	Call termination criteria defined by SPF13.
SPF13	0	Numeric data deformatting, call termination on first uncorrectable codeword.
	1	Numeric data deformatting on function code 00 only, call termination on two uncorrectable codewords.
SPF14	0	Duplicate call suppression disabled.
	1	Duplicate call suppression enabled.
SPF15	0	Out of range indication at OL output disabled, hold-off period is zero regardless of SPF06 and SPF07 setting.
	1	Out of range indication at OL output enabled, hold-off period is according to SPF06 and SPF07 setting.
SPF16	0	Repeat alert disabled.
	1	Repeat alert enabled.
SPF17	0	Call data output on OL disabled.
	1	Call data output on OL enabled.
SPF18	–	Spare.
SPF19	–	Program always 0.
SPF20 to SPF30	–	Spares.
SPF31	0	Alerter frequency 2048 Hz.
	1	Alerter frequency 2731 Hz.
SPF32	0	Frequency reference output 16384 Hz if SPF01 = 1 (Display pager mode).
	1	Frequency reference output 32768 Hz if SPF01 = 1 (Display pager mode).

Note

1. Call termination on:

   First codeword immediately following address codeword uncorrectable.

   Two consecutive codewords uncorrectable.

EEPROM Write operation

The program mode is entered in OFF status by setting the PD input LOW and the PS input HIGH at any time. The program mode is left and normal operation resumed by either removing the power supply or setting the PD input HIGH after the 38th data bit while continuing to clock the PS input. The three EEPROM arrays can be programmed in any order. Selection of array is made during the second and third pulse on the PS input. The program mode has to be left after programming of each array.

After entering the program mode, keeping input PD LOW during the first pulse on PS selects Memory Write operation. After selection of the current array an erase cycle of duration t_{PEW} has to be carried out, during which the supply voltage at V_{SS} input must be at least V_{PG}. Program data for the selected array is entered bit by bit using PD as data input and the rising edge on PS as data strobe pulse. See Fig.19 for timing during an EEPROM write operation.

After the last bit a special write cycle of duration t_{PEW} has to be carried out again, during which the supply voltage at V_{SS} input must be V_{PG}. During conditions when the supply voltage is increased to V_{PG} the maximum DC ratings at V_{ref} must not be exceeded. When the on-chip voltage converter is enabled a voltage regulator diode or a damping resistor of sufficiently low impedance has to be connected between V_{ref} and V_{SS} to limit the voltage level at V_{ref} during program operation.

EEPROM Read operation

After entrance to the program mode, keeping input PD HIGH during the first pulse on PS selects Memory Read operation. After selection of the current array the programmed data is output bit-by-bit using PD as data output. A positive edge on PS input switches to the next bit. See Fig.19 for timing during an EEPROM read operation.

Read-back operation via Microcontroller Interface

In display pager mode, the PCF5001 is capable of delivering the EEPROM contents to an external microcontroller using the serial interface outputs DO and DS. The EEPROM data transfer mode is selected by applying a LOW to input ON and a HIGH to input SK while pulsing the SR input, and the interface is enabled (IE is HIGH). The data transfer is triggered by the falling edge on input SR. The transfer is organized as 15-byte transfers. The contents of each array are extended to 40 bits by trailing zeros. The EEPROM data transfer starts with array 1, bit 0. A valid data bit at DO is indicated by a LOW-level on DS as shown in Fig.20.

During EEPROM Read-back operation, the PCF5001 configuration and the outputs FL, OL are undefined. After completion of the Read-Back operation, the PCF5001 will re-enter the programmed configuration.

Voltage converter

The PCF5001 contains a switched capacitor-type on-chip voltage converter, which can provide doubled supply voltage to the external microcontroller and display control devices. The microcontroller interface signals are level shifted accordingly.

A capacitor of 100 nF (C_S) must be connected between pins CP and CN while a load capacitor of 10 μF is connected to V_{ref} as shown in Fig.22. The voltage converter operates in display pager mode only, when enabled by programming SPF08 (see Table 9).

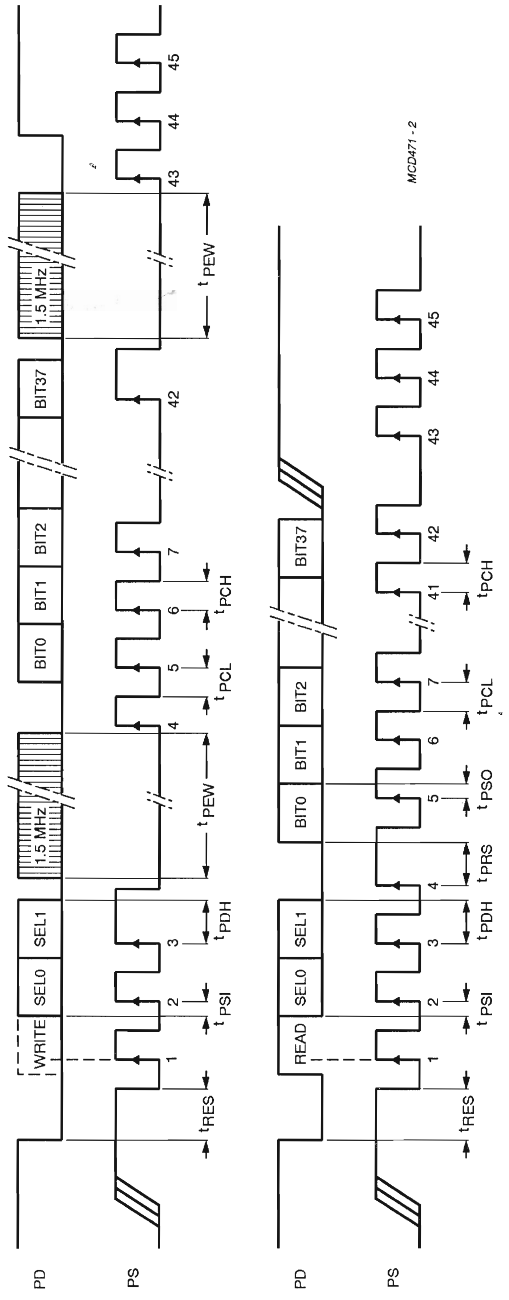


Fig.19 EEPROM read/write timing.

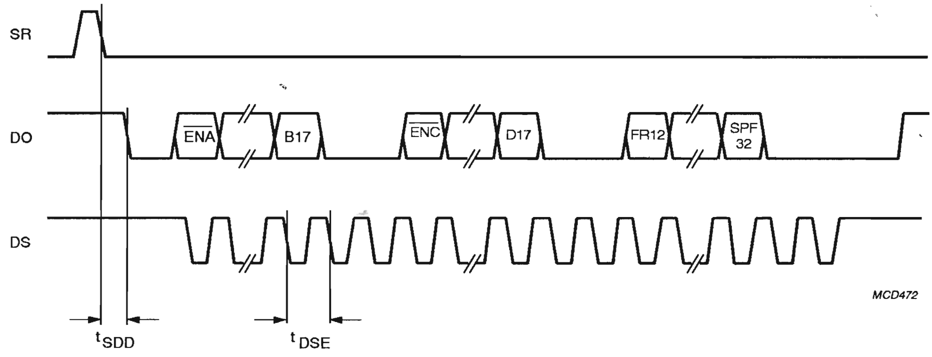


Fig.20 EEPROM data transfer to microcontroller timing.

Test modes of the decoder

The decoder supports two test modes, which are intended for use during pager production and type approval tests.

BOARD TEST MODE

Board test mode is selected by setting the PD input LOW at any time. In this test mode the following features are provided:

1. Receiver enable output is set constantly HIGH.
2. Output AL is activated by a LOW-level on ON input.
3. Output AH is activated by a HIGH-level on SR input.
4. Outputs OL and OM are activated by a HIGH-level on SK input.

Exit from board test mode is achieved by setting input PD HIGH.

PAGER TEST MODE (TYPE APPROVAL MODE)

Pager test mode is entered by reception of a valid call while board test mode is active, see above. In pager test mode:

1. Call alert cadences are terminated after 2 seconds.
2. Duplicate call suppression is disabled.

Exit from pager test mode is achieved by disconnecting the power supply from the decoder.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{SS}	supply voltage	note 1	+0.5	−8.0	V
V_{PG}	programming supply voltage		−5.5	–	V
V_I	input voltage on pins FL, DS, DO, OR, BL, AI, ON, SK, SR and IE		+0.8	V_{ref} − 0.8	V
V_I	input voltage on any other pin		+0.8	V_{SS} − 0.8	V
P_{tot}	total power dissipation		–	250	mW
P_O	power dissipation per output		–	100	mW
I_I	maximum input current (any input)		–	10	mA
$I_{O(max)}$	maximum output current				
	any output except AL		–	20	mA
	output AL		–	70	mA
T_{stg}	storage temperature		−55	+125	°C
T_{amb}	operating ambient temperature		−40	+85	°C

Note

1. Input V_{DD} is referred to as common, 0 V.

DC CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = −2.7 V; V_{ref} = 2.7 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Alert-only (SPF01 = 0).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{SS}	supply voltage		−1.5	−2.7	−6.0	V
I_{SS}	supply current	note 1	–	−60	−100	μA
V_{PG}	programming supply voltage	note 2	−4.5	−5.0	−5.5	V
I_{PG}	programming supply current		–	−500	–	μA
Inputs						
V_{IL1}	LOW level input voltage PD, PS, DI, BS, TS, TT and X1		0.7 V_{SS}	–	–	V
V_{IL2}	LOW level input voltage Ai, ON, SR, SK and IE		0.7V_{ref}	–	–	V
V_{IH1}	HIGH level input voltage PD, PS, DI, BS, TS, TT and X1		–	–	0.3V_{SS}	V
V_{IH2}	HIGH level input voltage AI, ON, SR, SK and IE		–	–	0.3V_{ref}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_I	input current					
	BS, PS, TS and TT	$V_I = V_{DD}$	7.0	–	20.0	μA
	PD	$V_I = V_{SS}$	–9.0	–	–24.0	μA
	DI	$V_I = V_{DD}$; RE = 0	7.0	–	20.0	μA
	DI	$V_I = V_{DD}$; RE = 1	0	–	0.5	μA
	ON and SK	$V_I = V_{SS}$	–0.5	–0.8	–1.1	μA
	AI and SR	$V_I = V_{DD}$	7.0	–	20.0	μA
C_I	input capacitance BS, DI, PD, PS, TS, TT, AI, ON, SR, SK, IE and X1		2	–	–	pF
Outputs						
I_{OL}	LOW level output current					
	OL, OM and AH	V_{OL} = –1.35 V	100	–	–	μA
	DO, DS, BL, FL and OR	V_{OL} = –1.35 V	100	–	–	μA
	AL	V_{OL} = –1.5 V	17.5	–	–	mA
	RE	V_{OL} = 2.2 V	200	–	–	μA
I_{OH}	HIGH level output current					
	OL, OM and AH	V_{OH} = –1.35 V	–0.8	–	–1.8	mA
	DO, DS, BL, FL and OR	V_{OH} = –1.35 V	–100	–	–	μA
	AL	AL high-impedance	–	–	–0.2	μA
	RE	V_{OH} = –0.5 V	–1.0	–	–	mA
Oscillator						
C_{XO}	output capacitance X2		–	40	–	pF
g_m	oscillator transconductance	V_{SS} = –1.5 V	15	29	43	μS
		V_{SS} = –6.0 V	25	39	55	μS
V_{PU}	power-up reset threshold voltage		–	–1.2	–	V

Notes

1. All inputs = V_{SS}; voltage converter off; all outputs open-circuit.
2. See Section “EEPROM Write operation” and Chapter “Limiting values” for limitations of V_{ref} when programming while the voltage converter is enabled.

DC CHARACTERISTICS (WITH VOLTAGE CONVERTER)

V_{DD} = 0 V; V_{SS} = –3.0 V; V_{ref} = –6.0 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Display Pager (SPF01 = 1).
Voltage converter enabled (SPF08 = 1); C_s = 100 nF.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{SS}	supply voltage		–1.5	–	–3.0	V
Voltage converter						
V_{ref0}	output voltage; no load	V_{SS} = –3.0 V	–5.8	–	–6.0	V
V_{ref}	output voltage	V_{SS} = –2.0 V; I_{ref} = 250 μA	–3.0	–3.5	–	V
I_{ref}	output current	V_{SS} = –2.0 V; V_{ref} = –2.7 V	400	600	–	μA
		V_{SS} = –3.0 V; V_{ref} = –4.5 V	600	900	–	μA
Inputs						
I_I	input current					
	AI, ON, SR and SK	V_I = V_{ref}	–	0	–0.5	μA
	ON and SK	V_I = V_{DD}	–	0	±0.5	μA
	SR	V_I = V_{DD}; V_{ref} = –6.0 V	–	17	–	μA

AC CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = –2.7 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 32768 or 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Display or Alert-only Pager (SPF01 = 1 or 0).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Alert frequency						
f_{AL}	alert frequency	SPF31 = 0	–	2048	–	Hz
f_{AWH}	high alert warble frequency		–	1024	–	Hz
f_{AWL}	low alert warble frequency		–	16	–	Hz
f_{AL}	alert frequency	SPF31 = 1	–	2731	–	Hz
f_{AWH}	high alert warble frequency		–	1365	–	Hz
f_{AWL}	low alert warble frequency		–	16	–	Hz
f_{FL}	frequency reference FL	SPF32 = 0	–	16384	–	Hz
		SPF32 = 1	–	32768	–	Hz
Call alert duration						
t_{ALT}	time-out period		–	16	–	s
t_{ALL}	alert time LOW (AL output only)		–	4	–	s
t_{ALH}	alert time HIGH (AH and AL outputs)		–	12	–	s

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{ALC}	call alert cycle time	see Fig.9	–	1	–	s
t_{ALP}	call alert pulse duration	see Fig.9	–	125	–	ms
t_{ALD}	call alert hold off period	see Fig.8	52	–	–	ms
t_{RPT}	repeat alert duration	see Fig.11	–	–	4	s
t_{RCR}	repeat alert recurrence time	see Fig.11	–	–	15	s
t_{RCP}	repeat alert cycle time		–	–	500	ms
t_{RPD}	repeat alert pulse duration		–	–	250	ms
t_{STON}	status alert time	see Fig.10	–	–	62.5	ms
t_{STOF}	status alert delay	see Fig.10	–	–	62.5	ms
t_{SUA}	start-up alert time	SPF02 = 0; see Fig.13	–	–	500	ms
		SPF02 = 1; see Fig.13	–	–	453	ms
t_{ORA}	out-of-range alert pulse width	see Fig.12	–	–	62.5	ms
t_{ORD}	out-of-range alert time	see Fig.12	–	–	2	s
t_{BLAL}	battery LOW-level alert time		–	–	16	s
Receiver control						
t_{RXT}	RE transition time	C_L = 5 pF	–	–	100	ns
t_{RXON}	RE establishment time	SPF04 = 0; SPF05 = 1	–	7.8	62.5	ms
Data output						
f_{DO}	data output rate		–	2048	–	bits/s
t_{DSD}	strobe period call data	see Fig.15	480	–	495	µs
t_{DSE}	strobe period EEPROM data	see Fig.20	200	488	1150	µs
t_{DSW}	data strobe pulse width	see Fig.15	230	–	250	µs
t_{TDO}	data output transition time	C_L = 10 pF; see Fig.15	–	–	100	ns
t_{DOS}	data output set-up time	see Fig.15	–	–	135	µs
t_{DOH}	data output hold time	see Fig.15	115	–	–	µs
t_{BYD}	consecutive byte delay		1210	–	1225	µs
t_{CWD}	inter-codeword delay	1200 bits/s numeric message	3420	–	–	µs
t_{ST}	start condition set-up time	see Fig.15	4750	–	–	µs
t_{SP}	stop condition set-up time	see Fig.15	595	–	615	µs
t_{STL}	start bit period OL output		480	–	495	µs
t_{SPL}	stop bit period OL output		480	488	495	µs
t_{SDD}	SPF output delay	see Fig.20	1	–	10	ms

TIMING CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = –2.7 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 32768 or 76800 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Display or Alert-only Pager (SPF01 = 1 or 0).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating frequency dependent						
f_{osc}	oscillator frequency	SPF03 = 0	–	32768	–	Hz
		SPF03 = 1	–	76800	–	Hz
t_{TDI}	data input transition time		–	–	100	μs
t_{DI1}	data input logic 1		–	∞	–	
t_{DI0}	data input logic 0		–	∞	–	
f_{DI}	data input rate	SPF02 = 0	–	512	–	bits/s
t_{BIT}	bit period		–	1.9531	–	ms
t_{CW}	codeword duration		–	62.5	–	ms
t_{PA}	preamble duration		1125	–	–	ms
t_{BAT}	batch duration		–	1062.5	–	ms
f_{DI}	data input rate	SPF02 = 1; f_{osc} = 76800 Hz	–	1200	–	bits/s
t_{BIT}	bit period		–	833.3	–	ms
t_{CW}	codeword duration		–	26.7	–	ms
t_{PA}	preamble duration		480	–	–	ms
t_{BAT}	batch duration		–	453.3	–	ms
Alert only mode (SPF01 = 0)						
t_{SDB}	switch debounce period		–	62.5	–	ms
Display pager mode (SPF01 = 1); see Figs 6 and 7						
t_{STP}	status set-up time	f_{osc} = 32768 Hz	35	–	–	μs
t_{STD}	status change delay		–	–	35	μs
t_{IEH}	interface enable hold time		35	–	–	μs
t_{STH}	status hold time		35	–	–	μs
t_{SPD}	status pulse duration		35	–	–	μs
t_{STP}	status set-up time	f_{osc} = 76800 Hz	15	–	–	μs
t_{STD}	status change delay		–	–	15	μs
t_{IEH}	interface enable hold time		15	–	–	μs
t_{STH}	status hold time		15	–	–	μs
t_{SPD}	status pulse duration		15	–	–	μs

PROGRAMMING CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = V_{PG} = −5.0 V; (see notes 1, 2 and 3); V_{ref} = V_{SS}; pins 2 and 3 open-circuit; T_{amb} = 25 °C.
Quartz crystal parameters: f = 32768 Hz; $R_{S(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder in OFF status.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Programming; see Fig.19						
t_{RES}	power-up reset pulse width	note 4	35	–	–	µs
t_{PEW}	erase/write time		10	–	–	ms
f_{EW}	erase/write frequency		1.0	1.5	2.0	MHz
t_{EW}	erase/write cycles		100	10000	–	–
t_{DR}	data retention time	T_{amb} = 85 °C	10	–	–	years
t_{PCH}	data clock HIGH time	note 4	65	–	–	µs
t_{PCL}	data clock LOW time	note 4	65	–	–	µs
t_{PRS}	read set-up time	note 4	–	–	35	µs
t_{PSI}	data set-up time on input	note 4	35	–	–	µs
t_{PSO}	data set-up time on output	note 4	–	–	35	µs
t_{PDH}	data hold time	note 4	35	–	–	µs

Notes

1. V_{SS} = V_{PG} only required during erase/write (t_{PEW} in Fig.19), otherwise $V_{SS(min)}$ = −1.5 V.
2. Maximum voltage for programming (V_{PG}) is −5.5 V.
3. See Section “EEPROM Write operation” and Chapter “Limiting values” for limitations of V_{ref} when programming while the voltage converter is enabled.
4. EEPROM programming is also possible at higher frequencies (76.8 kHz or 153.6 kHz). The timings shown then become proportionally smaller.

APPLICATION INFORMATION

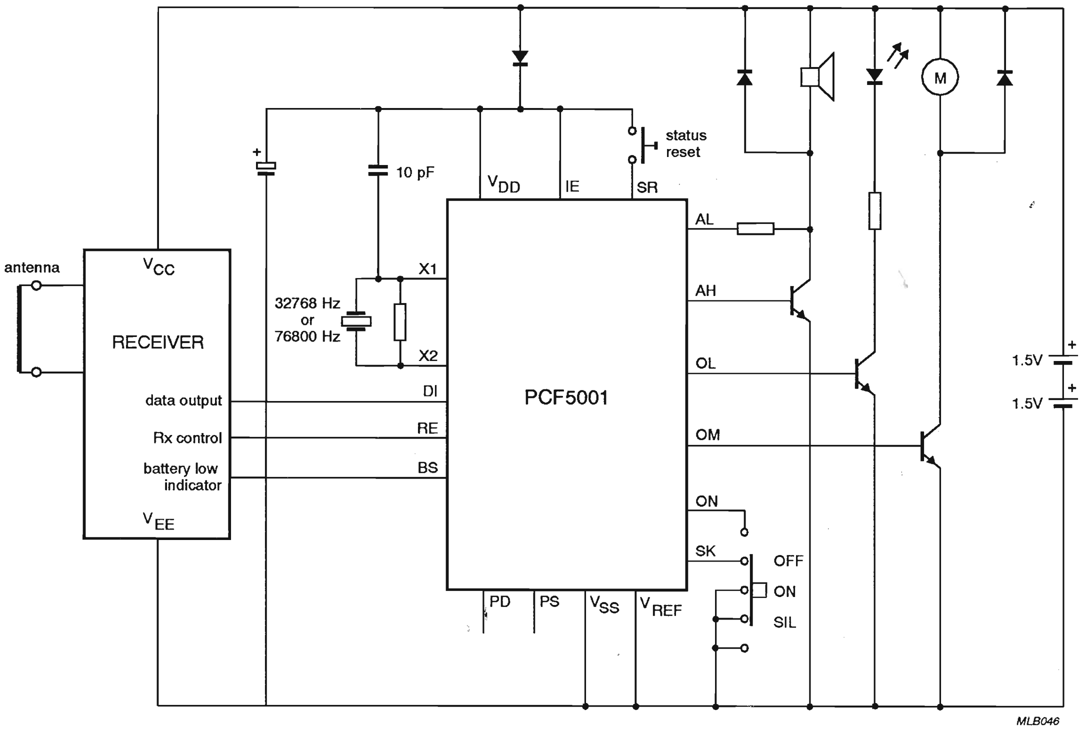


Fig.21 Alert-only pager application example.

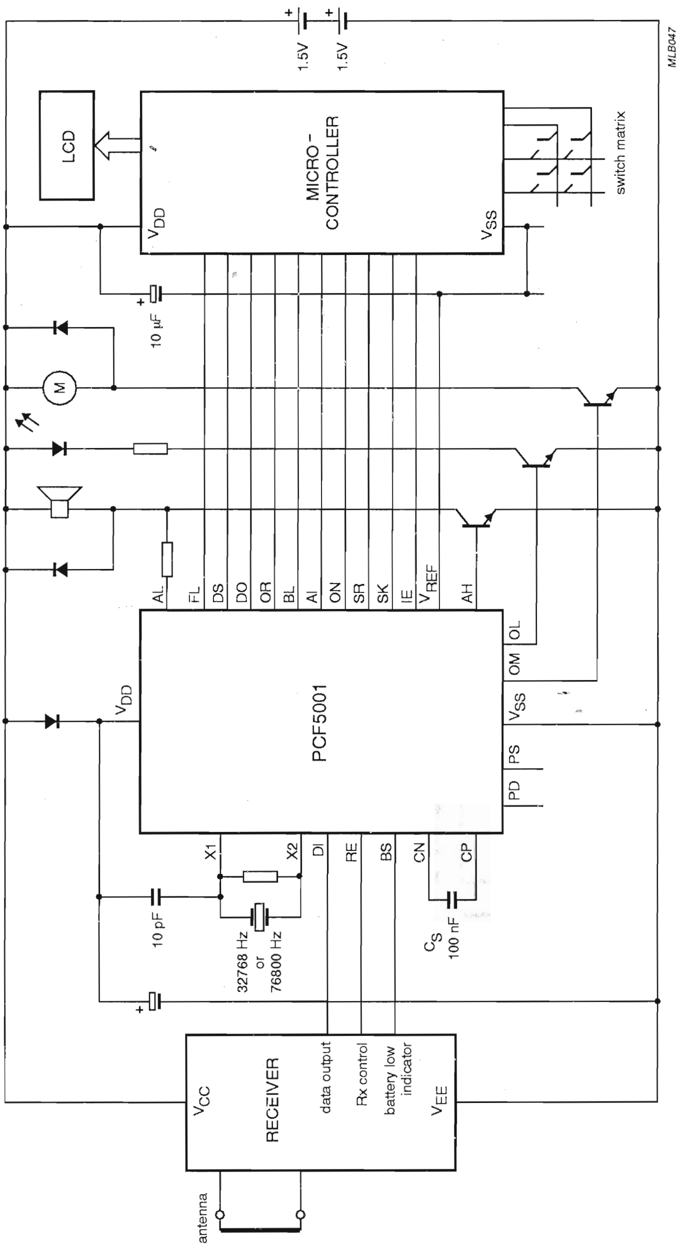
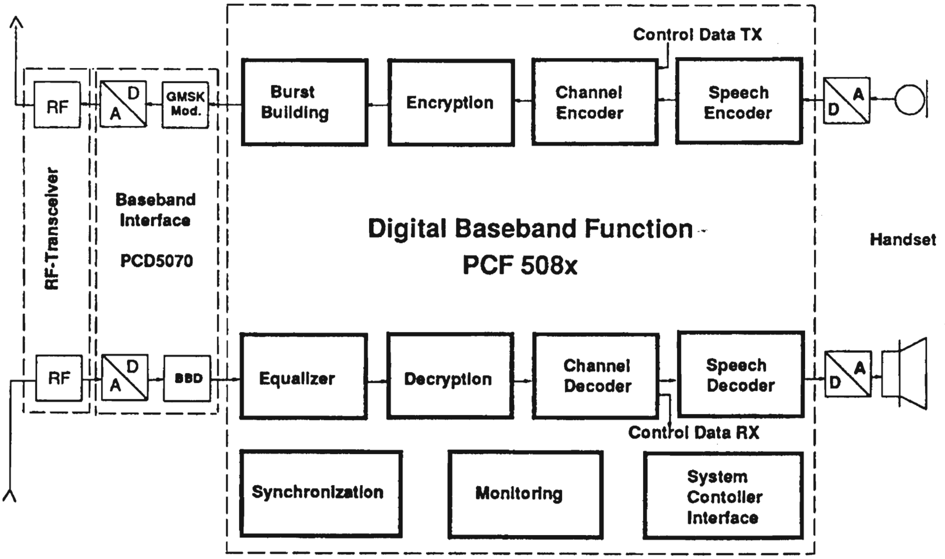


Fig.22 Display-pager application example.

GSM Baseband Signal processors

The PCF5081 and the PCF5082 are integral parts of the complete chip-set provided by Philips for the pan-European digital mobile cellular telephone system. The PCF5081 and PCF5082 are key elements for GSM, each performing all the baseband signal processing tasks. Because of their high-level of architectural modularity, these processors can easily be adapted to market requirements in respect to both hardware and software.

The PCF5081 (with ROM) is intended for use in GSM handsets, the PCF5082 (ROM-less) for implementation in the base station. These processors are also considered as the first devices of an entire product line introduced as PCF508x. This family provides powerful computational capabilities which supports the highly sophisticated baseband signal processing required by GSM.



Signal path in a GSM Mobile

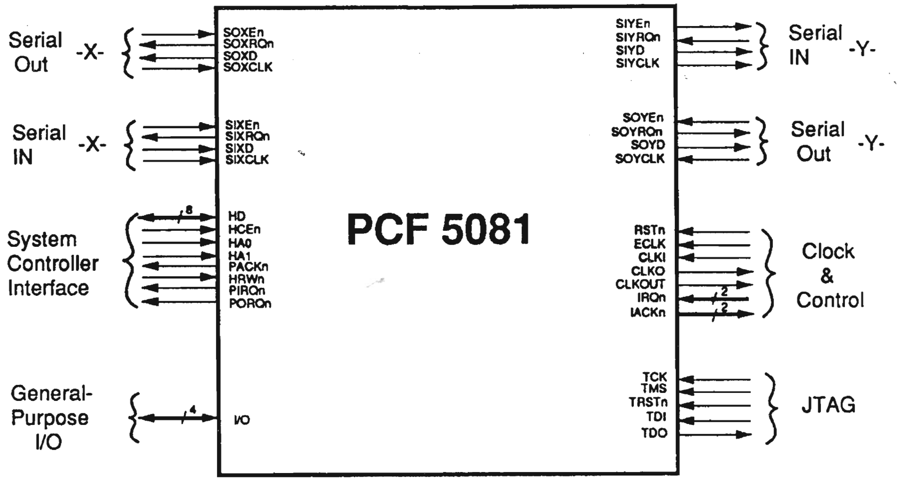
The different tasks performed in the baseband signal path of the GSM-system are carried out by means of software partitioned program modules in the signal processor. This implementation is supported by Application Specific Hardware (ASH) to speed up execution and overall performance.

This partitioning between software and hardware for the different processing tasks has been implemented as a trade-off between dedicated hardware and software to provide fast execution with an optimal level of flexibility.

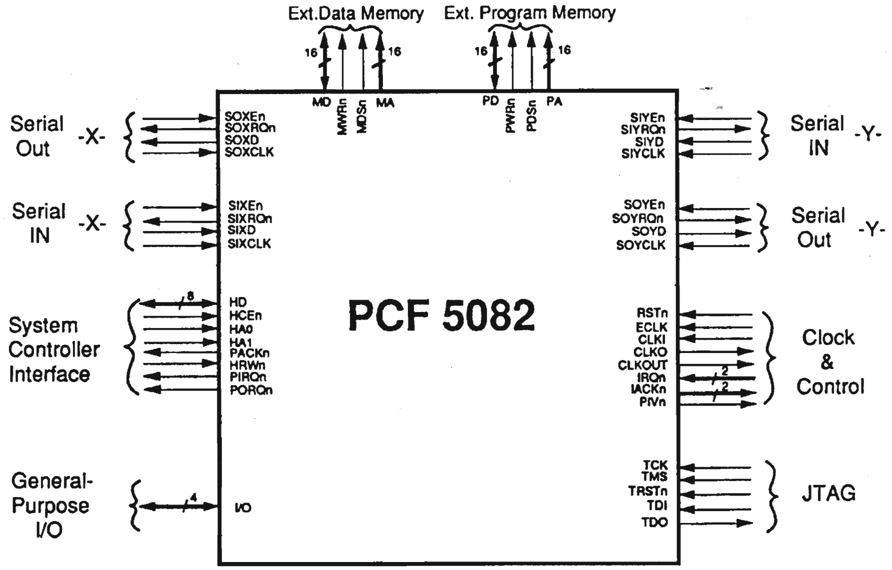
Main Features:

- ☐ **16-Bit fixed point double precision architecture**
- ☐ **40MHz master clock**
  20MHz internal clock (50ns instr.cycle)
- ☐ **Fully pre-programmed modules for GSM baseband tasks.***
- ☐ **Dedicated processor optimized for:**
  - **Equalization function**
  - **Channel Coder/Decoder**
  - **Encryption/Decryption**
- ☐ **Power-down mode with wake-up facility**
- ☐ **Several levels of interrupts**
- ☐ **Event counter**
- ☐ **Asynchronous serial I/O -X-**
- ☐ **Sophisticated serial I/O -Y- supporting both asynchronous and synchronous communication (i.e. GCI, PCM highway etc.)**
- ☐ **8-Bit parallel system controller interface supporting both request and acknowledge driven communication.**
- ☐ **Boundary scan facility**
- ☐ **Build-in self test (BIST)**
- ☐ **Self-Aligned-Contacts CMOS (SACMOS) technology with very high design density**
- ☐ **External memory interfaces for both data and program memory ****
- ☐ **Boot-strap facility* ***

*** on PCF5081 only**
**** on PCF5082 only**



Signal I/O of the PCF 5081



Signal I/O of the PCF 5082

Signal Description

Mnemonic	Type	Function
CLKI	I	Crystal or clock input. Input clock at twice the frequency of internal cycle.
CLKO	O	Crystal output
CLKOUT	O	Synchronization clock. Output clock at half of the frquency of CLKI.
ECLK	I	Event clock to count external events. The frequency of this input signal is limited to 1/4 of the CLKI if the duty cycle is 50%.
HA[1:0]	I	Host address bus. The address signals are used to select the source or destination of the data on the data bus HD. These signals must be stable before the enable signal HCEn is asserted.
PACKn	O	Output signal to acknowledge data on the data bus HD if the acknowledge mode is enabled. Acitve low.
HCEn	I	Global chip enable signal for the host interface. Active low.
HD[7:0]	B	Bidirectional host data bus, 8 bit wide. The high or low byte of the 16 bit I/O buffer registers are read or written via this port depending on the signals at the address bus HA[1:0]
PIRQn	O**	Data input request signal. Active low. The signal requests data for input if the request mod is enabled. It is driven low if the infput buffer register is empty.
PORQn	O**	Data output request signal. Active low. The signal requests for data to be read by the external device if the request mode is enabled. It is driven low if the output buffer register is full.
HWRn	I	Write signal. Active low. The signal controls the direction of the data transfer on the data bus HD [7:0]. When low, data are written by external device.
IACKn [2:1]	O*	External interrupt request acknowledge signals. Active low. The signals are set low if the related request is serviced. It is set high if the related flag is cleared.
IRQn[2:1]	I	External interrupt request signals. Active low and edge triggered. If low, the related interrupt is requested. It will be acknowledged if the related interrupt is enabled.
IO[4:1]	B***	General I/O pins. They have open drain outputs and a pull-up resistor. The states of these pins are reflected by four bits in a control register. The pulse width of an input signal has to be at least two internal processor cycles until a change will be frecognized in the control register.
RSTn	I	Reset signal, low active. A high-to-low transition causes entry into reset state. A low-to-high transition causes execution to begin at program memory location 0 or booting.

Mnemonic	Type	Function
SIXCLK	O*	Serial input clock port X. Asynchronous.
SIXD	I	Serial input data port X. Data are shifted into the input shift register X.
SIXEn	I	Serial input enable port X. Active low.
SIXRQn	O*	Serial input data request, port X. Handshake signal. Active low.
SOXCLK	I	Serial output clock port X. Asynchronous.
SOXD	O*	Serial output data port X. Data are shifted out of the ouputt shift register X.
SOXEn	I	Serial output enable port X. Active low.
SOXRQn	O*	Serial output data request, port X. Handshake signal, active low.
SIYCLK	I	Serial input clock port Y. Asynchronous clock.
SIYD	I	Serial input data port Y. Data are shifted into the input shift register Y.
SIYEn	I	Serial input enable port Y. Active low. Frame sync. signal in synchr. mode. Active high.
SIYRQn	O*	Serial input data request, port Y. Handshake signal, active low. Not used ir synchr. mode.
SOYCLK	I	Serial output clock port Y. Asynchronous.
SOYD	O***	Serial output data port Y. Data are shiftec out of the output shift register Y.
SOYEn	I	Serial output enable port Y. Active low. Serial output data read back for collision detection in synchr. mode.
SOYRQn	O*	Serial output data request, port Y. Handshake signal, active low. Not used ir synchr. mode.
TCK	I	JTAG signal. Test clock. Free running clock active rising edge.
TDI	I	JTAG signal. Test data input. Shifted in with the rising edge of TCK
TDO	O	JTAG signal. Test data output. Shifted ou with the falling edge of TCK.
TMS	I	JTAG signal. Test mode select.
TRSTn	I	JTAG signal. Test interface reset. Active low. When setting low, the TAP controller will be reset independently from the processor.

Signal Description

Mnemonic	Type	Function
MA[15:0] 1)	O*	Data address bus for addressing up to 64k x16 bits.
MD[15:0] 1)	B	Bidirectional 16 bit data bus connection to external data memory.
MDSn 1)	O*	Data strobe signal for external data memory. Active low.
MWRn 1)	O*	Write signal for external data memory. Active low. When low, data is written. When high, data is read.
1)	O*	Address bus for external program memory address up to 64k x 16 locations.
PD[15:0] 1)	B	Data bus for external program memory, 16 bit wide.
PDsn 1)	O*	Data strobe signal for external program memory. Active low.
PWRn 1)	O*	Write signal for external program memory. Active low. When low, data is written. When high, data is read.
PIVn 1)	O*	Output signal to support emulation. Active low.

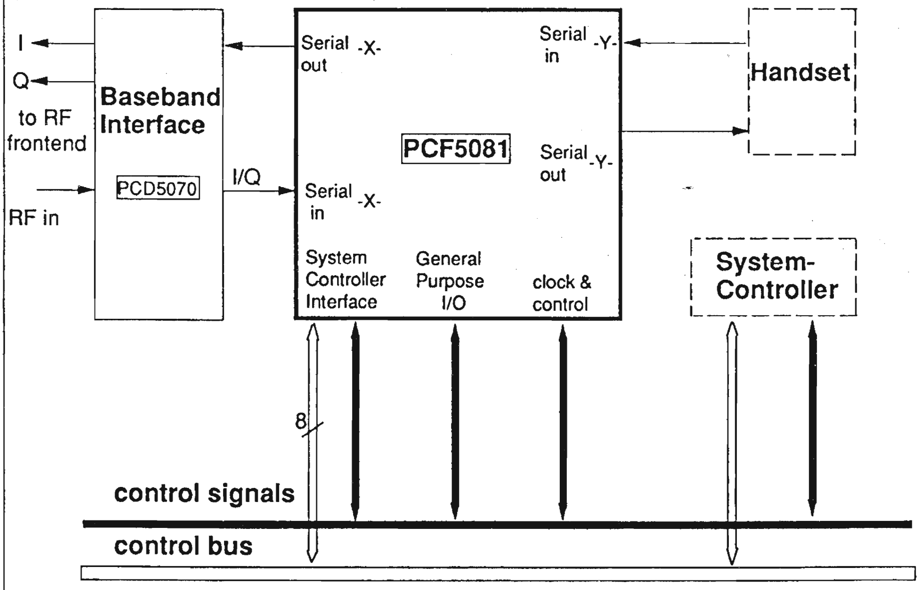
*: 3-state during	** : Open drain output.
O: Output signal	***: Open drain output and 3-state during reset.
I : Input signal	B : Bidirectional signal.
	1) : PCF5082 only.

Application of the PCF5081

This PCF5081 is designed to be used in the GSM mobile station. All the necessary baseband signal processing algorithms specified by the GSM-recommendations pertaining to the mobile station can be performed by means of this single chip.

The PCF5081 has on-chip memory (ROM) containing program modules for the different tasks implemented in firmware. A suitable amount of data-RAM/ROM is provided on-chip.

To allow flexible use of the different pre-programmed modules, the sequence of the baseband tasks is defined by the system controller by means of a circular tasks buffer. As soon as no task is left, the baseband processor enters a power-down mode to minimize current consumption.



Typical application of the PCD5081 in a GSM-Mobile Station

The main tasks to be performed by the baseband processor are the following:

- Equalization
- Channel encoder/decoder
- Speech encoder/decoder
- Encryption/Decryption
- Initial synchronization and monitoring of adjacent base station.

The architecture of the PCF5081 baseband processor was not designed for a single task within the baseband signal processing (eg. speech encoder/decoder), but rather to optimally accomplish all the necessary processing tasks. Special attention was placed on the equalization function where viterbi algorithm (MLSE receiver) and soft decision output code (4 bit coding) contribute to an optimal receiver algorithm in contribution with the channel decoder.

To be able to face up to the most severe conditions (hilly environment) a 6T algorithm is in preparation. Moreover, the equalization coefficients are continually updated during a burst to allow use of the mobile radio in vehicules travelling at very high speed.

The channel coder/decoder is capable of handling the speech Traffic Channel (TCH), the Fast and the Slow Associated Control Channel (FACCH and SACCH), the Random Access Channel (RACH) the Broadcast Control Channel (BCCH), the Paging Channel (PCH), the Access Grand Channel (AGCH), the synchronization Channel (SCH) and data transfer at all rates according to GSM Rec. 5.03.

The channel decoder is performed by viterbi algorithm based on soft decision equalizer output and by use of large path memory (up to 32 bits) for the MLSE algorithm.

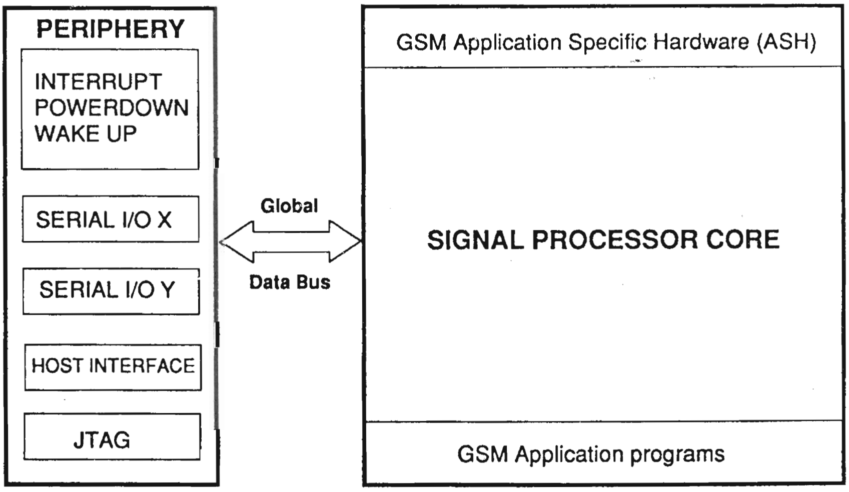
The speech encoder/decoder function includes voice activity detection, discontinous transmission as well as comfort noise insertion and generation.

The user-dataflow takes place via the serial interfaces X and Y. The X-interface looks in the direction of the frontend to the baseband interface (e.g. the Philips PCD5071) and the Y-interface is connected to the handset of the mobile.

The control-dataflow is transmitted via the system controller interface, the general purpose I/O pins, and other I/O available as part of the processor's periphery. The control data and signals are normally provided by the system controller of the mobile.

The architecture of the PCF5081 can be split into two major sections. The processor core consists of all the arithmetic units necessary to carry out the calculations as well as access memories containing data and program information. The application specific hardware is also part of the core. The periphery consists of all the necessary interfaces as well as the interrupt and powerdown/wake-up facilities.

Internal data between these two sections is exchanged via a global data bus.



Blockdiagram of the PCF5081

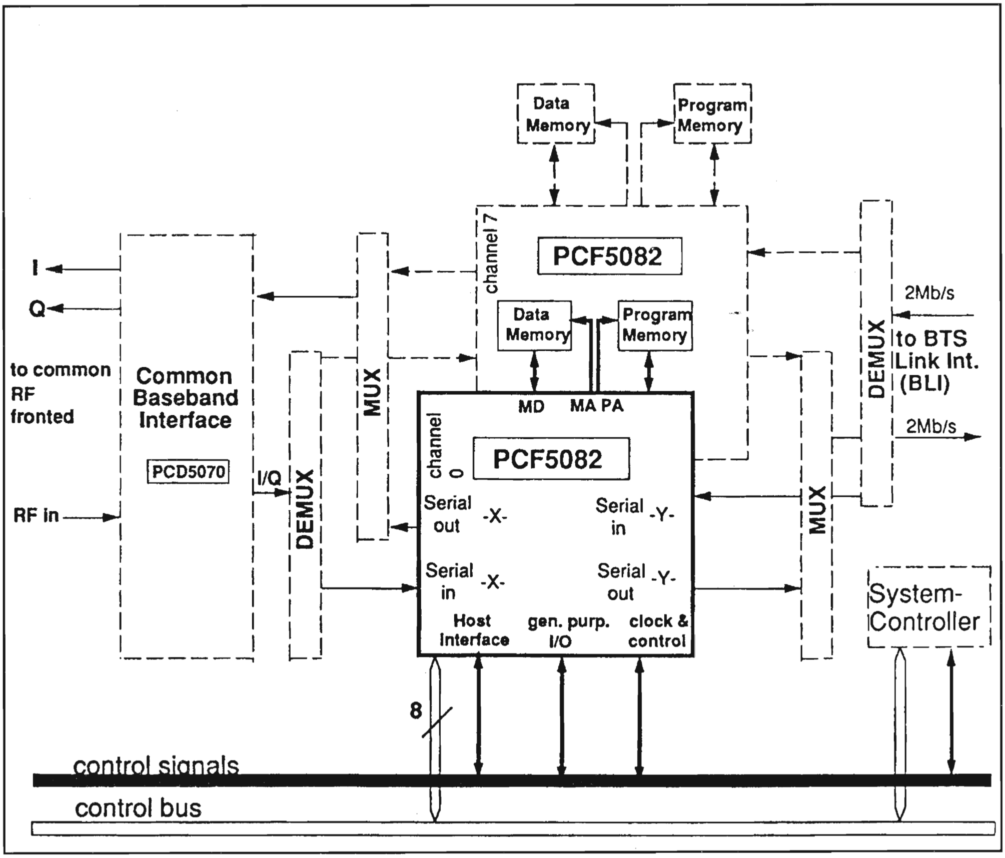
Application of the PCF5082

This version is targetted for use in GSM base station systems (BSS) as well as for real-time emulation purposes during software development and debugging.

ROM

As the baseband processing within a base station requires a certain degree of flexibility, the PCF5082 can externally address memory dedicated for the application program and user data.

The PCF5082 contains 1k x 16 bits or program-ROM used for Built-In Self Tests (BIST), boot-strap and emulation routines. External program memory (ROM/RAM) up to 63k x 16 bits can be connected to run application programs.



Possible application of the PCF5082 in a GSM-Base Taranceiver Station (BTS)

RAM

To keep the overall system costs low, 2k x 16 bits of on-chip data RAM is provided. This range can be extended by external devices (RAM/ROM) up to the maximum value of 64kx16 bits of data memory.

OTHERS

In the switching centre (MSC) the data streams of each of the eight channels are merged to a PCM-highway data-stream (2Mb/2) via a multiplexer (MUX) and vice versa via the BTS link interface (BLI). The serial interfaces Y of each of the processors are used for this data flow. In the frontend of the radio terminal (RT), each channel can be connected to a common baseband interface PCD5070 via a multiplexer (MUX) and a demultiplexer (DEMUX), respectively. The serial interfaces X of each of the processors are used for this data flow.
External memories containing user-data and application programs are connected. As in the PCF5081, the same interfaces are used for control-data and control-signal flow.

The architecture of both the PCF5081 and the PCF5082 can be split into two sections: processor core and the periphery. The PCF5082 processor core contains on-chip boot-strap facility, no user-program-memory and its periphery has additional memory interfaces to connect external memories for both user-data and application programs.

These are the main differences between both the PCF5081 and the PCF5082.

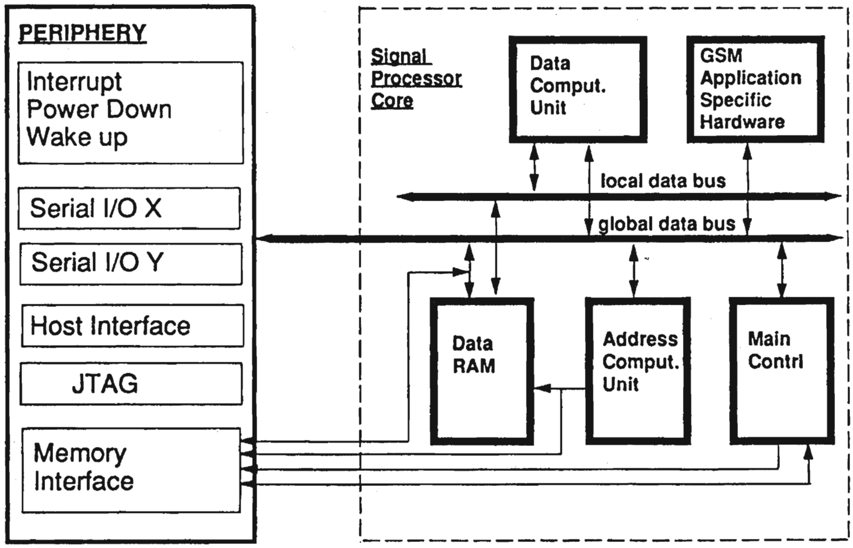
The boot-strap facility is an additional functionality of the PCF5082 allowing for convenient downloading of application programs to the external program memory (RAM) under the control of a host. Several sources for such a download can be selected by the user.

Due to the fact that application programs are stored or downloaded into external program memory, a large degree of flexibility is offered to the base station system designer.

Similar to the PCF5081, the PCF5082 contains application specific hardware to speed up the execution of the baseband signal processing algorithms.

There are several partitionings possible with respect to the different tasks which have to be performed. For instance, the baseband processing can be done by separating receiver and transmitter functions and using one PCF5082 for multiple time-slots (channels) within a TDMA-frame. Alternatively, the receiver and transmitter functions can be kept together and one PCF5082 used for processing both directions simultaneously.

In a typical application the PCF5082 is used for the baseband signal processing in a radio-terminal (RT) of a GSM Base Transceiver Station (BTS). Since the RT must serve all eight time-slots (channels) within a TDMA-frame, eight separate baseband signal-paths have to be used in parallel.



Block diagram of the PCF5082

I/O-Port Descriptions

Parallel Host Interface

The parallel port provides an 8-bit bidirectional link to a host or other external device. It is designed as a passive port, i.e. the external device has to be active in order to access the registers of the port. The communication takes place via 16-bit wide I/O registers with the aid of several control signals. The upper and lower bytes of these registers can be accessed independently.

Two flags are generated (input register full, output register empty) supporting efficient I/O-handling. Whether it is the high byte or the low byte which generates the flag setting is programmable.

By providing several control signals to the external controlling device, this parallel interface is very flexible and supports request-driven as well as acknowledge-driven communications. The selection is done by the external device by means of a status register. This register is exclusively dedicated to the external device and can be read or written.

Serial Interface X

This is a bidirectional 16-bit serial I/O which allows for simultaneous data communication in both directions.

During write operations, data is shifted serially into an input shift register. After termination of the shift operation the contents of the shift register is loaded in parallel into an input buffer register. This allows for a continous data stream transmission. A flag is generated indicating the input buffer register is full. The input port has a fully asynchronous handshake capability.

During read operation data is serially shifted out of an output shift register. After termination of the shift operation the output shift register is reloaded by an output buffer register. During a write operation it allows for a continous data stream transmission and autonomous operation. A flag is generated indicating the output buffer register is empty. The output port has a fully asynchronous handshake capability.

Serial Interface Y

The second serial interface Y covers the same functionality as the serial interface X. In addition, the serial interface Y meets several synchronous transfer protocols such as PCM-Highway or General Communication Interface (GCI). Control registers are provided to select up to 16 data words in a frame from the synchronous data stream. A collision detection unit supports collision detection on the output data stream. It is possible to select the bits in a data word which are considered for collison detection. If a collision occurs, an error flag will be set which can be used for interrupt processing allowing for efficient error recovery.

General Purpose I/O pins

Four bidirectional general purpose I/O pins are provided as an additional interface to external devices. The state of these pins is reflected in 4 bits of a control register. A write operation to this register causes the appropriate values to appear as output signals on the related pins. With a read operation the incoming signals can then be recognized.

JTAG Interface

The processors provide a standardized test access port which is fully compatible with the IEEE 1149.1 standard. Each time the command NMI is provided to the JTAG interface, a non-maskable interrupt is generated and fed to the interrupt unit of the processor-core. A jump to a non-maskable interrupt service routine will follow as a reaction. The interface provides two I/O registers to the external controlling host. These register are also fully accessable by the processor core which allows for data exchange between an external device and an application program, or service routine.

Several commands to support testing of the device are provided by the JTAG interface, including Boundary- Scan.

Peripheral Functions

Power-down mode

This mode is entered by executing a specific instruction in the application program. It switches the processors into a dormant state where only a fraction of the power dissipation is needed as compared with normal operation mode. The internal clock is stopped and only some synchronization and clock registers are operating.

Wake-up mode

The power-down mode is terminated if an I/O flag occurs and the related wake-up mode is enabled by the application program.

Interrupts

There are 13 different interrupt sources provided by the processors:

1 non-maskable interrupt initiated by a JTAG port instruction.

2 external interrupts initiated by external devices.

6 internal interrupts initiated by the processor's I/O devices.

1 internal interrupt initiated by the collision detection unit of the serial interface Y.

2 internal interrupts initiated by certain conditions in the arithmetic unit.

1 internal interrupt initiated by the event-counter.

Event Counter

A 16-bit event counter is provided as an additional peripheral function. The counter can be loaded by the application program and will be decremented every rising edge of the external signal ECLK, indicating an event to the counter.

ECLK is synchronized to the internal processor clock and is limited to half the frequency of this clock. Each time the counter detects a zero value, a flag is generated which can be used as an interrupt source. The counter will then automatically be reloaded with the start value which is stored in a buffer register.

Sound fader control circuit TEA6320

FEATURES

- Source selector for four stereo and one mono inputs
- Interface for noise reduction circuits
- Interface for external equalizer
- Volume, balance and fader control
- Special loudness characteristic automatically controlled in combination with volume setting
- Bass and treble control
- Mute control at audio signal zero crossing
- Fast mute control via I^{2}C-bus
- Fast mute control via pin
- I^{2}C-bus control for all functions
- Power supply with internal power-on reset

GENERAL DESCRIPTION

The sound fader control circuit TEA6320 is an I^{2}C-bus controlled stereo preamplifier for car radio hi-fi sound applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	positive supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	26	–	mA
$V_{o(RMS)}$	maximum output voltage level	V_{CC} = 8.5 V; THD ≤ 0.1%	–	2000	–	mV
G_v	volume gain		–86	–	+20	dB
G_{step}	step resolution (volume)		–	1	–	dB
G_b	bass control		–15	–	+15	dB
G_t	treble control		–12	–	+12	dB
G_{step}	step resolution (bass, treble)		–	1.5	–	dB
(S+N)/N	signal-plus-noise to noise ratio	V_o = 2.0 V; G_v = 0 dB; unweighted	–	105	–	dB
RR_{100}	ripple rejection	$V_{r(RMS)}$ < 200 mV; f = 100 Hz; G_v = 0 dB	–	75	–	dB
α_{cs}	channel separation	250 Hz ≤ f ≤ 10 kHz; G_v = 0 dB	90	96	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6320	32	SDIL	plastic	SOT232AG
TEA6320T	32	SO	plastic	SOT287AH

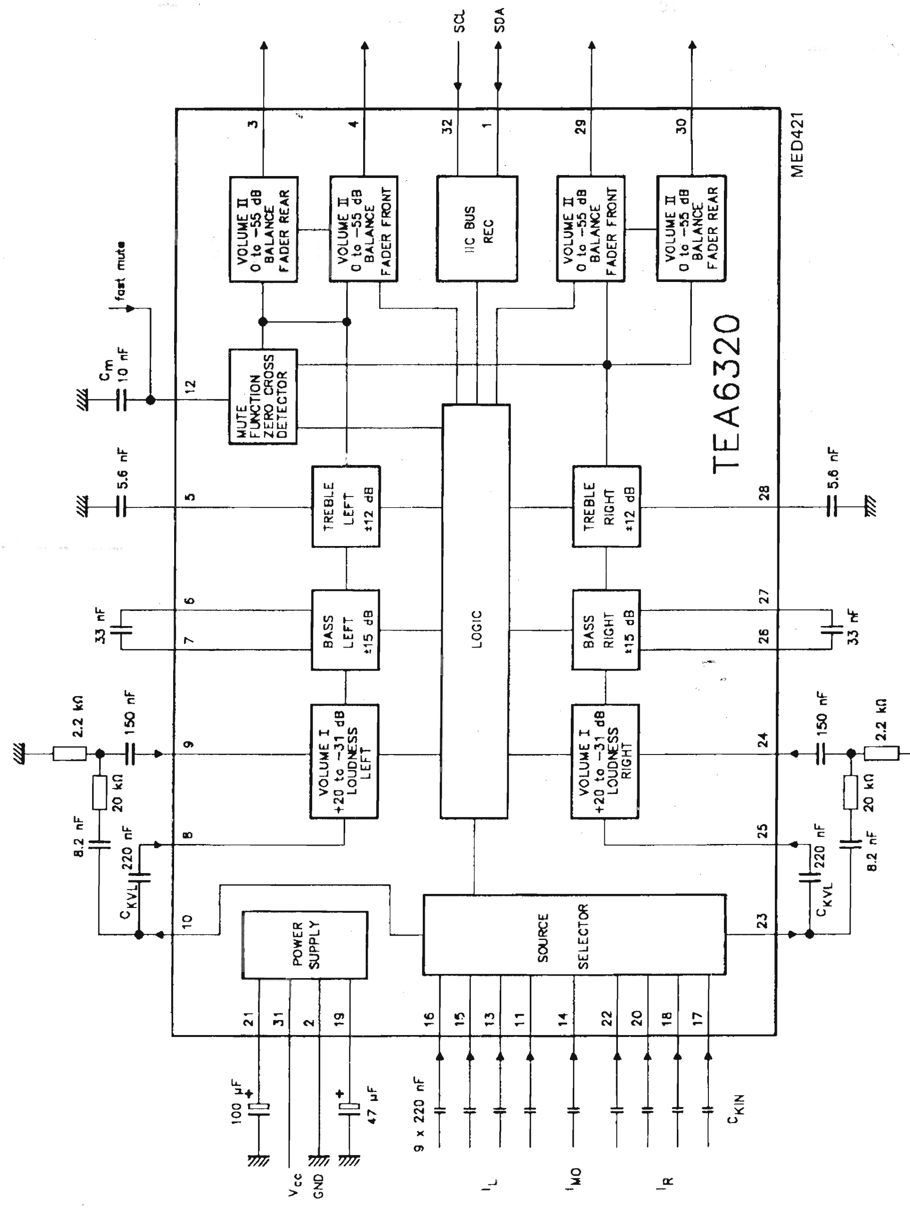


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	serial data input/output
GND	2	ground
OUTLR	3	output left rear
OUTLF	4	output left front
TL	5	treble control capacitor left channel or input from an external equalizer
B2L	6	bass control capacitor left channel or output to an external equalizer
B1L	7	bass control capacitor, left channel
IVL	8	input volume I, left control part
ILL	9	input loudness, left control part
QSL	10	output source selector, left channel
IDL	11	input D left source
MUTE	12	mute control
ICL	13	input C left source
IMO	14	input mono source
IBL	15	input B left source
IAL	16	input A left source
IAR	17	input A right source
IBR	18	input B right source
CAP	19	electronic filtering for supply
ICR	20	input C right source
V_{ref}	21	reference voltage ($0.5V_{CC}$)
IDR	22	input D right source
QSR	23	output source selector right channel
ILR	24	input loudness right channel
IVR	25	input volume I, right control part
B1R	26	bass control capacitor right channel
B2R	27	bass control capacitor right channel or output to an external equalizer
TR	28	treble control capacitor right channel or input from an external equalizer
OUTRF	29	output right front
OUTRR	30	output right rear
V_{CC}	31	supply voltage
SCL	32	serial clock input

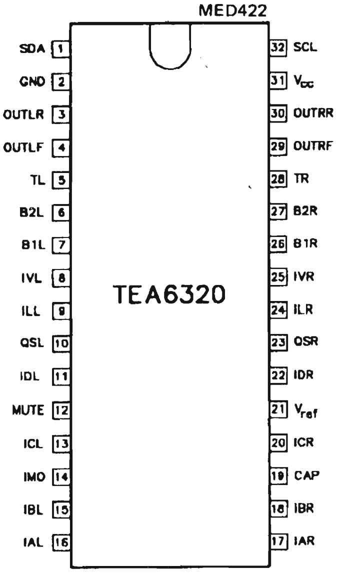


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The source selector selects one of 4 stereo inputs or the mono input. The maximum input signal voltage is $V_{i\,(RMS)} = 2$ V. The outputs of the source selector and the inputs of the following volume control parts are available at pins 8 and 10 for the left channel and pins 23 and 25 for the right channel. This offers the possibility of interfacing a noise reduction system.

The volume control function is split into two sections: volume I control block and volume II control block.

The control range of volume I is between +20 dB and –31 dB in steps of 1 dB. The volume II control range is between 0 dB and –55 dB in steps of 1 dB. Although the theoretical possible control range is 106 dB (+20 dB to –86 dB), in practice a range of 86 dB (+20 dB to –66 dB) is recommended. The gain/attenuation setting of the volume I control blocks is common for both channels.

The volume I control blocks operate in combination with the loudness control. The filter is linear when the maximum gain for the volume I control (+20 dB) is selected. The filter characteristic increases automatically over a range of 32 dB down to a setting of –12 dB. That means the maximum filter characteristic is obtained at –12 dB setting of volume I. Further reduction of the volume does not further influence the filter characteristic (see Fig.5). The maximum selected filter characteristic is determined by external components. The proposed application gives a maximum boost of 17 dB for bass and 4.5 dB for treble. The loudness may be switched on or off via I^{2}C-bus control (Table 7).

The volume I control block is followed by the bass control block. A single external capacitor of 33 nF for each channel in combination with internal resistors, provides the frequency response of the bass control (see Fig.3). The adjustable range is between –15 dB and +15 dB in steps of 1.5 dB at 40 Hz.

Both, loudness and bass control result in a maximum bass boost of 32 dB for low volume settings.

The treble control block offers a control range between –12 dB and +12 dB in steps of 1.5 dB at 15 kHz. The filter characteristic is determined by a single capacitor of 5.6 nF for each channel in combination with internal resistors (see Fig.4).

The basic step width of bass and treble control is 3 dB. The intermediate steps are obtained by switching 1.5 dB boost and 1.5 dB attenuation steps.

The bass and treble control functions can be switched off via I^{2}C-bus. In this event the internal signal flow is disconnected. The connections B2L / B2R are outputs and TL / TR are inputs for inserting an external equalizer.

The last section of the circuit is the volume II block. The balance and fader functions are performed using the same control blocks. This is realized by 4 independently controllable attenuators, one for each output. The control range of these attenuators is 55 dB in steps of 1 dB with an additional mute step.

The circuit provides 3 mute modes.
1) Zero crossing mode mute via I^{2}C-bus using 2 independent zero crossing detectors (ZCM, see Tables 2 and 9 and Fig.15).
2) Fast mute via mute pin (see Fig.9).
3) Fast mute via I^{2}C-bus either by general mute (GMU see Tables 2 and 9) or volume II block setting (see Table 4).
The mute function is performed immediately if ZCM is cleared (ZCM = 0). If the bit is set (ZCM = 1) the mute is activated after changing the GMU bit. The actual mute switching is delayed until the next zero crossing of the audio frequency signal. As the two audio channels (left and right) are independent, two comparators (window detectors) are required to control independent mute switches.

To avoid a large delay of the muting switching when very low frequencies are processed, the maximum delay time is limited to typically 100 ms by an integrated timing circuit and an external capacitor (C_m = 10 nF, see Fig.9). This timing circuit is triggered by reception of a new data word for the switch function which includes the GMU bit. After a discharge and charge period of an external capacitor the muting switch follows the GMU bit if no zero crossing was detected during that time.

The mute function can also be controlled externally. If the mute pin is switched to ground all outputs are muted immediately (hardware mute). This mute request overwrites all mute controls via the I^{2}C-bus for the time the pin is held low.
The hardware mute position is not stored in the TEA6320.

For the turn on/off behaviour the following explanation is generally valid. To avoid AF output caused by the input signal coming from preceding stages, which produce output during drop of V_{CC}. The mute has to be set, before the V_{CC} will drop. This can be achieved by I^{2}C-bus control or by grounding the mute pin.

For use where there is no mute in the application before turn off, a supply voltage drop of more than 1 x V_{BE} will result in a mute during the voltage drop.

The power supply should include a V_{CC} buffer capacitor, which provides a discharging time constant. If the input signal does not disappear after turn off the input will become audible after a certain time. A 4.7 kΩ resistor discharges the V_{CC} buffer capacitor, because the internal current of the IC does not discharge it completely.

The hardware mute function is favourable for use in RDS (Radio Data System) applications. The zero crossing mute avoids modulation plops. This feature is an advantage for mute during changing presets and/or sources (e. g. traffic announcement during cassette playback).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		0	10	V
T_{amb}	operating ambient temperature range		−40	+85	°C
T_{stg}	storage temperature range		−65	+150	°C
V_{es}	electrostatic handling	see note 1			
V_n	voltage at pins: pin 1 to 2 and 3 - 32 to 2		0	V_{CC}	V

Note to the limiting values

1. Human body model: C = 100 pF; R = 1.5 kΩ; V ≥ 2 kV
   Charge device model: C = 200 pF; R = 0 Ω; V ≥ 500 V

CHARACTERISTICS

V_{CC} = 8.5 V; R_S = 600 Ω, R_L = 10 kΩ, C_L = 2.5 nF, AC coupled; f = 1 kHz; T_{amb} = +25 °C; gain control G_v = 0 dB; bass linear; treble linear; fader off; balance in mid position; loudness off; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current		–	26	33	mA
V_{DC}	internal DC voltage at inputs and outputs		3.83	4.25	4.68	V
V_{ref}	internal reference voltage at pin 21		–	4.25	–	V
G_v	maximum voltage gain	R_S = 0 Ω; R_L = ∞	19	20	21	dB
$V_{o(RMS)}$	output voltage level for					
	P_{max} at the power output stage	THD ≤ 0.1%; see Fig.10	–	2000	–	mV
	start of clipping	THD = 1%	2300	–	–	mV
		R_L = 2 kΩ; C_L = 10 nF; THD = 1%	2000	–	–	mV
$V_{i(RMS)}$	input sensitivity	V_o = 2000 mV; G_v = 20 dB	–	200	–	mV
B	roll-off frequencies	C_{KIN} = 220 nF; C_{KVL} = 220 nF; $Z_i = Z_{i\,min}$				
		low frequency (–1 dB)	60	–	–	Hz
		low frequency (–3 dB)	30	–	–	Hz
		high frequency (–1 dB)	20000	–	–	Hz
		C_{KIN} = 470 nF; C_{KVL} = 100 nF; $Z_i = Z_{i\,typ}$				
		low frequency (–3 dB)	17	–	–	Hz
α_{CS}	channel separation	V_i = 2 V; frequency range 250 Hz to 10 kHz	90	96	–	dB
THD	total harmonic distortion	frequency range 20 Hz to 12.5 kHz				
		V_i = 100 mV; G_v = 20 dB	–	0.1	–	%
		V_i = 1000 mV; G_v = 0 dB	–	0.05	tbn	%
		V_i = 2000 mV; G_v = 0 dB	–	0.1	–	%
		V_i = 2000 mV; G_v = –10 dB	–	0.1	–	%
RR	ripple rejection	$V_{r(RMS)}$ < 200 mV				
		f = 100 Hz	tbn	76	–	dB
		f = 40 Hz to 12.5 kHz	–	66	–	dB
(S+N)/N	signal-plus-noise to noise ratio	unweighted; 20 Hz to 20 kHz RMS; V_o = 2.0 V; see Fig.6	–	105	–	dB
		CCIR 468-2 weighted; quasi peak; V_o = 2.0 V				
		G_v = 0 dB	–	95	–	dB
		G_v = 12 dB	–	88	–	dB
		G_v = 20 dB	–	81	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$P_{no(RMS)}$	noise output power (RMS value) only contribution of TEA6320; power amplifier for 6 W	mute position; note 1	–	–	10	nW
α_B	crosstalk (20 log $V_{bus(p-p)}$ / $V_{o(RMS)}$) between bus inputs and signal outputs	note 2	–	110	–	dB
Source selector						
Z_i	input impedance		25	35	45	kΩ
α_S	input isolation of one selected source	f = 1 kHz	–	105	–	dB
	to any other input	f = 12.5 kHz	–	95	–	dB
$V_{i(RMS)}$	maximum input voltage (RMS value)	THD < 0.5%; V_{CC} = 8.5 V	–	2.15	–	V
		THD < 0.5%; V_{CC} = 7.5 V	–	1.8	–	V
$V_{DC\ OFF}$	DC offset voltage at source selector out by selection of any inputs		–	–	10	mV
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		10	–	–	kΩ
C_L	output load capacity		0	–	2500	pF
G_v	voltage gain, source selector		–	0	–	dB
Control part (source selector disconnected; source resistance 600 Ω)						
Z_i	input impedance volume input		100	150	200	kΩ
	input impedance loudness input		25	33	40	kΩ
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance		2	–	–	kΩ
C_L	output load capacity		0	–	10	nF
$V_{i(RMS)}$	maximum input voltage (RMS value)	THD < 0.5%	–	2.15	–	V
V_{no}	noise output voltage	CCIR 468-2 weighted; quasi peak				
		G_v = 20 dB	–	110	220	μV
		G_v = 0 dB	–	33	50	μV
		G_v = –66 dB	–	13	22	μV
		mute position	–	10	–	μV
G_c	total continuous control range		–	106	–	dB
	recommended control range		–	86	–	dB
G_{step}	step resolution		–	1	–	dB
	step error between any adjoining step		–	–	0.5	dB
ΔG_a	attenuator set error	G_v = +20 to –50 dB	–	–	2	dB
		G_v = –51 to –66 dB	–	–	3	dB
ΔG_t	gain tracking error	G_v = +20 to –50 dB	–	–	2	dB
α_m	mute attenuation	see Fig.8	100	110	–	dB
$V_{DC\ OFF}$	DC step offset	G_v = 0 to –66 dB	–	0.2	10	mV
	between any adjoining step	G_v = 20 to 0 dB	–	tbn	15	mV
	between any step to mute	G_v = 0 to –66 dB	–	–	10	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Volume I control and loudness						
G_c	continuous volume control range		–	51	–	dB
G_v	volume gain		–31	–	20	dB
G_{step}	step resolution		–	1	–	dB
L_B	maximum loudness boost	loudness on; referred to loudness off; boost is determined by external components				
		f = 40 Hz	–	17	–	dB
		f = 10 kHz	–	4.5	–	dB
Bass control						
G_b	bass control, maximum boost	f = 40 Hz	14	15	16	dB
	maximum attenuation	f = 40 Hz	14	15	16	dB
G_{step}	step resolution (toggle switching)	f = 40 Hz	–	1.5	–	dB
	step error between any adjoining step	f = 40 Hz	–	–	0.5	dB
$V_{DC\ OFF}$	DC step offset in any bass position		–	–	20	mV
Treble control						
G_t	treble control, maximum boost	f = 15 kHz	11	12	13	dB
	maximum attenuation	f = 15 kHz	11	12	13	dB
	maximum boost	f > 15 kHz	–	–	15	dB
G_{step}	step resolution (toggle switching)	f = 15 kHz	–	1.5	–	dB
	step error between any adjoining step	f = 15 kHz	–	–	0.5	dB
$V_{DC\ OFF}$	DC step offset in any treble position		–	–	10	mV
Volume II, balance and fader control						
G_f	continuous attenuation fader and volume control range		53.5	55	56.5	dB
G_{step}	step resolution		–	1	2	dB
	attenuation set error		–	–	1.5	dB
Mute function (see Fig.9)						
a) Hardware mute						
V_{SW}	mute switch level (2 x V_{BE})		–	1.45	–	V
mute active:						
$V_{SW\ LOW}$	input level		–	–	1.0	V
I_{CH}	input current	$V_{SW\ LOW}$ = 1 V	–300	–	–	µA
mute passive: level internally defined						
$V_{SW\ HIGH}$	saturation voltage		–	–	V_{CC}	V
t_{DMU}	delay until mute passive		–	–	0.5	ms
b) Zero crossing mute						
I_D	discharge current		0.3	0.6	1.2	µA
I_{CH}	charge current		–300	–150	–	µA
V_{SWDEL}	delay switch level (3 x V_{BE})		–	2.2	–	V
t_{DEV}	delay time	C_m = 10 nF	–	100	–	ms
V_{WIND}	window for audio signal zero crossing detection		–	30	40	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Muting at power supply drop						
$V_{CC-DROP}$	supply drop for mute active		–	$V_{19} - 0.7$	–	V
Power on reset (when reset is active the GMU-bit (general mute) is set and the I²C-bus receiver is in reset position)						
V_{CC}	increasing supply voltage start of reset		–	–	2.5	V
	end of reset		5.2	6.0	6.8	V
	decreasing supply voltage start of reset		4.2	5.0	5.8	V
Digital part						
I²C-bus pins; see note 3						
V_{IH}	HIGH level input voltage		3	–	9.5	V
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
I_{IH}	HIGH level input current		–10	–	+10	µA
I_{IL}	LOW level input current		–10	–	+10	µA
V_{OL}	LOW level output voltage	$I_L = 3$ mA	–	–	0.4	V

Notes to the characteristics

1. The indicated values for output power assume a 6 W power amplifier at 4 Ω with 20 dB gain and a fixed attenuator of 12 dB in front of it. Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. The transmission contains: total initialization with MAD and Subaddress for volume and 8 data words, see also definition of characteristics, clock frequency = 50 kHz, repetition burst rate = 400 Hz, maximum bus signal amplitude = 5 V_{p-p}
3. The AC characteristics are in accordance with the I²C-bus specification. Full specification of I²C-bus will be supplied on request.

I²C-BUS PROTOCOL

I²C-bus format

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	A	P

Where:

S = start condition
SLAVE ADDRESS (MAD) = 1000 0000
A = acknowledge, generated by the slave
SUBADDRESS (SAD) = see Table 1
DATA = see Table 1
P = STOP condition

If more than 1 byte of DATA is transmitted, then auto-increment of the significant subaddress is performed.

Subaddress

Table 1 Second byte after MAD

FUNCTION	BIT	MSB							LSB
		7	6	5	4	3	2	1	0
volume/loudness	V	0	0	0	0	0	0	0	0
fader front right	FFR	0	0	0	0	0	0	0	1
fader front left	FFL	0	0	0	0	0	0	1	0
fader rear right	FRR	0	0	0	0	0	0	1	1
fader rear left	FRL	0	0	0	0	0	1	0	0
bass	BA	0	0	0	0	0	1	0	1
treble	TR	0	0	0	0	0	1	1	0
switch	S	0	0	0	0	0	1	1	1
							significant subaddress		

Definition of third byte

Table 2 Third byte after MAD and SAD

FUNCTION	BIT	MSB							LSB
		7	6	5	4	3	2	1	0
volume/loudness	V	ZCM	LOFF	V5	V4	V3	V2	V1	V0
fader front right	FFR	X	X	FFR5	FFR4	FFR3	FFR2	FFR1	FFR0
fader front left	FFL	X	X	FFL5	FFL4	FFL3	FFL2	FFL1	FFL0
fader rear right	FRR	X	X	FRR5	FRR4	FRR3	FRR2	FRR1	FRR0
fader rear left	FRL	X	X	FRL5	FRL4	FRL3	FRL2	FRL1	FRL0
bass	BA	X	X	X	BA4	BA3	BA2	BA1	BA0
treble	TR	X	X	X	TR4	TR3	TR2	TR1	TR0
switch	S	GMU	X	X	X	X	SC2	SC1	SC0

Function of the bits:

V0 to V5	volume control
LOFF	switch loudness on/off
FRR0 to FRR5	fader control front right
FFL0 to FFL5	fader control front left
FRR0 to FRR5	fader control rear right
FRL0 to FRL5	fader control rear left
BA0 to BA4	bass control
TR0 to TR4	treble control
SC0 to SC2	source selector control
GMU	mute control for all outputs (general mute)
ZCM	zero crossing mode
X	don't care bits (logic 1 during testing)

Table 3 Volume setting

G_v (dB)	DATA					
	V5	V4	V3	V2	V1	V0
20	1	1	1	1	1	1
19	1	1	1	1	1	0
18	1	1	1	1	0	1
17	1	1	1	1	0	0
16	1	1	1	0	1	1
15	1	1	1	0	1	0
14	1	1	1	0	0	1
13	1	1	1	0	0	0
12	1	1	0	1	1	1
11	1	1	0	1	1	0
10	1	1	0	1	0	1
9	1	1	0	1	0	0
8	1	1	0	0	1	1
7	1	1	0	0	1	0
6	1	1	0	0	0	1
5	1	1	0	0	0	0
4	1	0	1	1	1	1
3	1	0	1	1	1	0
2	1	0	1	1	0	1
1	1	0	1	1	0	0
0	1	0	1	0	1	1
–1	1	0	1	0	1	0
–2	1	0	1	0	0	1
–3	1	0	1	0	0	0
–4	1	0	0	1	1	1
–5	1	0	0	1	1	0
–6	1	0	0	1	0	1
–7	1	0	0	1	0	0
–8	1	0	0	0	1	1
–9	1	0	0	0	1	0
–10	1	0	0	0	0	1
–11	1	0	0	0	0	0

Loudness on: the increment of the loudness characteristic is linear at every volume step in the range from +20 dB to –11 dB.

Table 3 Volume setting (continued)

G_v (dB)	DATA					
	V5	V4	V3	V2	V1	V0
−12	0	1	1	1	1	1
−13	0	1	1	1	1	0
−14	0	1	1	1	0	1
−15	0	1	1	1	0	0
−16	0	1	1	0	1	1
−17	0	1	1	0	1	0
−18	0	1	1	0	0	1
−19	0	1	1	0	0	0
−20	0	1	0	1	1	1
−21	0	1	0	1	1	0
−22	0	1	0	1	0	1
−23	0	1	0	1	0	0
−24	0	1	0	0	1	1
−25	0	1	0	0	1	0
−26	0	1	0	0	0	1
−27	0	1	0	0	0	0
−28	0	0	1	1	1	1
−29	0	0	1	1	1	0
−30	0	0	1	1	0	1
−31	0	0	1	1	0	0

Loudness characteristic is constant in a range from −11 dB to −31 dB.

Table 3 Volume setting (continued)

G_v (dB)	DATA					
	V5	V4	V3	V2	V1	V0
−28	0	0	1	0	1	1
. . .			. . .			
−31	0	0	0	0	0	0

Repetition of steps in a range from −28 dB to −31 dB.

Table 4 Fader setting

G_v (dB)	DATA					
	FRR5 FRL5 FFL5 FFR5	FRR4 FRL4 FFL4 FFR4	FRR3 FRL3 FFL3 FFR3	FRR2 FRL2 FFL2 FFR2	FRR1 FRL1 FFL1 FFR1	FRR0 FRL0 FFL0 FFR0
0	1	1	1	1	1	1
−1	1	1	1	1	1	0
−2	1	1	1	1	0	1
−3	1	1	1	1	0	0
−4	1	1	1	0	1	1
−5	1	1	1	0	1	0
−6	1	1	1	0	0	1
−7	1	1	1	0	0	0
−8	1	1	0	1	1	1
−9	1	1	0	1	1	0
−10	1	1	0	1	0	1
−11	1	1	0	1	0	0
−12	1	1	0	0	1	1
−13	1	1	0	0	1	0
−14	1	1	0	0	0	1
−15	1	1	0	0	0	0
−16	1	0	1	1	1	1
−17	1	0	1	1	1	0
−18	1	0	1	1	0	1
−19	1	0	1	1	0	0
−20	1	0	1	0	1	1
−21	1	0	1	0	1	0
−22	1	0	1	0	0	1
−23	1	0	1	0	0	0
−24	1	0	0	1	1	1
−25	1	0	0	1	1	0
−26	1	0	0	1	0	1
−27	1	0	0	1	0	0
−28	1	0	0	0	1	1
−29	1	0	0	0	1	0
−30	1	0	0	0	0	1
−31	1	0	0	0	0	0
−32	0	1	1	1	1	1
−33	0	1	1	1	1	0
−34	0	1	1	1	0	1
−35	0	1	1	1	0	0
−36	0	1	1	0	1	1
−37	0	1	1	0	1	0
−38	0	1	1	0	0	1

G_v (dB)	DATA					
	FRR5 FRL5 FFL5 FFR5	FRR4 FRL4 FFL4 FFR4	FRR3 FRL3 FFL3 FFR3	FRR2 FRL2 FFL2 FFR2	FRR1 FRL1 FFL1 FFR1	FRR0 FRL0 FFL0 FFR0
−39	0	1	1	0	0	0
−40	0	1	0	1	1	1
−41	0	1	0	1	1	0
−42	0	1	0	1	0	1
−43	0	1	0	1	0	0
−44	0	1	0	0	1	0
−45	0	1	0	0	1	0
−46	0	1	0	0	0	1
−47	0	1	0	0	0	0
−48	0	0	1	1	1	1
−49	0	0	1	1	1	0
−50	0	0	1	1	0	1
−51	0	0	1	1	0	0
−52	0	0	1	0	1	1
−53	0	0	1	0	1	0
−54	0	0	1	0	0	1
−55	0	0	1	0	0	0
mute	0	0	0	1	1	1
mute	0	0	0	1	1	0
mute	0	0	0	1	0	1
mute	0	0	0	1	0	0
mute	0	0	0	0	1	1
mute	0	0	0	0	1	0
mute	0	0	0	0	0	1
mute	0	0	0	0	0	0

For a particular range the data is always the same, only the subaddress cha

Table 5 Bass setting

G_v (dB)	DATA				
	BA4	BA3	BA2	BA1	BA0
15	1	1	1	1	1
13.5	1	1	1	1	0
15	1	1	1	0	1
13.5	1	1	1	0	0
15	1	1	0	1	1
13.5	1	1	0	1	0
12	1	1	0	0	1
10.5	1	1	0	0	0
9	1	0	1	1	1
7.5	1	0	1	1	0
6	1	0	1	0	1
4.5	1	0	1	0	0
3	1	0	0	1	1
1.5	1	0	0	1	0
0 *	1	0	0	0	1
0 **	1	0	0	0	0
−1.5	0	1	1	1	1
−3	0	1	1	1	0
−4.5	0	1	1	0	1
−6	0	1	1	0	0
−7.5	0	1	0	1	1
−9	0	1	0	1	0
−10.5	0	1	0	0	1
−12	0	1	0	0	0
−13.5	0	0	1	1	1
−15	0	0	1	1	0
−13.5	0	0	1	0	1
−15	0	0	1	0	0
***	0	0	0	1	1
***	0	0	0	1	0
***	0	0	0	0	1
*** ****	0	0	0	0	0

* Recommended data word for step 0 dB.

** Result of 1.5 dB boost and 1.5 dB attenuation.

*** The last four bass control data words mute the bass response.

**** The last bass control and treble control data words (00000) enable the external equalizer connection.

Table 6 Treble setting

G_v (dB)	DATA TR4	TR3	TR2	TR1	TR0
12	1	1	1	1	1
10.5	1	1	1	1	0
12	1	1	1	0	1
10.5	1	1	1	0	0
12	1	1	0	1	1
10.5	1	1	0	1	0
12	1	1	0	0	1
10.5	1	1	0	0	0
9	1	0	1	1	1
7.5	1	0	1	1	0
6	1	0	1	0	1
4.5	1	0	1	0	0
3	1	0	0	1	1
1.5	1	0	0	1	0
0 *	1	0	0	0	1
0 **	1	0	0	0	0
–1.5	0	1	1	1	1
–3	0	1	1	1	0
–4.5	0	1	1	0	1
–6	0	1	1	0	0
–7.5	0	1	0	1	1
–9	0	1	0	1	0
–10.5	0	1	0	0	1
–12	0	1	0	0	0
***	0	0	1	1	1
***	0	0	1	1	0
***	0	0	1	0	1
***	0	0	1	0	0
***	0	0	0	1	1
***	0	0	0	1	0
***	0	0	0	0	1
*** ****	0	0	0	0	0

* Recommended data word for step 0 dB.

** Result of 1.5 dB boost and 1.5 dB attenuation.

*** The last eight treble control data words select treble cut.

**** The last treble control and bass control data words (00000) enable the external equalizer connection.

Table 7 Loudness setting

CHARACTERISTIC	DATA L OFF
with loudness	0
linear	1

Table 8 Selected inputs

INPUTS	DATA		
	SC2	SC1	SC0
IAL, IAR stereo	1	1	1
IBL, IBR stereo	1	1	0
ICC, ICR stereo	1	0	1
IDL, IDR stereo	1	0	0
IMO, mono	0	X	X

Table 9 Mute mode

GMU	ZCM	mode
0	0	direct mute off
0	1	mute off delayed until the next zero crossing
1	0	direct mute
1	1	mute delayed until the next zero crossing

X = don't care bits (logic 1 during testing)

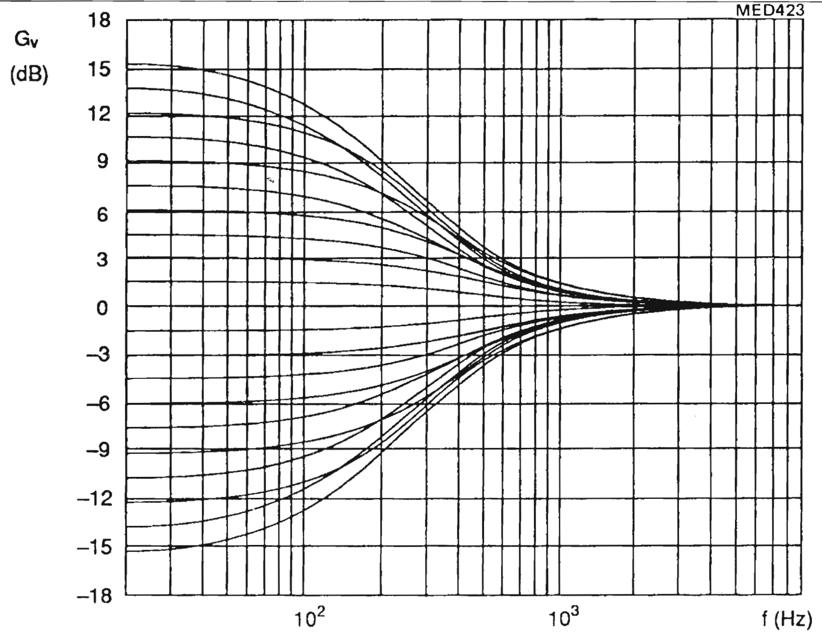


Fig.3 Bass control.

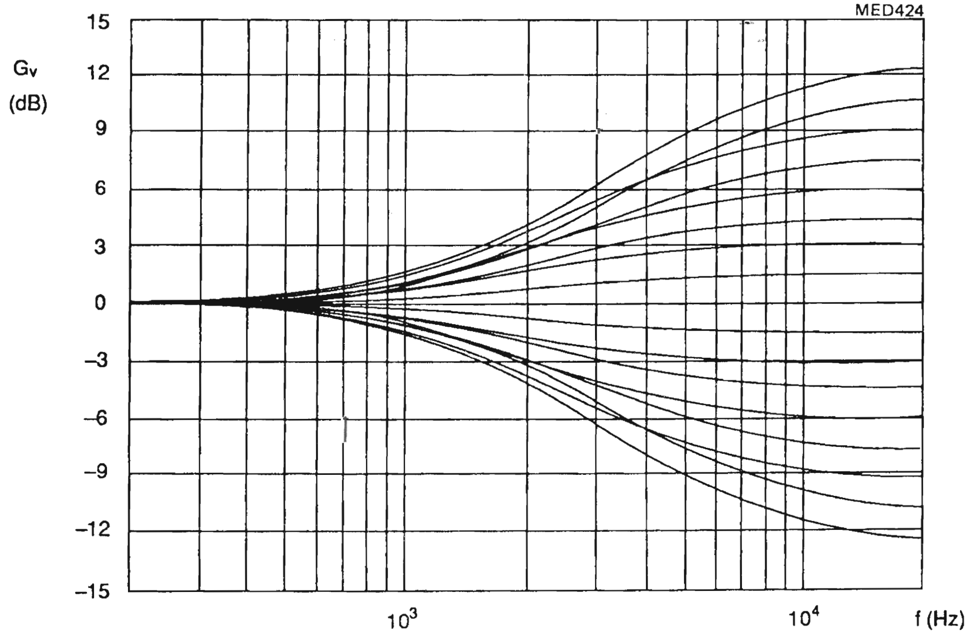


Fig.4 Treble control.

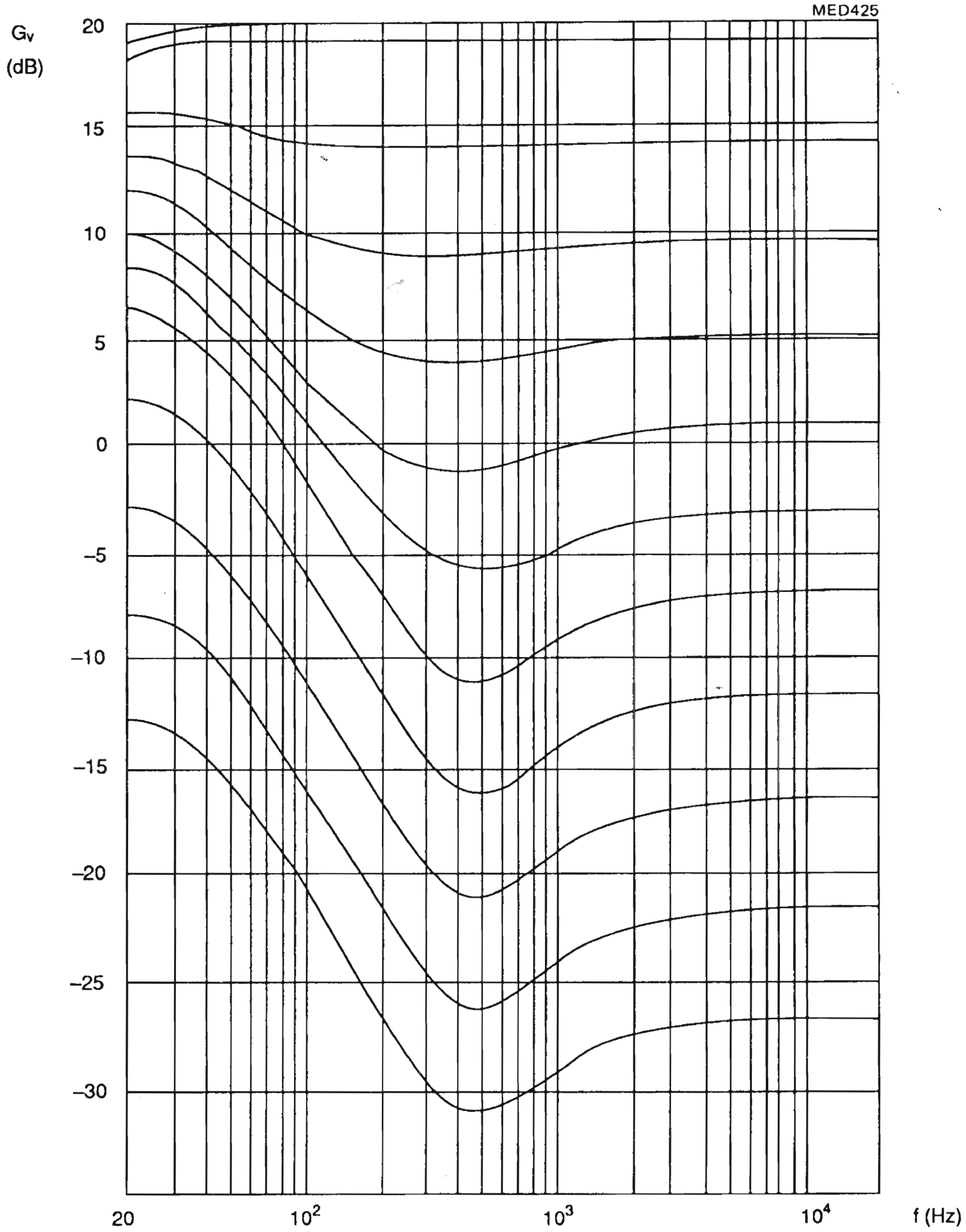


Fig.5 Volume control with loudness (including low roll-off frequency).

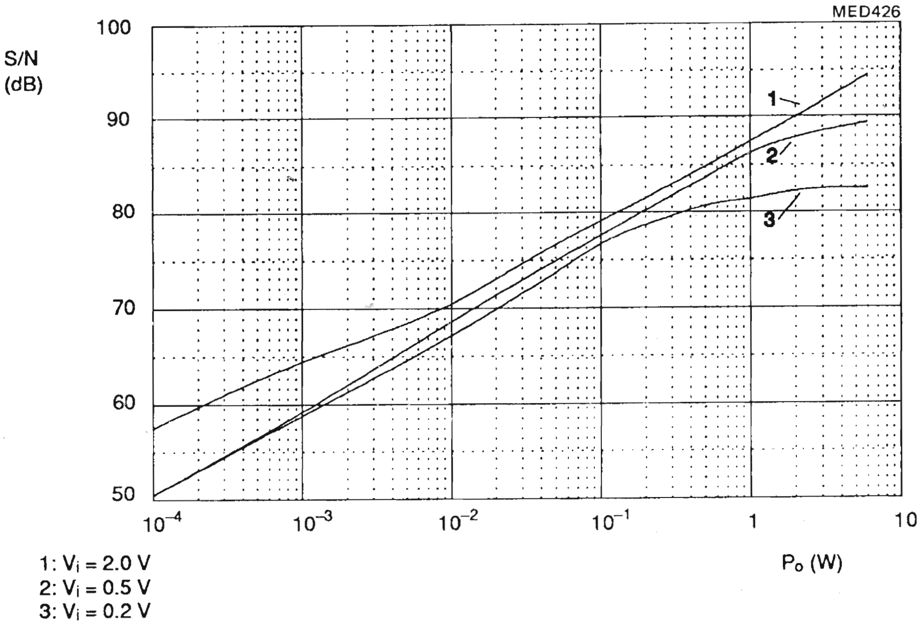


Fig.6(a) Signal-to-noise ratio; noise weighted: CCIR468-2, quasi peak.

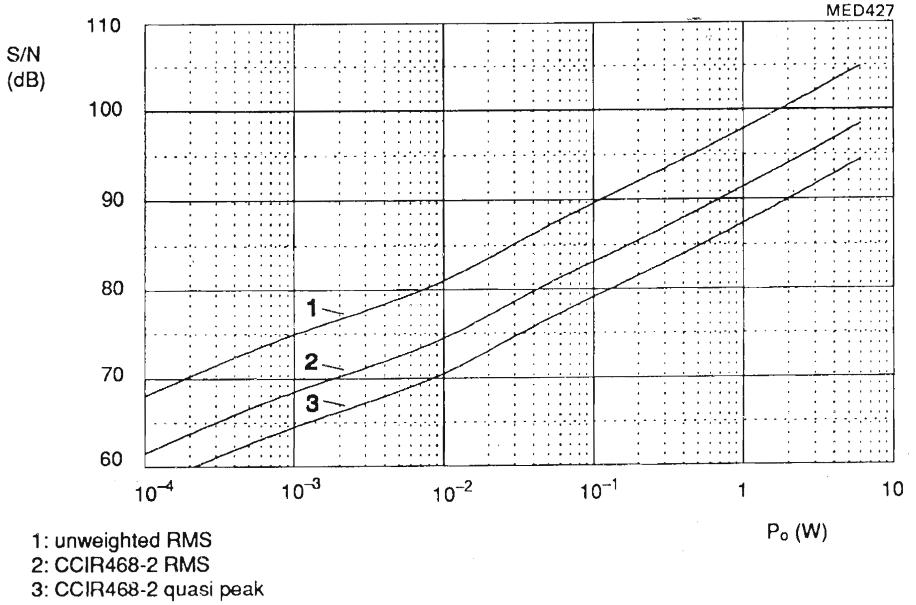


Fig.6(b) Signal-to-noise ratio; V_i = 2 V; P_{max} = 6 W.

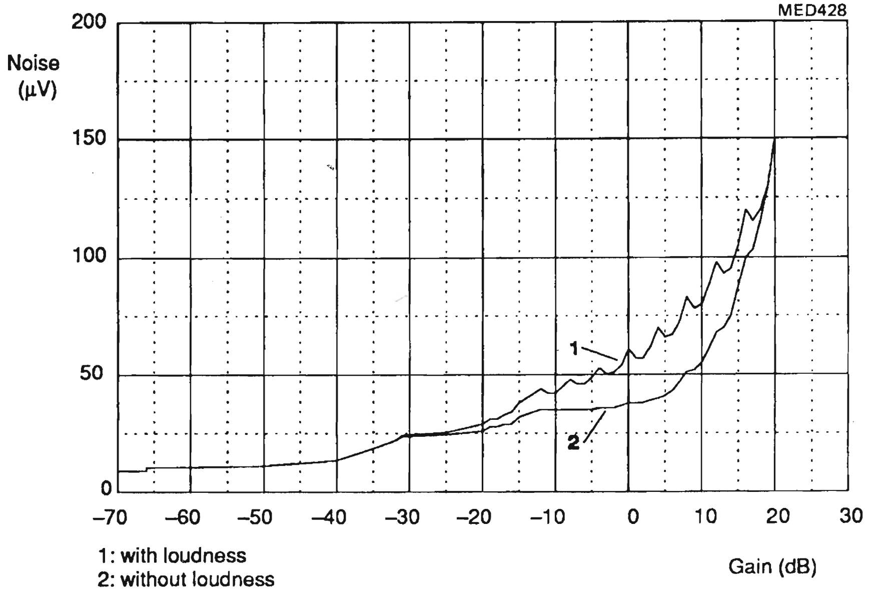


Fig.7 Noise output voltage; CCIR468-2, quasi peak.

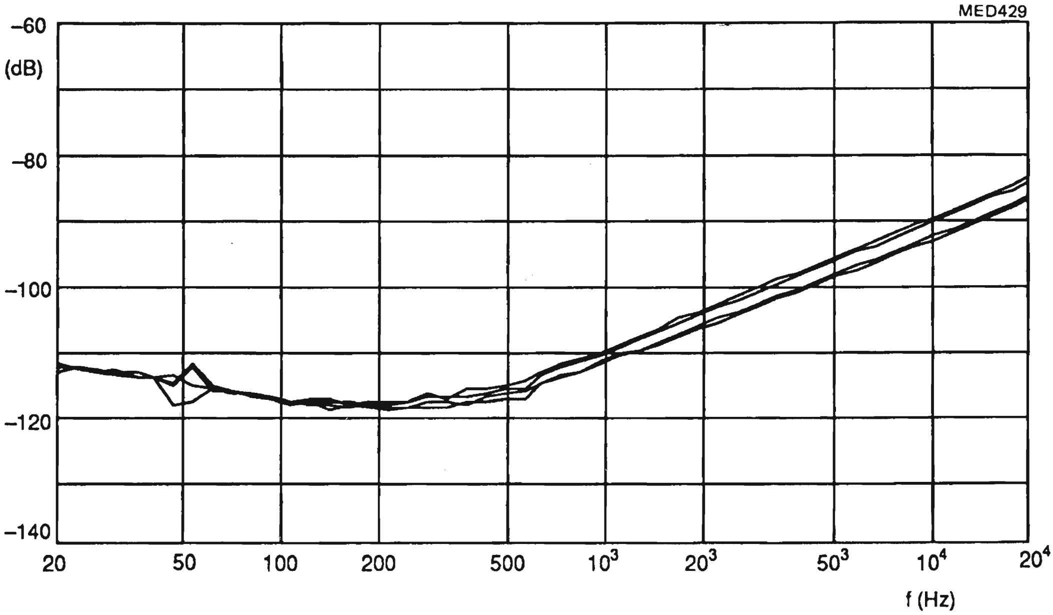
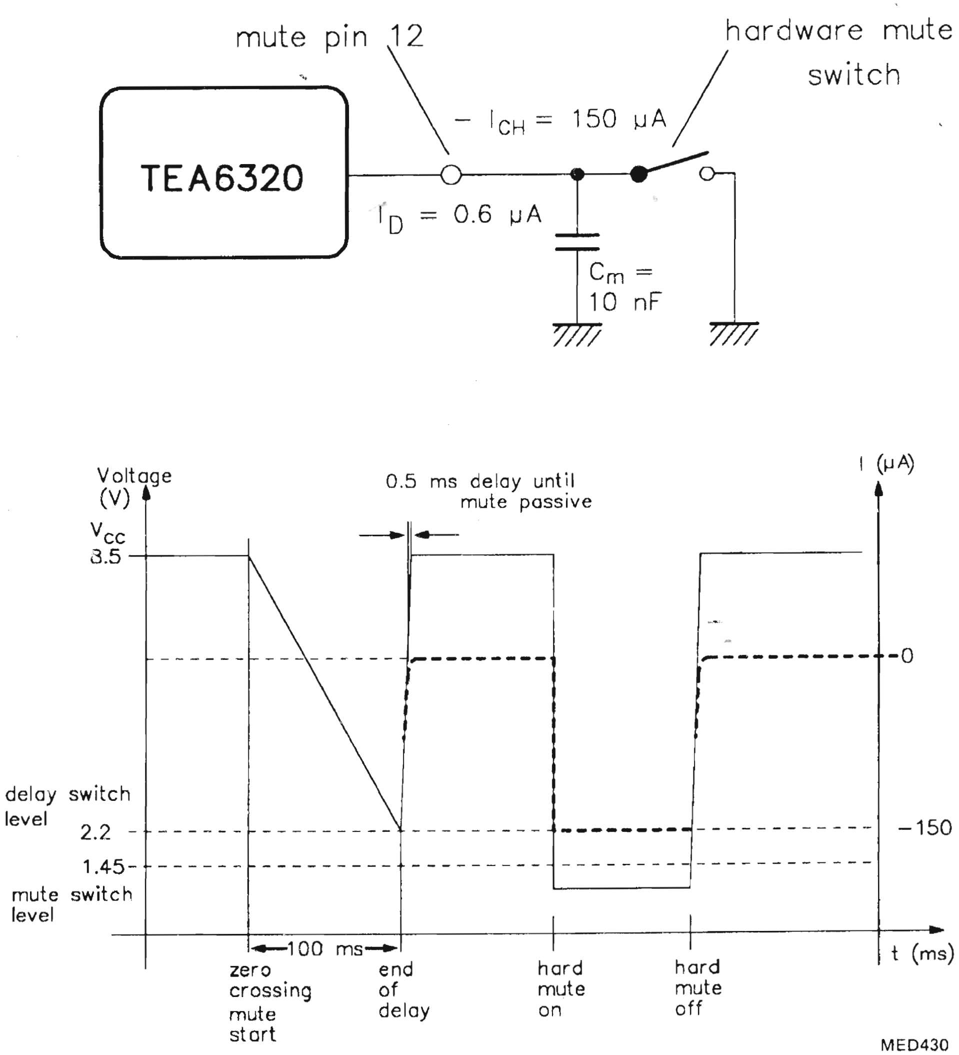


Fig.8 Muting.



delay switch level voltage is typically 2.2 V and is referenced to 3 x V_{BE}

Fig.9 Mute function diagram.

If the 20 dB gain is not required for the maximum volume position, it will be an advantage to use the maximum boost gain and then increased attenuation in the last section, Volume II.
Therefore the loudness will be at the correct place and a lower noise and offset voltage will be achieved.

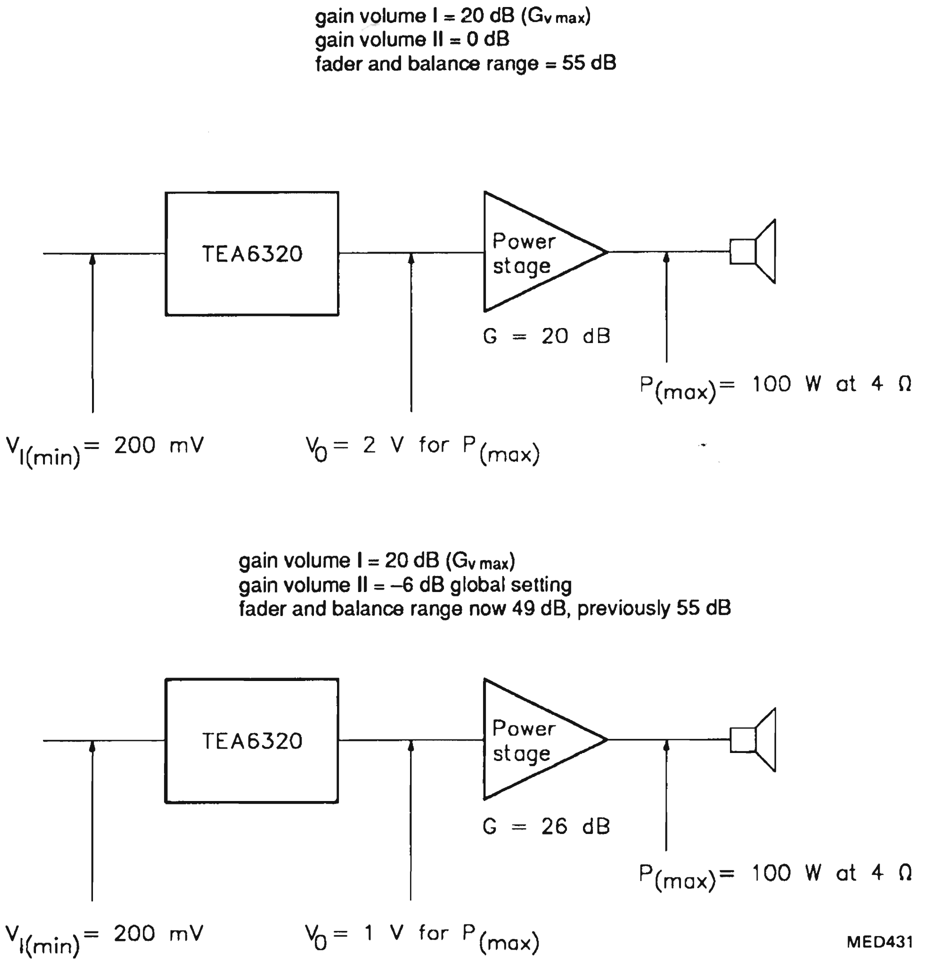


Fig.10 Level diagram.

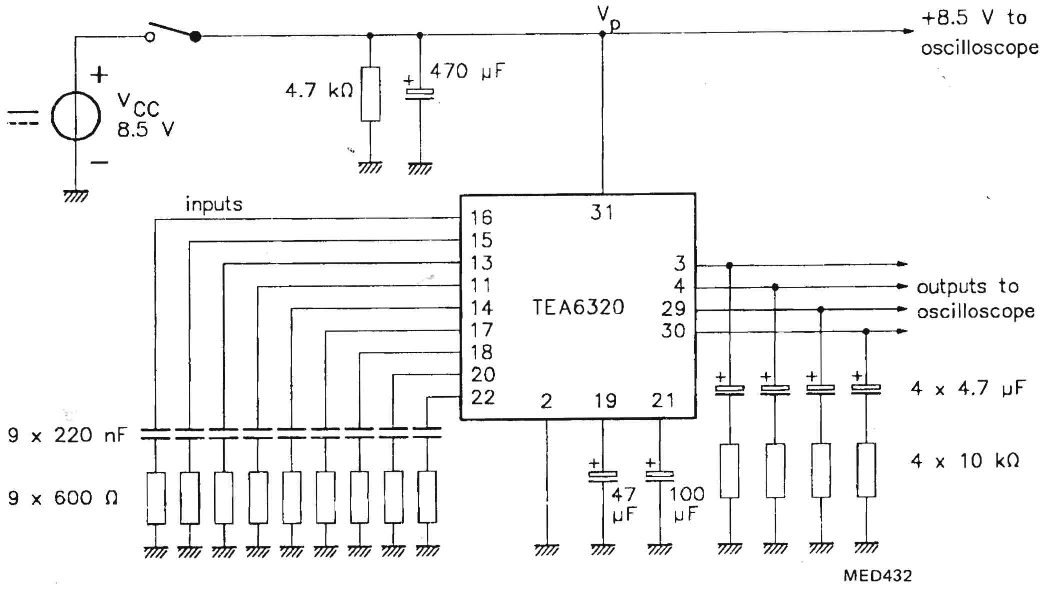


Fig.11 Turn-on/off power supply circuit diagram.

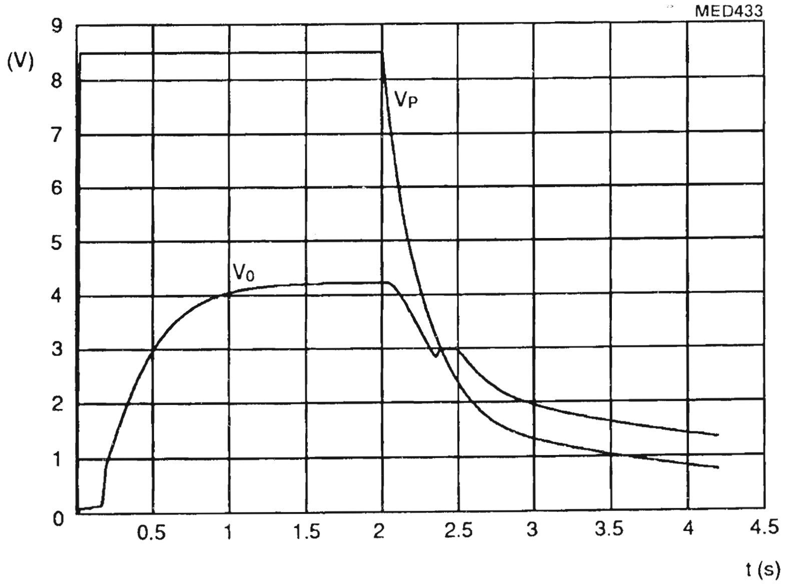


Fig.12 Turn-on/off behaviour.

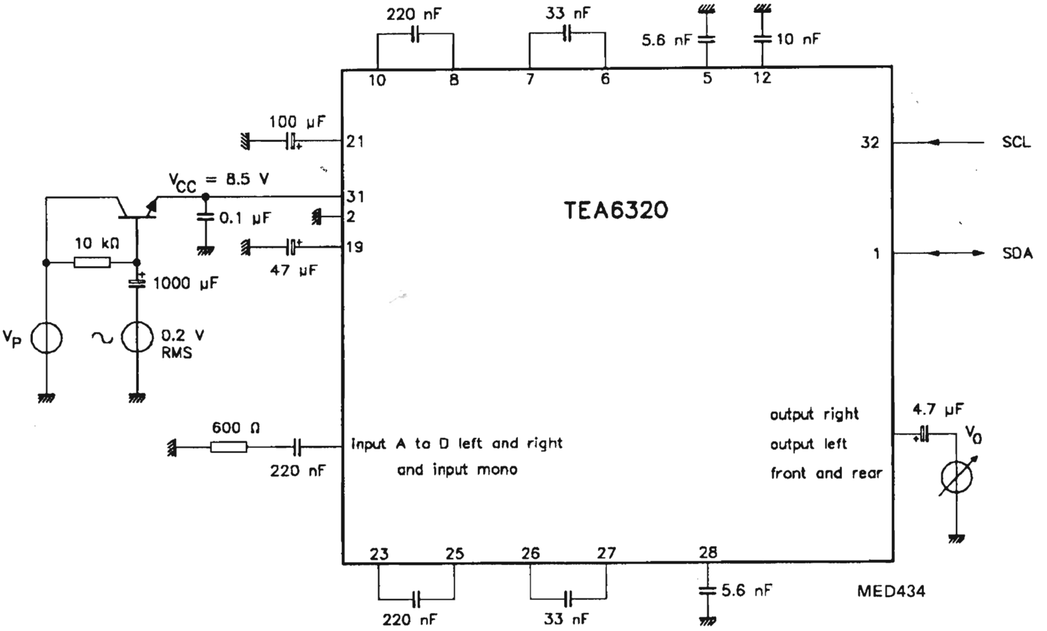


Fig.13 Test circuit for power supply ripple rejection (RR).

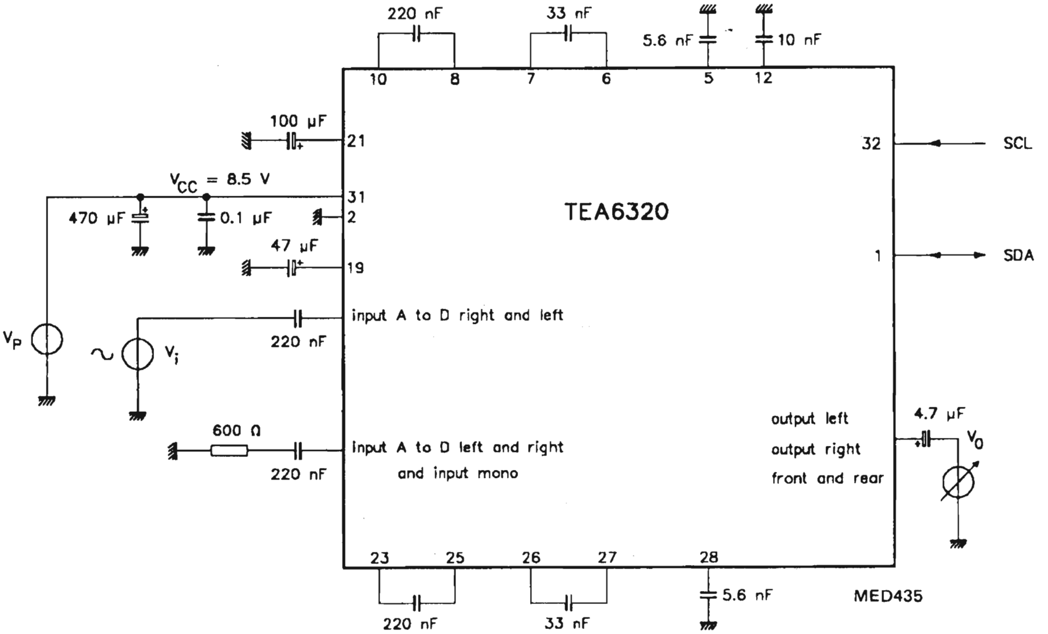


Fig.14 Test circuit for channel separation (α_{CS}).

Selection of input signals by using the zero crossing mute mode

A selection from input A (IAL) to input B (IBL) left sources produces a modulation click depending on the difference of the signal values at the time of switching.
At t_1 the maximum possible difference between signals is 7 $V_{(p-p)}$ and gives a large click. Using the zero cross detector no modulation click is audible.

For example: The selection is enabled at t_1, the microcontroller sets the zero cross bit (ZCM = 1) and then the mute bit (GMU = 1) via the I^2C-bus. The output signal follows the input A signal, until the next zero crossing occurs and then activates mute.
After a fixed delay time at t_2, the microcontroller sends the bits for input switching and mute inactive.

The output signal remains muted until the next signal zero crossing of input B (IBL) occurs, and then follows that signal.
The delay time $t_2 - t_1$ is e. g. 40 ms. Therefore is the capacity CM = 3.3 nF. The zero cross function is working at the lowest frequency of 40 Hz determined by the CM capacitor.

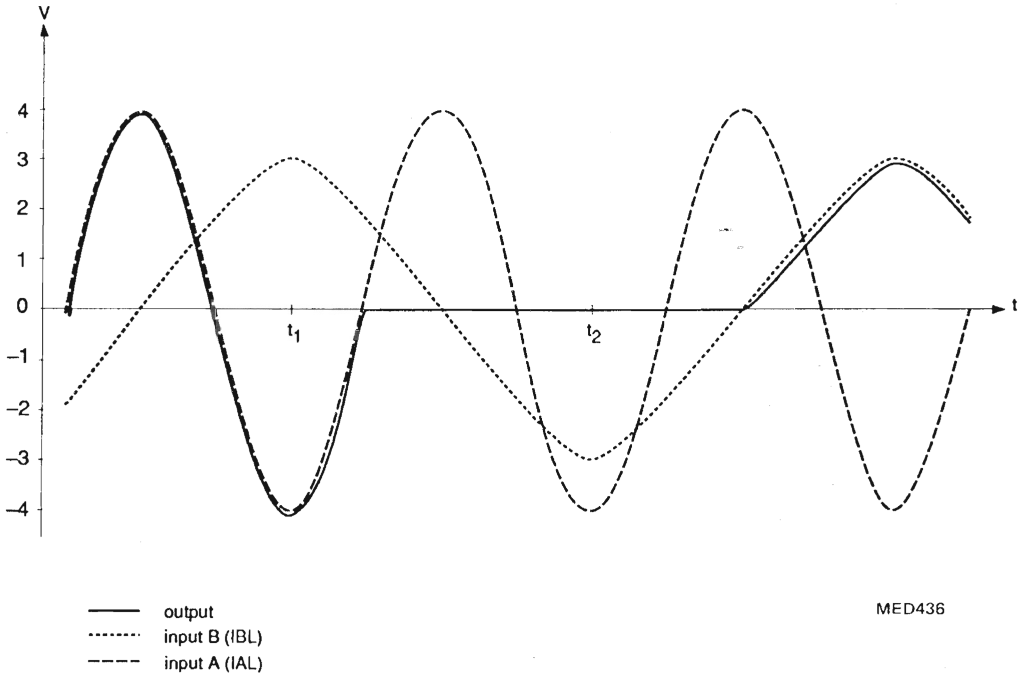


Fig.15 Zero cross function; only one channel shown.

Loudness filter calculation example

Fig.16 shows the basic loudness circuit with an external low pass filter application. R_1 allows an attenuation range of 21 dB while the boost is determined by the gain stage V_2. Both result in a loudness control range of +20 dB to −12 dB. Defining $f_{reference}$ as the frequency where the level does not change while switching loudness on/off. The external resistor R_3 for $f_{reference} \rightarrow \infty$ can be calculated as

$$R_3 = R_1 \frac{10^{G_v/20}}{1 - 10^{G_v/20}}$$

with $G_v = -21$ dB and $R_1 = 33$ kΩ $R_3 = 3.2$ kΩ is generated.
For the low pass filter characteristic the value of the external capacitor C_1 can be determined by setting a specific boost for a defined frequency and referring the gain to G_v at $f_{reference}$ as indicated above.

$$|j\omega C_1| = \frac{(R_1 + R_3) \times 10^{G_v/20} - R_3}{1 - 10^{G_v/20}}$$

For example: 3 dB boost at f = 1 kHz
$G_v = G_{v\,reference} + 3$ dB = −18 dB;
f = 1 kHz and $C_1 = 100$ nF
If a loudness characteristic with additional high frequency boost is desired, an additional high pass section has to be included in the external filter circuit as indicated in the block diagram. A filter configuration that provides AC coupling avoids offset voltage problems.

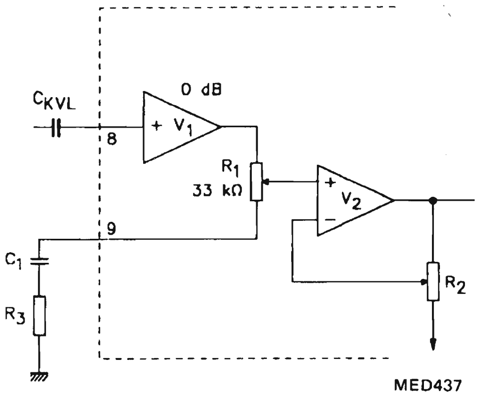
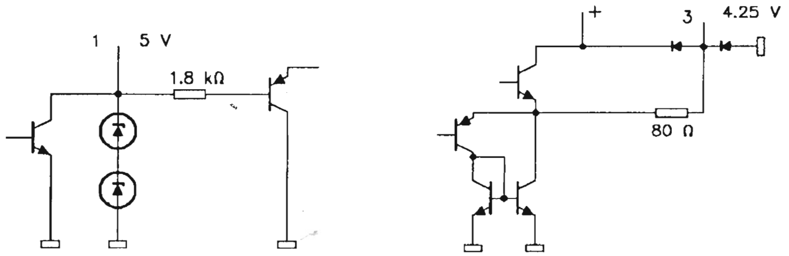


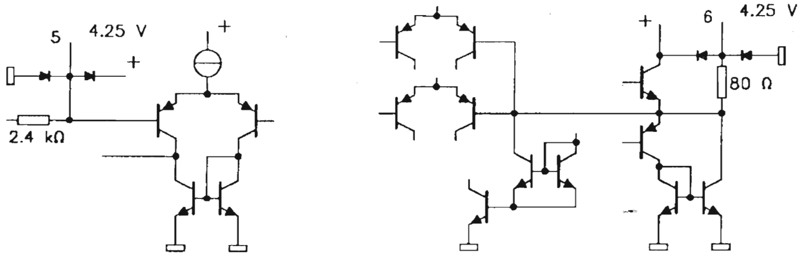
Fig.16 Basic loudness circuit.

INTERNAL PIN CONFIGURATIONS



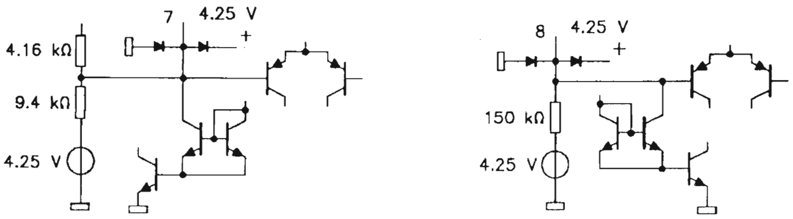
Pin 1: SDA (I^2C-bus data)

Pin 3: Output left, rear
Pin 4: Output left, front
Pin 29: Output right, front
Pin 30: Output right, rear



Pin 5: Treble control capacitor, left channel
Pin 28: Treble control capacitor, right channel

Pin 6: Bass control capacitor output, left channel
Pin 27: Bass control capacitor output, right channel



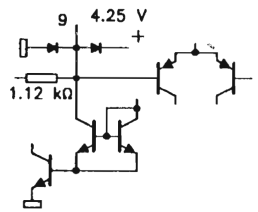
Pin 7: Bass control capacitor input, left channel
Pin 27: Bass control capacitor input, right channel

Pin 8: Input volume 1 left, control part
Pin 25: Input volume 1 right, control part

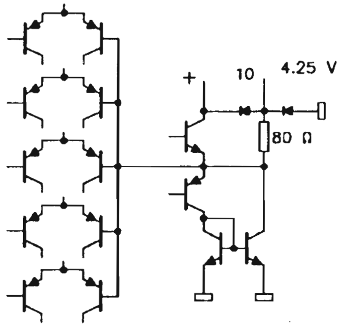
Pin equivalent circuits
V_{CC} = 8.5 V
(All values shown are typical DC values)

MED438

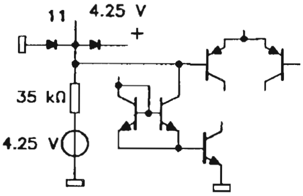
Fig.17(a) Internal circuits (continued in Fig.17(b)).



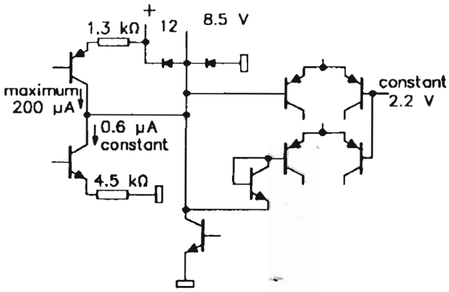
Pin 9: Input loudness left, control part
Pin 24: Input loudness right, control part



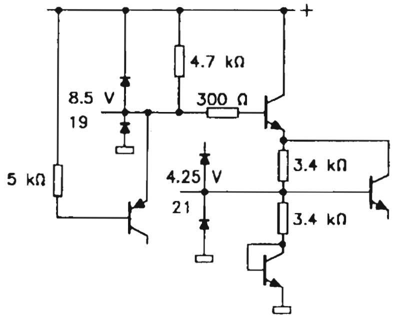
Pin 10: Output source selector, left channel
Pin 23: Output source selector, right channel



Pin 11: Input D left source
Pin 13: Input C left source
Pin 14: Input mono source
Pin 15: Input B left source
Pin 16: Input A left source
Pin 17: Input A right source
Pin 18: Input B right source
Pin 20: Input C right source
Pin 22: Input D right source



Pin 12: Mute control

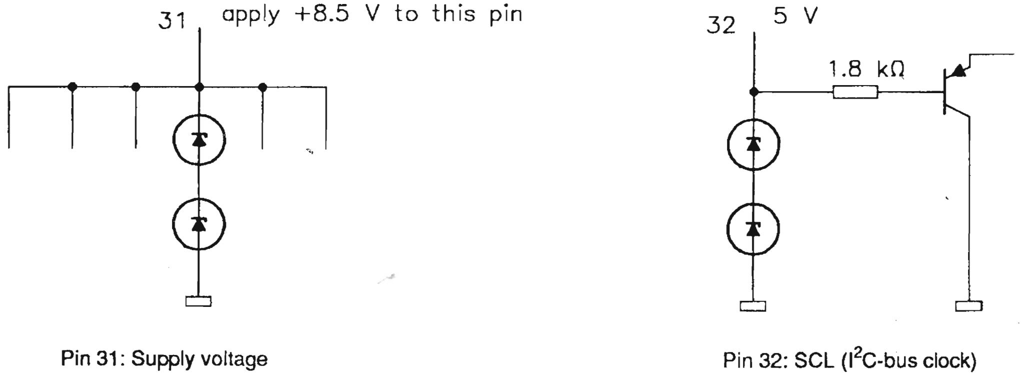


Pin 19: Filtering for supply
Pin 21: Reference voltage

Pin equivalent circuits
V_{CC} = 8.5 V
(All values shown are typical DC values)

MED439

Fig.17(b) Internal circuits (continued from Fig.17(a)).



Pin 31: Supply voltage

Pin 32: SCL (I^2C-bus clock)

Pin equivalent circuits
$V_{CC} = 8.5$ V
(All values shown are typical DC values)

Fig.17(c) Internal circuits (continued from Fig.17(b)).

Data processor for cellular radio (DPROC)

UMA1000LT

FEATURES

- Single chip solution to all the data handling and supervisory functions
- Configuration to both AMPS and TACS
- I²C serial bus control
- All analog interface and filtering functions fully implemented on chip
- Error handling in hardware reduces software requirements
- Robust SAT decoding and transponding circuitry
- Low current consumption
- Small physical size
- Minimum external peripheral components required.

GENERAL DESCRIPTION

The UMA1000LT is a low power CMOS LSI device incorporating the data tranceiving, data processing, and SAT functions (including on-chip filtering) for an AMPS or TACS hand-held portable cellular radio telephone.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage (pin 28)	3.0	5.0	5.5	V
I_{DD}	supply current (pin 28) normal operation with external clock	–	2.5	–	mA
T_{amb}	operating ambient temperature	–30	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UMA1000LT	28	SO28	plastic	SOT136A

The UMA1000T data sheet, also a data processor for cellular radio (DPROC), is available upon request. The UMA1000T has a minimum supply voltage, V_{DD}, of 4.5V; the UMA1000LT has a V_{DD} of 3V. The UMF1000T is pin-for-pin compatible with the UMA1000LT.

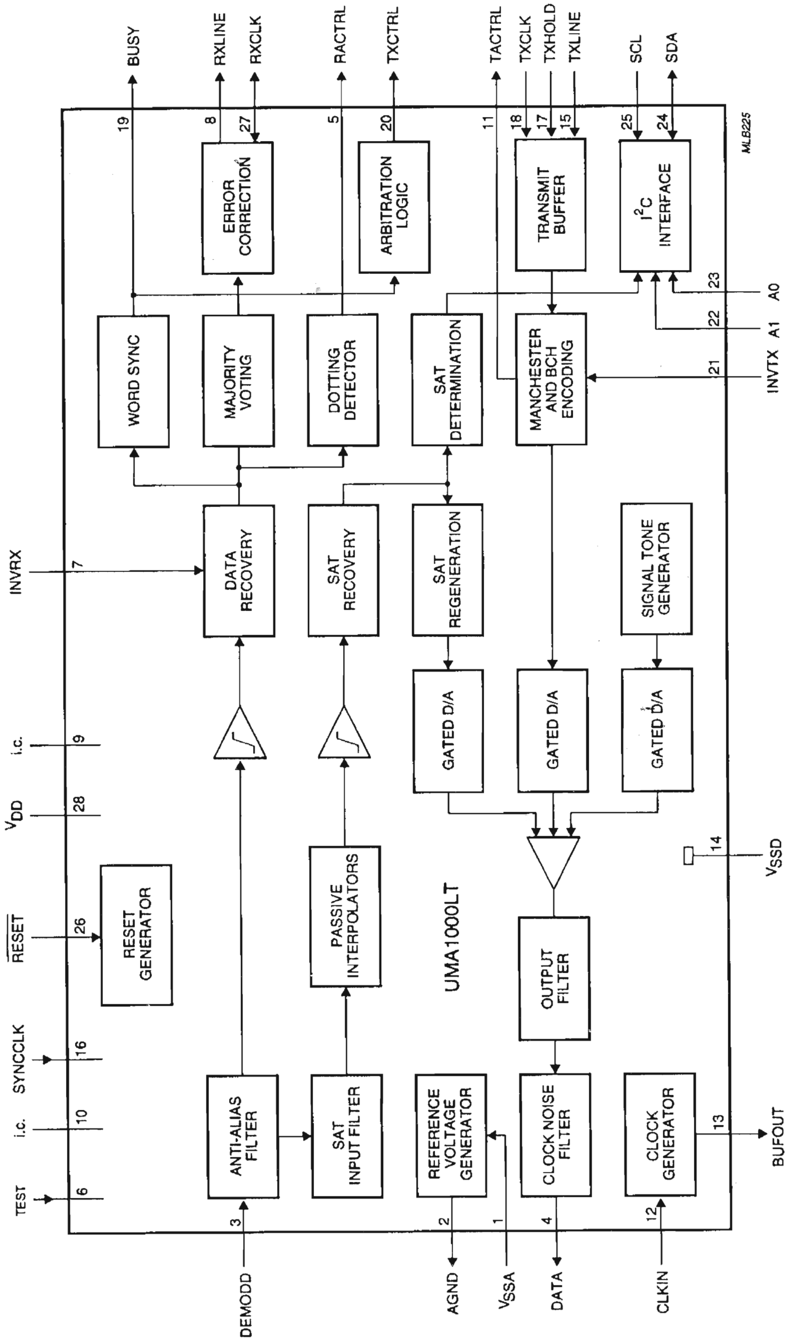


Fig.1 Block diagram.

Data processor for cellular radio (DPROC) UMA1000LT

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSA}	1	analog negative supply (0 V)
AGND	2	$(V_{DD} - V_{SSA})/2$ analog reference ground
DEMODD	3	received data signal input
DATA	4	transmitted data signal output
RACTRL	5	received audio control output
TEST	6	SCAN control input; used for power-on reset
INVRX	7	inverts sense of received data stream
RXLINE	8	received data signal output
i.c	9	internally connected; must be left open-circuit
i.c	10	internally connected; must be left open-circuit
TACTRL	11	transmitter audio control output
CLKIN	12	1.2 MHz external master clock input
BUFOUT	13	buffered output of internal clock oscillator
V_{SSD}	14	digital ground
TXLINE	15	transmitted data signal
SYNCCLK	16	SCAN CLOCK control input; used for power-on reset
TXHOLD	17	holds off transmission of data
TXCLK	18	transmitted data clock input
BUSY	19	reverse control channel status output
TXCTRL	20	transmitter control output
INVTX	21	inverts sense of transmitted data stream
A1	22	address input 1; used for power-on reset (I²C-bus)
A0	23	address input 0 (I²C-bus)
SDA	24	serial data input/output (I²C-bus)
SCL	25	serial clock input (I²C-bus)
$\overline{\text{RESET}}$	26	master reset input
RXCLK	27	received data clock input
V_{DD}	28	supply voltage (+5 V)

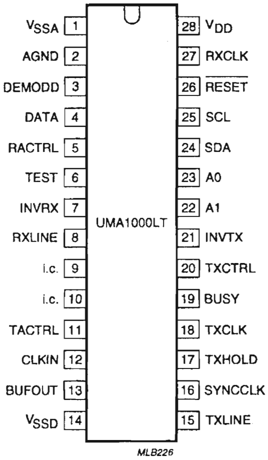


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.8	+8.0	V
I_{DD}	supply current	–	50	mA
I_I	DC current (any input)	–	±10	mA
I_O	DC current (any output)	–	±10	mA
V_I	all input voltages	−0.8	V_{DD}+0.8	V
P_{tot}	total power dissipation	–	300	mW
P_o	power dissipation per output	–	50	mW
T_{amb}	operating ambient temperature	−30	+70	°C
T_{stg}	storage temperature	−65	+150	°C

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = −30 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		3.0	5.0	5.5	V
I_{DD}	supply current	normal operation; note 1	–	2.5	–	mA
Digital inputs (note 2)						
V_{IL}	LOW level input voltage		−0.3	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD}+0.3	V
C_I	input capacitance		–	–	6	pF
Digital outputs (note 2)						
V_{OL}	LOW level output voltage	I_{sink} = 1 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{source} = 1 mA	V_{DD}−0.4	–	–	V
Open-drain outputs (note 3)						
V_{OL}	LOW level output voltage	I_{sink} = 2 mA	–	–	0.4	V
Open-drain SDA						
V_{OL}	LOW level output voltage	I_{sink} = 3 mA	–	–	0.4	V

Notes

1. 1.2 MHz clock on CLKIN, SYNCCLK HIGH, outputs unloaded analog part operating.
2. All digital inputs and outputs of DPROC are compatible with standard CMOS devices and the following general characteristics apply.
3. Open-drain outputs have no internal pull-up resistors.

FUNCTIONAL DESCRIPTION

General

The UMA1000LT (DPROC) is a single-chip CMOS device which handles the data and supervisory functions of an AMPS or TACS subscriber set.

These functions are:

- Data reception and transmission
- Control and voice channel exchanges
- Error detection, correction, decoding and encoding
- Supervisory Audio Tone decoding and transponding
- Signalling Tone generation.

In an AMPS or TACS cellular telephone system, mobile stations communicate with a base over full duplex RF channels. A call is initially set up using one out of a number of dedicated control channels. This establishes a duplex voice connection using a pair of voice channels. Any further transmission of control data occurs on these voice channels by briefly blanking the audio and simultaneously transmitting the data. The data burst is brief and barely noticeable by the user. A data rate of 10 kbits/s is used in the AMPS system and 8 kbits/s in TACS. The signalling formats for both Forward Channels (base to mobile) and Reverse Channels (mobile to base) are shown in Fig.3.

A function known as Supervisory Audio Tone (SAT), a set of 3 audio tones (5970, 6000 and 6030 Hz), is used to indicate the presence of the mobile on the designated voice channel. This signal, which is analogous to the On-Hook signal on land lines, is sent out to the mobile by the base station on the Forward Voice Channel. The signal must be accurately recovered and transponded back to the base station to complete the 'loop'. At the base station this signal is used to ascertain the overall quality of the communication link.

Another voice channel associated signal is Signalling Tone (ST). This tone (8 kHz TACS, 10 kHz AMPS) is generated by the mobile and is sent in conjunction with SAT on the Reverse Voice Channel to serve as an acknowledgement signal to a number of system orders.

The key requirements of a hand-held portable cellular set are:

- Small physical size
- Minimum number of interconnections (serial bus)
- Low power consumption
- Low cost.

The DPROC is a member of our Cellular Radio chip set, based on the I²C-bus, which meets these requirements. A cellular radio system schematic using the chip set is shown in Fig.4.

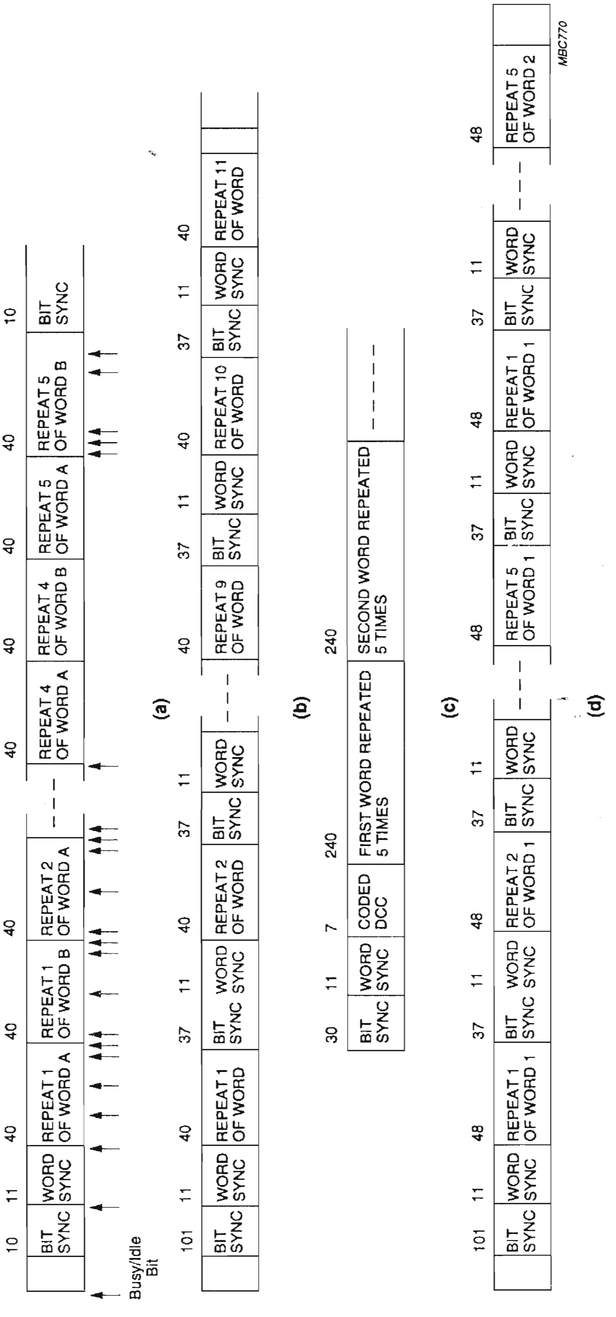


Fig.3 Signalling formats; (a) forward control channel; (b) forward voice channel; (c) reverse control channel; (d) reverse voice channel.

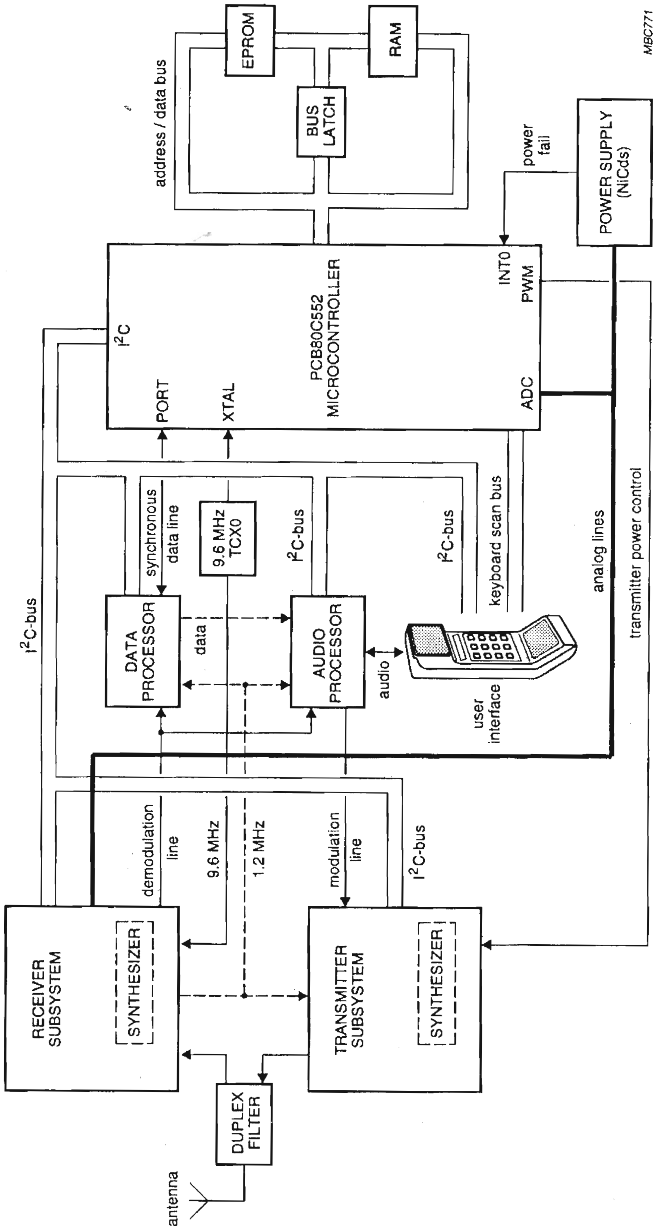


Fig.4 Cellular radio system schematic.

EXTERNAL PIN DESCRIPTION

Supply (V_{DD}; V_{SSA}; V_{SSD}; AGND)

Both V_{SSA} and V_{SSD} must be connected to common ground.

SYMBOL	DESCRIPTION
V_{DD}	positive supply voltage for digital and analog circuitry
V_{SSA}	negative supply voltage for analog circuitry (0 V)
V_{SSD}	digital ground (0 V)
AGND	internally generated reference ground based by internal analog circuitry; voltage level $(V_{DD}-V_{SSA})/2 \pm 2\%$

System clock (CLKIN; BUFOUT)

CLKIN is a digital input for the externally generated 1.2 MHz master clock. This signal should be accurate to 100 x 10^{-6} and have a worst case of 60:40 mark-space ratio. BUFOUT is the buffered output of the clock oscillator and provides the option of generating the clock signal on chip by connecting a 1.2 MHz crystal between BUFOUT and CLKIN.

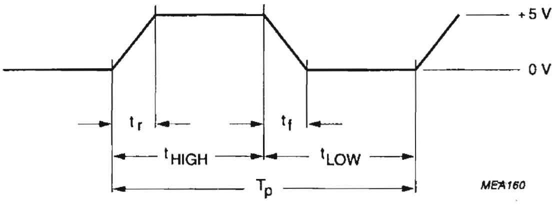


Fig.5 System clock timing diagram.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
T_p	clock period time	833.25	833.33	833.42	ns
t_{HIGH}	HIGH time	40%	50%	60%	T_p
t_{LOW}	LOW time	–	T_p-t_{HIGH}	–	
t_r	rise time	–	50	–	ns
t_f	fall time	–	50	–	ns

I²C serial data link (SDA; SCL)

SDA is the bi-directional data line; SCL the clock input from an I²C master. These constitute a typical I²C link and conform to standard characteristics as defined in the I²C-bus specification.

- Data rate: up to 100 kbits/s

Slave Address Select (A0; A1)

Selection of the device slave address is achieved by connecting A0 to either V_{SSD} or V_{DD} and connecting A1 to either pin 16 and pin 6 or to V_{DD}. The slave address is defined in accordance with the I^2C specifications as shown in Fig.6.

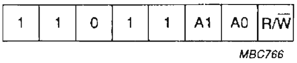


Fig.6 Device slave address.

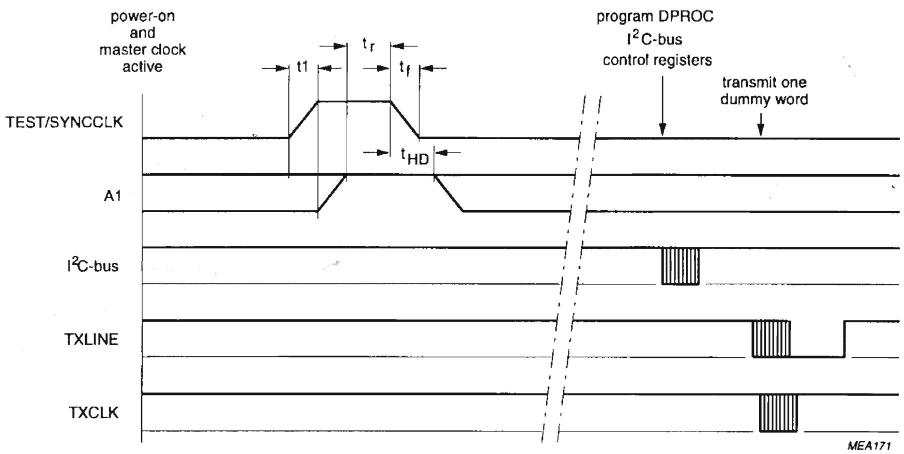
Power-up state

DPROC will not respond reliably to any inputs (including $\overline{\text{RESET}}$) until 100 µs after the power supply has settled within the specified tolerance. The analog sections of the device will have stabilized within 5 ms. No power-on reset is provided, therefore before the device can enter normal operation TEST and SYNCCLK must be pulsed HIGH. The reset pulse on these pins must have a minimum period of 250 µs and the fall time of the negative going edge must be faster than 1 µs. Pin A1 must remain HIGH during this reset period therefore if the A1 bit of the I^2C address is required to be logic 0. A1 may be connected to TEST and SYNCCLK. If it is required to be at logic 1 then A1 may be permanently connected to V_{DD}. If it is required that A0 = logic 1, then a normal master reset (pin 26) sequence must follow the power-on reset sequence to get the internal registers in the defined state.

After the power-on reset a dummy transmission should be made to initiate internal DPROC counters. This transmission should be made with arbitration (ABREN) disabled and the RF transmitter stage switched OFF. Figure 7 shows the power-on reset sequence.

Master reset ($\overline{\text{RESET}}$)

$\overline{\text{RESET}}$ is an asynchronous active LOW master reset input, with a minimum active pulse width of 2 µs which may be used to reset certain logic within DPROC to a predefined state as illustrated in Tables 1 and 2. Alternatively, DPROC may be set into a known initial state be setting the I^2C control register as required. The internal reset sequence after a negative pulse on $\overline{\text{RESET}}$ takes 250 µs.



Where:

t1 = time not critical

t_r = reset time = 250 μs maximum

t_f = pulse fall time = 1 μs maximum

t_{HD} = A1 hold time = 0 μs minimum

Note

The RF transmitter is OFF during reset sequence.

Fig.7 Power-on reset programming sequence.

Table 1 Predefined state of the digital output pins.

OUTPUT	STATE
RXLINE	HIGH
TXCTRL	HIGH
TACTRL	HIGH
RACTRL	HIGH
BUSY	HIGH

Table 2 Predefined state of I^2C registers.

REGISTER	BIT							
	7	6	5	4	3	2	1	0
Control	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
SATD	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
TST	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

Data Transfer Link (RXLINE; TXLINE; TXHOLD; TXCLK and RXCLK)

RXLINE, TXLINE, TXCLK and RXCLK provide a dedicated serial data link for the transfer of system data messages between DPROC and the system controller at variable rates of up to 200 kbits/s.
TXHOLD allows the system controller to preload the DPROC transmit register with one word without the data being transmitted. DPROC then starts transmitting the instant TXHOLD is driven LOW.

- RXCLK: clock input from system controller
- RXLINE: data output from DPROC to system controller
- TXCLK: clock input from system controller
- TXLINE: open drain data bi-directional line to the system controller
- TXHOLD: (HIGH) holds off transmission of data
- Data rate: up to 200 kbits/s

Note

A minimum mean data transfer rate for the received data of 2.1 kbits/s (AMPS) and 1.7 kbits/s (TACS) is required to ensure contiguity of message words.

The format for received and transmitted data words is shown in Fig.15(a) and Fig.15(b) respectively. The receive and transmit data timing is illustrated in Fig.16(a) and Fig.16(b) respectively.

Transmitter Control (TXCTRL)

TXCTRL is an open-drain output used to disable the transmitter during a Reverse Control Channel access failure.

- output level HIGH: RF enable
- output level LOW: RF disable

Transmitter Audio Enable (TACTRL)

TACTRL is an open-drain digital output signal used to blank the audio path and enable the data path to the modulator during data bursts on the Reverse Voice Channel.

- output level HIGH: audio enabled
- output level LOW: audio muted

Receiver Audio Enable (RACTRL)

RACTRL is an open-drain digital output used to blank the audio path to the earpiece when a sequence of dotting and word sync is detected.

RACTRL and TACTRL functions can be combined using one line.

- output level HIGH: audio enabled
- output level LOW: audio muted

Reverse Control Channel Status (BUSY)

BUSY is a digital output giving the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy/Idle bits and has the following logic levels:

- output level HIGH: channel busy
- output level LOW: channel idle

On a voice channel BUSY indicates channel idle.

Invert Receive Data (INVRX)

Enables an additional inverter in the receive data path. This allows RF demodulators with high or low local oscillators to be used. The TACS and AMPS specifications define a NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the demodulated data stream into DPROC depends on the receiver local oscillator.

- input HIGH: data inverted
- input LOW: data normal

Invert Transmit Data (INVTX)

Enables an additional inverter in the transmit data path. This allows RF modulators with high or low local oscillators to be used. The TACS and AMPS specifications define a NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the modulated data stream depends on the transmitter local oscillator.

- input HIGH: data inverted
- input LOW: data normal

Transmitted Data Output (DATA)

Data is an analog output which provides Manchester encoded and filtered data signal SAT and signalling tone. This signal should normally be AC coupled into the Audio/Data summer.

- DC level: analog ground (AGND)
- signal level: $\frac{2}{5}V_{DD}$ V (p-p) for signalling tone; signal level with filtered data signal
- signal tolerance: 2% + supply voltage variation (ΔV_{DD})
- minimum load capacitance: 10 kΩ
- maximum load capacitance: 2 nF
- maximum output impedance: 50 Ω

Received Data Input (DEMODD)

Demodd inputs analog data and SAT signals from the RF demodulator. This pin should normally be AC coupled.

- DC level: analog ground (AGND)
- maximum data level: $\frac{V_{DD}}{5}$ x 1 V (p-p)
- nominal data level: $\frac{V_{DD}}{5}$ x 250 mV (p-p)
- minimum data level: $\frac{V_{DD}}{5}$ x 200 mV (p-p)
- minimum SAT level: 50 mV (p-p)
- input impedance: min. 1 MΩ

CHARACTERISTICS OF THE I^{2}C-BUS

The I^{2}C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig.12.

Where:

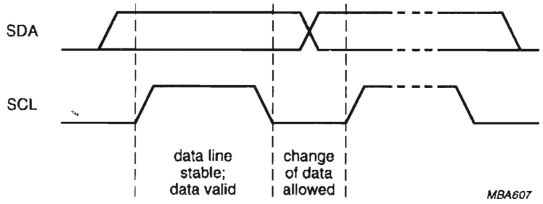


Fig.8 Bit transfer.

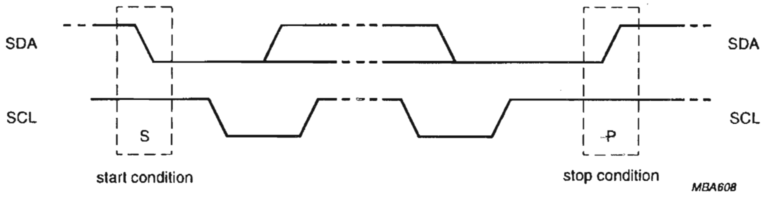


Fig.9 Definition of start and stop conditions.

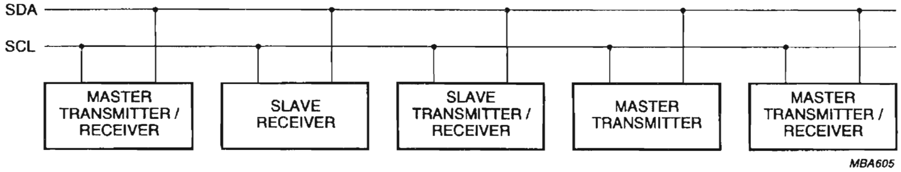


Fig.10 System configuration.

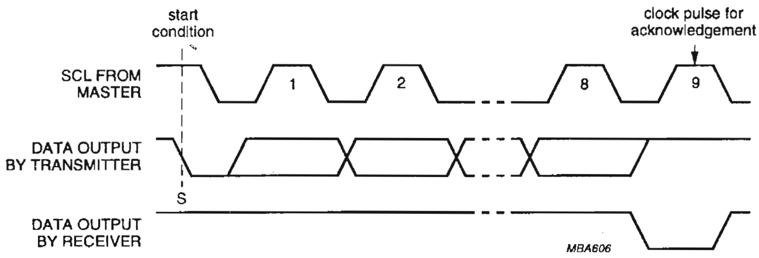
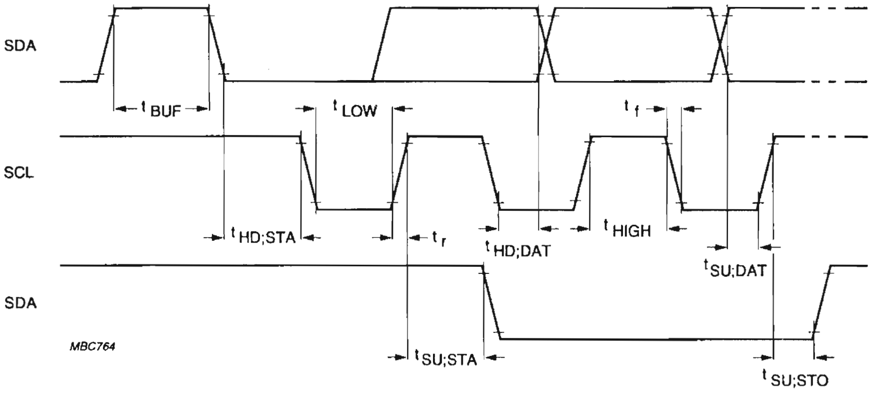
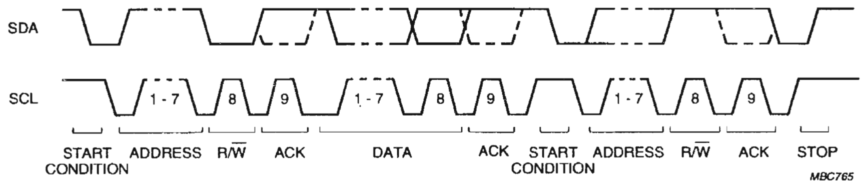


Fig.11 Acknowledgement on the I²C-bus.



All the values refer to 10% and 90% levels with a voltage swing of V_{DD} to V_{SS}.

SYMBOL	TIMING	DESCRIPTION
t_{BUF}	$t \geq t_{LOW(min)}$	the minimum time the bus must be free before a new transmission can start
$t_{HD;\ STA}$	$t \geq t_{HIGH(min)}$	start condition hold time
$t_{LOW(min)}$	4.7 µs	clock LOW period
$t_{HIGH(min)}$	4 µs	clock HIGH period
$t_{SU;\ STA}$	$t \geq t_{LOW(min)}$	start condition set-up time, only valid for repeated start code
$t_{HD;\ DAT}$	$t \geq 0$ µs	data hold time
$t_{SU;\ DAT}$	$t \geq 250$ ns	data set-up time
t_r	$t \leq 1$ µs	rise time of both the SDA and SCL line
t_f	$t \leq 300$ ns	fall time of both the SDA and SCL line
$t_{SU;\ STO}$	$t \geq t_{LOW(min)}$	stop condition set-up time



Where:

Clock $t_{LOW(min)}$: 4.7 µs

Clock $t_{HIGH(min)}$: 4 µs

The dashed line is the acknowledgement of the receiver

Maximum number of bytes: unrestricted

Premature termination of transfer: allowed by generation of STOP condition

Acknowledge clock bit: must be provided by the master.

Fig.13 Complete data transfer.

I²C REGISTERS

General

The I²C register block resides internally within the I²C interface block and contains various items of status and control information which are transferred to and from DPROC via the I²C-bus. The block is organized into four 8-bit registers:

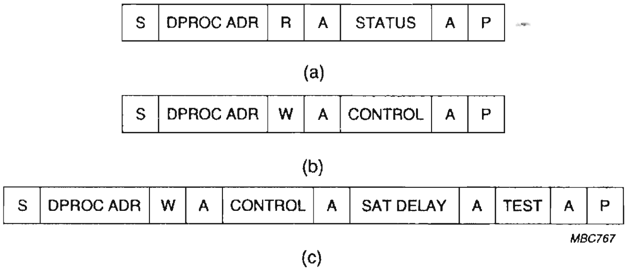
- Status Register: contain read only items
- Control Register: contain write only items
- SAT Programmable Phase Shift Register: contain write only items
- TEST Register

Note

In normal operation the SAT delay register and the TEST register require programming only after a device reset.

Table 3 Register map.

REGISTER	BIT							
	7	6	5	4	3	2	1	0
Status	–	–	WYNSC	BUSY	TXABRT	TXIP	MSCC1	MSCC0
Control	–	SERV	STS	TXRST	ABREN	FVC	STEN	SATEN
SATD	<------------------SAT delay data------------------>							



Where:

S: START condition

W: read/write bit (logic 0 = write)

R: read/write bit (logic 1 = read)

A: acknowledge bit

P: STOP condition

DPROC ADR: slave address of DPROC

TEST: must be programmed to logic 0 for normal operation.

Fig.14 I²C data format; (a) read from DPROC status register; (b) write to DPROC control register; (c) write to all DPROC registers.

Status Register

This is read only register containing DPROC status information.

MEASURED SAT COLOUR CODE (MSCC1; MSCC0)

MSCC1 and MSCC0 provide information about the current measured SAT colour code in accordance with Table 4.

Table 4 Measured SAT colour code.

MSCC1	MSCC0	SAT frequency (Hz)
0	0	5970
0	1	6000
1	0	6030
1	1	no valid SAT

TRANSMISSION IN PROGRESS (TXIP)

TXIP indicates whether DPROC is currently accessing the Reverse Control or Voice Channels.

- logic 1: data transmission in progress
- logic 0: transmission not in progress

TRANSMISSION ABORT STATUS (TXABRT)

TXABRT indicates that a Reverse Control Channel Access Attempt has been aborted by DPROC without successful message transmission.

- logic 1: transmission attempt aborted
- logic 0: no access collision detected

REVERSE CONTROL CHANNEL STATUS (BUSY)

BUSY gives the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy/Idle bits on the Forward Control Channel.

- logic 1: channel busy
- logic 0: channel idle

On a voice channel the BUSY bit defaults to the set state.

Note

This signal is also routed to the BUSY output pin.

WORD SYNCHRONIZATION INDICATOR (WSYNC)

WSYNC indicates whether DPROC has acquired frame synchronization according to the Forward Control Channel format.

- logic 1: frame synchronization acquired
- logic 0: no frame synchronization

Control Register

This is a write only register containing DPROC control information.

SAT PATH ENABLE (SATEN)

SATEN enables the SAT transponded signal to be output on external pin DATA.

- logic 1: SAT tone enabled
- logic 0: SAT tone inhibited

SIGNALLING TONE (ST) PATH ENABLE (STEN)

STEN enables the Signalling Tone to be output on external pin DATA.

- logic 1: ST enabled
- logic 0: ST inhibited

CHANNEL FORMAT SELECT (FVC)

FVC selects the required channel format.

- logic 1: voice channel format
- logic 0: control channel format

TRANSMISSION ABORT PERMISSION (ABREN)

ABREN indicates whether DPROC has permission to abort data transmission and disable RF on the Reverse Control Channel following the detection of a channel access attempt collision.

- logic 1: RF disable allowed
- logic 0: RF disable inhibited

MESSAGE TRANSMISSION ABORT (TXRST)

TXRST terminates a message being transmitted on the reverse channel. It is a monostable signal which when activated causes a reset of the message transmission circuitry and causes TXABRT and TXIP I²C signals to be reset.

This signal does not clear the DPROC transmit register; therefore if a word has been loaded into DPROC after a TXABRT has occured the control line TXHOLD should be held LOW to allow the word to be cleared from the DPROC input register.

- logic 1: reset active
- logic 0: reset inactive

SYSTEM TYPE SELECT (STS)

STS selects required system format.

- logic 1: AMPS
- logic 0: TACS

Note

Toggling this signal also resets the receive logic in DPROC.

SERVING SYSTEM SELECT (SERV)

SERV selects which of the serving system data streams (A or B) is accepted.

- logic 1: system A selected
- logic 0: system B selected

SAT PROGRAMMABLE DELAY REGISTER (SATD)

SATD programs the value of phase shift which is applied to the SAT tones in the SAT Regeneration Block. This value will be determined and programmed into the System Controller during manufacture. The recovered SAT is delayed in time by approximately 0.8 µs x value in the register which corresponds to approximately 1.8 degrees x value in the register. The total phase shift is limited to 360 degrees.

The ability to adjust SAT phase angle is not necessary in current AMPS and TACS systems. Therefore this register should normally be in AMPS and TACS, this function is not necessary and should programmed to zero.

DIGITAL CIRCUIT BLOCKS

General

The majority of the digital circuitry within the DPROC device is identical for both AMPS and TACS. The device has little additional redundancy to implement both systems. The functions of these blocks are described in the following sections and relate to those shown in Fig.1.

Data Recovery

The Data Recovery Block receives wideband Manchester encoded data in sampled and sliced form from the Strobed Comparator Block, on which it performs the following functions:

- clock recovery
- Manchester decoding
- data regeneration

The Clock Recovery Block extracts an 8 or 10 kHz (TACS or AMPS) phase-locked clock signal from the Manchester encoded data stream. This is implemented using a digital-phase-locked-loop (PLL) which has an adjustable 'bandwidth' to provide both fast acquisition and low jitter.

Manchester decoding is performed by exclusive ORing the recovered Manchester encoded data with the recovered clock.

The NRZ data regeneration is performed by a digital integrate and dump circuit. This consists of an up/down counter that counts 1.2 MHz cycles during the data period. The sense of the count is determined by the result of the Manchester Decoder output. The number of counts is sampled at the end of a data period. If this number exceeds a threshold the data is latched as a 1 otherwise it is latched as a 0.

SAT Processing

The Supervisory Audio Tone processing consists of the following functions:

- SAT recovery
- SAT determination
- SAT regeneration

SAT RECOVERY

The SAT Recovery Block receives a filtered and sliced SAT signal which must be recovered before being routed to the Determination and Regeneration Blocks.
The recovery is performed using a digital phase-locked-loop.

SAT DETERMINATION

The SAT Determination Block indicates which, if any, of the valid SAT tones is detected from the recovered SAT. The AMPS and TACS specifications require that a determination is made at least every 250 ms. Determination involves counting the number of cycles of the regenerated SAT in this time period. This count is then compared to a set of four known counts which define the boundaries between the SAT frequencies and the SAT not valid events. The result is then coded into the I^{2}C status registers MSCC0 and MSCC1 as shown in Table 5.

SAT REGENERATION

The SAT Regeneration Block generates a digital SAT stream from the recovered SAT stream for transponding back to the base station. The AMPS and TACS specifications require the SAT to be transponded with a maximum phase shift of 20 degrees between the point the modulated RF signal enters the mobile from the base station, and the point the modulated RF leaves the mobile. A variable phase compensation circuit is provided in DPROC to shift the recovered SAT through 0 to 360 degrees before being passed to the output summing network. The degree of phase shift is determined during manufacture of the set and the required additional phase shift is stored in non-volatile RAM and programmed via I^{2}C at each power-on cycle. The phase correction is performed by a counter delay method using signals which are phase locked to the recovered SAT.

Dotting Detector

The Dotting Detector Block determines whether a data inversion (dotting) pattern has been received on the Forward Voice Channel. The detection of 32 bits of data inversion indicates that the Clock Recovery Block has acquired bit synchronization and that the narrow bandwidth mode on the clock recovery phase-locked-loop is selected. This signal is also used to indicate that a data burst is expected and activates the audio mute RACTRL, after a Word Synchronization Block has been received, for the duration of the burst.

Table 5 Status registers MSCC0, MSCC1; decoded SAT frequencies.

REGISTER		SAT frequency band (Hz ±2 Hz)	decoded SAT (Hz)
MSCC0	MSCC1		
1	1	max. 5956	not valid
0	0	5956 to 5986	5970
0	1	5986 to 6014	6000
1	0	6014 to 6046	6030
1	1	min. 6046	not valid

Word Synchronization Detector

The Word Synchronization Block performs the following functions:

- Frame Synchronization
- Reverse Control Channel status (B/I determination)
- Valid Serving System determination

These functions are associated solely with the Forward Control Channel and have no meaning on the Forward Voice Channel.

Information in a data stream is identified by its position with respect to a unique synchronization word. This synchronization word is an 11-bit Barker code which has a low probability of simulation in an error environment, and can be easily detected. Data received is only considered valid at times when DPROC has achieved frame synchronization. In this condition the block leaves its search mode and enters its lock mode. This is indicated by bit WSYNC being set HIGH. In order to achieve this two consecutive synchronization words separated by 463 bits must be detected. Once in lock mode, the synchronization word detector is examined every 463 bits and only loses frame synchronization after 5 consecutive unsuccessful attempts at detecting the synchronization word have been made. At this point bit WSYNC is cleared and the device is returned to its search mode. On the Forward Voice Channel detection of the synchronization word indicates that the following 40 bits are valid data. Information detailing the status of the Reverse Control Channel is given by the Busy/Idle bits. These occur at intervals of 11 bits within the frame, the first occurring immediately following the synchronization word. The status of the channel is determined by a majority decision on the last three consecutive Busy/Idle bits.

Majority Voting Block

The Majority Voting Block performs the following functions:

- identifying position and validity of frames in the received data stream
- extracting five repeats of each word from a valid frame
- performing a bit-wise majority decision on the five repeats of the data word.

The validity of the frames is determined by setting a counter in operation which times out and resets the circuitry after 920 or 463 bit periods from detecting valid word synchronization. The time out period selected depends on whether DPROC is monitoring the Forward Voice or Control Channel respectively.

Up to five repeats of the message word are searched for and extracted by DPROC. On the forward Voice Channel DPROC will extract the first five words that occur for which a correct synchronization word is found. These words can occur in any position in the frame. A serial majority vote is performed as the fifth word is being extracted.

Error Correction Block

The Error Correction Block performs the following functions:

- extraction of a valid message from the Majority-Voted Word
- computation of the S1 and S3 syndromes
- correction of up to one error in the word
- communication of received data to the System Controller via the Received Data Serial Link.

Interpretation of parity of a received word is obtained from knowledge of the syndromes of the word. The syndromes are calculated using feedback shift registers with two characteristic equations:

$1 + X + X^6$ and $1 + X + X^2 + X^4 + X^6$

Once the syndromes of a received word are known, it is possible to determine if a correctable error is present. DPROC only corrects up to one error although the code used has a Hamming distance of five. The occurence of two or more errors is signalled by setting the BCH error flag, which is communicated to the System Controller via the Received Data Serial Link.

Received Data Serial Link

The Received Data Serial Link transfers data and control information from DPROC to the System Controller. The data is transferred on RXLINE under control of a clock signal RXCLK, generated by the System Controller. The system controller is informed of the arrival of a decoded data word in the DPROC output register by RXLINE being driven LOW. If the system controller chooses to ignore the received data or only partially clock the data out, the DPROC will reset the receive buffer for the next word after the period RWIN (see Fig.16).

DATA FORMAT

Each Received Data word consists of 4 bytes. The word format is shown in Fig.15(a). The sense and function of the fields is shown in Table 6.

LINK PROTOCOL

The Received Data protocol is described by the timing diagram Fig.16(a) and has the following parameters:

- maximum receive window (RWIN)
  Control Channel (TACS) = 47 ms
  Control Channel (AMPS) = 37 ms
- minimum clock period ($t_{CLK(min)}$) = 2 µs
- minimum clock hold-off (t_{WAIT}) = 100 µs

Transmit Data Serial Interface

The Transmit Data Serial Link performs reception of data from the System Controller to DPROC over a dedicated line TXLINE. The transfer of data is synchronous with a clock signal TXCLK, generated by the System Controller.

DATA FORMAT

Each Transmit Data word consists of 5 bytes. The word format is shown in Fig.15(b). The sense and function of the fields is shown in Table 7.

LINK PROTOCOL

Messages are normally up to 5 words in length on the Reverse Control Channel and up to 2 words in length on the Reverse Voice Channel. However, DPROC will transmit messages of any word length. These must be transmitted on the data stream without interruption. To avoid the need for large buffer areas, a flexible protocol is used to allow DPROC to control the transfer of data words. DPROC has an on-chip buffer which can hold one complete word of a message. While new words are being loaded into DPROC, within the time period Buffer clear to end of TWIN, DPROC will maintain uninterrupted data transmission. The System Controller can abort the transmission of a message at any point activating the I²C signal TXRST. This signal causes the interface to return to its power-up state and resets TXIP and TXABRT (see Table 3). On completion of these tasks TXRST will return to its inactive state. The Transmit Data Protocol is described by the timing diagram shown in Fig.16(b) and has the following parameters:

- maximum transmit window (TWIN)
  voice channel (TACS) = 60 ms
  voice channel (AMPS) = 48 ms
  control channel (TACS) = 29 ms
  control channel (AMPS) = 23 ms
- minimum clock period ($t_{CLK(min)}$) = 2 µs

Table 6 Received Data word.

BIT	TITLE	SENSE	FUNCTION
31	start	LOW	identifies start of word
30	BCH error	active HIGH	indicates that an uncorrected BCH error is associated with the word
29 to 2	received data	binary data	received data word
1	RXLINE error	LOW	if detected as HIGH indicates that a transmission error has occured on the microprocessor to DPROC serial link
0	stop	HIGH	identifies end of the word

Table 7 Transmit data word.

BIT	TITLE	SENSE	FUNCTION
39	start	LOW	identifies start of word
38, 37	DCC	binary data	digital colour code
36 to 1	transmit data	binary data	transmit data word
0	stop	HIGH	identifies end of the word

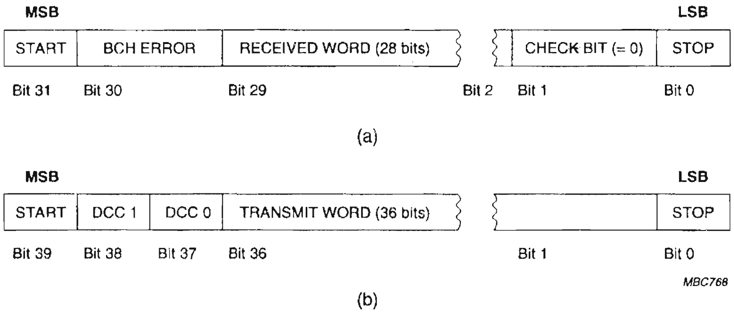
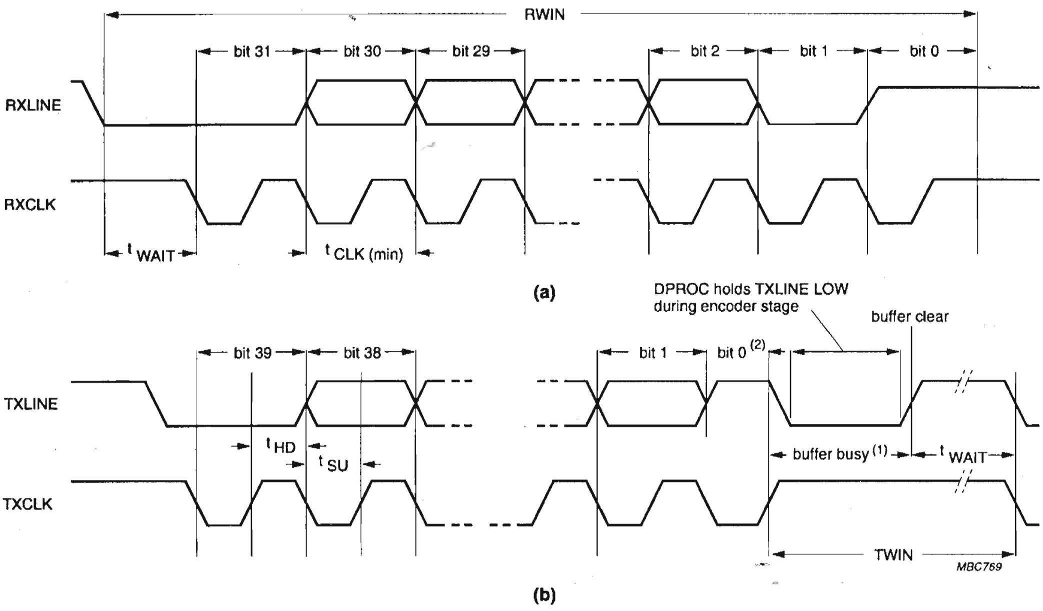


Fig.15 Data word formats; (a) received data word; (b) transmit data word.



Where:

t_{HD} = 100 ns minimum

t_{SU} = 0 ns minimum

t_{WAIT} = 0 ns minimum

(1) The buffer busy time depends on whether the first or subsequent words are being loaded.

(2) The system controller should monitor the TXLINE during bit 0, if the status of TXLINE does not change from a HIGH to a LOW on the rising edge of TXCLK, then a framing error has occured. This can be caused by glitches on the clock line or if an arbitration error occured while the DPROC transmit register was being loaded. The system controller should recover the situation by holding TXLINE HIGH and supplying clocks on TXCLK until TXLINE goes LOW. Then the situation should be treated as a normal channel arbitration failure as described in **Reverse Control Channel Access Arbitration** - Abort Procedure.

Fig.16 Data timing diagrams; (a) DPROC to microcontroller link; receive data timing; (b) microcontroller to DPROC link; transmit data timing.

BCH and Manchester Encoding Block

The functions performed by this circuit block include:

- reception of data from the System Controller
- parity generation
- message construction
- Manchester encoding

Each 36-bit Information Word sent on the Reverse Voice and Control Channels is coded into a 48-bit code word. The code word consists of the 36-bit word followed by 12 parity bits. These parity bits are formed by clocking the information word into a 12-bit feedback shift register with characteristic equation:

$1 + X^3 + X^4 + X^5 + X^8 + X^{10} + X^{12}$

The BCH Encoder Block constructs the Reverse Voice and Control Channel data streams from the information it receives from the System Controller.
The streams are formed out of the four possible field types:

- Dotting (data inversions)
- 11-bit Synchronization Word
- Digital Colour Code
- 48-bit code word

The 2 bits of DCC received from the System Controller are coded into a 7-bit word as shown in Table 8.

The data sense for Manchester Encoding has a NRZ logic 1 encoded as a 0-to-1 transition and a NRZ logic 0 encoded as a 1-to-0 transition.

Reverse Control Channel Access Arbitration

The AMPS and TACS specifications require a method of arbitration on the Reverse Control Channel to prevent two mobiles from transmitting on the same channel at the same time. This function is performed by DPROC monitoring the Busy/Idle stream sent on the Forward Control Channel.

The AMPS and TACS specifications state that once the mobile has commenced transmitting on the Reverse Control Channel it must monitor the Busy/Idle stream. If this stream becomes active outside a predetermined 'window', measured from the start of the transmission of the message, the mobile must terminate its transmission and disable the transmitter immediately.

In the Cellular Radio chip-set there are two levels of control of the RF transmitter; the first is absolute control by the System Controller, the second is conditional by other devices in the set. In DPROC the conditional control of the transmitter is performed via the output TXCTRL. This line is effectively wired ANDed together, using open-drain outputs, with other devices which may wish to control the transmitter. When these devices do not wish to disable the transmitter their output is in a HIGH impedance state.

An exception to this procedure occurs when the Serving System instructs the mobile not to monitor the Busy/Idle bits. In this event the arbitration logic can be disabled by clearing I²C register bit ABREN.

The flow of events during a Control Channel Access attempt is as follows:

INITIAL STATE

- transmitter power off via I²C
- DPROC transmit circuitry in power-up state
- TXCTRL line HIGH

ACCESS ATTEMPT PROCEDURE

1. System Controller decides to send message (see **Note to the Access Attempt Procedure**).
2. System Controller drives TXCTRL LOW directly.
3. System Controller switches transmitter power-on and waits for power-up for the transmitter module (RF transmitter is still disabled by TXCTRL).
4. System Controller sets TXRST via I²C to DPROC.
5. System Controller sets ABREN via I²C (if required) allowing DPROC to control the transmitter.
6. System Controller determines status of Reverse Control Channel by monitoring the Busy/Idle bit. If busy, waits a random time then tries again.
7. System Controller releases TXCTRL allowing it to be pulled HIGH enabling the transmitter output.
8. System Controller transfers the first word of the message to DPROC via serial link (see **Note to the Access Attempt Procedure**).
9. DPROC sets I²C signal TXIP and starts sending message while monitoring Busy/Idle status.
10. If channel becomes busy before 56 bits and ABREN is set then perform Abort Procedure.
11. If channel remains idle after 104 bits and ABREN is set then perform Abort Procedure.
12. System controller loads the subsequent words of the message into DPROC when the buffer becomes clear (Fig.16b).

13. On completion of entire message DRPCO clears TXIP and 25 ms later the System Controller disables transmitter via I²C.
14. System Controller finally sends TXRST to prepare DPROC for next transmission.

Note to the Access Attempt Procedure

At stage 1 the system controller may choose to preload DPROC with the first word of the message and hold it from transmission until stage 7 using the TXHOLD line. This gives a lower time overhead between detecting an IDLE channel and commencing the transmission. To use this feature TXHOLD must be driven HIGH before the last bit of data has been transferred into DPROC. Figure 17 illustrates the DPROC data transmission timing.

ABORT PROCEDURE (SEE FIG.18)

1. DPROC immediately disables transmitter output by driving TXCTRL LOW.
2. DPROC sets TXABRT.
3. System Controller detects failure by monitoring TXCTRL and TXABRT.
4. System Controller disables transmitter via RF power amplifier.
5. System Controller sends TXRST to prepare DPROC for next transmission.

Note to the Abort Procedure

If a message is loaded into DPROC after a TXABRT has occured this word will remain in the DPROC transmit register and will not be cleared to TXRST.

If this situation arises the method of clearing the buffer ready for a second access attempt is to leave TXHOLD LOW and then send a TXRST prior to setting up a new transmission after TXLINE goes HIGH; this will clear any residual data in the buffer.

Signal Tone Generation (ST)

The 8 or 10 kHz (TACS or AMPS) tone generated from the Manchester Encoding Block is used as the Signalling Tone stream.

ANALOG CIRCUIT BLOCKS

General

The analog signal processing functions on DPROC are implemented using switched-capacitor techniques. The main filtering functions are operated at 300 kHz, and these circuits are 'interfaced' to the continuous time and sampled digital domains by distributed RC active filters, passive interpolators and comparators.

The distributed RC sections, the Anti-Alias Filter and the Clock Noise Filter, are non-critical and are designed to tolerate process spreads. The critical filtering in the SAT Filter and the Output Filter, is performed by 300 kHz switched-capacitor circuitry. The Passive Interpolators increase the sampling rate from 300 kHz to 1.2 MHz. The sampled analog signals from the Passive Interpolators are converted to sampled 2-state digital signals by the Strobed Comparators. The Gated Digital-to-Analog converters and Analog Summer blocks perform resynchronization and sub-sampling of the digitally generated DPROC output signals, and conversion to the sampled analog domain.

These analog section of the device are shown in Fig.1.

Reference Voltage Generator

The Reference Voltage Generator generates the analog ground reference voltage (AGND) used internally within the DPROC device. To minimize noise AGND must be externally decoupled to VSSA as shown in Fig.19.

Anti-Alias Filter

The Anti-Alias Filter is placed before the SAT sampling block to prevent any unwanted signals or high-frequency noise present on the DEMODD pin being aliased into the pass-band by the sampling action of the switched-capacitor filter. To achieve this the Anti-Alias Filter is a continuous time-distributed RC-active low-pass filter.

Table 8 Digital Colour Code; 7-bit word.

DCC1	DCC0	Coded DCC						
0	0	0	0	0	0	0	0	0
0	1	0	0	1	1	1	1	1
1	0	1	1	0	0	0	1	1
1	1	1	1	1	1	1	0	0
		DCC1		DCC0			DCC1.EXOR.DCC0	

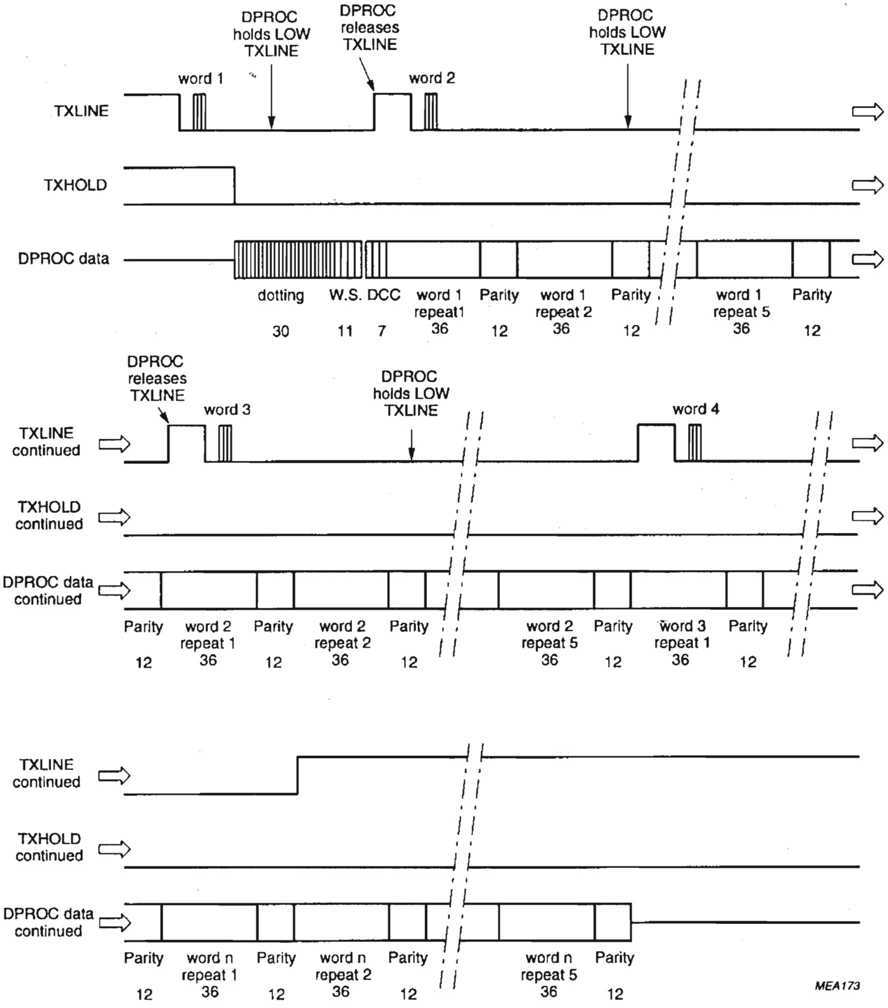


Fig.17 DPROC data transmission timing/microcontroller interface.

SAT Input Filter

The SAT Input Filter is a switched-capacitor filter which provides band-pass filtering of the SAT signals from the DEMODD pin to improve the SAT signal-to-noise ratio prior to recovery and transponding.

Passive Interpolator

The function of the Passive Interpolator is to increase the sampling rate at the output of the switched-capacitor filters. This reduces the coarseness of the zero-crossing information which would otherwise cause unacceptable isochronous distortion in the recovered signal.

Strobed Comparators

The Strobed Comparators form the analog-to-digital interface for the received data and SAT signals from the DEMODD pin. These comparators act as limiting amplifiers which convert the filtered sampled analog signals into 2-state sampled digital signals containing only the zero-crossing information from the analog signal.

Gated Digital-to-Analog and Analog Summer

The Gated Digital-to-Analog converters and Analog Summer form the interface between the digital and analog circuitry on the transmit path of DPROC. It is at this point that the three sampled digital signals, containing SAT, ST and encoded digital data, are combined to form a composite signal.

The data streams are enabled by the I²C signals STEN, SATEN and the internal signal DATAEN respectively (DATAEN disables SAT and ST when data is being transmitted). The digital-to-analog conversion and sub-sampling operation is performed by the Gated Digital-to-Analog converters and Analog Summer. The relative signal weights applied in the summer (with respect to the data path) are shown in Table 9.

Output Filter

The Output Filter is a switched-capacitor filter which performs band-limiting of the DPROC output signals in accordance with the AMPS and TACS specifications. The required below band roll-off is achieved via external AC coupling from the DATA pin.

Clock Noise Filter

The filter is a non-critical continuous time-distributed RC-active low-pass filter used to remove any switching transient residues from the output signal.

Table 9 Relative signal weights.

SIGNAL	RELATIVE OUTPUT LEVEL AMPS AND TACS
ST	1.0
SAT	0.25
DATA	1.0

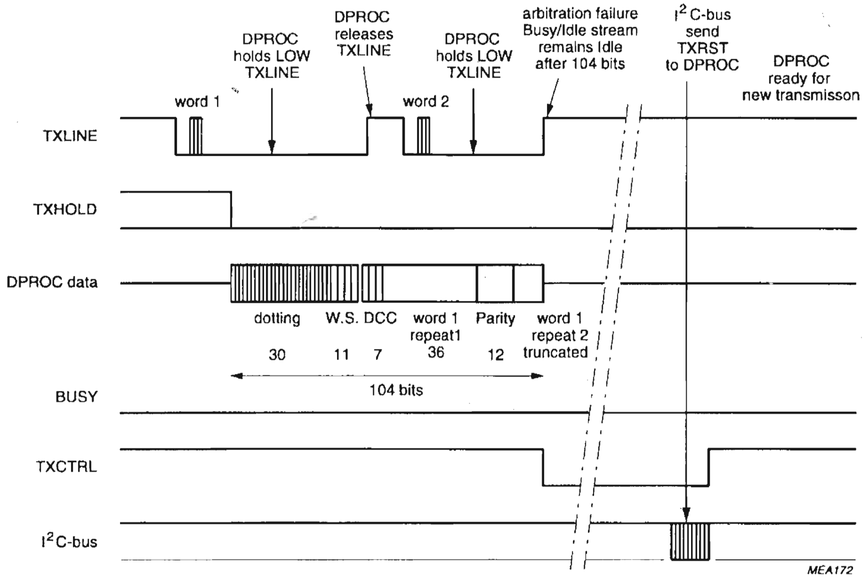


Fig.18 DPROC data transmission timing/microcontroller interface during arbitration failure.

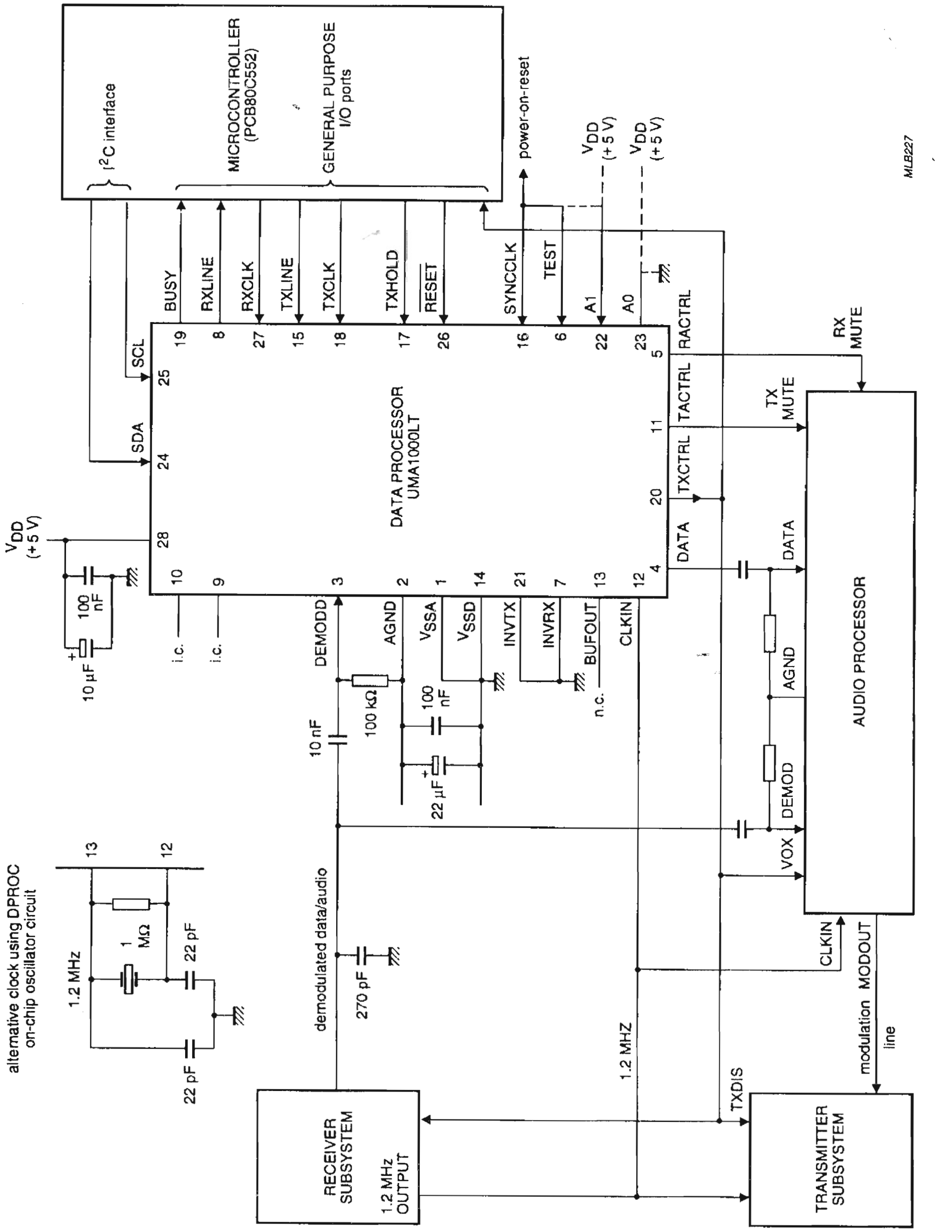


Fig.19 DPROC application circuit.

Section 8
Compandors

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RF Communications

The Philips Family of High Performance Compandors

	Vcc	Icc	Pins	Packages	ALC Voltage	Reference Gain	Unity Down	Power Features	Key	Applications
NE/SA570	6-24V	3.2mA	16	D, F, N	Both Channels	Fixed 1.8V	775mVrms	NO	-Excellent Unity Gain Tracking Error -Excellent THD	High Performance Audio Circuits "Hi-Fi Commercial Quality"
NE/SA571	6-18V	3.2mA	16	D, F, N	Both Channels	Fixed 1.8V	775mVrms	NO	-Excellent Unity Gain Tracking Error -Excellent THD	High Performance Audio Circuits "Hi-Fi Commercial Quality"
NE/SA572	6-22V	6mA	16	D, F, N	Both Channels	Fixed 2.5V	100mVrms	NO	-Independent Attack & Release Time -Good THD -Needs an Ext Summing Op Amp	High Performance Audio Circuits "Hi-Fi Studio Quality"
NE/SA575	3-7V	3-5.5mA*	20	D, DK, N	Right Channels	Vcc/2	100mVrms	NO	-2 Uncommitted On-Chip Op Amps Available -Low Voltage	Consumer Audio Audio Circuits "Commercial Quality"
NE/SA576	2-7V	1-3mA*	14	D, N	Right Channels	Vcc/2	100mVrms	NO	-Low Power -Low External Component Count	Battery Powered Systems "Commercial Quality"
NE/SA577	2-7V	1-2mA*	14	D, N	Right Channels	Vcc/2	10mV to 1V(rms)	NO	-Low Power -Programmable Unity Gain	Battery Powered Systems "Commercial Quality"
NE/SA578	2-7V	1-2mA*	16	D, N	Right	Vcc/2 Channel	10mV to 1V(rms)	YES (170uA)	-Low Power -Programmable Unity Gain -Power Down -Mute Function Summing Capability (DTMF) -600Ω Drive Capability	Battery Powered Systems "Commercial Quality"

NOTE: NE/SA5750/5751 & SA5752/5753are also Excellent Audio Processor Components for High Performance Cordless and Cellular Applications that include the Companding Function

* Icc varies with VCC

Packages include: NE: 0 to +70 C; SA: -40 to +85 C; N: Plastic DIP; D: Plastic SO; F: Cer DIP; DK: SSOP (Shrink Small Outline Package)

Applications include: Cordless Phones, Cellular Phones, Wireless Mics, Modems, Consumer Audio, and Two-way Communications

Compandor NE570/571/SA571

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full-wave rectifier to detect the average value of the signal, a linerarized temperature-compensated variable gain cell, and an operational amplifier.

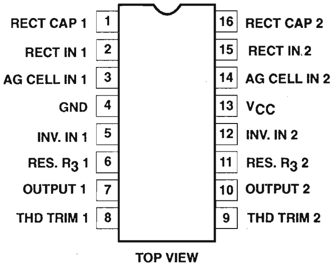
The NE570/571 is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio systems.

FEATURES

- Complete compressor and expandor in one IChip
- Temperature compensated
- Greater than 110dB dynamic range
- Operates down to 6VDC
- System levels adjustable with external components
- Distortion may be trimmed out
- Dynamic noise reduction systems
- Voltage-controlled amplifier

PIN CONFIGURATION

D, F, and N Packages[1]



NOTE:
1. SOL - Released in Large SO Package Only.

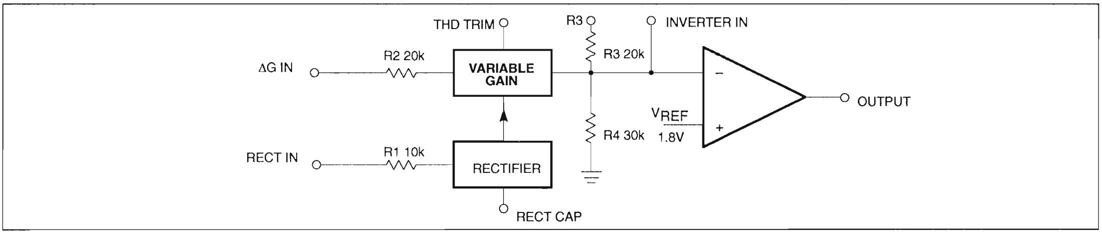
APPLICATIONS

- Cellular radio
- Telephone trunk compandor—570
- Telephone subscriber compandor—571
- High level limiter
- Low level expandor—noise gate
- Dynamic filters
- CD Player

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline Large (SOL)	0 to +70°C	NE570D	0171B
16-Pin Ceramic Dual In-Line Package (Cerdip)	0 to +70°C	NE570F	0582B
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE570N	0406C
16-Pin Plastic Small Outline Large (SOL)	0 to +70°C	NE571D	0171B
16-Pin Ceramic Dual In-Line Package (Cerdip)	0 to +70°C	NE571F	0582B
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE571N	0406C
16-Pin Plastic Small Outline Large (SOL)	-40 to +85°C	SA571D	0171B
16-Pin Ceramic Dual In-Line Package (Cerdip)	-40 to +85°C	SA571F	0582B
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA571N	0406C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Maximum operating voltage 570 571	 24 18	VDC
T_A	Operating ambient temperature range NE SA	 0 to 70 -40 to +85	°C
P_D	Power dissipation	400	mW

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = +6V$, $T_A = 25°C$; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			LIMITS			UNITS
			NE570			NE/SA571[5]			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		6		24	6		18	V
I_{CC}	Supply current	No signal		3.2	4.8		3.2	4.8	mA
I_{OUT}	Output current capability		±20			±20			mA
SR	Output slew rate			±.5			±.5		V/µs
	Gain cell distortion[2]	Untrimmed Trimmed		0.3 0.05	1.0		0.5 0.1	2.0	%
	Resistor tolerance			±5	±15		±5	±15	%
	Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
	Output DC shift[3]	Untrimmed		±20	±100		±30	±150	mV
	Expandor output noise	No signal, 15Hz-20kHz[1]		20	45		20	60	µV
	Unity gain level[6]	1kHz	-1	0	+1	-1.5	0	+1.5	dBm
	Gain change[2, 4]			±0.1	±0.2		±0.1		dB
	Reference drift[4]			±5	±10		+2, -25	+20, -50	mV
	Resistor drift[4]			+1, -0			+8, -0		%
	Tracking error (measured relative to value at unity gain) equals [V_O - V_O (unity gain)] dB - V_2dBm	Rectifier input, V_2 = +6dBm, V_1 = 0dB		+0.2			+0.2		dB
		V_2 = -30dBm, V_1 = 0dB		+0.2	-0.5, +1		+0.2	-1, +1.5	
	Channel separation			60			60		dB

NOTES:

1. Input to V_1 and V_2 grounded.
2. Measured at 0dBm, 1kHz.
3. Expandor AC input change from no signal to 0dBm.
4. Relative to value at T_A = 25°C.
5. Electrical characteristics for the SA571 only are specified over -40 to +85°C temperature range.
6. 0dBm = 775mV_{RMS}.

CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full-wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full-wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively-coupled voltage inputs as shown in the following equation. Note that for capacitively-coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|\ avg}{R_1}$$

or

$$G \propto \frac{|V_{IN}|\ avg}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expander or compressor application, this would lead to third harmonic distortion, so there is a trade-off to be made between fast attack and decay times and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})e^{-t/\tau} + G_{final}\ ;\ \tau = 10k \times C_{RECT}$$

The variable gain cell is a current-in, current-out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively-coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

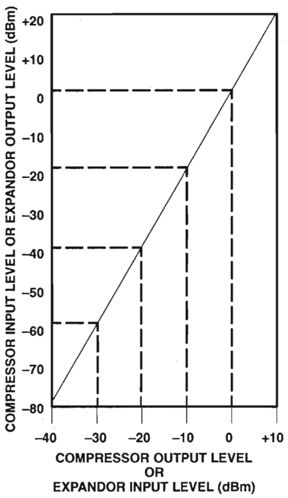
A compensation scheme built into the ΔG cell compensates for temperature and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expander gain to be determined only by internal components.

The output stage is capable of ±20mA output current. This allows a +13dBm ($3.5V_{RMS}$) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

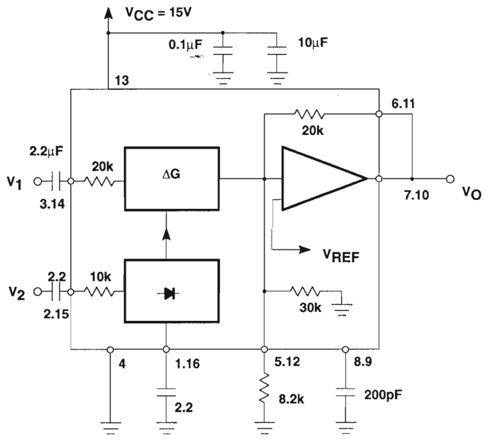
A bandgap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expander circuits.



Basic Input-Output Transfer Curve

TYPICAL TEST CIRCUIT



INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high-performance is required, one has to resort to complex discrete circuitry with many expensive, well-matched components. This paper describes an inexpensive integrated circuit, the NE570 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (<0.1%), high signal-to-noise ratio (90dB), and wide dynamic range (110dB).

CIRCUIT BACKGROUND

The NE570 Compandor was originally designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal-to-noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 1 graphically shows what a compandor can do for the signal-to-noise ratio of a restricted dynamic range channel. The input level range of +20 to -80dB is shown undergoing a 2-to-1 compression where a 2dB input level change is compressed into a 1dB output level change by the compressor. The original 100dB of dynamic range is thus compressed to a 50dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45dB.

The significant circuits in a compressor or expander are the rectifier and the gain control element. The phone system requires a simple full-wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. These features make the circuit useful in audio and data systems as well as in telecommunications systems.

BASIC CIRCUIT HOOK-UP AND OPERATION

Figure 2 shows the block diagram of one half of the chip, (there are two identical channels on the IC). The full-wave averaging rectifier provides a gain control current, I_G, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output DC bias.

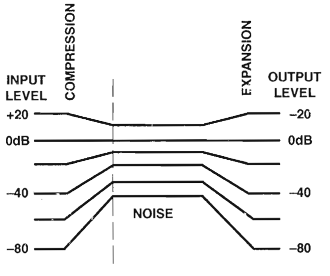


Figure 1. Restricted Dynamic Range Channel

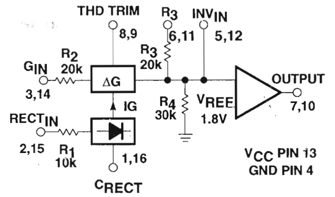
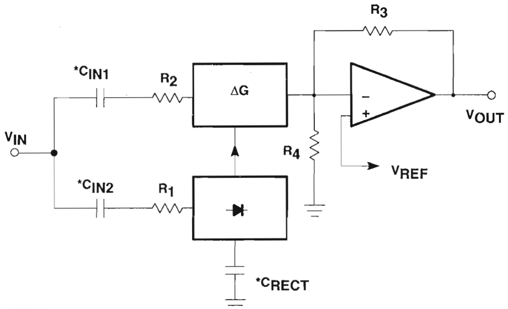


Figure 2. Chip Block Diagram (1 of 2 Channels)



NOTE:

$$\text{GAIN} = \frac{2\, R_3\, V_{IN}\ (\text{avg})}{R_1\, R_2\, I_B}$$

$I_B = 140\mu A$

*EXTERNAL COMPONENTS

Figure 3. Basic Expander

The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8V reference denoted V_{REF}. The non-inverting input of the op amp is tied to V_{REF}, and the summing nodes of the rectifier and ΔG cell (located at the right of R_1 and R_2) have the same potential. The THD trim pin is also at the V_{REF} potential.

Figure 3 shows how the circuit is hooked up to realize an expandor. The input signal, V_{IN}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6dB, the gain control current will drop by a factor of 2, and so the gain will drop 6dB. The output level at V_{OUT} will thus drop 12dB, giving us the desired 2-to-1 expansion.

Figure 4 shows the hook-up for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is setup to provide AC feedback only, so a separate DC feedback loop is provided by the two R_{DC} and C_{DC}. The values of R_{DC} will determine the DC bias at the output of the op amp. The output will bias to:

$$V_{OUT}\ DC = 1 + \frac{R_{DC1} + R_{DC2}}{R_4}$$

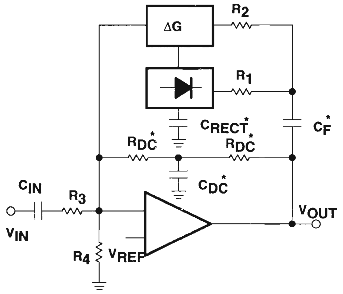
$$V_{REF} = \left(1 + \frac{R_{DCTOT}}{30k}\right) 1.8V$$

The output of the expander will bias up to:

$$V_{OUT}\ DC = 1 + \frac{R_3}{R_4} V_{REF}$$

$$V_{REF} = \left(1 + \frac{20k}{30k}\right) 1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the DC bias to any desired value.



NOTES:

$$\text{GAIN} = \left(\frac{R_1\ R_2\ I_B}{2R_3\ V_{INavg}}\right)^{\frac{1}{2}}$$

$I_B = 140\mu A$

* External components

Figure 4. Basic Compressor

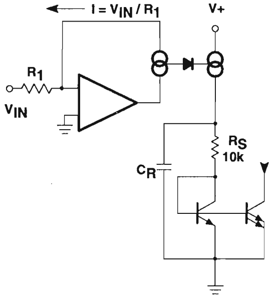
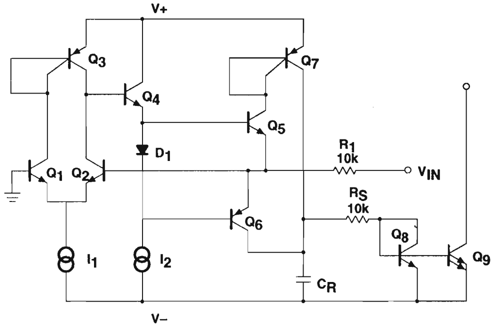


Figure 5. Rectifier Concept

CIRCUIT DETAILS—RECTIFIER

Figure 5 shows the concept behind the full-wave averaging rectifier. The input current to the summing node of the op amp, $V_{IN}R_1$, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R_5, CR, which set the averaging time constant, and then mirrored with a gain of 2 to become I_G, the gain control current.



NOTE:

$$I_G = 2\frac{V_{IN}\ avg}{R\ 1}$$

Figure 6. Simplified Rectifier Schematic

Figure 6 shows the rectifier circuit in more detail. The op amp is a one-stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8V V_{REF}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the *a* of Q_5 or Q_6 on negative or positive signal swings, respectively. ICs such as this have typical NPN βs of 200 and PNP βs of 40. The *a*'s of 0.995 and 0.975 will produce errors of 0.5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere 0.13dB gain error.

At very low input signal levels the bias current of Q_2, (typically 50nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by DC coupling into the rectifier. If an offset voltage exists between the V_{IN} input pin and the base of Q_2, an error current of V_{OS}/R_1 will be generated. A mere 1mV of offset will cause an input current of 100nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the PNP Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250µA. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 7 shows the rectifier accuracy vs input level at a frequency of 1kHz.

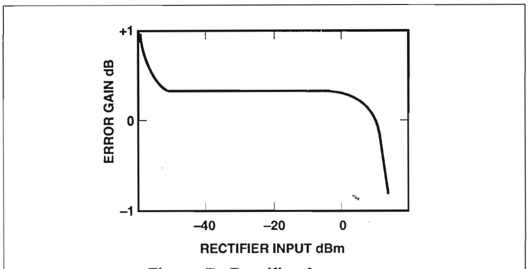


Figure 7. Rectifier Accuracy

At very high frequencies, the response of the rectifier will fall off. The roll-off will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0dBm, -20dBm, and -40dBm is shown in Figure 8. The response at all three levels is flat to well above the audio range.

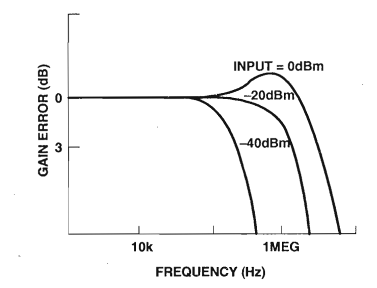


Figure 8. Rectifier Frequency Response vs Input Level

VARIABLE GAIN CELL

Figure 9 is a diagram of the variable gain cell. This is a linearized two-quadrant transconductance multiplier. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3 and Q_4. The gain is controlled by I_G and a current mirror provides the output current.

The op amp maintains the base and collector of Q_1 at ground potential (V_{REF}) by controlling the base of Q_2. The input current I_{IN} ($=V_{IN}/R_2$) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1}=I_1+I_{IN}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is:

$$I_2-(I_1+I_{IN})=I_1-I_{IN}=I_{C2}.$$

The op amp has thus forced a linear current swing between Q_1 and Q_2 by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the non-linearity of the differential pair, Q_1 and Q_2, under large signal conditions.

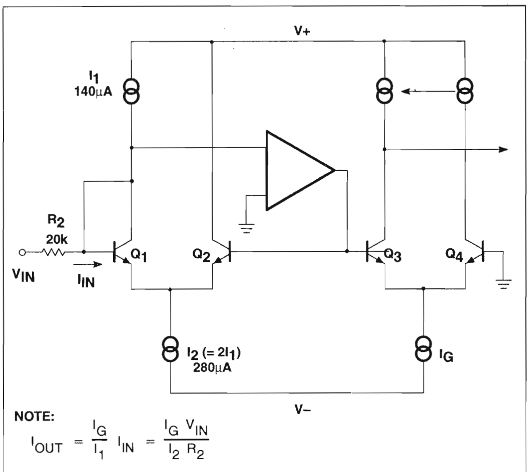
The key to the circuit is that this same predistorted drive signal is applied to the gain control pair, Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1 + I_{IN}}{I_1 - I_{IN}}$$

plus the relationships $I_G=I_{C3}+I_{C4}$ and $I_{OUT}=I_{C4}-I_{C3}$ will yield the multiplier transfer function,

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{V_{IN}}{R_2}\frac{I_G}{I_1}$$

This equation is linear and temperature-insensitive, but it assumes ideal transistors.



NOTE:

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{I_G\, V_{IN}}{I_2\, R_2}$$

Figure 9. Simplified ΔG Cell Schematic

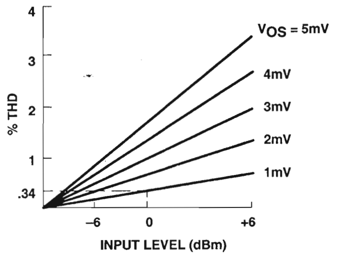


Figure 10. ΔG Cell Distortion vs Offset Voltage

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in second harmonic distortion. Figure 10 gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mV offset will yield 0.34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about mV. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 11 shows the simple trim network required.

Figure 12 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20dB of gain reduction. At high gains, the signal to noise ratio is 90dB, and the total dynamic range from maximum signal to minimum noise is 110dB.

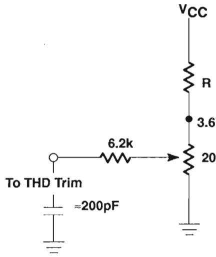


Figure 11. THD Trim Network

Control signal feedthrough is generated in the gain cell by imperfect device matching and mismatches in the current sources, I_1 and I_2. When no input signal is present, changing I_G will cause a small output signal. The distortion trim is effective in nulling out any control signal feedthrough, but in general, the null for minimum feedthrough will be different than the null in distortion. The control signal feedthrough can be trimmed independently of distortion by tying a current source to the ΔG input pin. This effectively trims I_1. Figure 13 shows such a trim network.

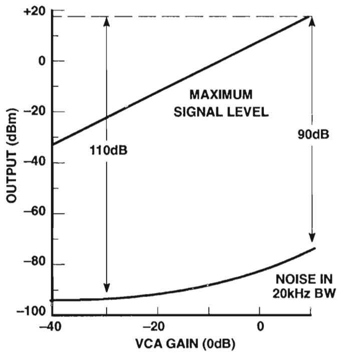


Figure 12. Dynamic Range of NE570

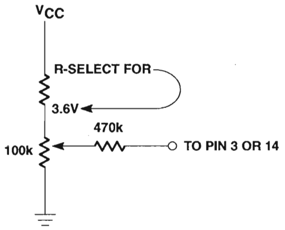


Figure 13. Control Signal Feedthrough

OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1MHz bandwidth. Figure 14 shows the basic circuit. Split collectors are used in the input pair to reduce g_M, so that a small compensation capacitor of just 10pF may be used. The output stage, although capable of output currents in excess of 20mA, is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

RESISTORS

Inspection of the gain equations in Figures 3 and 4 will show that the basic compressor and expander circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hook-ups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 15 shows the effects of temperature on the diffused resistors which are normally used in integrated circuits, and the ion-implanted resistors which are used in this circuit. Over the critical 0°C to +70°C temperature range, there is a 10-to-1 improvement in drift from a 5% change for the diffused resistors, to a 0.5% change for the implemented resistors. The implanted resistors have another advantage in that they can be made the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.

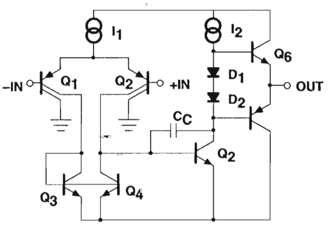


Figure 14. Operational Amplifier

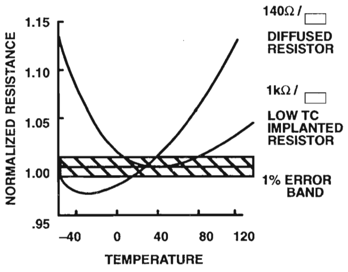


Figure 15. Resistance vs Temperature

Applications for compandors NE570/571/SA571

APPLICATIONS

The following circuits will illustrate some of the wide variety of applications for the NE570.

BASIC EXPANDOR

Figure 1 shows how the circuit would be hooked up for use as an expandor. Both the rectifier and ΔG cell inputs are tied to V_{IN} so that the gain is proportional to the average value of (V_{IN}). Thus, when V_{IN} falls 6dB, the gain drops 6dB and the output drops 12dB. The exact expression for the gain is

$$\text{Gain exp.} = \left[\frac{2\ R_3\ V_{IN}\ (\text{avg})}{R_1\ R_2\ I_B}\right]^2$$

$I_B = 140\mu A$

The maximum input that can be handled by the circuit in Figure 1 is a peak of 3V. The rectifier input current can be as large as $I=3V/R_1=3V/10k=300\mu A$. The ΔG cell input current should be limited to $I=2.8V/R_2=2.8V/20k=140\mu A$. If it is necessary to handle larger input voltages than 0 ±2.8V peak, external resistors should be placed in series with R_1 and R_2 to limit the input current to the above values.

Figure 1 shows a pair of input capacitors C_{IN1} and C_{IN2}. It is now necessary to use both capacitors if low level tracking accuracy is not important. If R_1 and R_2 are tied together and share a common capacitor, a small current will flow between the ΔG cell summing node and the rectifier summing node due to offset voltages. This current will produce an error in the gain control signal at low levels, degrading tracking accuracy.

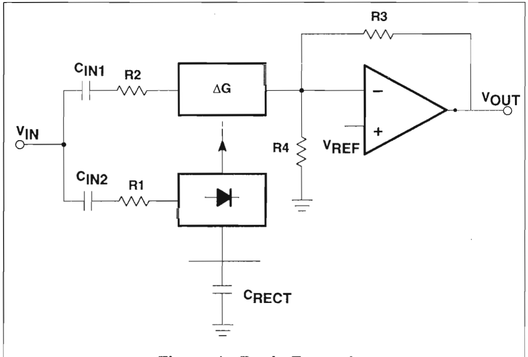


Figure 1. Basic Expandor

The output of the expandor is biased up to 3V by the DC gain provided by R_3, R_4. The output will bias up to

$$V_{OUTDC} = 1 + \frac{R_3}{R_4}\ V_{REF}$$

For supply voltages higher than 6V, R_4 can be shunted with an external resistor to bias the output up to V_{CC}.

Note that it is possible to externally increase R_1, R_2, and R_3, and to decrease R_3 and R_4. This allows a great deal of flexibility in setting up system levels. If larger input signals are to be handled, R_1 and R_2 may be increased; if a larger output is required, R_3 may be increased. To obtain the largest dynamic range out of this circuit, the rectifier input should always be as large as possible (subject to the ±300µA peak current restriction).

BASIC COMPRESSOR

Figure 2 shows how to use the NE570/571 as a compressor. It functions as an expandor in the feedback loop of an op amp. If the input rises 6dB, the output can rise only 3dB. The 3dB increase in output level produces a 3dB increase in gain in the ΔG cell, yielding a 6dB increase in feedback current to the summing node. Exact expression for gain is

$$\text{Gain comp.} = \left[\frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}\ (\text{avg})}\right]^{\frac{1}{2}}$$

The same restrictions for the rectifier and ΔG cell maximum input current still hold, which place a limit on the maximum compressor output. As in the expandor, the rectifier and ΔG cell inputs could be made common to save a capacitor, but low level tracking accuracy would suffer. Since there is no DC feedback path around the op amp through the ΔG cell, one must be provided externally. The pair of resistors R_{DC} and the capacitor C_{DC} must be provided. The op amp output will bias up to

$$V_{OUTDC} = \left(1 + \frac{R_{DC}}{R_4}\right)\ V_{REF}$$

For the largest dynamic range, the compressor output should be as large as possible so that the rectifier input is as large as possible (subject to the ±300µA peak current restriction). If the input signal is small, a large output can be produced by reducing R_3 with the attendant decrease in input impedance, or by increasing R_1 or R_2. It would be best to increase R_2 rather than R_1 so that the rectifier input current is not reduced.

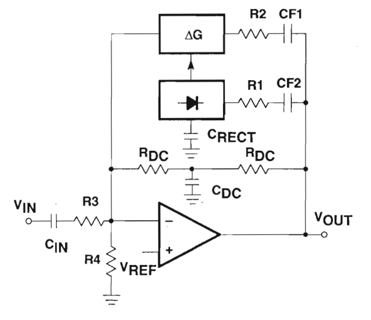


Figure 2. Basic Compressor

DISTORTION TRIM

Distortion can be produced by voltage offsets in the ΔG cell. The distortion is mainly even harmonics, and drops with decreasing input signal (input signal meaning the current into the ΔG cell). The THD trim terminal provides a means for trimming out the offset voltages and thus trimming out the distortion. The circuit shown in Figure 3 is suitable, as would be any other capable of delivering ±30µA into 100Ω resistor tied to 1.8V.

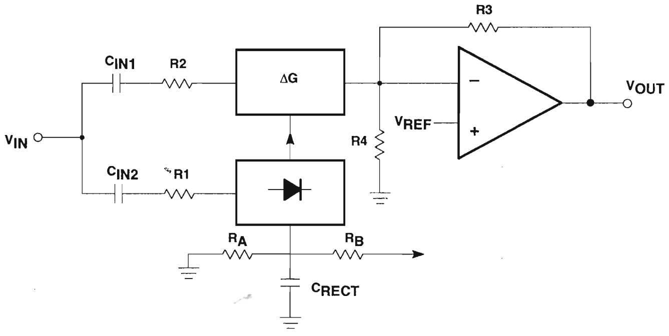


Figure 4. Expandor With Low Level Mistracking

LOW LEVEL MISTRACKING

The compandor will follow a 2-to-1 tracking ratio down to very low levels. The rectifier is responsible for errors in gain, and it is the rectifier input bias current of <100nA that produces errors at low levels. The magnitude signal level drops to a $1\mu A$ average, the bias current will produce a 10% or 1dB error in gain. This will occur at 42dB below the maximum input level.

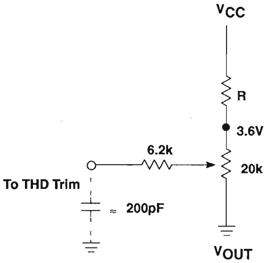


Figure 3. THD Trim Network

It is possible to deviate from the 2-to-1 transfer characteristic at low levels as shown in the circuit of Figure 4. Either R_A or R_B, (but not both), is required. The voltage on C_{RECT} is $2\times V_{BE}$ plus V_{IN} avg. For low level inputs V_{IN} avg is negligible, so we can assume 1.3V as the bias on C_{RECT}. If R_A is placed from C_{RECT} to AND we will bleed off a current $I=1.3V/R_A$. If the rectifier average input current is less than this value, there will be no gain control input to the ΔG cell so that its gain will be zero and the expandor output will be zero. As the input level is raised, the input current will exceed $1.3V/R_A$ and the expandor output will become active. For large input signals, R_A will have little effect. The result of this is that we will deviate from the 2-to-1 expansion, present at high levels, to an infinite expansion at low levels where the output shuts off completely. Figure 5 shows some examples of tracking curves which can be obtained. Complementary curves would be obtained for a compressor, where at low level signals the result would be infinite compression. The bleed current through R_A will be a function of temperature because of the two V_{BE} drops, so the low level tracking will drift with temperature. If a negative supply is available, if would be desirable to tie R_A to that, rather than ground, and to increase its value accordingly. The bleed current will then be less sensitive to the V_{BE} temperature drift.

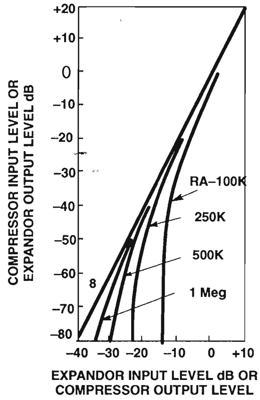


Figure 5. Mistracking With R_A

R_B will supply an extra current to the rectifier equal to $(V_{CC}-1.3V)R_B$. In this case, the expandor transfer characteristic will deviate towards 1-to-1 at low levels. At low levels the expandor gain will stop dropping and the expansion will cease. In a compressor, this would lead to a lack of compression at low levels. Figure 6 shows some typical transfer curves. An R_B value of approximately 2.5M would trim the low level tracking so as to match the Bell system N2 trunk compandor characteristic.

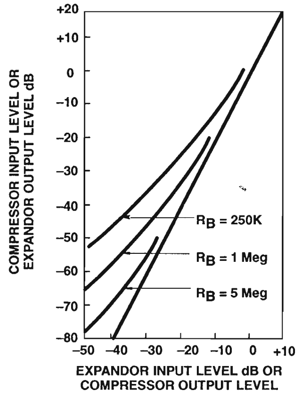


Figure 6. Mistracking With R_B

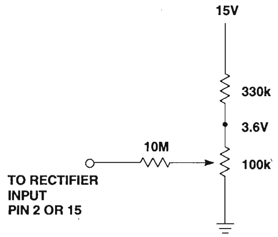


Figure 7. Rectifier Bias Current Compensation

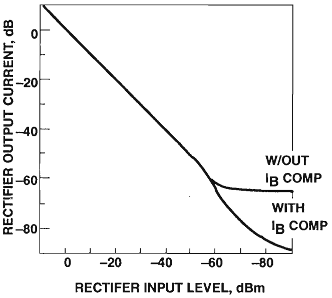


Figure 8. Rectifier Performance With Bias Current Compensation

RECTIFIER BIAS CURRENT CANCELLATION

The rectifier has an input bias current of between 50 and 100nA. This limits the dynamic range of the rectifier to about 60dB. It also limits the amount of attenuation of the ΔG cell. The rectifier dynamic range may be increased by about 20dB by the bias current trim network shown in Figure 7. Figure 8 shows the rectifier performance with and without bias current cancellation.

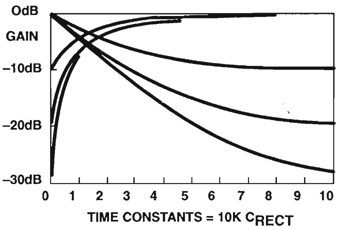


Figure 9. Gain vs Time Input Steps of ±10, ±20, ±30dB

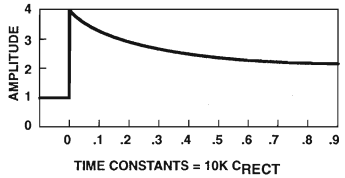


Figure 10. Compressor Attack Envelope +12dB Step

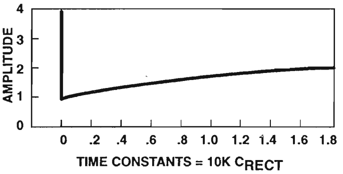


Figure 11. Compressor Release Envelope –12dB Step

ATTACK AND DECAY TIME

The attack and decay times of the compandor are determined by the rectifier filter time constant 10k×C_{RECT}. Figure 9 shows how the gain will change when the input signal undergoes a 10, 20, or 30dB change in level.

The attack time is much faster than the decay, which is desirable in most applications. Figure 10 shows the compressor attack envelope for a +12dB step in input level. The initial output level of 1 unit instantaneously rises to 4 units, and then starts to fall towards its final value of 2 units. The CCITT recommendation on attack and decay times for telephone system compandors defines the attack time as when the envelope has fallen to a level of 3 units, corresponding to t=0.15 in the figure. The CCITT recommends an attack time of 3 ±2ms, which suggests an RC product of 20ms. Figure 11 shows the compressor output envelope when the input level is suddenly reduced 12dB. The output, initially at a level of 4 units, drops 12dB to 1 unit and then rises to its final value of 2 units. The CCITT defines release time as when the output has risen to 1.5 units, and suggests a value of 13.5 ±9ms. This corresponds to t=0.675 in the figure, which again suggests a 20ms RC product. Since R_1=10k, the CCITT recommendations will be met if C_{RECT}=2μF.

There is a trade-off between fast response and low distortion. If a small C_{RECT} is used to get very fast attack and decay, some ripple will appear on the gain control line and produce distortion. As a rule, a 1µF C_{RECT} will produce 0.2% distortion at 1kHz. The distortion is inversely proportional to both frequency and capacitance. Thus, for telephone applications where C_{RECT}=2µF, the ripple would cause 0.1% distortion at 1kHz and 0.33% at 800Hz. The low frequency distortion generated by a compressor would be cancelled (or undistorted) by an expandor, providing that they have the same value of C_{RECT}.

FAST ATTACK, SLOW RELEASE HARD LIMITER

The NE570/571 can be easily used to make an excellent limiter. Figure 12 shows a typical circuit which requires of an NE570/571, of an LM339 quad comparator, and a PNP transistor. For small signals, the ΔG cell is nearly off, and the circuit runs at unity gain as set by R_8, R_7. When the output signal tries to exceed a + or −1V peak, a comparator threshold is exceeded. The PNP is turned on and rapidly charges C_4 which activates the ΔG cell. Negative feedback through the ΔG cell reduces the gain and the output signal level. The attack time is set by the RC product of R_{18} and C_4, and the release time is determined by C_4 and the internal rectifier resistor, which is 10k. The circuit shown attacks in less than 1ms and has a release time constant of 100ms. R_9 trickles about 0.7µA through the rectifier to prevent C_4 from becoming completely discharged. The gain cell is activated when the voltage on Pin 1 or 16 exceeds two diode drops. If C_4 were allowed to become completely discharged, there would be a slight delay before it recharged to >1.2V and activated limiting action.

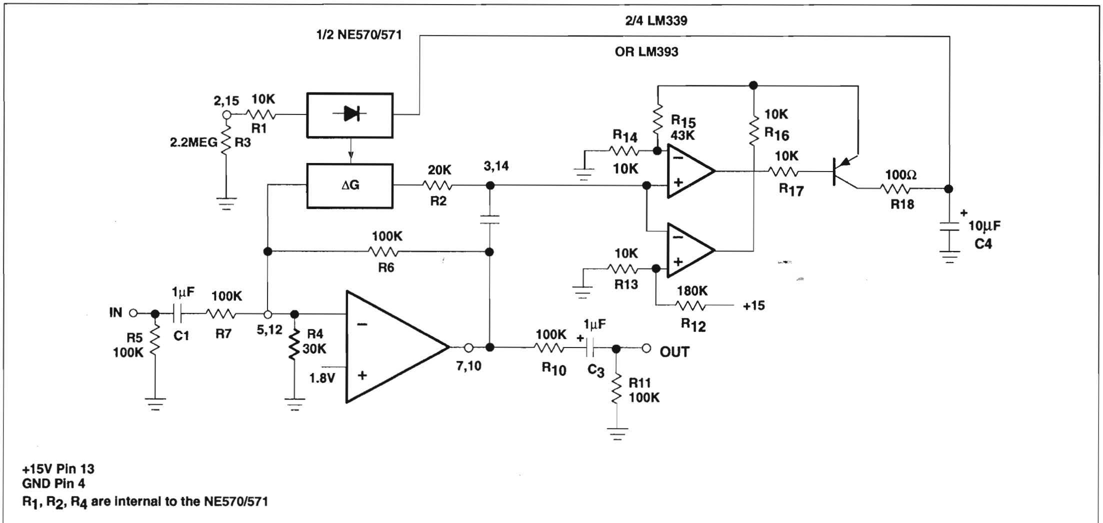


Figure 12. Fast Attack, Slow Release Hard Limiter

A stereo limiter can be built out of 1 NE570/571, 1 LM339 and two PNP transistors. The resistor networks R_{12}, R_{13} and R_{14}, R_{15}, which set the limiting thresholds, could be common between channels. To gang the stereo channels together (limiting in one channel will produce a corresponding gain change in the second channel to maintain the balance of the stereo image), then Pins 1 and 16 should be jumpered together. The outputs of all 4 comparators may then be tied together, and only one PNP transistor and one capacitor C_4 need be used. The release time will then be the product 5k×C_4 since two channels are being supplied current from C_4.

USE OF EXTERNAL OP AMP

The operational amplifiers in the NE570/571 are not adequate for some applications.

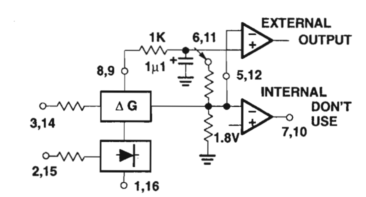


Figure 13. Use of External Op Amp

The slew rate, bandwidth, noise, and output drive capability can limit performance in many systems. For best performance, an external op amp can be used. The external op amp may be powered by bipolar supplies for a larger output swing.

Figure 13 shows how an external op amp may be connected. The non-inverting input must be biased at about 1.8V. This is easily accomplished by tying it to either Pin 8 or 9, the THD trim pins, since these pins sit at 1.8V. An optional RC decoupling network is shown which will filter out the noise from the NE570/571 reference (typically about 10µV in 20kHz BW). The inverting input of the external op amp is tied to the inverting input of the internal op amp. The output of the external op amp is then used, with the internal op amp output left to float. If the external op amp is used single supply (+V_{CC} and ground), it must have an input common-mode range down to less than 1.8V.

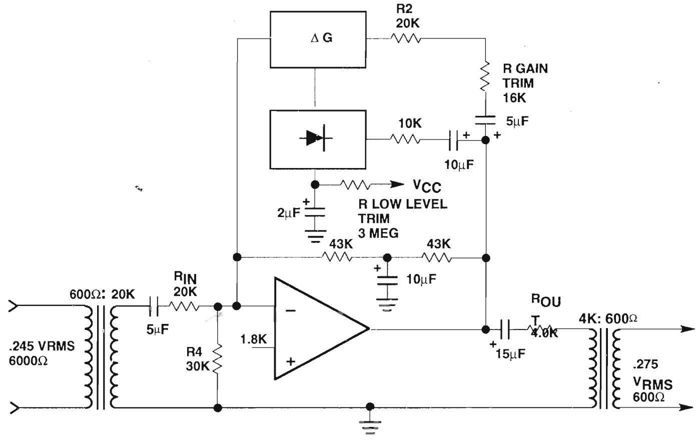


Figure 14. N2 Compressor

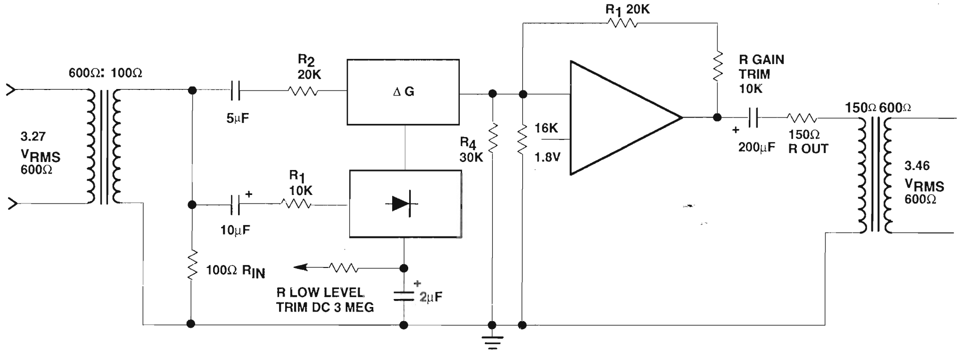


Figure 15. N2 Expandor

N2 COMPANDOR

There are four primary considerations involved in the application of the NE570/571 in an N2 compandor. These are matching of input and output levels, accurate 600Ω input and output impedances, conformance to the Bell system low level tracking curve, and proper attack and release times.

Figure 14 shows the implementation of an N2 compressor. The input level of $0.245V_{RMS}$ is

stepped up to $1.41V_{RMS}$ by the 600Ω: 20kΩ matching transformer. The 20k input resistor properly terminates the transformer. An internal 20kΩ resistor (R_3) is provided, but for accurate impedance termination an external resistor should be used. The output impedance is provided by the 4kΩ output resistor and the 4kΩ: 600Ω output transformer.

The $0.275V_{RMS}$ output level requires a 1.4V op amp output level. This can be provided by increasing the value of R_2 with an external resistor, which can be selected to fine trim the gain. A rearrangement of the compressor gain equation (6) allows us to determine the value for R_2.

$$R_2 = \frac{\text{Gain}^2 \times 2\ R_3\ V_{IN}\ \text{avg}}{R_1\ I_B}$$

$$= \frac{1^2 \times 2 \times 20k \times 1.27}{10k \times 140\mu A}$$

$$= 36.3k$$

The external resistance required will thus be 36.3k–20k=16.3k.

The Bell-compatible low level tracking characteristic is provided by the low level trim resistor from C_{RECT} to V_{CC}. As shown in Figure 6, this will skew the system to a 1:1 transfer characteristic at low levels. The 2µF rectifier capacitor provides attack and release times of 3ms and 13.5ms, respectively, as shown in Figures 10 and 11. The R-C-R network around the op amp provides DC feedback to bias the output at DC.

An N2 expandor is shown in Figure 15. The input level of $3.27V_{RMS}$ is stepped down to 1.33V by the 600Ω:100Ω transformer, which is terminated with a 100Ω resistor for accurate impedance matching. The output impedance is accurately set by the 150Ω output resistor and the 150Ω:600Ω output transformer. With this configuration, the 3.46V transformer output requires a 3.46V op amp output. To obtain this output level, it is necessary to increase the value of R_3 with an external trim resistor. The new value of R_3 can be found with the expandor gain equation

$$R_3 = \frac{R_1\ R_2\ I_B\ \text{Gain}}{2\ V_{IN}\ \text{avg}}$$
$$= \frac{10k \times 20k \times 140\mu A \times 2.6}{2 \times 1.20}$$
$$= 30.3k$$

An external addition to R_3 of 10k is required, and this value can be selected to accurately set the high level gain.

A low level trim resistor from C_{RECT} to V_{CC} of about 3M provides matching of the Bell low-level tracking curve, and the 2μF value of C_{RECT} provides the proper attack and release times. A 16k resistor from the summing node to ground biases the output to $7V_{DC}$.

VOLTAGE-CONTROLLED ATTENUATOR

The variable gain cell in the NE570/571 may be used as the heart of a high quality voltage-controlled amplifier (VCA). Figure 16 shows a typical circuit which uses an external op amp for better performance, and an exponential converter to get a control characteristic of –6dB/V. Trim networks are shown to null out distortion and DC shift, and to fine trim gain to 0dB with 0V of control voltage.

Op amp A_2 and transistors Q_1 and Q_2 form the exponential converter generating an exponential gain control current, which is fed into the rectifier. A reference current of 150μA, (15V and R_{20}=100k), is attenuated a factor of two (6dB) for every volt increase in the control voltage. Capacitor C_6 slows down gain changes to a 20ms time constant ($C_6 \times R_1$) so that an abrupt change in the control voltage will produce a smooth sounding gain change. R_{18} assures that for large control voltages the circuit will go to full attenuation. The rectifier bias current would normally limit the gain reduction to about 70dB. R_{18} draws excess current out of the rectifier. After approximately 50dB of attenuation at a –6dB/V slope, the slope steepens and attenuation becomes much more rapid until the circuit totally shuts off at about 9V of control voltage. A_1 should be a low noise high slew rate op amp. R_{13} and R_{14} establish approximately a 0V bias at A_1's output.

With a 0V control voltage, R_{19} should be adjusted for 0dB gain. At 1V(–6dB gain) R_9 should be adjusted for minimum distortion with a large (+10dBm) input signal. The output DC bias (A_1 output) should be measured at full attenuation (+10V control voltage) and then R_8 is adjusted to give the same value at 0dB gain. Properly adjusted, the circuit will give typically less than 0.1% distortion at any gain with a DC output voltage variation of only a few millivolts. The clipping level (140μA into Pin 3, 14) is ±10V peak. A signal-to-noise ratio of 90dB can be obtained.

If several VCAs must track each other, a common exponential converter can be used. Transistors can simply be added in parallel with Q_2 to control the other channels. The transistors should be maintained at the same temperature for best tracking.

AUTOMATIC LEVEL CONTROL

The NE570 can be used to make a very high performance ALC as shown in Figure 17. This circuit hook-up is very similar to the basic compressor shown in Figure 2 except that the rectifier input is tied to the input rather than the output. This makes gain inversely proportional to input level so that a 20dB drop in input level will produce a 20dB increase in gain. The output will remain fixed at a constant level. As shown, the circuit will maintain an output level of ±1dB for an input range of +14 to –43dB at 1kHz. Additional external components will allow the output level to be adjusted. Some relevant design equations are:

$$\text{Output level} = \frac{R_1\ R_2\ I_B}{2\ R_3} \left(\frac{V_{IN}}{V_{IN}\ (\text{avg})}\right)$$
$$I_B = 140mA$$

$$\text{Gain} = \frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}\ (\text{avg})} \quad \text{where}$$

$$\frac{V_{IN}}{V_{IN}\ (\text{avg}} = \frac{\pi}{2\sqrt{2}} = 1.11 \ \text{(for sine wave)}$$

If ALC action at very low input levels is not desired, the addition of resistor R_X will limit the maximum gain of the circuit.

$$\text{Gain max} = \frac{\frac{R_1 + R_X}{1.8V} \times R_2 \times I_B}{2\ R_3}$$

The time constant of the circuit is determined by the rectifier capacitor, C_{RECT}, and an internal 10k resistor.

$$\tau = 10k\ C_{RECT}$$

Response time can be made faster at the expense of distortion. Distortion can be approximated by the equation:

$$\text{THD} = \left(\frac{1\mu F}{C_{RECT}}\right)\left(\frac{1kHz}{\text{freq.}}\right) \times 0.2\%$$

VARIABLE SLOPE COMPRESSOR-EXPANDOR

Compression and expansion ratios other than 2:1 can be achieved by the circuit shown in Figure 18. Rotation of the dual potentiometer causes the circuit hook-up to change from a basic compressor to a basic expandor. In the center of rotation, the circuit is 1:1, has neither compression nor expansion. The (input) output transfer characteristic is thus continuously variable from 2:1 compression, through 1:1 up to 1:2 expansion. If a fixed compression or expansion ratio is desired, proper selection of fixed resistors can be used instead of the potentiometer. The optional threshold resistor will make the compression or expansion ratio deviate towards 1:1 at low levels. A wide variety of (input) output characteristics can be created with this circuit, some of which are shown in Figure 18.

HI-FI COMPANDOR

The NE570 can be used to construct a high performance compandor suitable for use with music. This type of system can be used for noise reduction in tape recorders, transmission systems, bucket brigade delay lines, and digital audio systems. The circuits to be described contain features which improve performance, but are not required for all applications.

A major problem with the simple NE570 compressor (Figure 2) is the limited op amp gain at high frequencies.

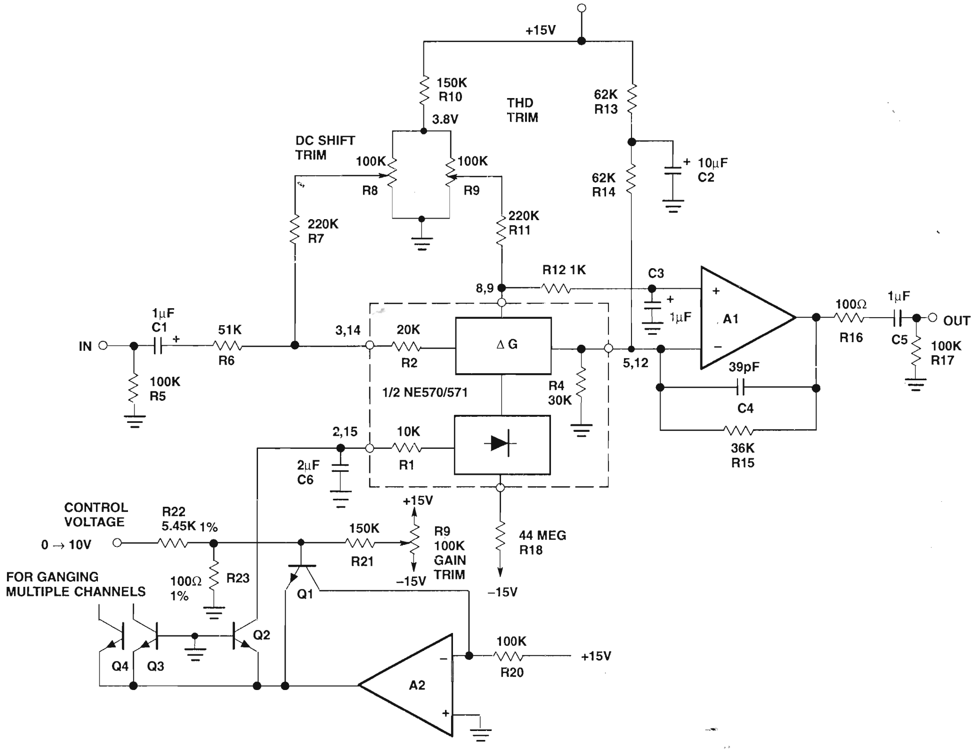


Figure 16. Voltage-Controlled Attenuator

For weak input signals, the compressor circuit operates at high gain and the 570 op amp simply runs out of loop gain. Another problem with the 570 op amp is its limited slew rate of about 0.6V/µs. This is a limitation of the expandor, since the expandor is more likely to produce large output signals than a compressor.

Figure 20 is a circuit for a high fidelity compressor which uses an external op amp and has a high gain and wide bandwidth. An input compensation network is required for stability.

Another feature of the circuit in Figure 20 is that the rectifier capacitor (C_9) is not grounded, but is tied to the output of an op amp circuit. This circuit, built around an LM324, speeds up the compressor attack time at low signal levels. The response times of the simple expandor and compressor (Figures 1 and 2) become longer at low signal levels. The time constant is not simply $10k \times C_{RECT}$, but is really:

$$\left(10k + 2\left(\frac{0.026V}{I_{RECT}}\right)\right) \times C_{RECT}$$

When the rectifier input level drops from 0dBm to –30dBm, the time constant increases from $10.7k \times C_{RECT}$ to $32.6k \times C_{RECT}$. In systems where there is unity gain between the compressor and expandor, this will cause no overall error. Gain or loss between the compressor and expandor will be a mistracking of low signal dynamics. The circuit with the LM324 will greatly reduce this problem for systems which cannot guarantee the unity gain.

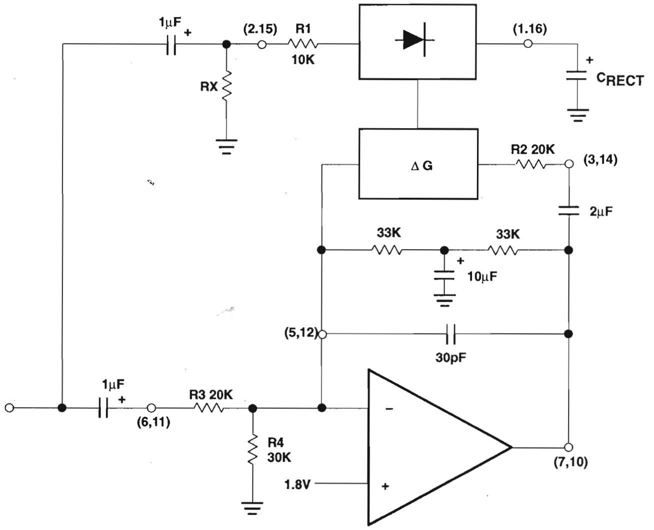


Figure 17. Automatic Level Control

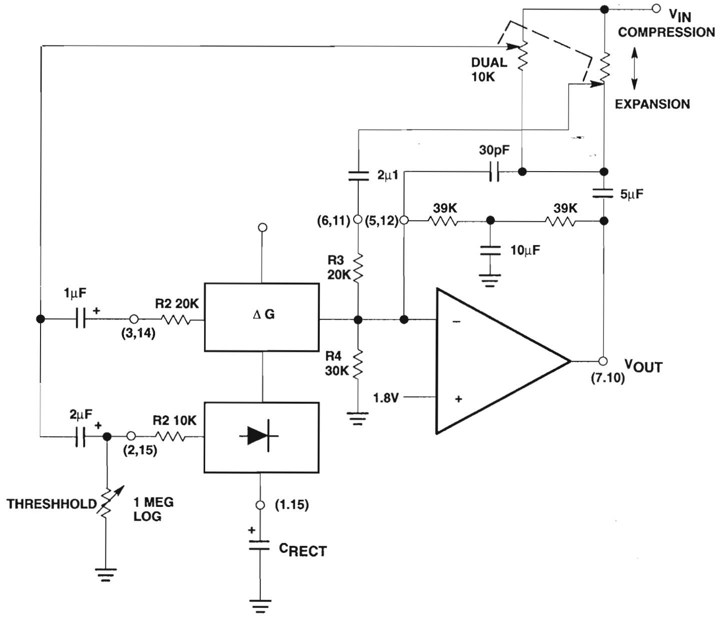


Figure 18. Variable Slope Compressor-Expandor

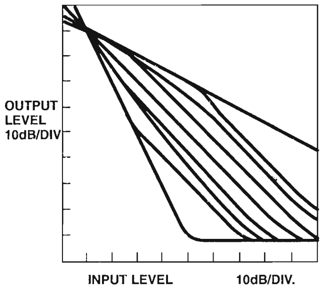


Figure 19. Typical Input-Output Tracking Curves of Variable Ratio Compressor-Expandor

When a compressor is operating at high gain, (small input signal), and is suddenly hit with a signal, it will overload until it can reduce its gain. Overloaded, the output will attempt to swing rail to rail. This compressor is limited to approximately a $7V_{P-P}$ output swing by the brute force clamp diodes D_3 and D_4. The diodes cannot be placed in the feedback loop because their capacitance would limit high frequency gain. The purpose of limiting the output swing is to avoid overloading any succeeding circuit such as a tape recorder input.

The time it takes for the compressor to recover from overload is determined by the rectifier capacitor C_9. A smaller capacitor will allow faster response to transients, but will produce more low frequency third harmonic distortion due to gain modulation. A value of 1µF seems to be a good compromise value and yields good subjective results. Of course, the expandor should have exactly the same value rectifier capacitor for proper transient response. Systems which have good low frequency amplitude and phase response can use compandors with smaller rectifier capacitors, since the third harmonic distortion which is generated by the compressor will be undistorted by the expandor.

Simple compandor systems are subject to a problem known as breathing. As the system is changing gain, the change in the background noise level can sometimes be heard.

The compressor in Figure 20 contains a high frequency pre-emphasis circuit (C_2, R_5 and C_8, R_{14}), which helps solve this problem. Matching de-emphasis on the expandor is required. More complex designs could make the pre-emphasis variable and further reduce breathing.

The expandor to complement the compressor is shown in Figure 21. Here an external op amp is used for high slew rate. Both the compressor and expandor have unity gain levels of 0dB. Trim networks are shown for distortion (THD) and DC shift. The distortion trim should be done first, with an input of 0dB at 10kHz. The DC shift should be adjusted for minimum envelope bounce with tone bursts. When applied to consumer tape recorders, the subjective performance of this system is excellent.

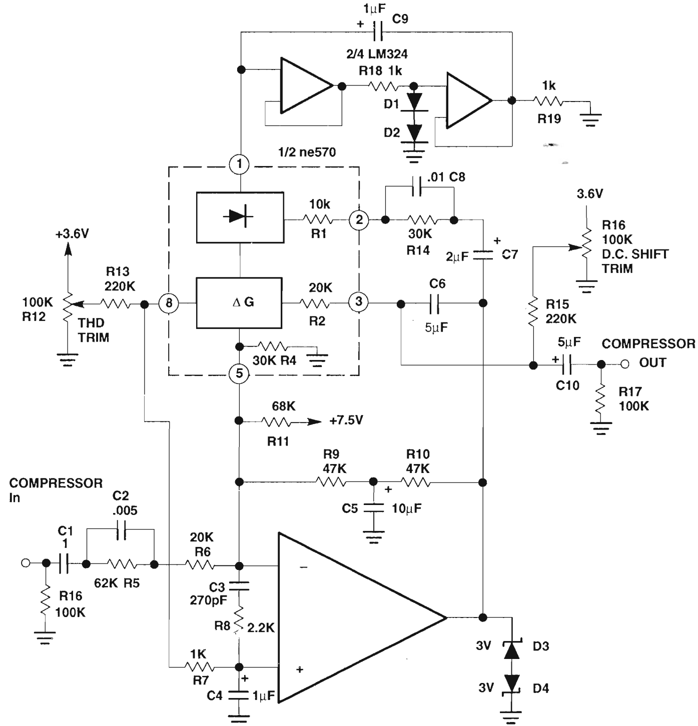


Figure 20. Hi-Fi Compressor With Pre-emphasis

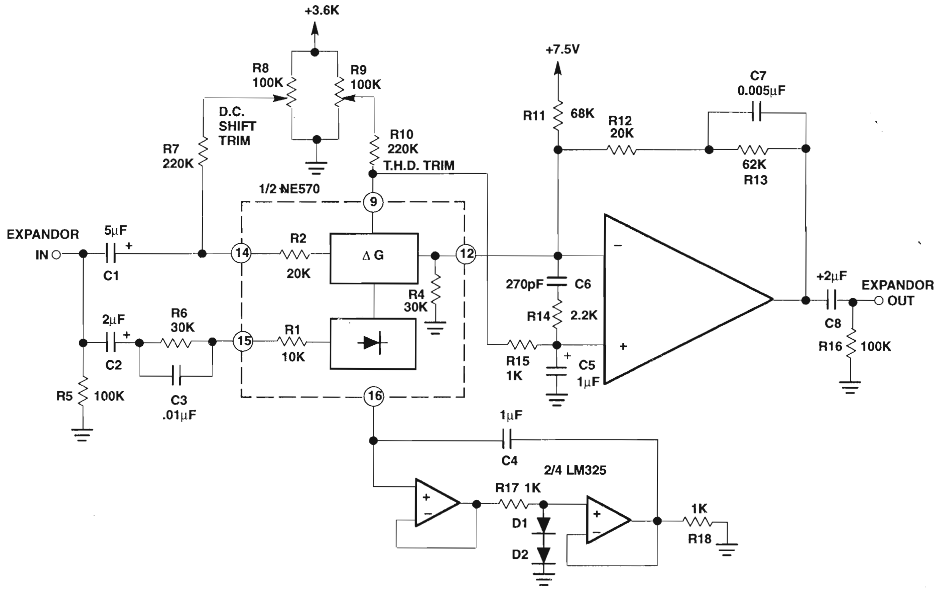


Figure 21. Hi-Fi Expandor With De-emphasis

Compandor cookbook

AN176

Compandors are versatile, low cost, dual-channel gain control devices for audio frequencies. They are used in tape decks, cordless telephones, and wireless microphones performing noise reduction. Electronic organs, modems and mobile telephone equipment use compandors for signal level control.

So what is companding? Why do it at all? What happens when we do it? Compandor is the contraction of the two words compressor and expandor. There is one basic reason to compress a signal before sending it through a telephone line or recording it on a cassette tape: to process that signal (music, speech, data) so that all parts of it are above the inherent noise floor of the transmission medium and yet not running into the max. dynamic range limits, causing clipping and distortion. The diagrams below demonstrate the idea; they are not totally correct because in the real world of electronics the 3kHz tone is riding on the 1kHz tone. They are shown separated for better explanation.

Figure 1 is the signal from the source. Figure 2 shows the noise always in the transmission medium. Figure 3 shows the max limits of the transmission medium and what happens when a signal larger than those limits is sent through it. Figure 4 is the result of compressing the signal (note that the larger signal would not be clipped when transmitted).

The received/playback signal is processed (expanded) in exactly the same — only inverted — ratio as the input signal was compressed. The end result is a clean, undistorted signal with a high signal-to-noise ratio.

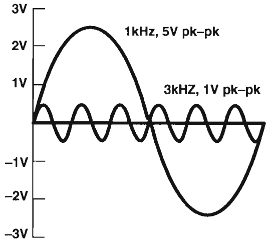


Figure 1. Original Signal Input

Figure 2. Wide-Band Noise Floor of Transmission Line

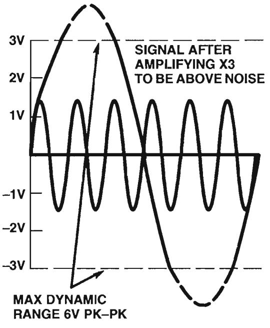


Figure 3.

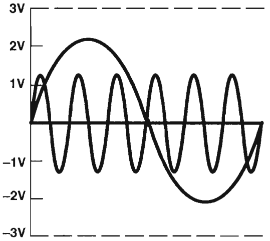


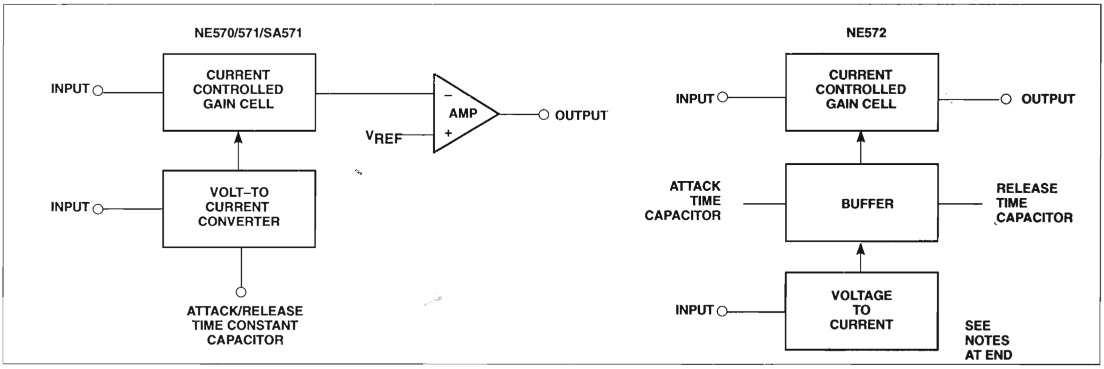
Figure 4. Signal After Compression

This document has been designed to give the reader a basic working knowledge of the Signetics Compandor family. The analyses of three primary applications will be accompanied by "recipes" describing how to select external components (for both proper operation and function modification). Schematic and artwork for an application board are also provided. For comprehensive technical information consult the Compandor Product Guide or the Linear Data Manual.

The basic blocks in a compandor are the current-controlled variable gain cell (ΔG), voltage-to-current converter (rectifier), and operational amplifier. Each Signetics compandor package has two identical, independent channels with the following block diagrams (notice that the 570/71 is different from the 572).

The operational amplifier is the main signal path and output drive.

BLOCK DIAGRAMS



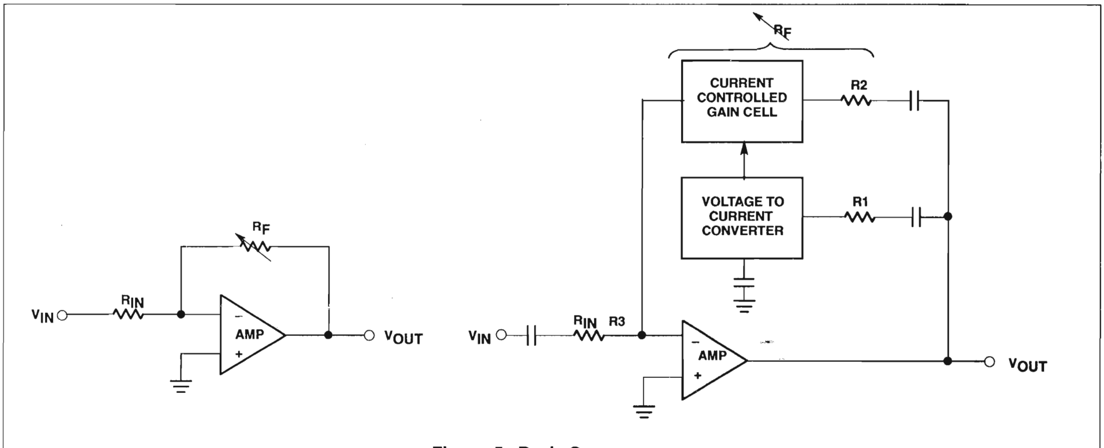


Figure 5. Basic Compressor

The full-wave averaging rectifier measures the AC amplitude of a signal and develops a control current for the variable gain cell.

The variable gain cell uses the rectifier control current to provide variable gain control for the operational amplifier gain block.

The compandor can function as a Compressor, Expandor, and Automatic Level Controller or as a complete compressor/expandor system as described in the following:

1) The COMPRESSOR function processes uncontrolled input signals into controlled output signals. The purpose of this is to avoid distortion caused by a narrow dynamic range medium, such as telephone lines, RF and satellite transmissions, and magnetic tape. The Compressor can also limit the level of a signal.

2) The EXPANDOR function allows a user to increase the dynamic range of an incoming compressed signal such as radio broadcasts.

3) The compressor/expandor system allows a user to retain dynamic range and reduce the effects of noise introduced by the transmission medium.

4) The AUTOMATIC LEVEL CONTROL (ALC) function (like the familiar automatic gain control) adjusts its gain proportionally with the input amplitude. This ALC circuit therefore transforms a widely varying input signal into a fixed amplitude output signal without clipping and distortion.

HOW TO DESIGN COMPANDOR CIRCUITS

The rest of the cookbook will provide you with basic compressor, expandor, and automatic level control application information. A NE570/571 has been used in all of the circuits. If high-fidelity audio or separately programmable attack and decay time are needed, the NE572 with a low noise op amp should be used.

The compressor (see Figure 5) utilizes all basic building blocks of the compandor. In this configuration, the variable gain cell is placed in the feedback loop of the standard inverting amplifier circuit. The gain equation is $A_V=-R_F/R_{IN}$. As shown above, the variable gain cell acts as a variable feedback resistor (R_F) (See Figure 5).

As the input signal increases above the crossover level of 0dB, the variable resistor decreases in value. This causes the gain to decrease, thus limiting the output amplitude.

Below the crossover level of 0dB, an increase in input signal causes the variable resistor to increase in value, thereby causing the output signal's amplitude to increase.

In the compressor configuration, the rectifier is connected to the output.

The complete equation for the compressor gain is:

$$\text{Gain comp.} = \left[\frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}\ (\text{avg})}\right]^{\frac{1}{2}}$$

where:

$R_1 = 10k$

$R_2 = 20k$

$R_3 = 20k$

$I_B = 140\mu A$

$V_{IN}(\text{avg})=0.9(V_{IN(RMS)})$

COMPRESSOR RECIPE

1) DC bias the output half way between the supply and ground to get maximum headroom. The circuit in Figure 6 is designed around a system supply of 6V, thus the output DC level should be 3V.

$V_{OUT\ DC}=(1+(2R_{DC}/R_4))\ V_{REF}$

where:

$R_4=30k$

$V_{REF}=1.8V$

R_{DC} is external

manipulating the equation, the result is. . .

$$R_{DC} = \left(\left(\frac{V_{OUT}}{V_{REF}}\right) - 1\right)\frac{R_4}{2}$$

Note that the $C_{(DC)}$ should be large enough to totally short out any AC in this feedback loop.

2) Analyze the OUTPUT signal's anticipated amplitude.

a) if larger than 2.8V peak, R_2 needs to be increased. (see INGREDIENTS section)

b) if larger than 3.0V peak, R_1 will also need to be increased.

By limiting the peak input currents we avoid signal distortion.

3) The input and output coupling caps need to be large enough not to attenuate any desired frequencies ($X_C=1/(6.28xf)$).
4) The C_{RECT} should be 1μF to 2μF for initial setup. This directly affects Attack and Release times.
5) An input buffer may be necessary if the source's output impedance needs matching.
6) Pre-emphasis may be used to reduce noisepumping, breathing, etc., if present. See the NE570/571 data sheet for specific details.
7) Distortion (THD) trim pins are available if the already low distortion needs to be further reduced. Refer to data sheet for trimming network. Note that if not used, the THD trim pins should have 200pF caps to ground.

8) At very low input signal levels, the rectifier's errors become significant and can be reduced with the Low Level Mistracking network. (This technique prevents infinite compression at low input levels.)

The EXPANDOR utilizes all the basic building blocks of the compandor (see Figure 7). In this configuration the variable gain cell is placed in the inverting input lead of the operational amplifier and acts as a variable input resistance, R_{IN}. The basic gain equation for operational amplifiers in the standard inverting feedback loop is $A_V=-R_F/R_{IN}$.

As the input amplitude increases above the crossover level of 0dBM, this variable resistor decreases in value, causing the gain to increase, thus forcing the output amplitude to increase (refer to Figure 10).

Below the crossover level, an increase in input amplitude causes the variable resistor to increase in value, thus forcing the output amplitude to decrease.

The complete equation for the expandor gain is:

$\text{Gain expandor}=(2R_3V_{IN}(\text{avg}))/R_1R_2I_B$

where:

$R_1 = 10k$

$R_2 = 20k$

$R_3 = 20k$

$I_B = 140\mu A$

$V_{IN}(\text{avg})=0.9\ (V_{IN(RMS)})$

In the expandor configuration the rectifier is connected to the input.

EXPANDOR RECIPE

1) DC bias the output halfway between the supply and ground to get maximum headroom. The circuit in Figure 8 is designed around a system supply of 6V so the output DC level should be 3V.

$V_{OUT\ DC}=(1+R_3/R_4)V_{REF}$

where:

$R_3 = 20k$

$R_4 = 30k$

$V_{REF} = 1.8V$

Note that when using a supply voltage higher than 6V the DC output level should be adjusted. To increase the DC output level, it is recommended that R_4 be decreased by adding parallel resistance to it. (Changing R_3 would also affect the expandor's AC gain and thus cause a mismatch in a companding system.)

2) Analyze the input signal's anticipated amplitude:

a) if larger than 2.8V peak, R_2 needs to be increased. (see INGREDIENTS section)

b) if larger than 3.0V peak, R_1 will also need to be increased. (see INGREDIENTS)

By limiting the peak input currents we avoid signal distortion.

3) The input and output decoupling caps need to be large enough not to attenuate any desired frequencies.

4) The C_{RECT} should be 1μF to 2μF for initial setup.

5) An input buffer may be necessary if the source's output impedance needs matching.

6) De-emphasis would be necessary if the complementary compressor circuit had been pre-emphasized (as in a tape deck application). See the Hi-Fi Expandor application in the Linear Data Manual.

7) Distortion (THD) trim pins are available if the already low distortion needs to be further reduced. See Linear Data Manual for trimming network. Note that if not used, the THD trim pins should have 200pF caps to ground.

8) At very low input signal levels, the rectifier's errors become significant and can be reduced with the Low Level Mistracking network (see Linear Data Manual). (This technique prevents infinite expansion at low input levels.)

In the ALC configuration, (Figure 9), the variable gain cell is placed in the feedback loop of the operational amplifier (as in the Compressor) and the rectifier is connected to the input.

As the input amplitude increases above the crossover point, the overall system gain decreases proportionally, holding the output amplitude constant.

As the input amplitude decreases below the crossover point, the overall system gain increases proportionally, holding the output amplitude at the same constant level.

The complete gain equation for the ALC is:

$$\text{Gain} = \frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}\ (\text{avg})}$$

$$\text{Output Level} = \frac{R_1\ R_2\ I_B}{2\ R_3}\left(\frac{V_{IN}}{V_{IN}\ (\text{avg})}\right)$$

$$\text{where } \frac{V_{IN}}{V_{IN}\ (\text{avg})} = \frac{\pi}{2\sqrt{2}} = 1.11 \text{ (for sine wave)}$$

Note that for very low input levels, ALC may not be desired and to limit the maximum gain, resistor R_X has been added. The modified gain equation is:

$$\text{Gain max.} = \frac{(R_1 + R_X) \cdot R_2 \cdot I_B}{2\ R_3}$$

$R_X \cong$ ((desired max gain)×26k)−10k

INGREDIENTS

[Application guidelines for internal and external components (and input/output constraints) needed to tailor (cook) each of the three entrees (applications) to your taste.]

R_1 (10kΩ) limits input current to the rectifier. This current should not exceed an AC peak value of ±300μA. An external resistor may be placed in series with R_1 if the input voltage to the rectifier will exceed ±3.0V peak (i.e., 10k×300μA=3.0V).

R_2 (20kΩ) limits input current to the variable gain cell. This current should not exceed an AC peak value of ±140μA. Again, an external resistor has to be placed in series with R_2 if the input voltage to the variable gain cell exceeds ±2.8V (i.e., 20k×140μA).

R_3 (20kΩ) acts in conjunction with R_4 as the feedback resistor (R_F) (expandor configuration) in the equation. (R_3's value can be either reduced or increased externally.) However, it is recommended that R_4 be the one to change when adjusting the output DC level.

R_4 (30kΩ) acts as the input resistor (R_{IN}) in the standard non-inverting op amp circuit. (Its value can only be reduced.)

$V_{OUT\ DC}=(1+(R_3/R_4))V_{REF}$
(for the Expandor)
$V_{OUT\ DC}=(1+(2R_{DC}/R_4))V_{REF}$
(for the Compandor, ALC)

[The purpose of these DC biasing equations is to allow the designer to set the output halfway between the supply rails for largest headroom (usually some positive voltage and ground).]

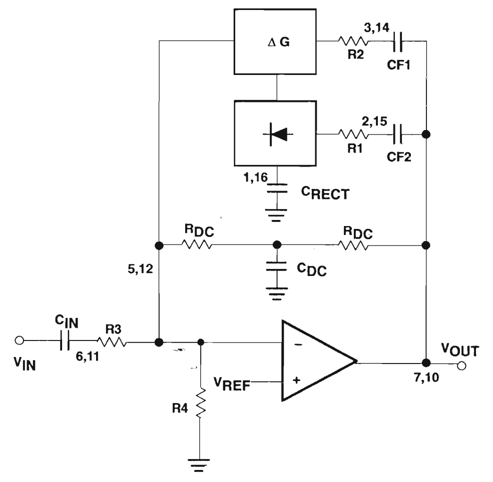


Figure 6. Basic Compressor

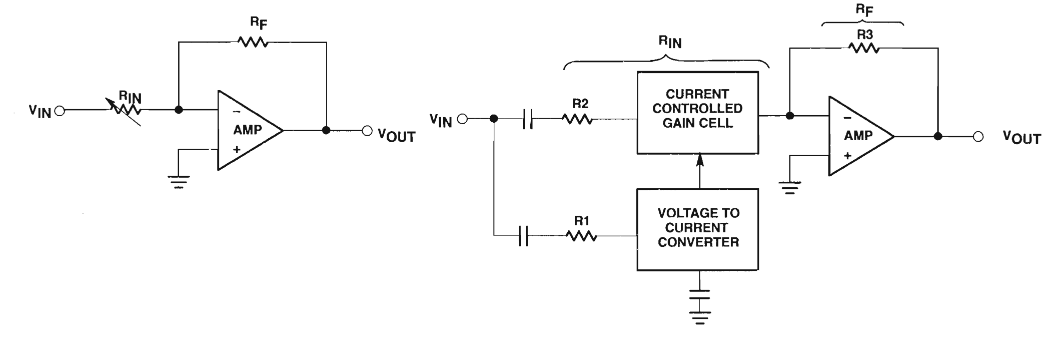


Figure 7. Basic Expandor

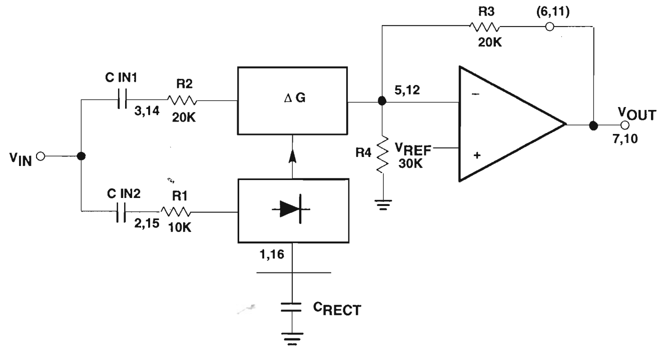


Figure 8. Basic Expandor

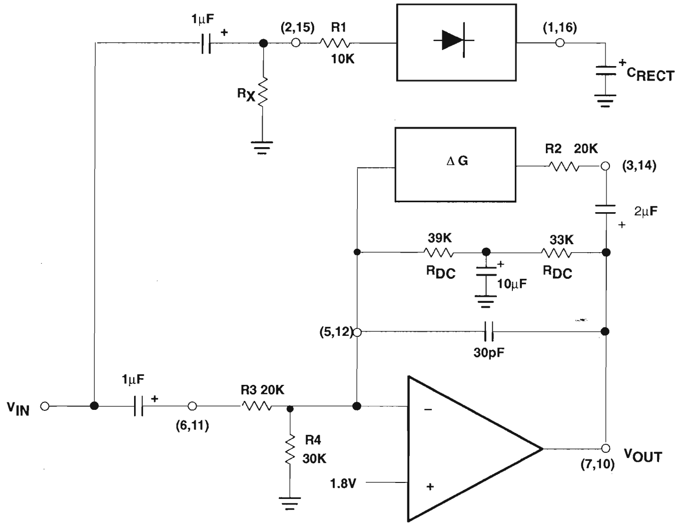


Figure 9. Automatic Level Control

C_{DC} acts as an AC shunt to ground to totally remove the DC biasing resistors from the AC gain equation.

C_F caps are AC signal coupling caps.

C_{RECT} acts as the rectifier's filter cap and directly affects the response time of the circuit. There is a trade-off, though, between fast attack and decay times and distortion.

The time constant is: $10k \times C_{RECT}$

The total harmonic distortion (THD) is approximated by:

$THD \cong (1\mu F/C_{RECT})(1kHz/freq.) \times 0.2\%$

NOTES:

The NE572 differs from the 570/571 in that:

1. There is no internal op amp.
2. The attack and release times are programmed separately.

SYSTEM LEVELS OF A COMPLETE COMPANDING SYSTEM

Figure 10 demonstrates the compressing and expanding functions:

Point A represents a wide dynamic range signal with a maximum amplitude of +16dB and minimum amplitude of –80dB.

Point B represents the compressor output showing a 2:1 reduction in dynamic range (–40dB is increased to –20dB, for example). Point B can also be seen as the dynamic range of a transmission medium. Transmission noise is present at the –60dB level from Point B to Point C.

Point C represents the input signal to the expandor.

Point D represents the output of the expandor. The signal transformation from Point C to D represents a 1:2 expansion.

APPLICATION BOARD

Shown below is the schematic (Figure 11) for Signetics' NE570/571 evaluation/demo board. This board provides one channel of Expansion and one channel of Compression (which can be switched to Automatic Level Control).

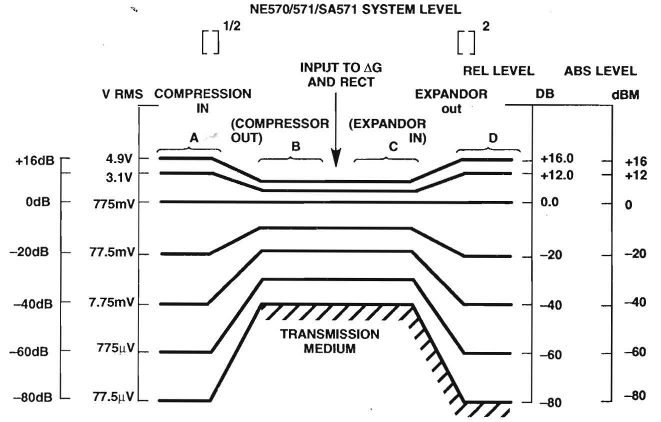


Figure 10. System Levels of a Complete Companding System

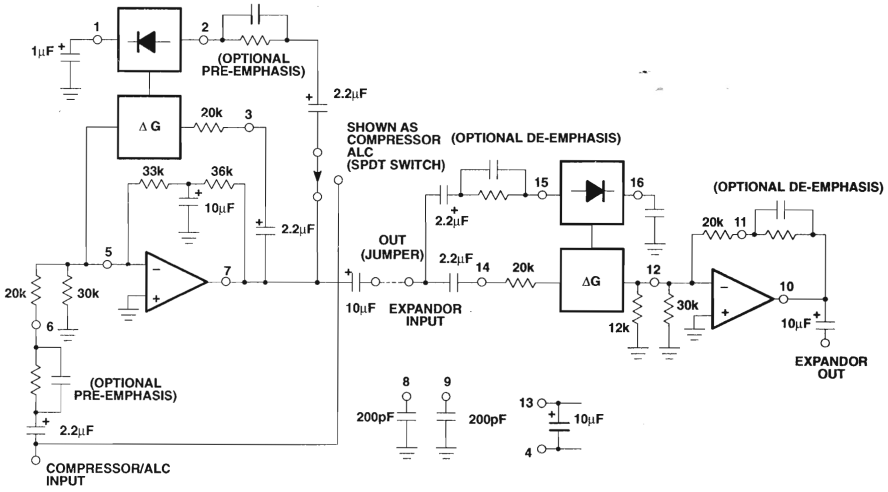


Figure 11.

Programmable analog compandor NE/SA572

DESCRIPTION

The NE572 is a dual-channel, high-performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full-wave rectifier to detect the average value of input signal, a linearized, temperature-compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

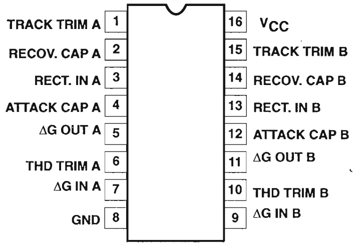
The NE572 is intended for noise reduction in high-performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

- Independent control of attack and recovery time
- Improved low frequency gain control ripple
- Complementary gain compression and expansion with external op amp
- Wide dynamic range—greater than 110dB
- Temperature-compensated gain control
- Low distortion gain cell
- Low noise—6µV typical
- Wide supply voltage range—6V-22V
- System level adjustable with external components

PIN CONFIGURATION

D[1], N, F Packages



NOTE:
1. D package released in large SO (SOL) package only.

APPLICATIONS

- Dynamic noise reduction system
- Voltage control amplifier
- Stereo expandor
- Automatic level control
- High-level limiter
- Low-level noise gate
- State variable filter

ORDERING INFORMATION

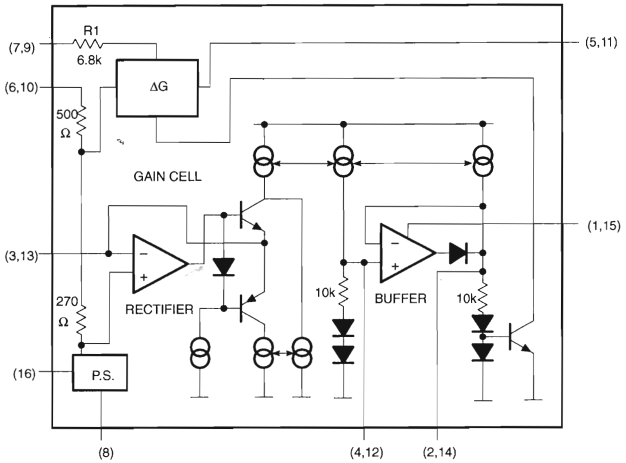
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO)	0 to +70°C	NE572D	0005D
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE572N	0406C
16-Pin Plastic Small Outline (SO)	–40 to +85°C	SA572D	0005D
16-Pin Ceramic Dual In-Line Package (Cerdip)	–40 to +85°C	SA572F	0582B
16-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA572N	0406C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	22	V_{DC}
T_A	Operating temperature range		°C
	NE572	0 to +70	
	SA572	–40 to +85	
P_D	Power dissipation	500	mW

Programmable analog compandor NE/SA572

BLOCK DIAGRAM

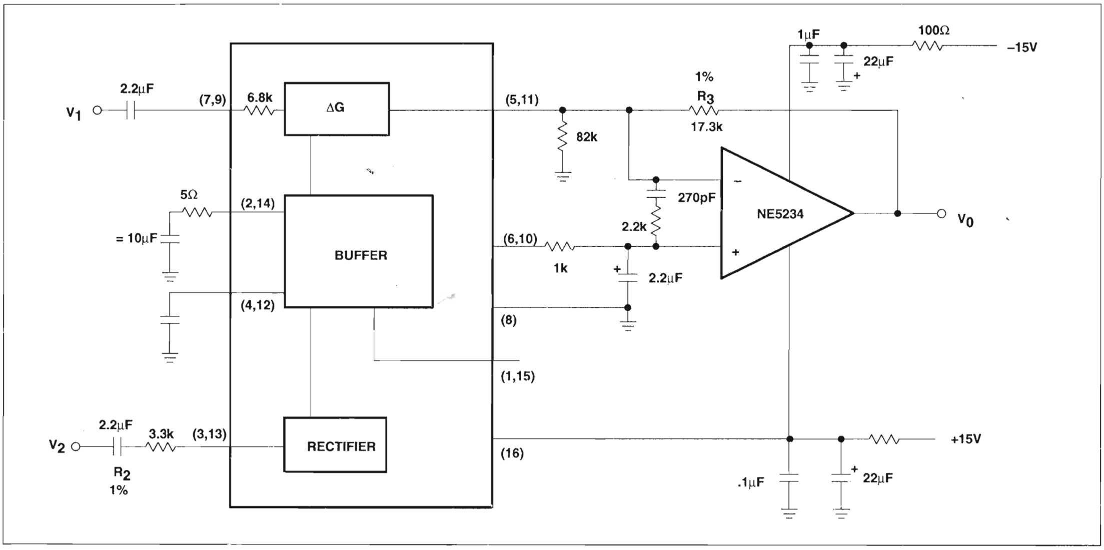


DC ELECTRICAL CHARACTERISTICS

Standard test conditions (unless otherwise noted) V_{CC}=15V, T_A=25°C; Expandor mode (see Test Circuit). Input signals at unity gain level (0dB) = 100mV$_{RMS}$ at 1kHz; $V_1 = V_2$; R_2 = 3.3kΩ; R_3 = 17.3kΩ.

SYMBOL	PARAMETER	TEST CONDITIONS	NE572			SA572			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		6		22	6		22	V_{DC}
I_{CC}	Supply current	No signal			6			6.3	mA
V_R	Internal voltage reference		2.3	2.5	2.7	2.3	2.5	2.7	V_{DC}
THD	Total harmonic distortion (untrimmed)	1kHz C_A=1.0µF		0.2	1.0		0.2	1.0	%
THD	Total harmonic distortion (trimmed)	1kHz C_R=10µF		0.05			0.05		%
THD	Total harmonic distortion (trimmed)	100Hz		0.25			0.25		%
	No signal output noise	Input to V_1 and V_2 grounded (20–20kHz)		6	25		6	25	µV
	DC level shift (untrimmed)	Input change from no signal to 100mV$_{RMS}$		±20	±50		±20	±50	mV
	Unity gain level		−1	0	+1	−1.5	0	+1.5	dB
	Large–signal distortion	V_1=V_2=400mV		0.7	3.0		0.7	3	%
	Tracking error (measured relative to value at unity gain)= [V_O–V_O (unity gain)]dB –V_2dB	Rectifier input V_2=+6dB V_1=0dB V_2=–30dB V_1=0dB		±0.2 ±0.5	–1.5 +0.8		±0.2 ±0.5	–2.5 +1.6	dB
	Channel crosstalk	200mV$_{RMS}$ into channel A, measured output on channel B	60			60			dB
PSRR	Power supply rejection ratio	120Hz		70			70		dB

TEST CIRCUIT



AUDIO SIGNAL PROCESSING IC COMBINES VCA AND FAST ATTACK/SLOW RECOVERY LEVEL SENSOR

In high-performance audio gain control applications, it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Signetics NE572 this high-performance noise reduction concept becomes feasible for consumer hi fi applications. The NE572 is a dual channel gain control IC. Each channel has a linearized, temperature-compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current-to-voltage conversion, the VCA features low distortion, low noise and wide dynamic range.

The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor C_A with an internal 10k resistor R_A defines the attack time t_A. The recovery time t_R of a tone burst is defined by a recovery capacitor C_R and an internal 10k resistor R_R. Typical attack time of 4ms for the high-frequency spectrum and 40ms for the low frequency band can be obtained with 0.1μF and 1.0μF attack capacitors, respectively. Recovery time of 200ms can be obtained with a 4.7μF recovery capacitor for a 100Hz signal, the third harmonic distortion is improved by more than 10dB over the simple RC ripple filter with a single 1.0μF attack and recovery capacitor, while the attack time remains the same.

The NE572 is assembled in a standard 16-pin dual in-line plastic package and in oversized SOL package. It operates over a wide supply range from 6V to 22V. Supply current is less than 6mA. The NE572 is designed for consumer application over a temperature range 0-70 The SA572 is intended for applications from –40°C to +85°C.

NE572 BASIC APPLICATIONS

Description

The NE572 consists of two linearized, temperature-compensated gain cells (ΔG), each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 1 shows the circuit configuration of the gain cell. Bases of the differential pairs Q_1-Q_2 and Q_3-Q_4 are both tied to the output and inputs of OPA A_1. The negative feedback through Q_1 holds the V_{BE} of Q_1-Q_2 and the V_{BE} of Q_3-Q_4 equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\Delta V_{BE_{Q3Q4}} = \Delta_{BE_{Q1Q2}}$$

$(V_{BE} = V_T \, l_{IN} \, IC/IS)$

$$V_T l_n \left(\frac{\frac{1}{2} I_G + \frac{1}{2} I_O}{I_S} \right) - V_T l_n \left(\frac{\frac{1}{2} I_G - \frac{1}{2} I_O}{I_S} \right)$$

where $I_{IN} = \frac{V_{IN}}{R_1}$

$R_1 = 6.8k\Omega$
$I_1 = 140\mu A$
$I_2 = 280\mu A$

$$V_T l_n \left(\frac{I_1 + I_{IN}}{I_S} \right) - V_T l_n \left(\frac{I_2 - I_1 - I_{IN}}{I_S} \right) \quad (2)$$

where $I_{IN} = \frac{V_{IN}}{R_1}$

$R_1 = 6.8k\Omega$
$I_1 = 140\mu A$
$I_2 = 280\mu A$

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, equation (2) can be simplified to:

$$I_O = \frac{2}{I_2} \cdot I_{IN} \cdot I_G - \frac{1}{I_2}(I_2 - 2I_1) \cdot I_G \qquad (3)$$

The first term of Equation 3 shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feedthrough due to the mismatch of devices. In the design, this has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within ±25µA into the THD trim pin.

The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improve ripple distortion significantly. At the unity gain level of 100mV, the gain cell gives THD (total harmonic distortion) of 0.17% typ. Output noise with no input signals is only 6µV in the audio spectrum (10Hz-20kHz). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at V_{REF} if the output current I_O is DC coupled.

Rectifier

The rectifier is a full-wave design as shown in Figure 2. The input voltage is converted to current through the input resistor R_2 and turns on either Q_5 or Q_6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A_2. If AC coupling is used, the rectifier error comes only from input bias current of gain block A_2. The input bias current is typically about 70nA. Frequency response of the gain block A_2 also causes second-order error at high frequency. The collector current of Q_6 is mirrored and summed at the collector of Q_5 to form the full wave rectified output current I_R. The rectifier transfer function is

$$I_R = \frac{V_{IN} - V_{REF}}{R_2} \qquad (4)$$

If V_{IN} is AC-coupled, then the equation will be reduced to:

$$I_{RAC} = \frac{V_{IN}(AVG)}{R_2}$$

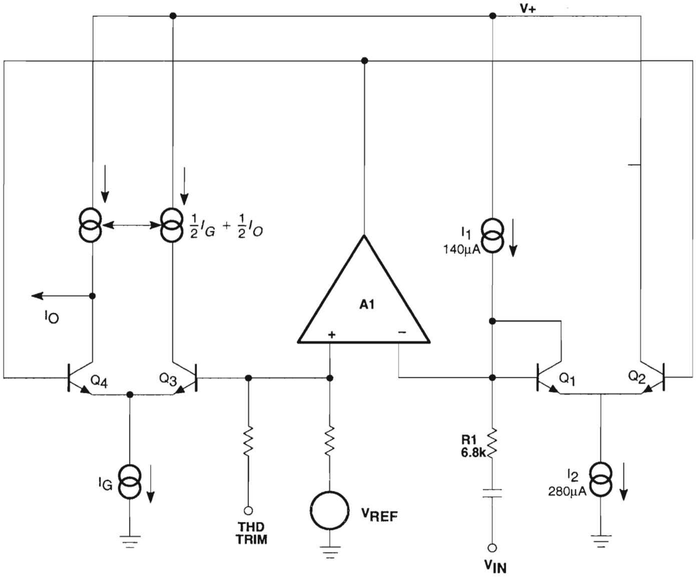


Figure 1. Basic Gain Cell Schematic

The internal bias scheme limits the maximum output current I_R to be around 300µA. Within a ±1dB error band the input range of the rectifier is about 52dB.

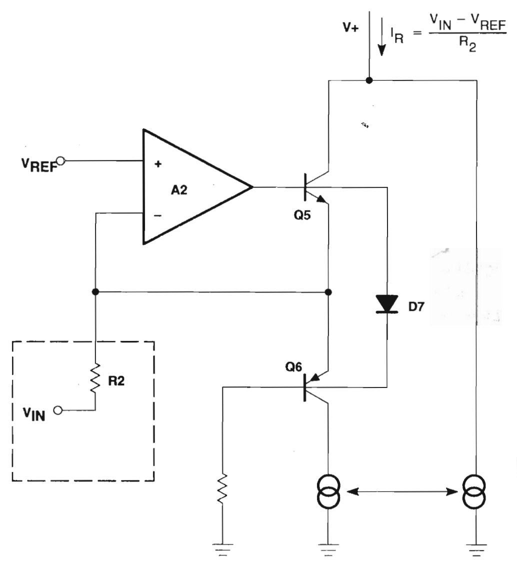


Figure 2. Simplified Rectifier Schematic

Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low-frequency ripple distortion. The low-frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Referring to Figure 3, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A_3 through Q_8, Q_9 and Q_{10}. Diodes D_{11} and D_{12} improve tracking accuracy and provide common-mode bias for A_3. For a positive-going input signal, the buffer amplifier acts like a voltage-follower. Therefore, the output impedance of A_3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance, the gain Ga(t) for ΔG can be expressed as follows:

$$Ga(t) = (Ga_{INT} - Ga_{FNL}\, e^{\frac{-t}{\tau_A}} + Ga_{FNL}$$

Ga_{INT}=Initial Gain

Ga_{FNL}=Final Gain

$\tau_A = R_A \bullet CA = 10k \bullet CA$

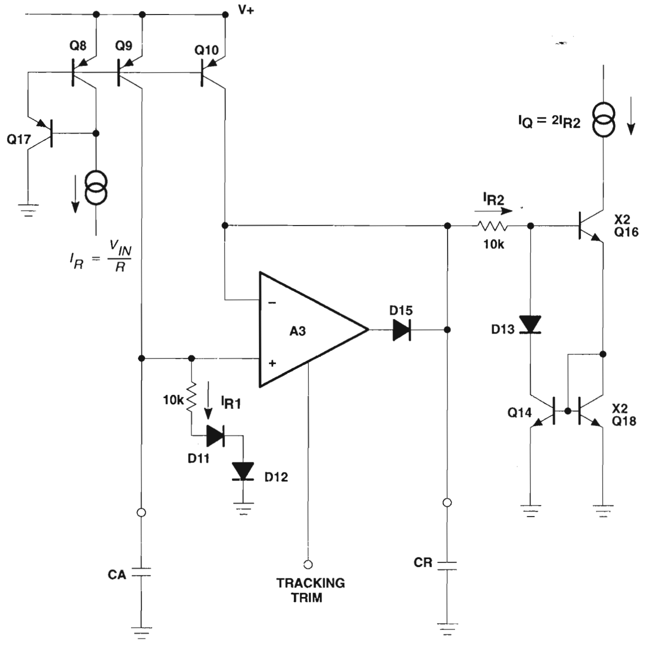


Figure 3. Buffer Amplifier Schematic

where τ_A is the attack time constant and R_A is a 10k internal resistor. Diode D_{15} opens the feedback loop of A_3 for a negative-going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR • R_R. If the diode impedance is assumed negligible, the dynamic gain G_R (t) for ΔG is expressed as follows.

$$G_R(t) = (G_{RINT} - G_{RFNL}\, e^{\frac{-t}{\tau_R}} + G_{RFNL}$$

$$G_R(t)=(G_{R\ INT}-G_{R\ FNL})\ e\ +G_{R\ FNL}$$

$$\tau R=R_R \bullet CR=10k \bullet CR$$

where τR is the recovery time constant and R_R is a 10k internal resistor. The gain control current is mirrored to the gain cell through Q_{14}. The low level gain errors due to input bias current of A_2 and A_3 can be trimmed through the tracking trim pin into A_3 with a current source of ±3μA.

Basic Expandor

Figure 4 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{I_1} \cdot \frac{R_3 \cdot V_{IN(AVG)}}{R_2 \cdot R_1} \qquad (5)$$

$(I_1=140\mu A)$

Both the resistors R_1 and R_2 are tied to internal summing nodes. R_1 is a 6.8k internal resistor. The maximum input current into the gain cell can be as large as 140μA. This corresponds to a voltage level of 140μA • 6.8k=952mV peak. The input peak current into the rectifier is limited to 300μA by the internal bias system. Note that the value of R_1 can be increased to accommodate higher input level. R_2 and R_3 are external resistors. It is easy to adjust the ratio of R_3/R_2 for desirable system voltage and current levels. A small R_2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer A_1 may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA A_2. R_3 and A_2 convert the gain cell output current to the output voltage. In high-performance applications, A_2 has to be low-noise, high-speed and wide band so that the high-performance output of the gain cell will not be degraded. The non-inverting input of A_2 can be biased at the low noise internal reference Pin 6 or 10. Resistor R_4 is used to bias up the output DC level of A_2 for maximum swing. The output DC level of A_2 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_3}{R_4}\right) - V_B\,\frac{R_3}{R_4} \qquad (6)$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant. *5COL

Basic Compressor

Figure 5 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A_1. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{I_1}{2} \cdot \frac{R_2 \cdot R_1}{R_3 \cdot V_{IN(AVG)}}\right)^{\frac{1}{2}} \qquad (7)$$

R_{DC1}, R_{DC2}, and CDC form a DC feedback for A_1. The output DC level of A_1 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right) \qquad (8)$$

$$- V_B \cdot \left(\frac{R_{DC1} + R_{DC2}}{R_4}\right)$$

The zener diodes D_1 and D_2 are used for channel overload protection.

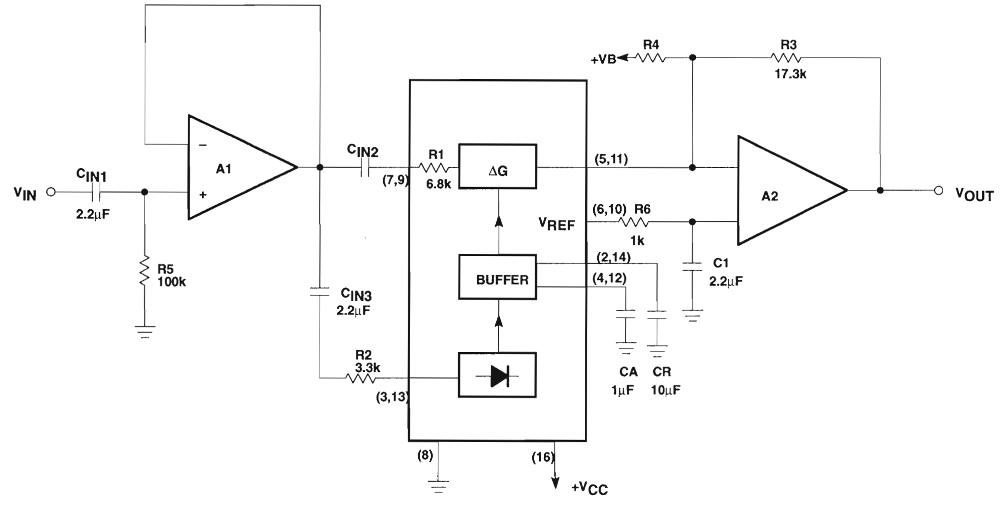


Figure 4. Basic Expandor Schematic

Basic Compandor System

The above basic compressor and expandor can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 6 shows the system level diagram for reference.

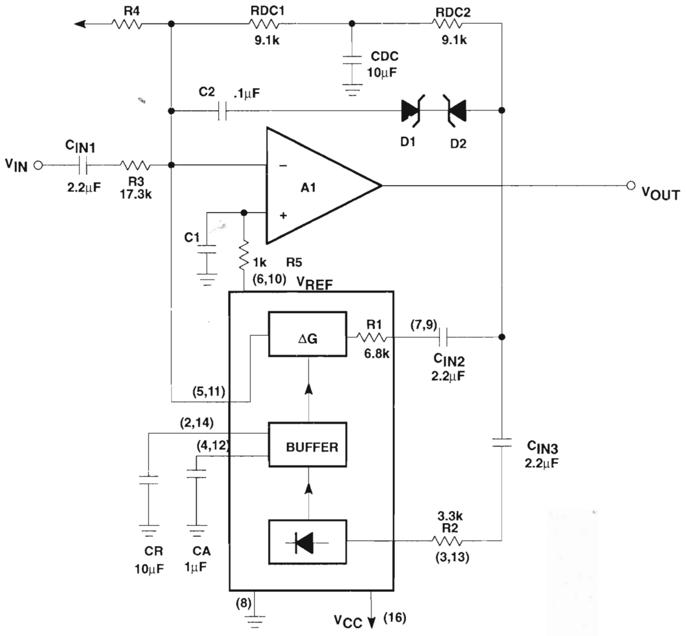


Figure 5. Basic Compressor Schematic

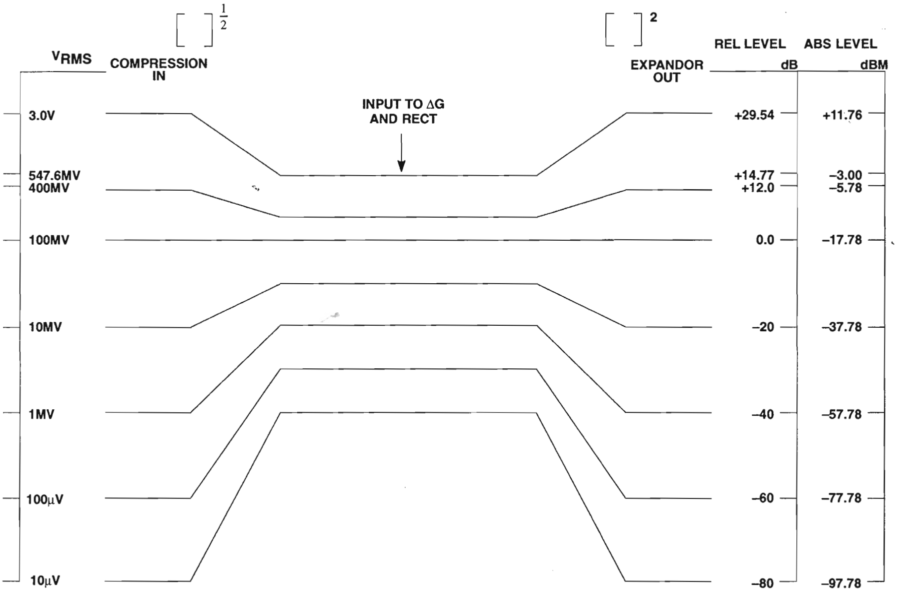
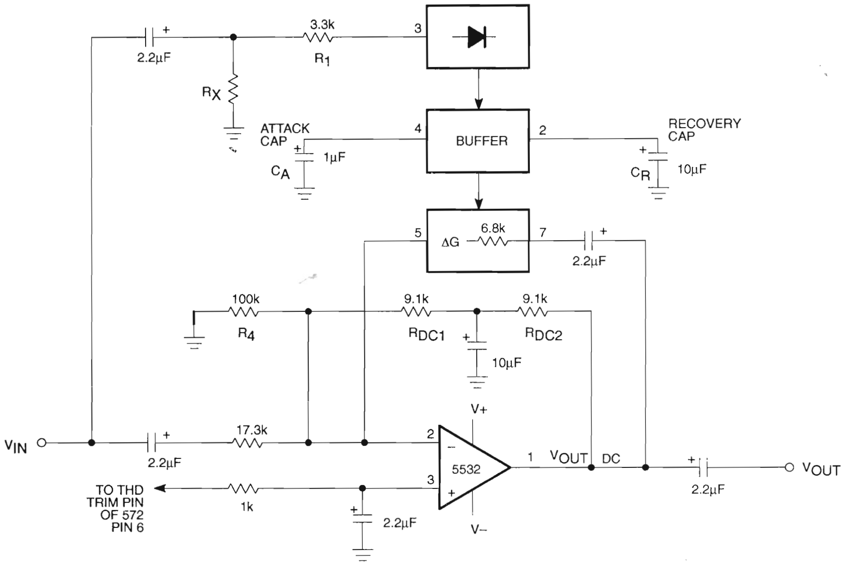


Figure 6. NE572 System Level

NE572 AUTOMATIC LEVEL CONTROL



$$V_{ODC} = V_{REF}\left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right)$$

WHERE: $R_4 = 100k$
$R_{DC1} = R_{DC2} = 9.1k$
$V_{REF} = 2.5V$

$$\text{OUTPUT LEVEL} = \left(\frac{R_1\ R_2\ I_B}{2R_3}\right)\left(\frac{V_{IN}}{V_{IN(avg)}}\right)$$

WHERE: $R_1 = 6.8k$ (Internal)
$R_2 = 3.3k$
$R_3 = 17.3k$
$I_B = 140\mu A$

$$\text{Gain} = \frac{R_1\ R_2\ I_B}{2R_3\ V_{IN}\ (\text{avg})}$$

ATTACK TIME = (10k) C_A

RECOVERY TIME = (10k) C_R

TO LIMIT THE GAIN AT VERY LOW INPUT LEVELS, ADD R_X:

$$\text{GAIN MAX.} = \frac{\dfrac{R_1 + R_X}{2.5V} \times R_2 \times I_B}{2R_3}$$

$$\frac{V_{IN}}{V_{IN(avg)}} = \frac{\pi}{2\sqrt{2}} = 1.11$$

(FOR SINE WAVES)

NOTE:
Pin numbers are for side A of the NE572.

Low voltage compandor

NE/SA575

DESCRIPTION

The NE/SA575 is a precision dual gain control circuit designed for low voltage applications. The NE/SA575's channel 1 is an expandor, while channel 2 can be configured either for expandor, compressor, or automatic level controller (ALC) application.

FEATURES

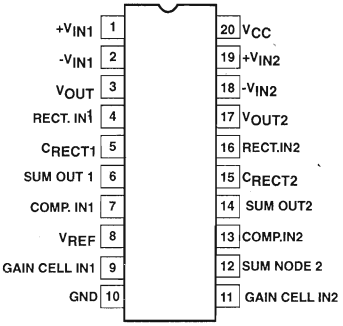
- Operating voltage range from 3V to 7V
- Reference voltage of 100mV$_{RMS}$ = 0dB
- One dedicated summing op amp per channel and two extra uncommitted op amps
- 600Ω drive capability
- Single or split supply operation
- Wide input/output swing capability
- 3000V ESD protection

APPLICATIONS

- Portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Portable broadcast mixers
- Wireless microphones
- Modems
- Electric organs
- Hearing aids

PIN CONFIGURATION

N, D[1] and DK Packages



NOTE:
1. Available in large SOL package only.

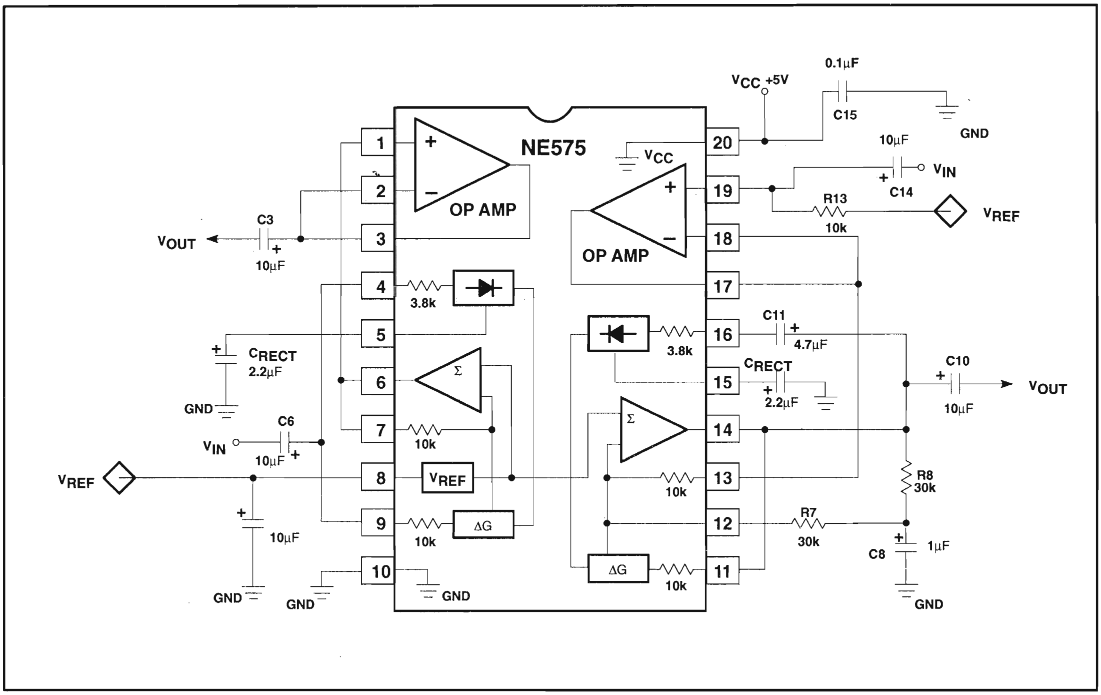
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG
20-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE575N	0408B
20-Pin Plastic Small Outline Large	0 to +70°C	NE575D	0172D
20-Pin Plastic Shrink Small Outline Package (SSOP)	0 to +70°C	NE575DK	1563–
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA575N	0408B
20-Pin Plastic Small Outline Large	-40 to +85°C	SA575D	0172D
20-Pin Plastic Shrink Small Outline Package (SSOP)	-40 to +85°C	SA575DK	1563–

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING		UNITS
			NE575	SA575	
V_{CC}	Single supply voltage		–0.3 to 8	–0.3 to 8	V
V_{IN}	Voltage applied to any other pin		–0.3 to (V_{CC}+0.3)	–0.3 to (V_{CC}+0.3)	V
T_A	Operating ambient temperature range		-40 to +85	-40 to +85	°C
T_{STG}	Storage temperature range		-65 to +150	-65 to +150	°C
θ_{JA}	Thermal impedance	DIP	68	68	°C/W
		SOL	112	112	°C/W
		SSOP	117	117	°C/W

BLOCK DIAGRAM and TEST CIRCUIT



DC ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 25°C. Minimum and Maximum values are for the full operating temperature range: 0 to 70°C for NE575, -40 to +85°C for SA575, except SSOP package is tested at +25°C only. V_{CC} = 5V, unless otherwise stated. Both channels are tested in the Expandor mode (see Test Circuit)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE575			SA575			
			MIN	TYP	MAX	MIN	TYP	MAX	
For compandor, including summing amplifier									
V_{CC}	Supply voltage[1]		3	5	7	3	5	7	V
I_{CC}	Supply current	No signal	3	4.2	5.5	3	4.2	5.5	mA
V_{REF}	Reference voltage[2]	V_{CC} = 5V	2.4	2.5	2.6	2.4	2.5	2.6	V
R_L	Summing amp output load		10			10			kΩ
THD	Total harmonic distortion	1kHz, 0dB BW = 3.5kHz		0.12	1.0		0.12	1.5	%
E_{NO}	Output voltage noise	BW = 20kHz, R_S = 0Ω		6	20		6	30	µV
0dB	Unity gain level	1kHz	-1.0		1.0	-1.5		1.5	dB
V_{OS}	Output voltage offset	No signal	-100		100	-150		150	mV
	Output DC shift	No signal to 0dB	-50		50	-100		100	mV
	Tracking error relative to 0dB	Gain cell input = 0dB, 1kHz Rectifier input = 6dB, 1kHz	-0.5		0.5	-1.0		1.0	dB
		Gain cell input = 0dB, 1kHz Rectifier input = -30dB, 1kHz	-0.5		0.5	-1.0		1.0	dB

DC ELECTRICAL CHARACTERISTICS (cont.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE575			SA575			
			MIN	TYP	MAX	MIN	TYP	MAX	
	Crosstalk	1kHz, 0dB, C_{REF} = 220µF		-80	-65		-80	-65	dB
For operational amplifier									
V_O	Output swing	R_L = 10kΩ	V_{CC}-0.4	V_{CC}		V_{CC}-0.4	V_{CC}		V
R_L	Output load	1kHz	600			600			Ω
CMR	Input common-mode range		0		V_{CC}	0		V_{CC}	V
CMRR	Common-mode rejection ratio		60	80		60	80		dB
I_B	Input bias current	V_{IN} = 0.5V to 4.5V	-0.5		0.5	-1		1	µA
V_{OS}	Input offset voltage			3			3		mV
A_{VOL}	Open-loop gain	R_L = 10kΩ		80			80		dB
SR	Slew rate	Unity gain		1			1		V/µs
GBW	Bandwidth	Unity gain		3			3		MHz
E_{NI}	Input voltage noise	BW = 20kHz		2.5			2.5		µV
PSRR	Power supply rejection ratio	1kHz, 250mV		60			60		dB

NOTES:
1. Operation down to V_{CC} = 2V is possible, but performance is reduced. See curves in Figure 5a and 5b.
2. Reference voltage, V_{REF}, is typically at 1/2V_{CC}.

FUNCTIONAL DESCRIPTION

This section describes the basic subsystems and applications of the NE/SA575 Compandor. More theory of operation on compandors can be found in AN174 and AN176. The typical applications of the NE/SA575 low voltage compandor in an Expandor (1:2), Compressor (2:1) and Automatic Level Control (ALC) function are explained. These three circuit configurations are shown in Figures 1, 2, 3 respectively.

The NE/SA575 has two channels for a complete companding system. The left channel, A, can be configured as a 1:2 Expandor while the right channel, B, can be configured as either a 2:1 Compressor, a 1:2 Expandor or an ALC. Each channel consists of the basic companding building blocks of rectifier cell, variable gain cell, summing amplifier and V_{REF} cell. In addition, the NE/SA575 has two additional high performance uncommitted op amps which can be utilized for application such as filtering, pre-emphasis/de-emphasis or buffering.

Figure 4 shows the complete schematic for the applications demo board. Channel A is configured as an expandor while channel B is configured so that it can be used either as a compressor or as an ALC circuit. The switch, S1, toggles the circuit between compressor and ALC mode. Jumpers J1 and J2 can be used to either include the additional op amps for signal conditioning or exclude them from the signal path. Bread boarding space is provided for R1, R2, C1, C2, R10, R11, C10 and C11 so that the response can be tailored for each individual need. The components as specified are suitable for the complete audio spectrum from 20Hz to 20kHz.

The most common configuration is as a unity gain non-inverting buffer where R1, C1, C2, R10, C10 and C11 are eliminated and R2 and R11 are shorted. Capacitors C3, C5, C8, and C12 are for DC blocking. In systems where the inputs and outputs are AC coupled, these capacitors and resistors can be eliminated. Capacitors C4 and C9 are for setting the attack and release time constant.

C6 is for decoupling and stabilizing the voltage reference circuit. The value of C6 should be such that it will offer a very low impedance to the lowest frequencies of interest. Too small a capacitor will allow supply ripple to modulate the audio path. The better filtered the power supply, the smaller this capacitor can be. R12 provides DC reference voltage to the amplifier of channel B. R6 and R7 provide a DC feedback path for the summing amp of channel B, while C7 is a short-circuit to ground for signals. C14 and C15 are for power supply decoupling. C14 can also be eliminated if the power supply is well regulated with very low noise and ripple.

DEMONSTRATED PERFORMANCE

The applications demo board was built and tested for a frequency range of 20Hz to 20kHz with the component values as shown in Figure 4 and V_{CC} = 5V. In the expandor mode, the typical input dynamic range was from -34dB to +12dB where 0dB is equal to 100mV_{RMS}. The typical unity gain level measured at 0dB @ 1kHz input was ±0.5dB and the typical tracking error was ±0.1dB for input range of -30 to +10dB.

In the compressor mode, the typical input dynamic range was from -42dB to ±18dB with a tracking error +0.1dB and the typical unity gain level was ±0.5dB.

In the ALC mode, the typical input dynamic range was from -42dB to +8dB with typical output deviation of ±0.2dB about the nominal output of 0dB. For input greater than +9dB in ALC configuration, the summing amplifier sometimes exhibits high frequency oscillations. There are several solutions to this problem. The first is to lower the values of R6 and R7 to 20kΩ each. The second is to add a current limiting resistor in series with C12 at Pin 13. The third is to add a compensating capacitor of about 22 to 30pF between the input and output of summing amplifier (Pins 12 and 14). With any one of the above recommendations, the typical ALC mode input range increased to +18dB yielding a dynamic range of over 60dB.

EXPANDOR

The typical expandor configuration is shown in Figure 1. The variable gain cell and the rectifier cell are in the signal input path. The V_{REF} is always 1/2 V_{CC} to provide the maximum headroom without clipping. The 0dB ref is 100mV_{RMS}. The input is AC coupled through C5, and the output is AC coupled through C3. If in a system the inputs and outputs are AC coupled, then C3 and C5 can be eliminated, thus requiring only one external component, C4. The variable gain cell and rectifier cell are DC coupled so any offset

voltage between Pins 4 and 9 will cause small offset error current in the rectifier cell. This will affect the accuracy of the gain cell. This can be improved by using an extra capacitor from the input to Pin 4 and eliminating the DC connection between Pins 4 and 9.
The expandor gain expression and the attack and release time constant is given by Equation 1 and Equation 2, respectively.

Equation 1.

$$\text{Expandor gain} = \frac{4V_{IN}(avg)}{3.8k \times 100\mu A}$$

where $V_{IN}(avg) = 0.95V_{IN(RMS)}$

Equation 2.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$$

COMPRESSOR

The typical compressor configuration is shown in Figure 2. In this mode, the rectifier cell and variable gain cell are in the feedback path. R6 and R7 provide the DC feedback to the summing amplifier. The input is AC coupled through C12 and output is AC coupled through C8. In a system with inputs and outputs AC coupled, C8 and C12 could be eliminated and only R6, R7, C7, and C13 would be required. If the external components R6, R7 and C7 are eliminated, then the output of the summing amplifier will motor-boat in absence of signals or at extremely low signals. This is because there is no DC feedback path from the output to input. In the presence of an AC signal this phenomenon is not observed and the circuit will appear to function properly.
The compressor gain expression and the attack and release time constant is given by Equation 3 and Equation 4, respectively.

Equation 3.

$$\text{Compressor gain} = \left[\frac{3.8k \times 100\mu A}{4V_{IN}(avg)}\right]^{1/2}$$

where $V_{IN}(avg) = 0.95V_{IN(RMS)}$

Equation 4.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$$

AUTOMATIC LEVEL CONTROL

The typical Automatic Level Control circuit configuration is shown in Figure 3. It can be seen that it is quite similar to the compressor schematic except that the input to the rectifier cell is from the input path and not from the feedback path. The input is AC coupled through C12 and C13 and the output is AC coupled through C8. Once again, as in the previous cases, if the system input and output signals are already AC coupled, then C12, C13 and C8 could be eliminated. Concerning the compressor, removing R6, R7 and C7 will cause motor-boating in absence of signals. C_{COMP} is necessary to stabilize the summing amplifier at higher input levels. This circuit provides an input dynamic range greater than 60dB with the output within ±0.5dB typical. The necessary design expressions are given by Equation 5 and Equation 6, respectively.

Equation 5.

$$\text{ALC gain} = \frac{3.8k \times 100\mu A}{4V_{IN}(avg)}$$

Equation 6.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C9$$

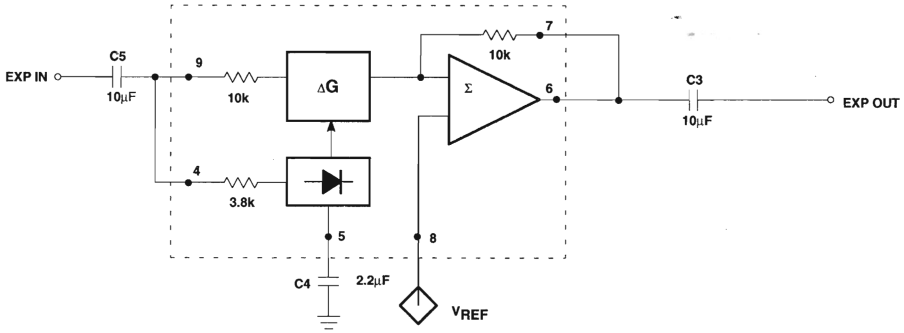


Figure 1. Typical Expandor Configuration

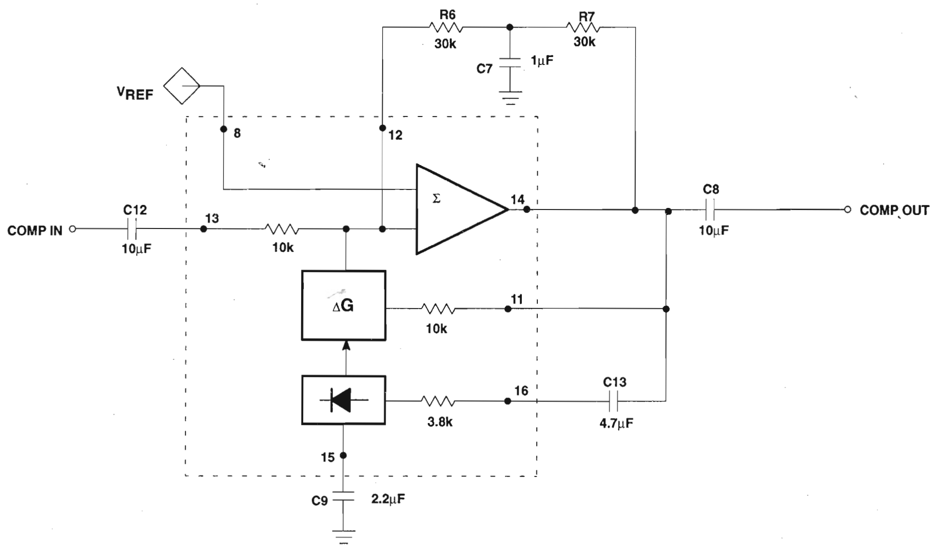


Figure 2. Typical Compressor Configuration

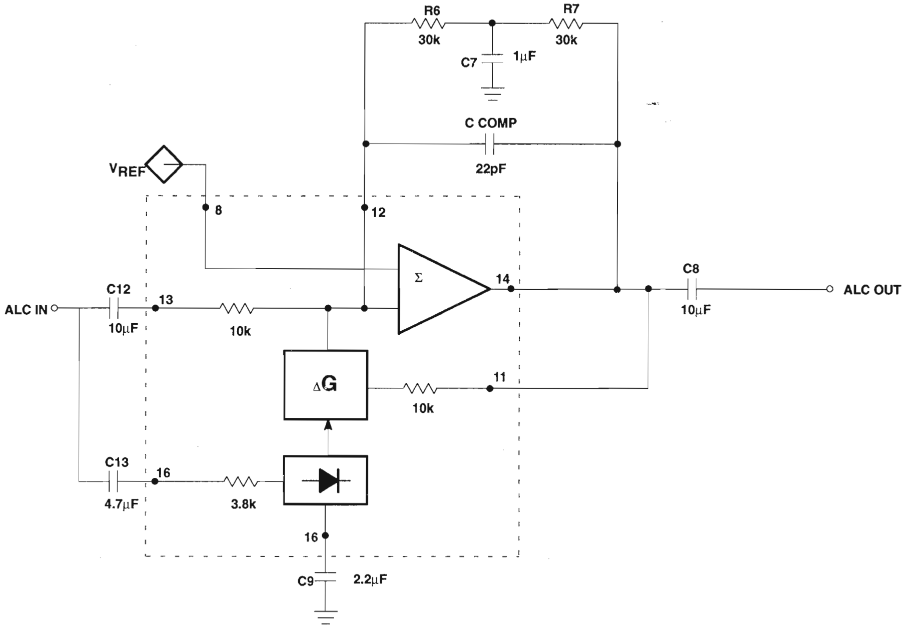


Figure 3. Typical ALC Configuration

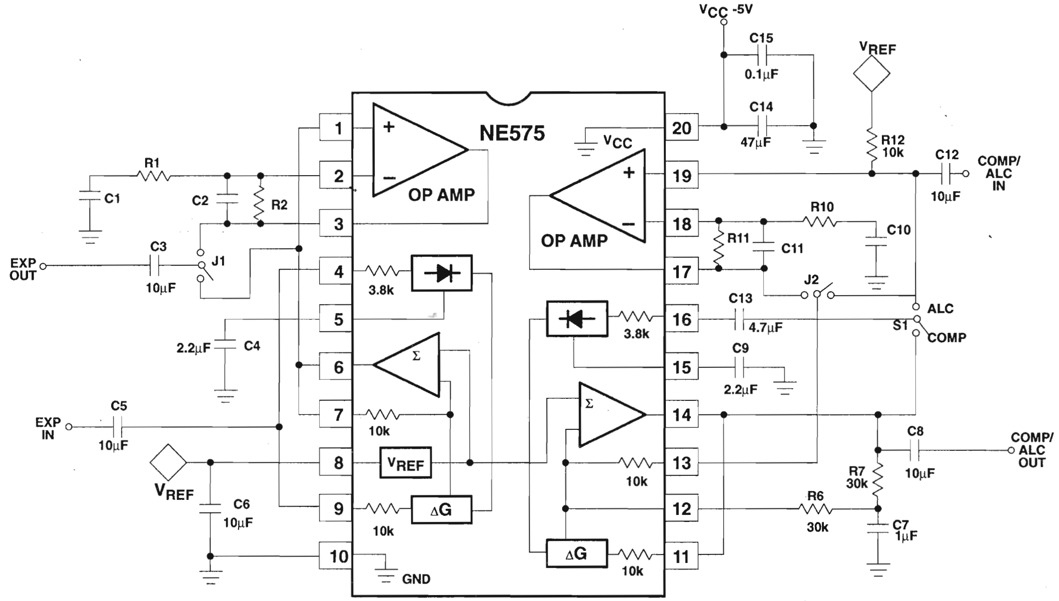
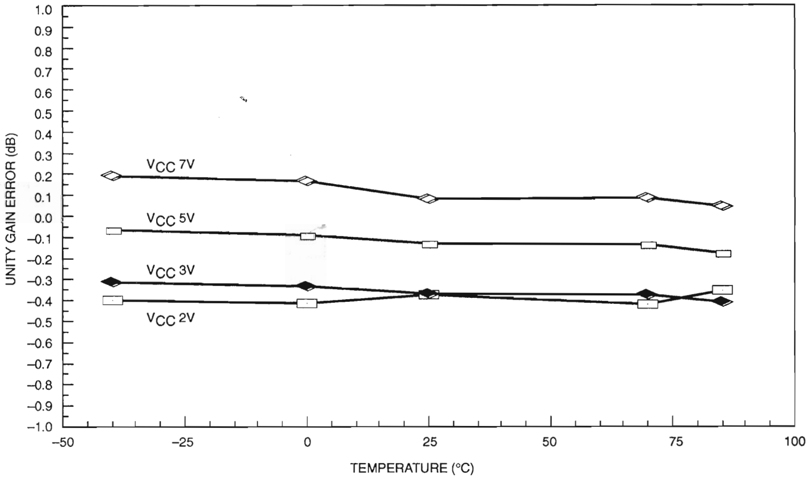
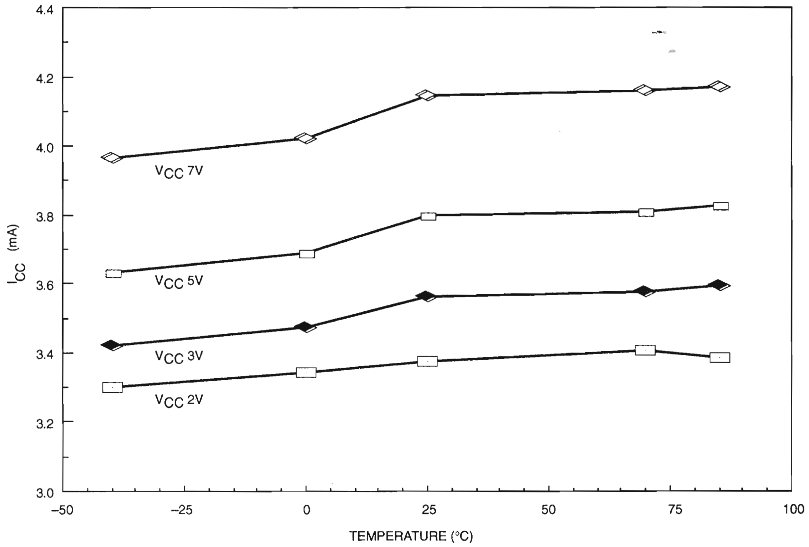


Figure 4. NE/SA575 Low Voltage Expandor/Compressor/ALC Demo Board



a. Unity Gain Error vs Temperature and V_{CC}



b. I_{CC} vs Temperature and V_{CC}

Figure 5. Temperature and V_{CC} Curves

TYPICAL PERFORMANCE CHARACTERISTICS

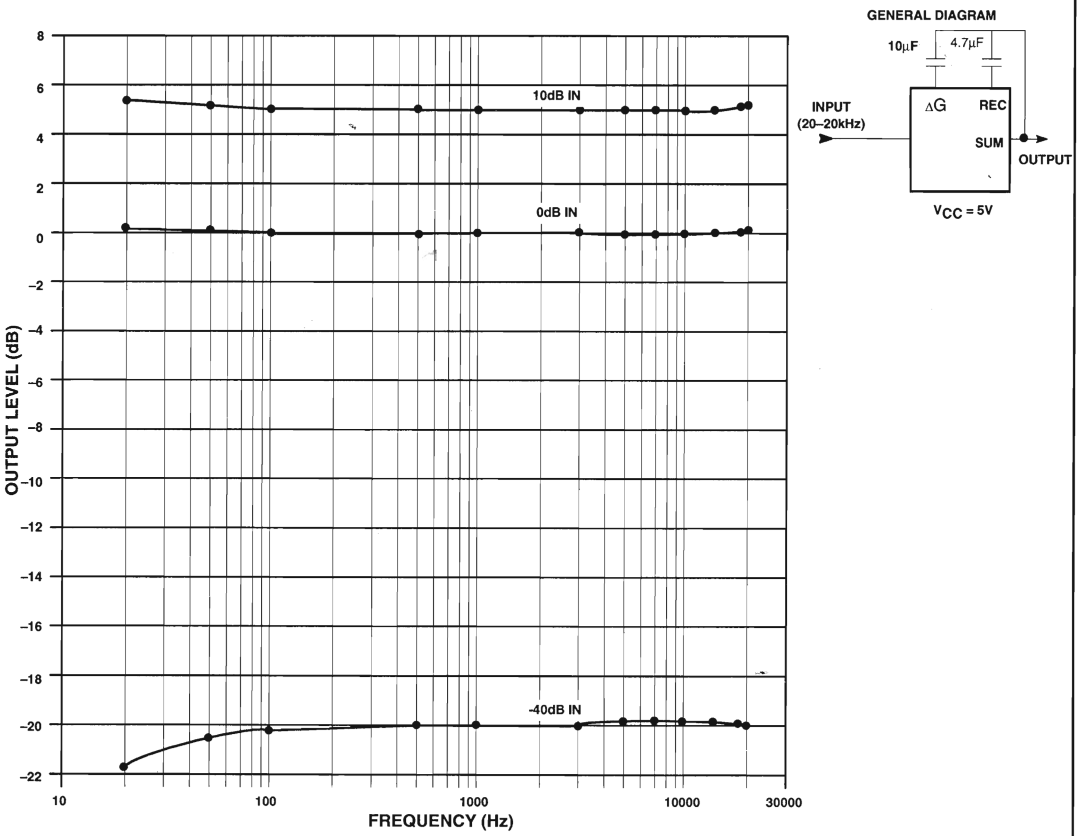


Figure 6. Compressor Output Frequency Response

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

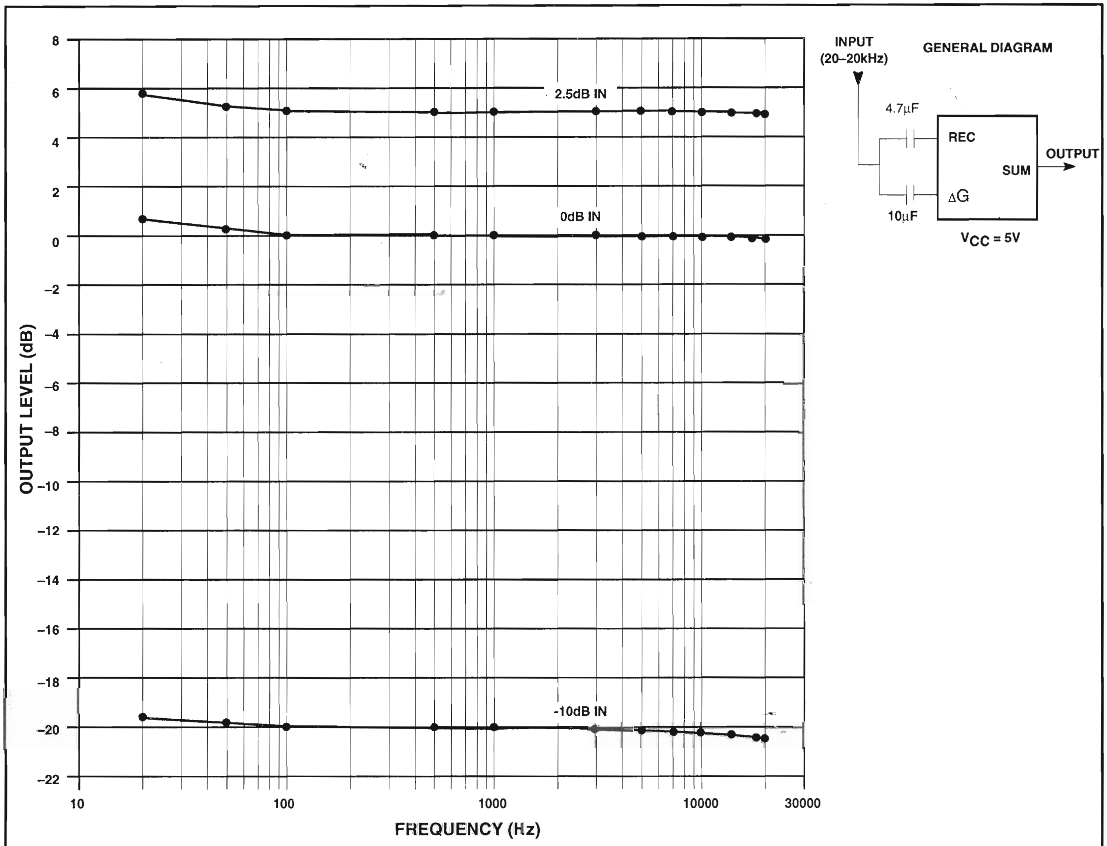


Figure 7. Expandor Output Frequency Response

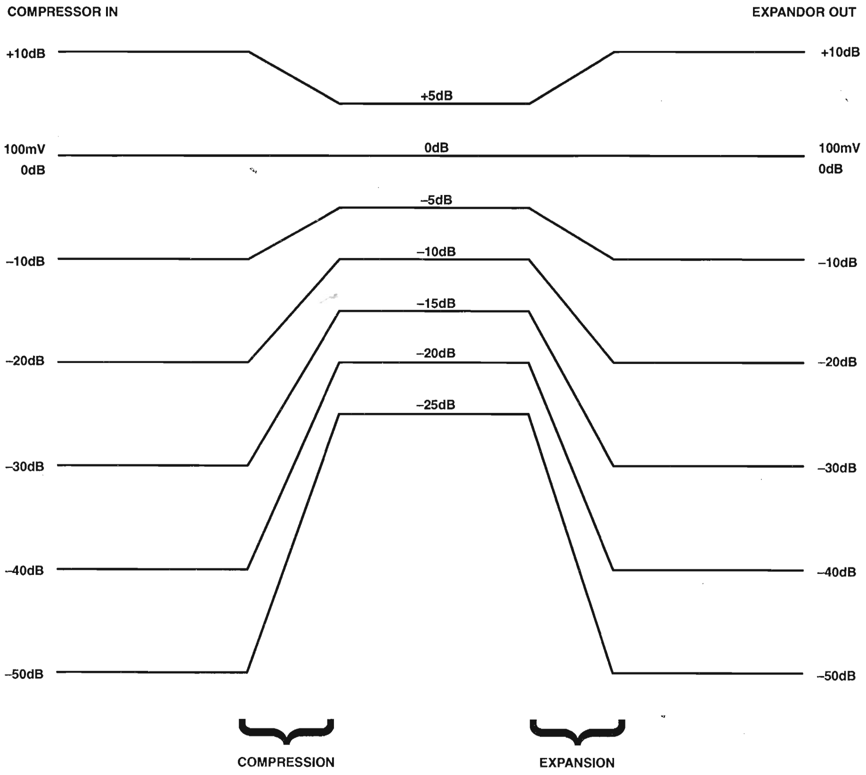


Figure 8. The Companding Function

DESCRIPTION

The NE/SA576 is a unity gain level programmable compandor designed for low power applications. The NE576 is internally configured as an expandor and a compressor to minimize external component count.

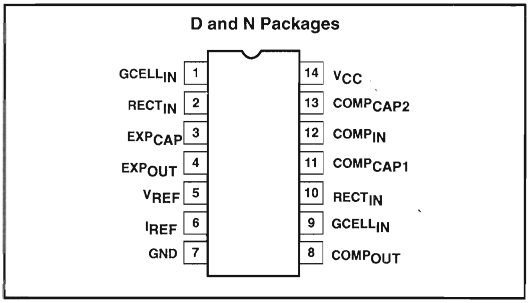
The NE576 can operate at 1.8V. During normal operations, the NE576 can operate from at least a 2V battery. If the battery voltage drops to 1.8V, this part will still continue to function, however, turning on the part at a V_{CC} of 1.8V requires two external resistors to bring V_{REF} to half V_{CC}. One resistor connects between V_{CC} and V_{REF}; the other connects from V_{REF} to ground. A typical value for these external resistors is approximately 20k. A lower value can be used, but the power consumption will go up.

The NE576 is available in a 14-pin plastic DIP and SO packages.

FEATURES

- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- Over 80dB of dynamic range
- Wide input/output swing capability (rail-to-rail)
- Low external component count
- ESD hardened

PIN CONFIGURATION



APPLICATIONS

- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control

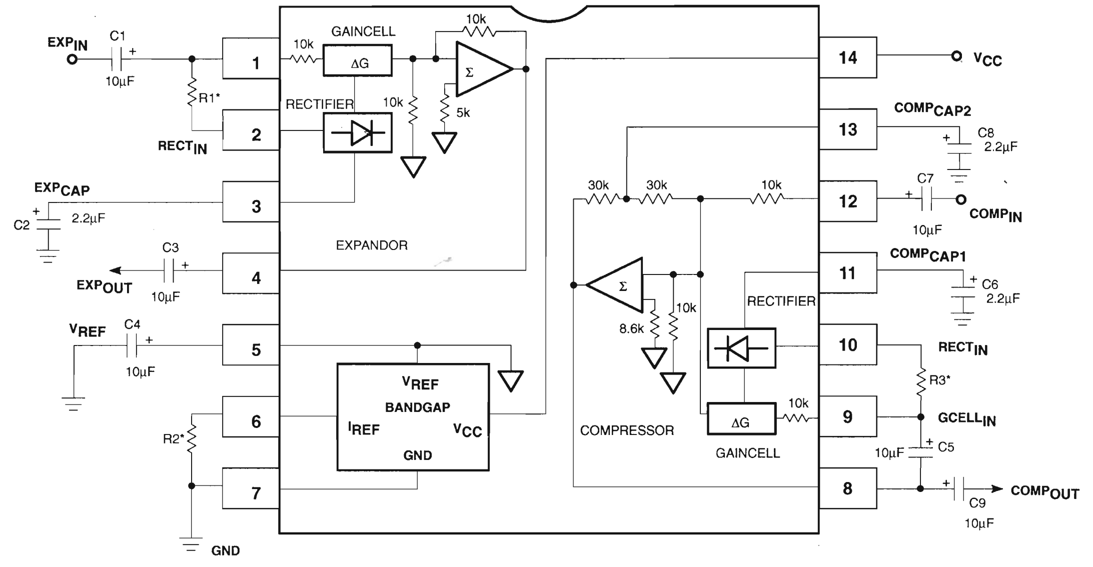
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE576N	0405B
14-Pin Plastic Small Outline (SO)	0 to +70°C	NE576D	0175D
14-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA576N	0405B
14-Pin Plastic Small Outline (SO)	–40 to +85°C	SA576D	0175D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE576	SA576	
V_{CC}	Supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance DIP SO	90 125	90 125	°C/W °C/W

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT



*R1, R2 and R3 are 1% resistors.

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 3.6VDC$, compandor 0dB level = –20dBV = 100mV$_{RMS}$, output load $R_L = 10k\Omega$, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA576 MIN	LIMITS NE/SA576 TYP	LIMITS NE/SA576 MAX	UNITS
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current	No signal $R_2 = 100k\Omega$		1.4	3	mA
V_{REF}	Reference voltage[2]	$V_{CC} = 3.6V$		1.8		V
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.5	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, $R_S = 0\Omega$		10	30	µV
0dB	Unity gain level	0dB at 1kHz	–1.5	0.18	1.5	dB
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, $C_{REF} = 10\mu F$		–80		dB
V_O	Output swing low			0.2		V
	Output swing high			$V_{CC} - 0.2$		

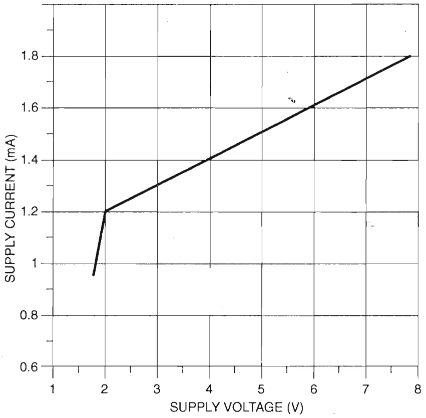
NOTE:

1. Operation down to $V_{CC} = 1.8V$ is possible, see description on front page of NE576 data sheet.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.

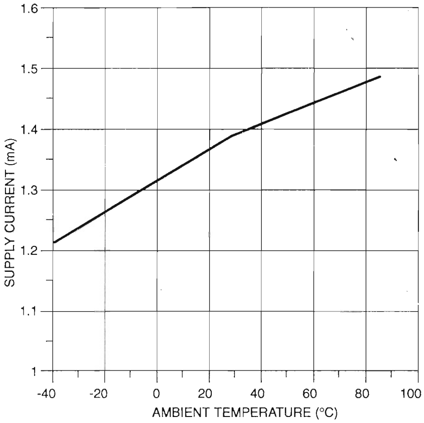
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=7.15kΩ, R2=100kΩ, 0dB level = 100mV, Freq. = 1kHz

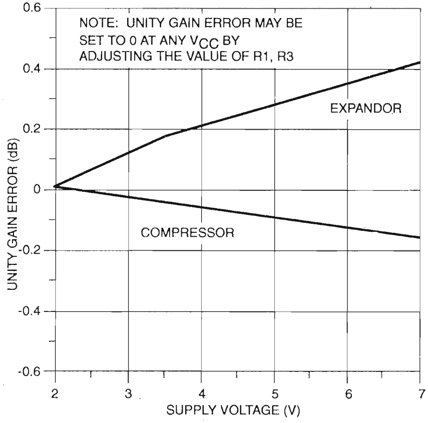
SUPPLY CURRENT vs SUPPLY VOLTAGE



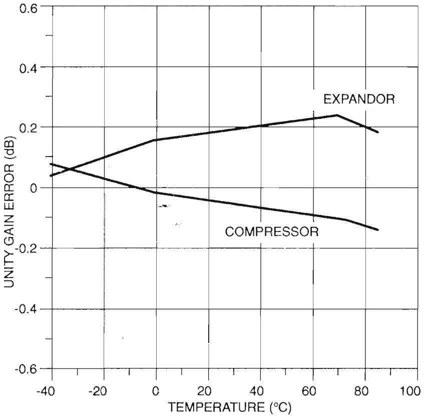
SUPPLY CURRENT vs TEMPERATURE



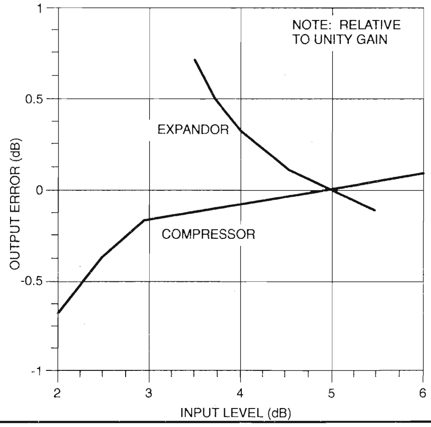
UNITY GAIN ERROR vs SUPPLY VOLTAGE



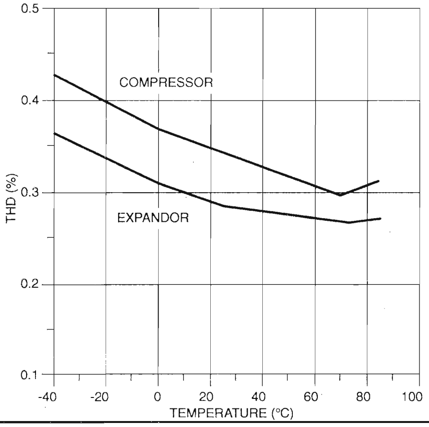
UNITY GAIN ERROR vs TEMPERATURE



TRACKING ERROR vs INPUT LEVEL



THD vs TEMPERATURE



Unity gain level programmable low power compandor NE/SA577

DESCRIPTION

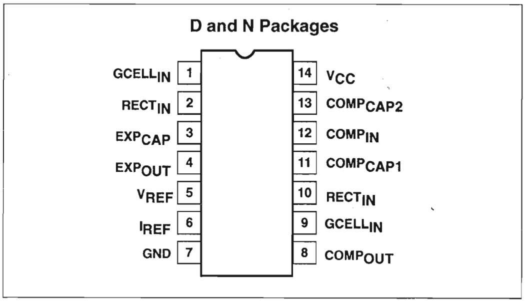
The NE/SA577 is a unity gain level programmable compandor designed for low power applications. The NE577 is internally configured as an expandor and a compressor to minimize external component count.

The NE577 is available in a 14-pin plastic DIP and SO packages.

FEATURES

- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- 0dB level programmable ($10mV_{RMS}$ to $1.0V_{RMS}$)
- Over 90dB of dynamic range
- Wide input/output swing capability (rail-to-rail)
- Low external component count
- SA577 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION



APPLICATIONS

- High performance portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control (ALC)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE577N	0405B
14-Pin Plastic Small Outline (SO)	0 to +70°C	NE577D	0175D
14-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA577N	0405B
14-Pin Plastic Small Outline (SO)	–40 to +85°C	SA577D	0175D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE577	SA577	
V_{CC}	Supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance DIP SO	90 125	90 125	°C/W °C/W

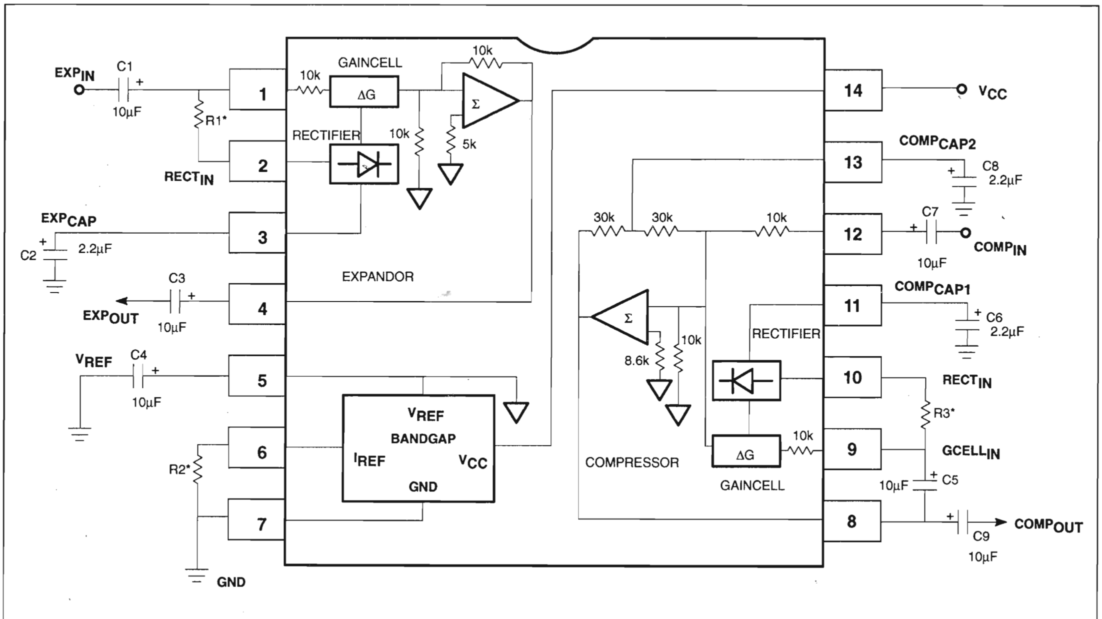
ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 3.6VDC$, compandor 0dB level = –20dBV = 100mV$_{RMS}$, output load $R_L = 10kΩ$, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA577			
			MIN	TYP	MAX	
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current	No signal $R_2 = 100kΩ$		1.4	2	mA
V_{REF}	Reference voltage[2]	$V_{CC} = 3.6V$	1.7	1.8	1.9	V
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.5	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, $R_S = 0Ω$		10	25	µV
0dB	Unity gain level	0dB at 1kHz	–1.5	0.18	1.5	dB
	Programmable range[3]	R1 = R3 = 18.7kΩ, R2 = 24.3kΩ		0		dBV
		R1 = R3 = 22.6kΩ, R2 = 100kΩ		–10		
		R1 = R3 = 7.15kΩ, R2 = 100kΩ		–20		
		R1 = R3 = 1.33kΩ, R2 = 200kΩ		–40		
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, $C_{REF} = 10µF$		–80	–65	dB
V_O	Output swing low			0.2		V
	Output swing high			$V_{CC} - 0.2$		

NOTE:
1. Operation down to $V_{CC} = 1.8V$ is possible, see application note AN1762.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.
3. Unity gain level can be adjusted CONTINUOUSLY between –40dBV = 10mV$_{RMS}$ and 0dBV = 1.0V$_{RMS}$. For details see application note AN1762.

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT

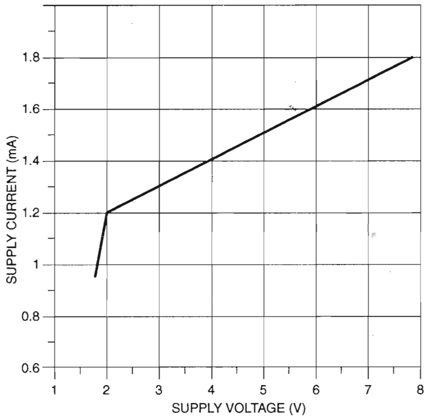


*R1, R2 and R3 are 1% resistors.

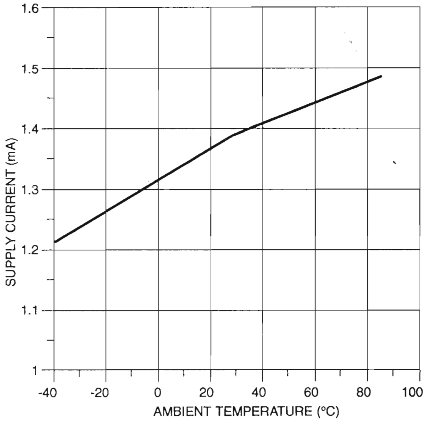
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=7.15kΩ, R2=100kΩ, 0dB level = 100mV, Freq. = 1kHz

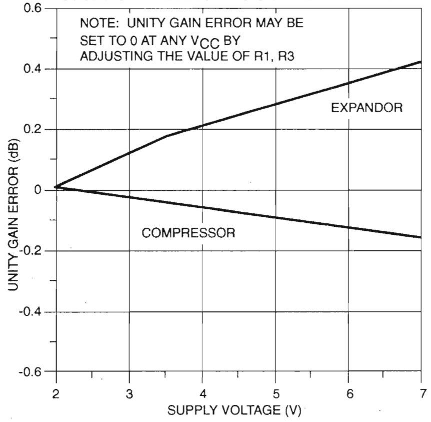
SUPPLY CURRENT vs SUPPLY VOLTAGE



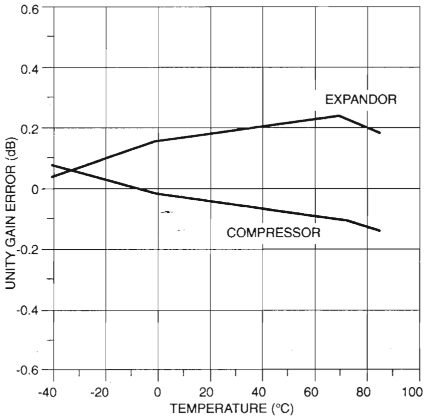
SUPPLY CURRENT vs TEMPERATURE



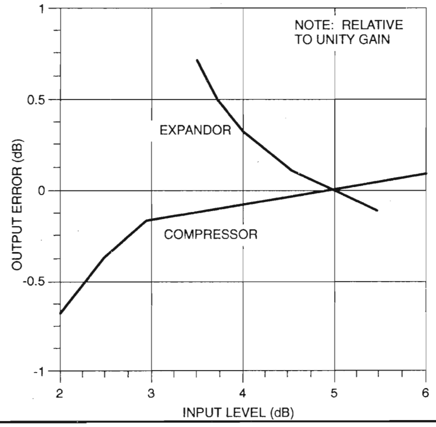
UNITY GAIN ERROR vs SUPPLY VOLTAGE



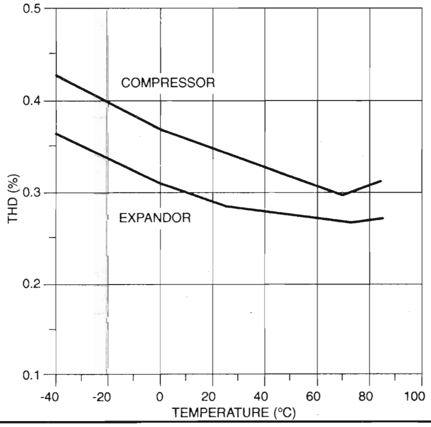
UNITY GAIN ERROR vs TEMPERATURE



TRACKING ERROR vs INPUT LEVEL



THD vs TEMPERATURE



Unity gain level programmable low power compandor NE/SA578

DESCRIPTION

The NE/SA578 is a unity gain level programmable compandor designed for low power applications. The NE578 is internally configured as an expandor and a compressor to minimize external component count.

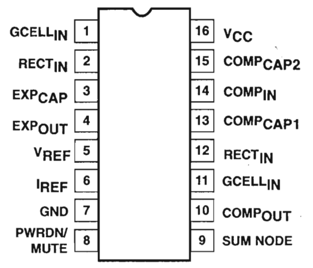
The summing amplifiers of the NE578 have 600Ω drive capability and the inverting input of the compressor amplifier is accessible through Pin 9 for summing multiple external signals. Power Down/Mute function is active low and requires an open collector output logic configuration at Pin 8. If Power Down/Mute is not needed, Pin 8 should be left open. When the part is muted, supply current drops to 170mA at 3.6V. The NE578 is available in a 16-pin plastic DIP and SO packages.

FEATURES

- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- 0dB level programmable (10mV$_{RMS}$ to 1.0V$_{RMS}$)
- Over 90dB of dynamic range
- Wide input/output swing capability
- Low external component count
- SA578 meets cellular radio specifications
- ESD hardened
- Power Down mode (I_{CC} = 170µA @ 3.6V)
- Mute function
- Multiple external summing capability
- 600Ω drive capability

PIN CONFIGURATION

D and N Packages



APPLICATIONS

- High performance portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control (ALC)

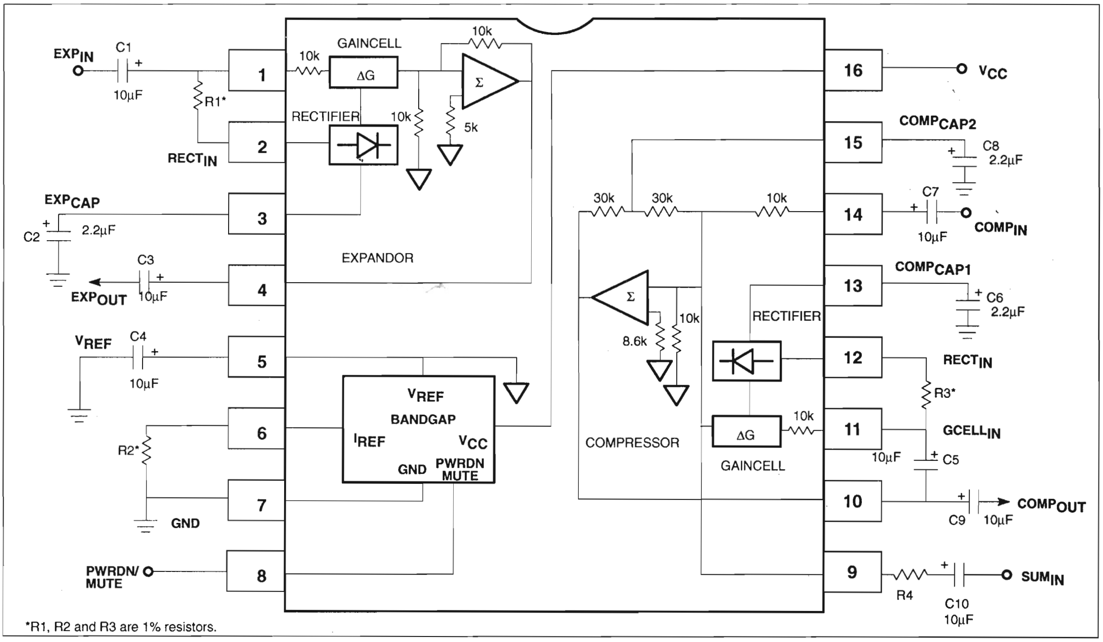
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE578N	0406C
16-Pin Plastic Small Outline (SO)	0 to +70°C	NE578D	0005D
16-Pin Plastic Dual In-Line Package (DIP)	–40 to +85°C	SA578N	0406C
16-Pin Plastic Small Outline (SO)	–40 to +85°C	SA578D	0005D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE578	SA578	
V_{CC}	Supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance DIP SO	90 125	90 125	°C/W °C/W

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT



*R1, R2 and R3 are 1% resistors.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA578			
			MIN	TYP	MAX	
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current operating power down	No signal, R_2 = 100kΩ		1.4 170	2	mA μA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V	1.7	1.8	1.9	V
R_L	Summing amp minimum output load			600		Ω
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.0	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω		10	20	μV
0dB	Unity gain level	0dB at 1kHz	–1.0	0.18	1.0	dB
	Programmable range[3]	R1 = R3 = 18.7kΩ, R2 = 24.3kΩ		0		dBV
		R1 = R3 = 22.6kΩ, R2 = 100kΩ		–10		
		R1 = R3 = 7.15kΩ, R2 = 100kΩ		–20		
		R1 = R3 = 1.33kΩ, R2 = 200kΩ		–40		
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10μF		–80	–65	dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		
	Power Down/Mute low level		0		0.4	V
	Power Down/Mute input current	Pin 8 grounded		–65		μA

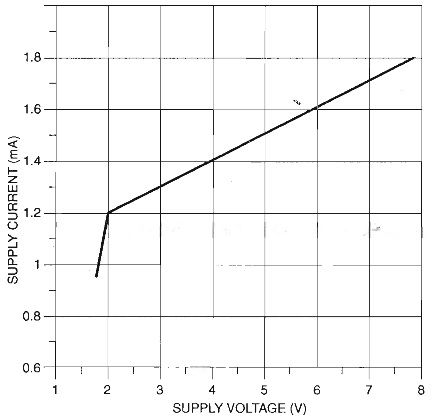
NOTE:

1. Operation down to V_{CC} = 1.8V is possible.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.
3. Unity gain level can be adjusted CONTINUOUSLY between –40dBV = 10mV_{RMS} and 0dBV = 1.0V_{RMS}. For details see application note AN1762.

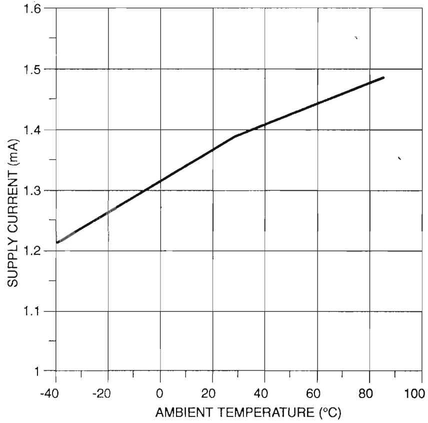
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=7.15kΩ, R2=100kΩ, 0dB level = 100mV, Freq. = 1kHz

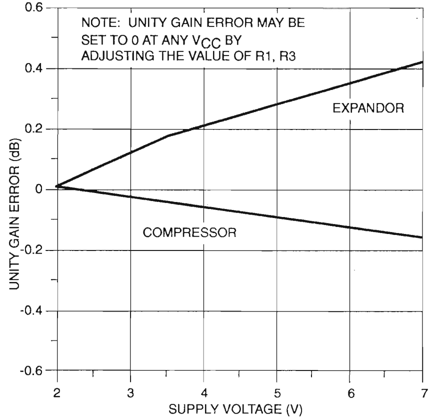
SUPPLY CURRENT vs SUPPLY VOLTAGE



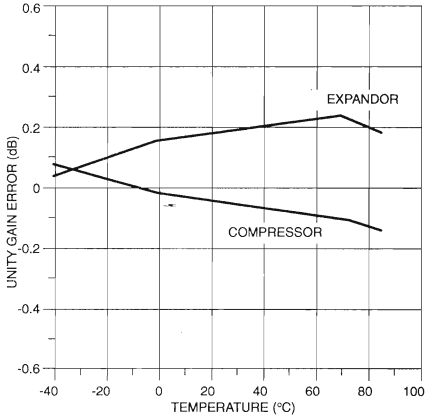
SUPPLY CURRENT vs TEMPERATURE



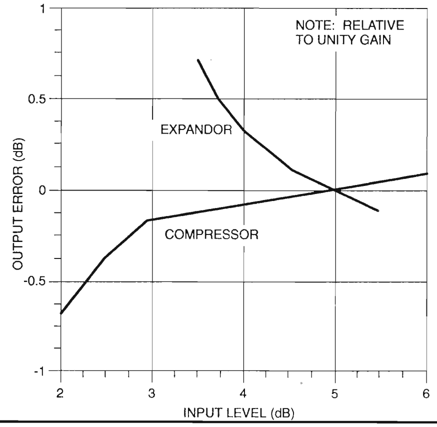
UNITY GAIN ERROR vs SUPPLY VOLTAGE



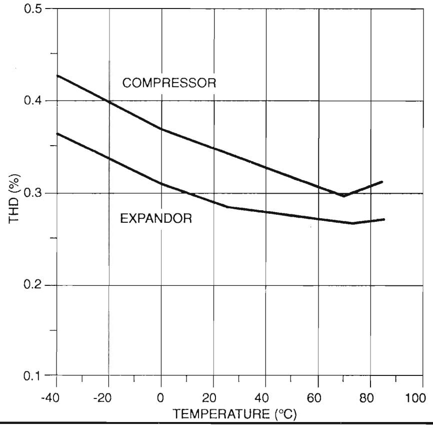
UNITY GAIN ERROR vs TEMPERATURE



TRACKING ERROR vs INPUT LEVEL



THD vs TEMPERATURE



Companding with the NE577 and NE578

AN1762

Author: Alvin K. Wong

INTRODUCTION

This application note is written for the designer who understands the basic functions of companding and wants to use the NE577 or NE578. If a designer is not familiar with the functionality of compandors, a good discussion can be found in the earlier Philips Semiconductors compandor data sheets and applications notes.

Key topics discussed in this paper are:

- How to program the unity gain level (0dB)
- How to implement an automatic level control
- How to get the best companding performance under strict design requirements
- How to set the attack and recovery time
- How to operate at 1.8V
- How to sum external signals using the NE578
- How to power-down the NE578
- How to mute the NE578
- How to use the NE577 and NE578 as a dual expandor

But before reviewing these areas, a summary of Philips Components- Signetics compandor family will be presented. A system designer can then determine which compandor is best for the design.

SUMMARY OF COMPANDOR FAMILY

In the past, Philips Semiconductors offered four different types of compandors: the NE570, NE571, NE572, and NE575. Each of the four compandors has its own 'claim to fame'. The NE570 and NE571 are known to work well in high performance audio applications. The only real difference between the two is that the NE570 has a slight edge in performance. However when separate attack and recovery times are needed, the NE572 is the compandor to choose. The NE575 becomes useful when there are low voltage requirements.

With the increasing demand for low current consumption, good flexibility, and ease of use in semiconductors, Philips Semiconductors is offering three additional compandors to its family, the NE576, NE577 and NE578. These compandors typically require an I_{CC} of 1.4mA at a V_{CC} of 3.6V, but Philips Semiconductors has demonstrated that these new chips are functional down to 1.8V.

In addition to having low power consumption, the NE578 has a power-down mode. In this mode, the chip consumes only 170μA. This power-down mode is useful when the functionality of the chip is not needed at all times. In the power-down mode , the NE578 maintains all of its pin voltages at all their normal DC operating voltages. Because all of the capacitors remain charged in this mode, the power-up state will occur quickly. Powering down automatically mutes the NE578. Having the mute function internal to the NE578 audio section eliminates the need for an external switch. The NE578 is the only compandor in the family that has power-down and mute functions.

To allow for greater flexibility, the 0dB level is now programmable for the NE577 and NE578. However, for the NE576, the 0dB level is specified and set at $100mV_{RMS}$. The earlier compandors also have a set unity gain (0dB) level. The NE570 and NE571 have a set 0dB level at $775mV_{RMS}$. While the NE572 and the NE575 both have their 0dB levels at $100mV_{RMS}$. If a designer wanted a different 0dB level, two op amps would have to be implemented in the design. One of the op amps would connect to the input of the compandor, while the other op amp would connect to the output. But with the NE577 and NE578, these external op amps are no longer needed. The 0dB level can be programmed from $10mV_{RMS}$ to $1V_{RMS}$ with three external resistors.

Many of the external parts in the previous family of compandors are now internal to the device. Additionally, the left side of the chip is configured as an expandor, and the right side is configured as a compressor. This allows for minimum part count and fewer variations in systems design. The external capacitors are also reduced in value which saves board space and cost. The only trade-off with using smaller capacitors is that there is less filtering. Because of this new approach, the NE576, NE577 and NE578 are easy to implement in any design.

Table 1 shows a brief summary of all the compandors. The seven different compandors offer a wide range of flexibility: different types of packages, power-down capability, programmable or fixed unity gain, different reference voltages, a wide range of operating voltages and currents, different pin outs, etc. From this information, a designer can quickly choose a compandor which best meets the design requirements. After a compandor is chosen from the table, a designer can find additional help from data sheets and application notes.

Since power consumption is important in most designs, it is important to discuss them in this application note. The NE570, NE571, and NE572 have built in voltage regulators, therefore, the current consumption remains roughly the same over the specified supply voltages. This can be especially useful when the power supply is not regulated very well. However with the NE575, NE576, NE577, and NE578, the current consumption will drop as the supply voltage decreases. For this, the power consumption will drop also. This means one can operate the part at a very low power level. This is a good feature for any design having strict power consumption guidelines.

INTRODUCING NE577 AND NE578

Figure 1 and 2 show block diagrams of the NE577 and NE578 respectively. The only substantial difference between the two is that the NE578 has a power-down capability, mute function and summing capabilities (for signals like DTMF tones). In addition the NE578 summing amplifiers are capable of driving 600Ω loads. Listed below are the basic functions of each external component for Figure 1 (NE577).

Companding with the NE577 and NE578

AN1762

Table 1. Compandor Family Overview

	NE570	NE571	NE572	NE575	NE576	NE577	NE578
V_{CC}	6–24V	6–18V	6–22V	3–7V	2–7V	2–7V	2–7V
I_{CC}	3.2mA	3.2mA	6mA	3–5.5mA*	1–3mA*	1–2mA*	1–2mA*
Number of Pins	16	16	16	20	14	14	16
Packages NE: 0 to +70°C SA: –40 to +85°C N: Plastic DIP D: Plastic SO F: Ceramic DIP DK: SSOP (Shrink Small Outline Package)	NE570F NE570N NE570D	NE571F NE571N NE571D SA571F SA571N SA571D	NE572N NE572D SA572F SA572N SA572D	NE575N NE575D NE575DJ SA575N SA575D SA575DK	NE576N NE576D SA576N SA576D	NE577N NE577D SA577N SA577D	NE578N NE578D SA578N SA578D
ALC (Automatic Level Control)	Both Channels	Both Channels	Both Channels	Right Channel	Right Channel	Right Channel	Right Channel
Reference Voltage	Fixed 1.8V	Fixed 1.8V	Fixed 2.5V	$V_{CC} / 2$	$V_{CC} / 2$	$V_{CC} / 2$	$V_{CC} / 2$
Unity Gain	$775mV_{RMS}$	$775mV_{RMS}$	$100mV_{RMS}$	$100mV_{RMS}$	$100mV_{RMS}$	10mV to $1V_{RMS}$	10mV to $1V_{RMS}$
Power-Down	NO	NO	NO	NO	NO	NO	YES (170µA)
Key Features	-Excellent Unity Gain Tracking Error -Excellent THD	-Excellent Unity Gain Tracking Error -Excellent THD	-Independent Attack & Recovery Time -Good THD -Needs ext. summing op amp	-2 Uncommited on-chip op amps available -Low voltage	-Low power -Low external component count	-Low power -Programmable unity gain	-Low power -Programmable unity gain -Power down -Mute function -Summing capability (DTMF) -600Ω drive capability
Applications Cordless Phones Cellular Phones Wireless Mics Modems Consumer Audio Two-way Communications	High performance audio circuits "Hi–Fi Commercial Quality"	High performance audio circuits "Hi–Fi Commercial Quality"	High performance audio circuits "Hi–Fi Studio Quality"	Consumer audio circuits "Commercial Quality"	Battery powered systems "Commercial Quality"	Battery powered systems "Commercial Quality"	Battery powered systems "Commercial Quality"

NOTES: NE5750/5751 are also excellent audio processor components for high performance cordless and cellular applications that include the companding function..
$^*I_{CC}$ varies with V_{CC}.

R1 – Determines the Unity Gain Level for the Expandor

R2 – Determines What Value the Reference Current (I_{REF}) will be for the Part (Also Affects Unity Gain Level)

R3 – Determines the Unity Gain Level for the Compressor

C1 – DC Blocking Capacitor

C2 – Determines the Attack and Recovery Time for the Expandor

C3 – DC Blocking Capacitor

C4 – Used to AC Ground the V_{REF} Pin

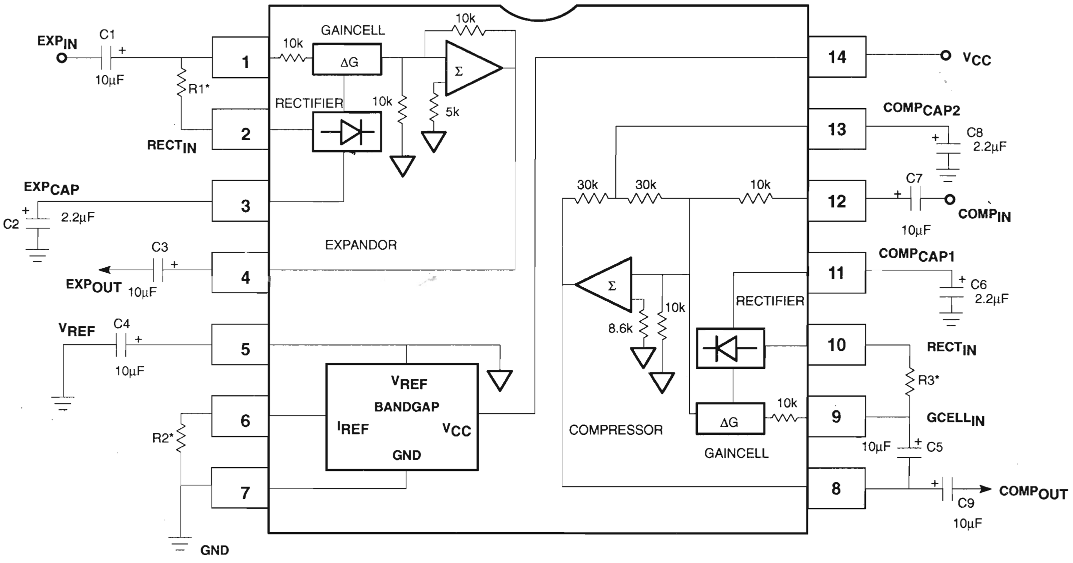
C5 – Provides AC Path from Gain Cell to Output of Summing Amp

C6 – Determines the Attack and Recovery Time for the Compressor

C7 – DC Blocking Capacitor

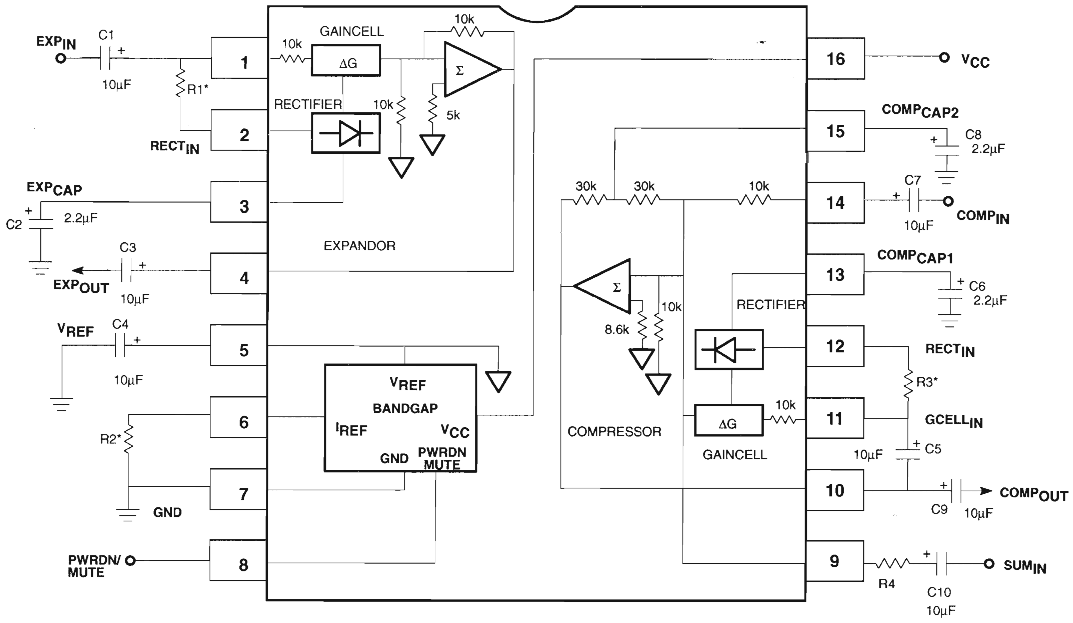
C8 – Provides AC Ground for the DC Feedback Path

C9 – DC Blocking Capacitor



*R1, R2 and R3 are 1% resistors.

Figure 1 . NE577 Block Diagram



*R1, R2 and R3 are 1% resistors.

Figure 2 . NE578 Block Diagram

Listed below are the basic functions of each external component for Figure 2 (NE578).

R1 – Determines the Unity Gain Level for the Expandor

R2 – Determines What Value the Reference Current (I_{REF}) will be for the Part (Also Affects Unity Gain Level)

R3 – Determines the Unity Gain Level for the Compressor

R4 – Used to Set the Gain of an External Signal like DTMF Tones and Sum them with the Companded Signal

C1 – DC Blocking Capacitor

C2 – Determines the Attack and Recovery Time for the Expandor

C3 – DC Blocking Capacitor

C4 – Used to AC Ground the V_{REF} Pin

C5 – Provides AC Path from Gain Cell to Output of Summing Amp

C6 – Determines the Attack and Recovery Time for the Compressor

C7 – DC Blocking Capacitor

C8 – Provides AC Ground for the DC Feedback Path

C9 – DC Blocking Capacitor

C10 – DC Blocking Capacitor

HOW TO PROGRAM THE UNITY GAIN LEVEL (0dB)

Three external resistors R1, R2, and R3 define the unity gain level. Both the NE577 and the NE578 0dB levels can vary from $10mV_{RMS}$ to $1.0V_{RMS}$. These limits are used in product characterization, but these parts can function over a wider 0dB level range.

In most applications the 0dB level is equal for both the compressor and expandor side. Therefore, R1 and R3 are equal in value. R3 sets the 0dB level for the compressor side, and R1 sets the 0dB level for the expandor side. However, there could be a situation where a design requires different 0dB levels for compression and expansion. This will not be a problem with the NE577 or NE578, due to the separate 0dB level programming.

Using the formulas below, a designer can calculate the resistor values for a desired unity gain level.

Formula 1: $$R_2 = \frac{V_{BG}}{I_{REF}}$$

where

V_{BG} = Bandgap Voltage

I_{REF} = Reference Current

(V_{BG} is brought out on Pin 6 and R2 determines the I_{REF} value)

Formula 2: $$R_1 = \frac{0.9 \cdot V_{IN_{RMS}}}{I_{REF}}$$

where $V_{IN_{RMS}}$ is the 0dB level

($R_1 = R_3$ in most cases)

Programming the Unity Gain Level for the NE577 also applies for the NE578.

Example:

Program the NE577 or NE578 for a 0dB Level at $100mV_{RMS}$

Step 1: V_{BG}=1.26V.......Typically

I_{REF}=12.6μA.....Good Starting Point

$$R_2 = \frac{1.26V}{12.6}\mu A$$

R_2 = 100k

Step 2:

$$R_1 = R_3 = \frac{0.9V_{IN_{RMS}}}{I_{REF}}$$

$$R_1 = R_3 = \frac{(0.9V)\ (100mV_{RMS})}{12.6\mu A}$$

\ $R_1 = R_3$ = 7.15k

Step 3: $R_1 = R_3$ = 7.15k (1% value)

R_2 = 100k (1% value)

Step 4: Plug in these resistor values and measure for unity gain. Adjust accordingly for accuracy.

NOTE: Rough Limits for Resistors:

1k ≤ R1 ≤ 100k (1% values)

20k ≤ R2 ≤ 200k (1% values)

1k ≤ R3 ≤ 100k (1% values)

Rough Limits for I_{REF}

$6.3\mu A \leq I_{REF} \leq 63\mu A$

The example above gives pretty close results. A designer should use 1% resistors to get the best performance. Below in Table 2 are some recommended values to get started:

Table 2. Recommended Resistor Values for Different 0dB Levels

0dB Level	dBv	R_2	R_1 & R_3
$1.0V_{RMS}$	0	24.3k	18.7k
$316.2mV_{RMS}$	–10	100k	22.6k
$100mV_{RMS}$	–20	100k	7.15k
$10mV_{RMS}$	–40	200k	1.33k

PARAMETERS THAT LIMIT THE DYNAMIC RANGE

The above example is a good place to start, but to get the optimum performance from the NE577 and NE578, a designer needs to understand certain key parameters. I_{REF} is important because it determines the values for all three resistors (R1, R2, and R3). Since I_{REF} is directly related to I_{CC} (see Figure 3), one should be careful in choosing a value. If one chooses a high I_{REF} current, power consumption goes up. However the output signal will have excellent low level distortion (see Figures 4 and 5). If one chooses a low I_{REF} value, distortion at the output will increase slightly. Conversely, the power consumption is reduced, which might be worth the trade-off in battery operated designs.

The dynamic range of the NE577 and NE578 is determined by supply voltage (V_{CC}) and reference current (I_{REF}). I_{REF} determines how well the compandor will perform with low level input signals. The supply voltage determines how high (in level) an input signal can be before clipping appears on the output (in some cases increasing I_{REF} also helps). A designer needs to estimate the input range going into the compandor so that an appropriate V_{CC} and I_{REF} can be chosen.

The bandgap voltage (V_{BG}) slightly varies over a wide range of I_{REF} currents (Figure 6). Figure 7 shows how I_{REF} varies with R2. The higher R2 is, the lower I_{REF} is. Figure 8 shows how the dynamic range varies over different values of I_{REF} (the higher the supply voltage the better the dynamic range). The graphs in Figures 3 - 8 were taken at V_{CC}=3.6V, F=1kHz and 0dB level=100mV$_{RMS}$. The I_{REF} current was limited between 5µA and 40µA.

It can be seen that I_{REF} plays an important role in current consumption, THD, and dynamic range. With the aid of these figures, one can determine an I_{REF} which meets the design goals.

Example:

Making use of the graphs in Figures 3 - 8 and formulas 1 and 2, design a compandor with a 0dB level of 100mV$_{RMS}$. Try to achieve a THD of 0.1 on the compressor side with wide dynamic range. Operate at a supply voltage of 3.6V but with the lowest possible current consumption.

Step 1: According to Figure 5, an I_{REF} of 30µA is required for approximately 0.1% distortion.

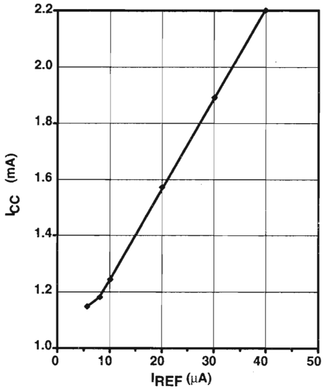


Figure 3. I_{REF} **vs** I_{CC}

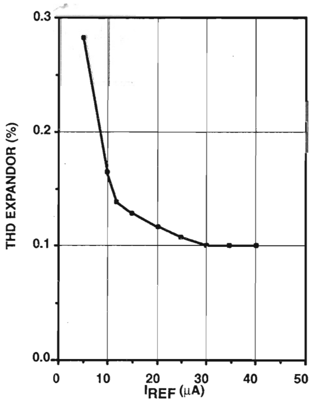


Figure 4. I_{REF} **vs THD, Expandor Side**

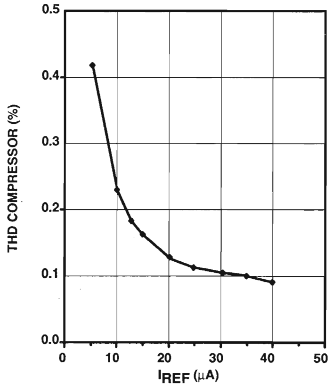


Figure 5. I_{REF} **vs THD, Compressor Side**

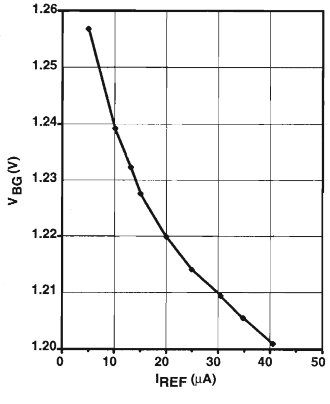


Figure 6. I_{REF} **vs** V_{BG}

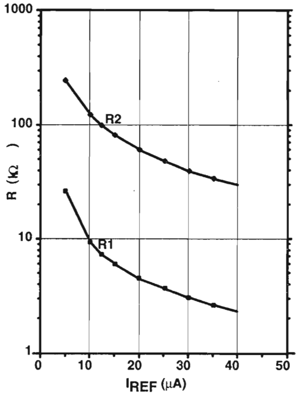


Figure 7. I_{REF} **vs R2, R1**

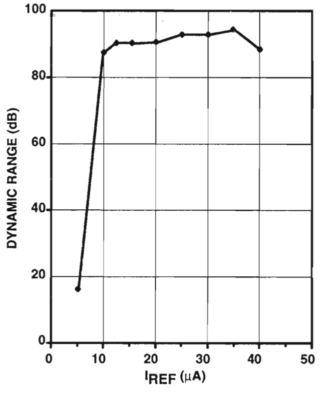


Figure 8. I_{REF} **vs Dynamic Range**

Test Conditions: V_{CC} = 3.6V F = 1kHz 0dB = 100mV$_{RMS}$

Step 2: From Figure 8, the dynamic range is approximately 92dB. So far the requirements have been met.

Step 3: Figure 3 shows us that I_{CC} is at 1.9mA with no input signal (that's not bad at all!).

Step 4: Calculating R1, R2, and R3

Graphical Method:
From Figure 7: For I_{REF}=30μA and 0dB=100mV_{RMS} R1=R3=3k R2=40k

Actual resistors available: R1=R3=3.01k (1%) R2=40.2k (1%)

Formula Method:
From Figure 6: V_{BG}=1.21V for I_{REF}=30μA therefore, using formula 1:

$$R_2 = \frac{V_{BG}}{I_{REF}}$$

$$R_2 = \frac{1.21V}{30\mu A}$$

R_2 = 40.33k

R_2 = 40.2k (available in 1%)

Recall from formula 2:

$$R_1 = \frac{0.9V_{IN_{RMS}}}{I_{REF}}$$

$$R_1 = \frac{(0.9V)\ (100mV_{RMS})}{30\mu A}$$

R_1 = 3k

R_1 = 3.01k (available in 1%)

Connect these external resistors with the determined values and adjust for optimum performance.

Bench results:
After completing the exercise above, the resistors were connected and the results are given below.

I_{CC} = 1.89mA (with no input signal)
THD = 0.1 (meausured on spectrum analyzer)
0dB = 109mV_{RMS} (off by 0.8dB...good!) Dynamic Range = 92dB

These results are very close to what was predicted and by tweaking R1 and R3, the 0dB error can be further reduced to zero.

BANDWIDTH OF COMPANDOR

Figure 9 shows the typical bandwidth for the NE577 and NE578. The graphs were taken with a V_{CC} of 3.6V and a 0dB level of 100mV_{RMS}. The bandwidth of the expandor, the compressor, and the compandor (where a signal goes through the compressor and the expandor) is shown in this figure. Although the NE577 and NE578 are conservatively specified with a 20kHz bandwidth, Figure 9 reveals that it is actually around 300kHz.

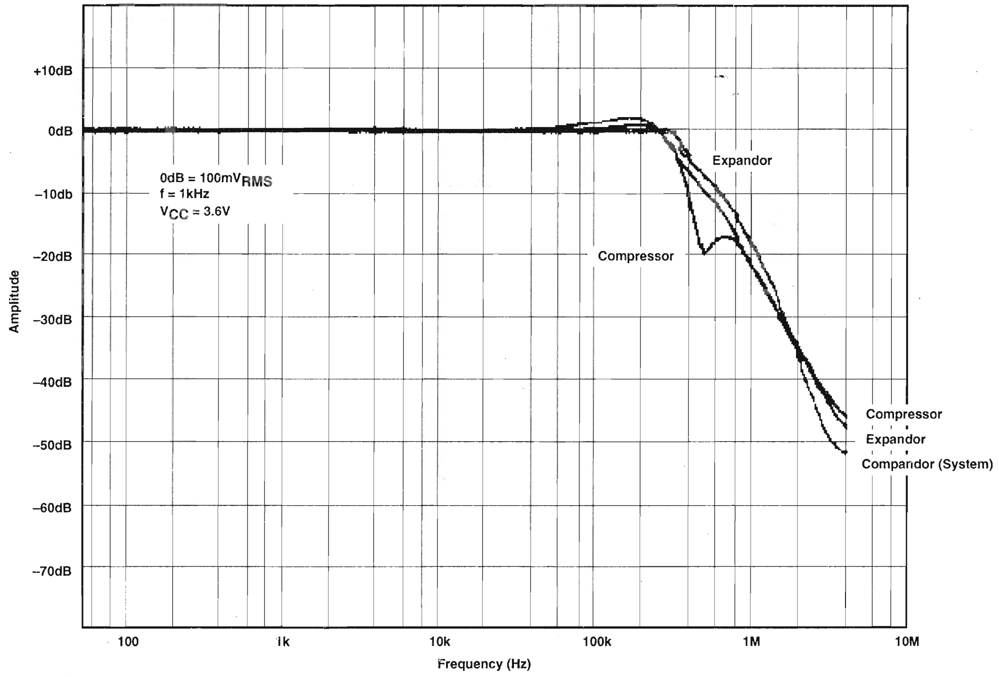


Figure 9. Bandwidth of NE577 and NE578 Demo Board

HOW TO SET THE ATTACK AND RECOVERY TIMES

C2 and C6, from figures 1 and 2, set the attack and recovery times for the NE577 and NE578. Application Note 174 (AN174) defines A and R times and also describes how they are measured on the bench. Formula 3 shows how the A and R time can be calculated.

Formula 3:

Attack Time [ms] = 10k * C2 or C6
Release Time [ms] = 4 * Attack Time

Although a fast attack time is desirable, one must remember that there is a trade-off with low distortion. As a general rule, a 1µF capacitor for C2 will produce 0.2% THD at 1kHz. Since CCITT recommends an RC time constant of 20ms for the attack time, a 2µF capacitor is recommended for telephony applications because it has only 0.1% THD at 1kHz and 0.33% at 800Hz.

Note: AN174 can be found in the 1989 Linear Data Manual, Volume 1, or the RF Handbook.

IMPLEMENTING A PROGRAMMABLE AUTOMATIC LEVEL CONTROL

The function of an automatic level control (ALC) is to take a given range of input signals and provide a constant AC output level. This type of function is useful in many audio applications. One such application can be found in tape recorders. When a tape recorder with ALC is recording a conversation, a soft spoken person will be heard just as well as a loud spoken person during play back. Another useful application for ALC could be with telephony. A person who has difficulty hearing, will not have to ask the other party to speak up. If the phone already has a volume control, the user has to adjust the volume for different parties. But with the ALC, the volume only has to be set once.

Different constant AC output levels of an ALC can be 'programmed' with the NE577 and NE578. This allows the designer to choose the output level that is needed in the design, and eliminates the need for an external op amp.

The compressor side of the NE577 and NE578 can be configured to function as an automatic level control (ALC). Figure 10 and 11 show how this can be done. The circuit shown for the NE577/78 ALC is set up to provide a constant output level of 100mV$_{RMS}$ with an input range from –34dB to +20dB at 1kHz (see Figure 12).

Below are some design equations for the ALC:

Eq 1.

$$\text{AC output level}(V_{RMS}) = \left[\frac{R_3 \cdot R_{2_a} \cdot I_{REF}}{R_{1_a}}\right] \cdot 1.11$$

$$\text{where } R_{1_a} = R_{2_a} = 10\text{k (internal)}$$

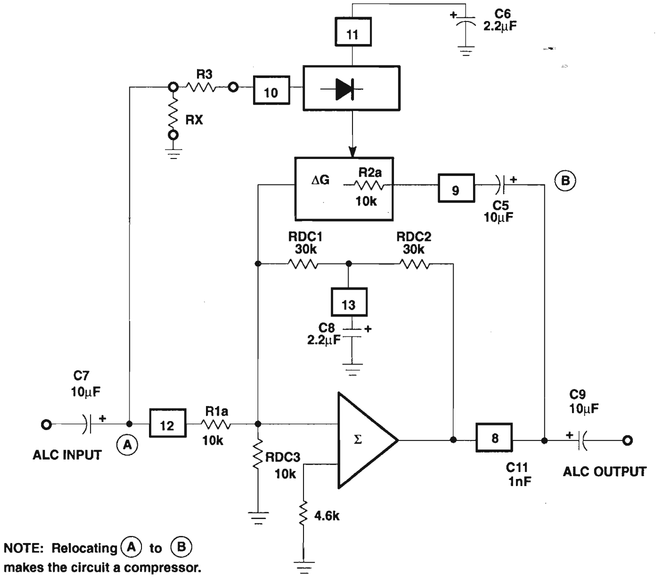
$$I_{REF} = \frac{V_{BG}}{R_2}$$

Eq 2.

$$\text{Maximum Gain} = \frac{4(R_3 + R_X) \cdot R_{2_a} \cdot I_{REF}}{R_{1_a} \cdot V_{CC}}$$

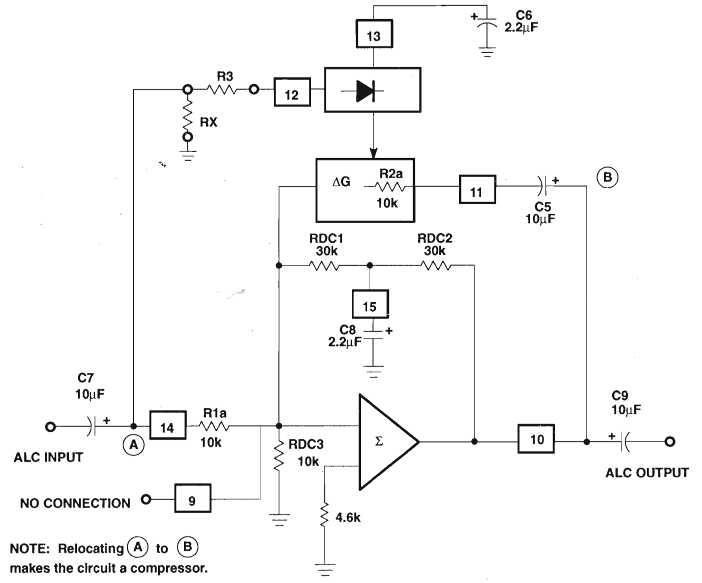
Eq 3.

$$\text{Gain} = \frac{R_3 \cdot R_{2_a} \cdot I_{REF}}{R_{1_a} \cdot V_{IN_{RMS}}}$$



NOTE: Relocating (A) to (B) makes the circuit a compressor.

Figure 10. NE577 ALC Configuration



NOTE: Relocating Ⓐ to Ⓑ makes the circuit a compressor.

Figure 11. NE578 ALC Configuration

Example:
Design an ALC with a constant output level of 100mV$_{RMS}$ with a maximum gain of 10.

Step 1: From Eq 1

$$\text{AC output level}(V_{RMS}) = \left[\frac{R_3 \cdot R_{2_a} \cdot I_{REF}}{R_{1_a}}\right] \cdot 1.11$$

$$\text{where } R_{1_a} = R_{2_a} = 10k \text{ (internal)}$$

$$I_{REF} = \frac{V_{BG}}{R_2}$$

In terms of R_3

$$R_3 = \frac{[\text{AC output level}(V_{RMS})]\ R_{1_a}}{(1.11)\ (R_{2_a})\ I_{REF}}$$

assuming $R_2 = 100k$ and $V_{BG} = 1.26V$.

$$R_3 = \frac{100mV_{RMS} \cdot 10k}{1.11 \cdot 10k \cdot 12.6\mu A}$$

$$R_3 = 7.15k$$

Step 2: From Eq 2

$$\text{Maximum Gain} = \frac{4(R_3 + R_X) \cdot R_{2_a} \cdot I_{REF}}{R_{1_a} \cdot V_{CC}}$$

In terms of R_X

$$R_X = \frac{(\text{Max. Gain})\ (V_{CC})\ (R_{1_a})}{4R_{2_a} \cdot I_{REF}} - R_3$$

$$R_X = \frac{(10)\ (3.6V)\ (10k)}{4\ (10k)\ 12.6\mu A} - 7.15k$$

$$R_X = 707.1k$$

$$R_X = 715k \text{ (available)}$$

Step 3:

–connect resistors to circuit
–measure AC output level and adjust R3 for best accuracy
–check maximum gain by applying a low input level and adjust Rx for best results

Figure 12 shows the characteristics of the NE577/578 ALC circuit without Rx. The output stays at a constant $100mV_{RMS}$ level for a wide range of different input AC voltages. Any AC input signal above the cross-over point (unity gain level) is attenuated while any signal below the cross-over point is amplified. The cross-over point is where the input signal is equal to the output signal, where $A_V=1$.

Figure 13 reveals the dynamic range of the NE577 ALC circuit using Rx. The input range of the ALC is reduced. Instead of a $2mV_{RMS}$ input signal to get $100mV_{RMS}$ on the output, a $10mV_{RMS}$ input signal is now required (for Rx=681k). The purpose of limiting the maximum gain of the circuit is to prevent amplification of background noise. To alleviate this problem, Rx is used. Since the ALC was designed with a maximum gain of 10, any input signal below 10mV will not be amplified with a gain greater than 10 ($100mv_{RMS}/10=10mv_{RMS}$). Using Rx can be an advantage because the threshold of the ALC can be set.

Figure 14 shows that as Rx increases so does A_V. In some applications it might be useful to make Rx a potentiometer. This will allow the user to adjust the threshold for different environmental conditions.

Figures 15-18 show the results of using the ALC for different constant output levels. V_{CC} and I_{REF} limit the dynamic range. The upper part of the range can be increased by either increasing V_{CC} and/or I_{REF}. The lower part of the range can be improved by increasing I_{REF}.

EXTRA FEATURES FOR NE578

The NE578 has three extra functions over the NE577. These are power-down, mute and summing capabilities. To implement the power-down/mute mode, Pin 8 should be active low (open collector configuration, see Figure 19). If the power-down/mute feature is not used, Pin 8 should be left open. The NE578 only consumes 170µA of current at 3.6V when Pin 8 is activated. The power-down/mute mode is useful in designs when the function of the chip is not utilized at all times. This feature is a necessity where power conservation is critical.

In cellular and cordless applications, it is common to mix DTMF tones with the audio signal. This usually requires another op amp in which to mix the signals. With the NE578, however, the DTMF tones can be mixed internally on the compressor side. The DTMF signal is also compressed with the audio signal and ready for data transmission. Figure 2 shows that the summing of signals can be done at Pin 9 with R4 and C10. If amplification is not needed, then a 10k resistor is a recommended value for R4. In addition the summing amplifiers are capable of driving 600Ω loads.

THE NE577 AND NE578 AS A DUAL EXPANDOR

The compressor side can actually be configured as an expandor for both the NE577 and NE578. Figure 20 shows how this can be done. Because Pin 9 of the NE578 is available to the designer, the compressor side can not only be configured as an expandor, but as an expandor with summing capabilities.

OPERATING AT 1.8V

The NE577 and NE578 can operate at 1.8V.

NE577 AND NE578 DEMO BOARDS

Figures 21 shows the DIP package layout for the NE577 and NE578 demo boards, respectively. Figures 22 shows the SO layout for the NE577 and NE578 demo boards, respectively. The layouts are configured such that R1, R2, R3, and Rx can be removed and replaced easily. A switch is also available to change the operating mode of the compressor to an ALC configuration and vice versa (position the switch to the right for ALC mode).

When the compressor side is being evaluated, disconnect Rx completely from the socket on the demo boards. Rx should only be used when the compandor is being used for ALC.

For the NE578 demo board, two extra post are available. One is for power-down; the other is for summing external signals. To power-down, simply ground this post. To sum signals, connect the external signal to the proper post.

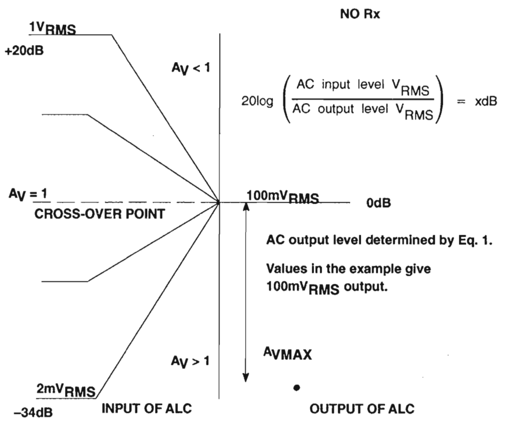

NO Rx
$1V_{RMS}$
+20dB
$A_V < 1$
$20\log\left(\frac{\text{AC input level } V_{RMS}}{\text{AC output level } V_{RMS}}\right) = xdB$
$A_V = 1$
CROSS-OVER POINT
$100mV_{RMS}$
0dB
AC output level determined by Eq. 1.
Values in the example give $100mV_{RMS}$ output.
A_{VMAX}
$A_V > 1$
$2mV_{RMS}$
–34dB
INPUT OF ALC
OUTPUT OF ALC

Figure 12. Dynamic Range of NE577 ALC Demonstration Board Without R_X

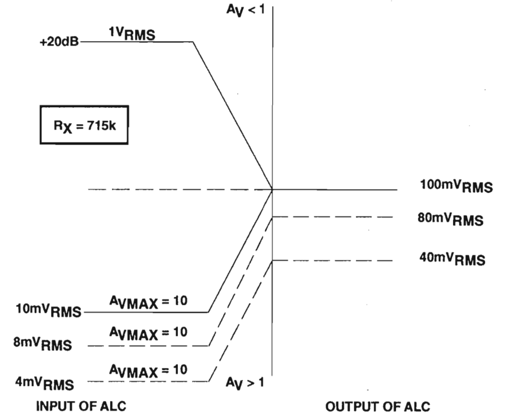


Figure 13. Dynamic Range of NE577 ALC Demo Board with R_X = 715kW

Companding with the NE577 and NE578

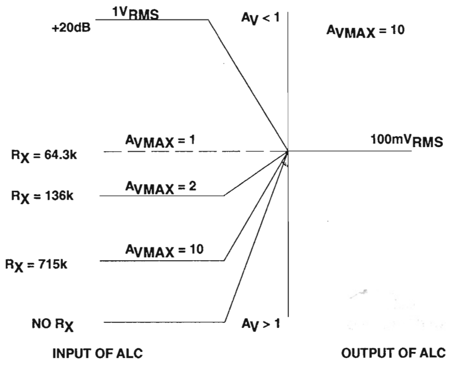


Figure 14. Dynamic Range of NE577 ALC Demo Board with Different R_X Values

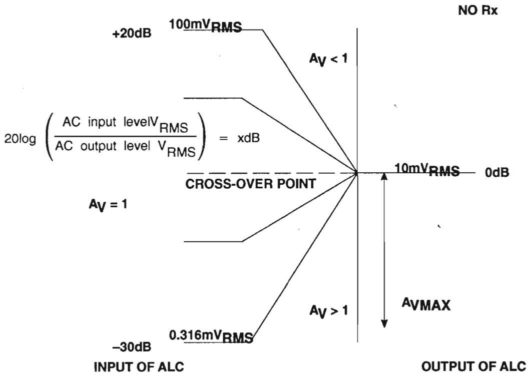


Figure 15. NE577 ALC: AC Output Level = $10mV_{RMS}$

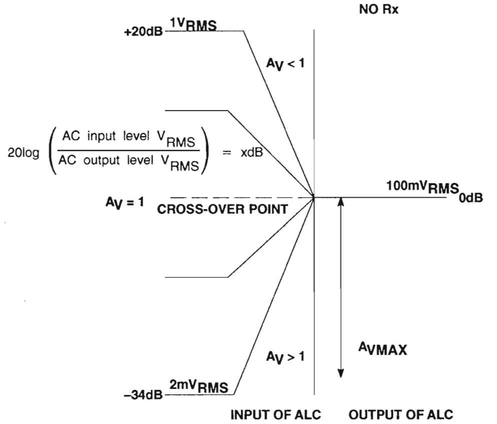


Figure 16. NE577 ALC: AC Output Level = $100mV_{RMS}$

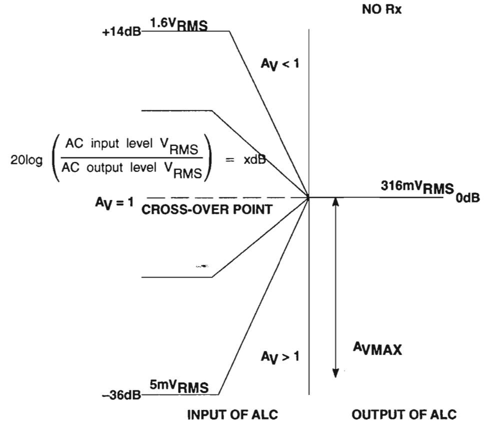


Figure 17. NE577 ALC: AC Output Level = $316mV_{RMS}$

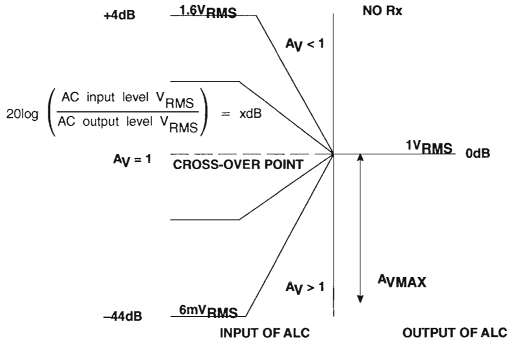
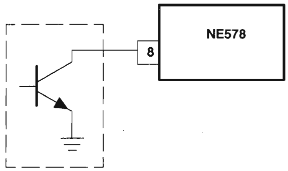


Figure 18. NE577 ALC: AC Output Level = $1V_{RMS}$



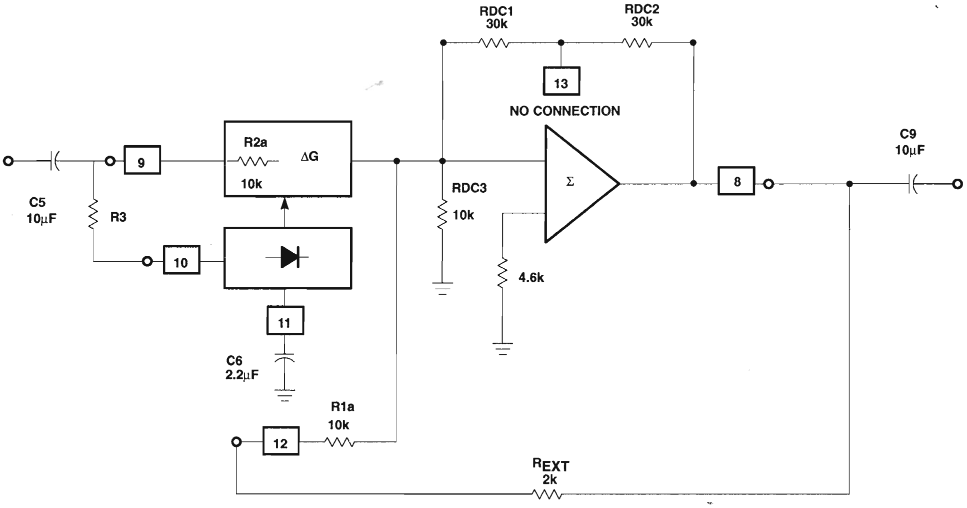
LEVEL AT PIN 8 SHOULD BE OPEN COLLECTOR TTL LEVELS

THE REASON FOR OPEN COLLECTOR CONFIGURATION IS TO ENSURE:

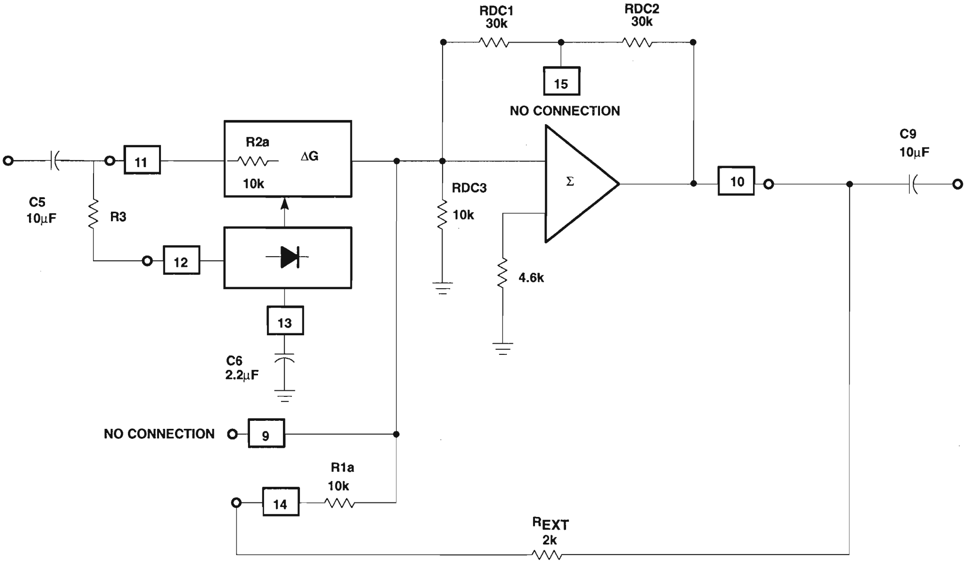
1) PIN 8 IS FLOATING WHEN POWER-DOWN/MUTE IS NOT IMPLEMENTED

2) PIN 8 IS GROUNDED WHEN POWER-DOWN/MUTE IS ACTIVE

Figure 19. Proper Use of NE578 Pin 8

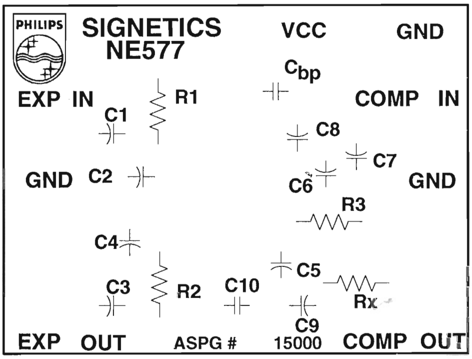


a. NE577

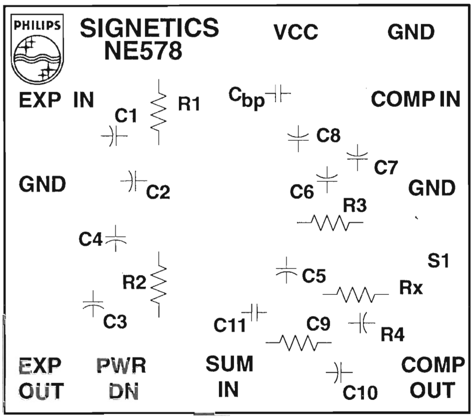


b. NE578

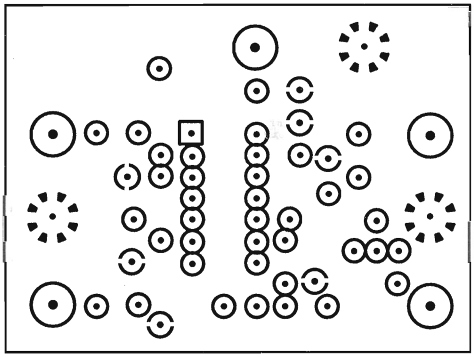
Figure 20. Expandor Configuration for the Compressor Side



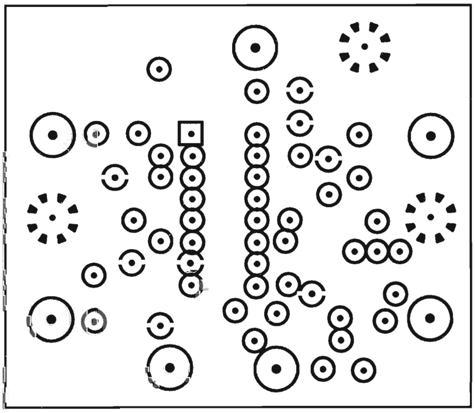
NE577 DIP Top Silk Screen



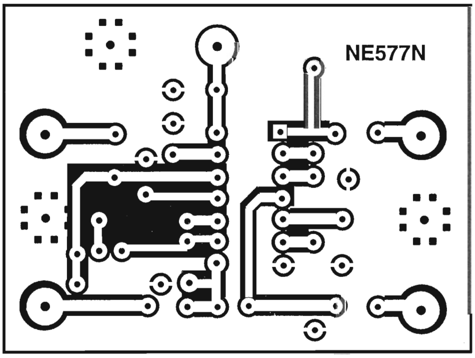
NE578 DIP Top Silk Screen



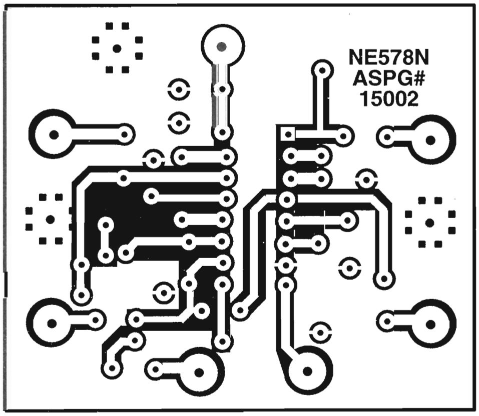
Top View



Top View



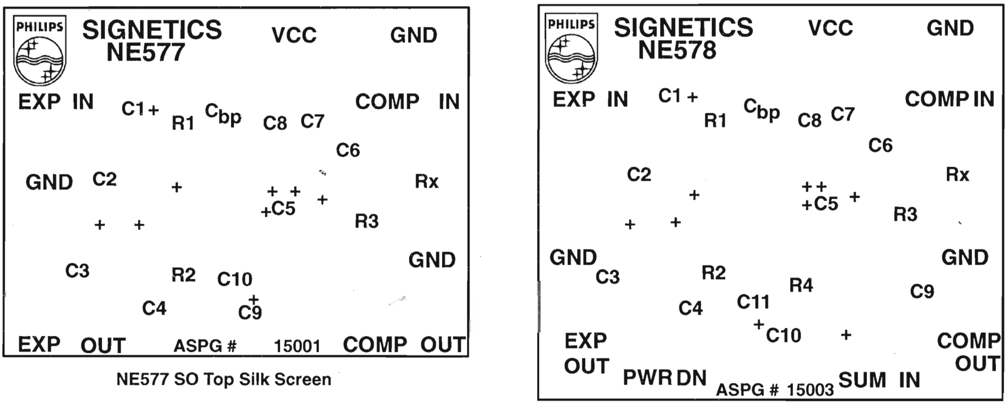
Bottom View



Bottom View

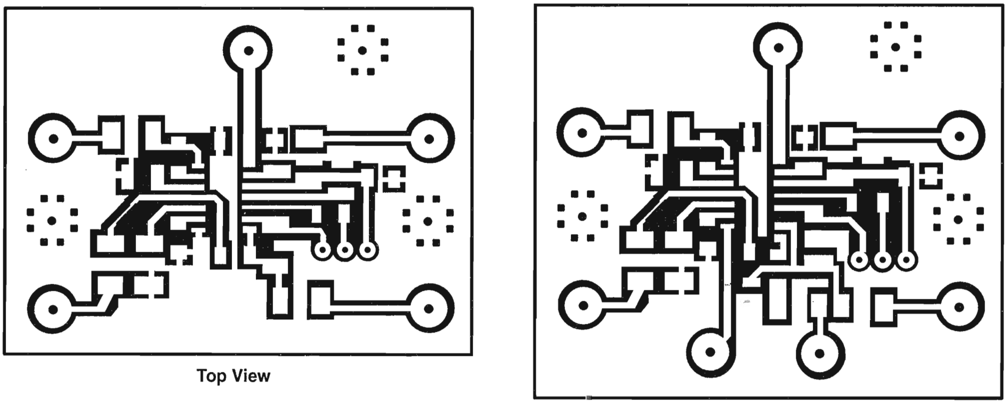
NOTE: C10 eliminated as of 11/30/94.

Figure 21. NE577 and NE578 DIP Application Board Layout



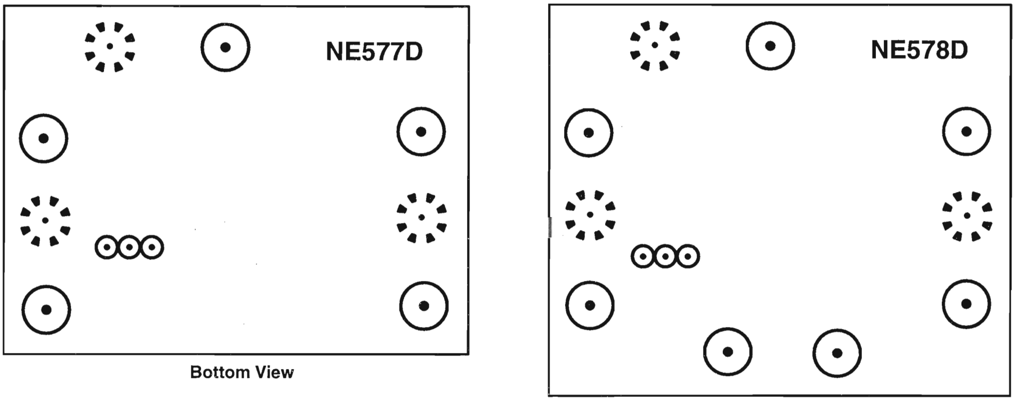
NE577 SO Top Silk Screen

NE578 SO Top Silk Screen



Top View

Top View



Bottom View

Bottom View

NOTE: C11 eliminated as of 11/30/94.

Figure 22. NE577 and NE578 SO Application Board Layout

Section 9
Wireless System Solutions

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AMPS/(E)TACS/CDPD Analog Cellular 1398
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SYSTEM SOLUTIONS FOR RF/WIRELESS STANDARDS

As the fastest growing area in electronics, the wireless personal communications market is fiercely competitive for semiconductor, communication equipment and EDP vendors alike. As a market characterized by a multiplicity of standards, only vendors with resources, vision and a commitment to innovation will realize the standards of the future. Philips Semiconductors is such a vendor, with complete system solutions for virtually all current cellular, cordless and paging standards, and with roadmaps for the global systems of the future.

The following section contains information on chipsets for several cellular telephone, cordless telephone, and wireless data standards. The system solutions and block diagrams presented in this section represent Philips chipset solutions that are currently available. Detailed information on individual ICs can be found in the preceding sections of this or other referenced data handbooks.

The list of solutions presented is by no means exhaustive, and is intended to demonstrate Philips' products and capabilities in several important wireless markets. Philips is constantly moving forward with new solutions for existing, as well as emerging, standards. If you would like more information on current chipsets and standard ICs, or would like to see what we are planning for the future, please contact your local Philips sales engineer or Philips representative.

System Standard Selector Guide

RF/Wireless Communications

System Standard — Product Selector Guide

● Recommended part-type / system solution
X Alternate solution

PRODUCTS			TARGET SYSTEMS										
Function	Type	Description	Cellular			Cordless					Wireless Data		
			(N)AMPS /(E)TACS	IS-54/ TDMA	GSM	CT0	CT1	SS	DECT	PHS	802.11	CDPD	PAGERS
RF Amplifiers	SA5200	Gain block – 1GHz			X		X	X					
RF Front-End	SA600	LNA/Mixer – 1GHz	X	X				X				X	
	SA601	LNA/Mixer – 1GHz	●	●			●	●				●	
	SA1620	Low voltage GSM RF transceiver			●								
	UAA2072M	Image reject GSM front-end			X								
	UAA2080T	Advanced pager receiver											X
	UAA2082	Advanced pager receiver											●
Synthesizers\ Prescalers	UMA1014T	Synthesizer – BIP – 1GHz	X				X					X	
	UMA1015M	Low-voltage, dual – 1GHz	●				●					●	
	UMA1017M	Low-voltage, single loop – 1GHz			X			X					
	UMA1018M	Low-voltage, low noise – 1GHz			●								
	UMA1019M	Low-voltage, single loop - 2GHz			●				●				
	UMA1020M	Low-voltage, low noise – 2.4GHz							●	X	●		
	UMA1005T	Synthesizer, Fractional-N		X	X								
	SA7025	Low-voltage, Fractional-N – 1GHz		●	X								
	SA8025	Low-voltage, Fractional-N – 2GHz								●	X		
Mixer / IF / Demod	SA605	High perf/wide BW mixer FM/IF	X	X	X			X	X	X	X	X	
	SA606/7/8	Low-voltage, high perf mixer FM/IF	●	●		●	●					●	
	SA626	Low-voltage/Wide BW/fast RSSI						●		●			
	SA636	SA626 with Wideband data output							X		●		
	SA637	SA626 with Digital IF		●									
	SA639	Low-voltage mixer FM/IF w/switch							●		●		
	SA1638	Low-voltage GSM IF transceiver			●								
Transmitter	SA900	I/Q transmit modulator		●									

RF/Wireless Communications

System Standard — Product Selector Guide

● Recommended part-type / system solution
X Alternate solution

PRODUCTS			TARGET SYSTEMS										
			Cellular			Cordless					Wireless Data		
Function	Type	Description	(N)AMPS /(E)TACS	IS-54/ TDMA	GSM	CT0	CT1	SS	DECT	PHS	802.11	CDPD	PAGERS
Audio Processing	SA5752	Audio processor system – 3V	●									●	
	SA5753	Audio processor system – 3V	●									●	
	NE576/77/78	Compandor	X			●	●						
Data Processing	UMA1000LT	Data processor – 3V	●									●	
	PCD5032	ADPCM – codec							●				
	PCD5040/41	Burst Mode controller							●				
	PCF5081/82	Digital signal processor			●								
	PCD5071	Baseband interface			●								
	PCF5001	POCSAG paging decoder											●
	PCF5003	Advanced POCSAG paging decoder											●
Control	89CE558	Microcontroller with flash memory	X									X	
	P90CL301	Low-voltage 16-bit microcontroller			●				X				
	P80CL51	Low-voltage 8-bit microcontroller				●	X						X
	P80CLxxx	Low-voltage 8-bit microcontroller							●				
	TDA8005	Smart card interface			●								
(IC20)	P83CL580	Microcontroller	●									●	
(IC20)	P83CL781/2	Microcontroller				X	●						X
(IC20)	P83CL410	Microcontroller											X
Misc.	PCA5075*	RF PA controller			●								
	TDA7050	Audio amplifier	●										
	TDA8781	Log amplifier			X								

AMPS/(E)TACS/CDPD Analog Cellular

Analog Cellular Chipset
AMPS (Advanced Mobile Phone Service)
TACS (Total Access Communication System)
CDPD (Cellular Digital Packet Data)

AMPS/(E)TACS AND CDPD

Although the AMPS/(E)TACS analog cellular market is now in a stage of maturity, price erosion has led to rapid growth and a transformation from a business only to a mass consumer market. This growth continues not only in the US and UK (where the standards originated) but also in mainland Europe, Asia and Latin America. Interest in wireless data communications is also fuelling growth of the related Cellular Digital Packet Data (CDPD) standard.

For manufacturers facing shorter product life cycles, rapidly decreasing market prices and faster times-to-market, our system solutions present a unique opportunity. A worldwide network of application support centers is equipped to provide valuable assistance at all stages of the development process, from initial design through qualification and final production.

Current AMPS/(E)TACS and CDPD chip-set

Out current chip-set uses 3V technology to improve power consumption and standby- and talk-time in today's hand-held phones. Evaluation kits are available for AMPS (OM4753), and will shortly be available for (E)TACS (OM4751) and AMPS/CDPD (OM15001) standards. The AMPS/(E)TACS kits include a fully functional target system: handset, LCD, keypad, 3 evaluation boards (baseband board, RF transceiver board, software emulation board) and object code. The AMPS/CDPD kit contains a multilayer test board, which integrates RF and baseband functions, and demonstration software.

RF Transceiver

The RF transceiver is composed of three low voltage, high performance ICs. The SA601 RF front end incorporates a low noise amplifier (LNA) and downconvert mixer to translate the incoming RF signal to the first IF. The SA606 FM IF further downconverts and demodulates the 1st IF signal to provide the audio/data and RSSI signals. The UMA1015 dual frequency synthesizer locks the receive and transmit VCOs. These three ICs typically draw a total of 20mA or less from a 2.7 to 5.5V supply.

Our BGY series of power modules provide a complete, integrated solution for all power classes of AMPS/(E)TACS and CDPD products.

Baseband Section

The AMPS/(E)TACS baseband solution handles all audio and data processing, control and memory functions. The SA5752, SA5753 audio processors and TDA7050 audio amplifier provide companding, VOX, filtering, amplification and control functions needed to meet AMPS and (E)TACS system requirements. The UMA1000LT data processor incorporates all of the necessary data transceiving, processing and SAT functions. The P83CL580 8-bit microcontroller, PCF8582T EEPROM and PSD312L EPROM provide the control and memory for the entire handset.

Software

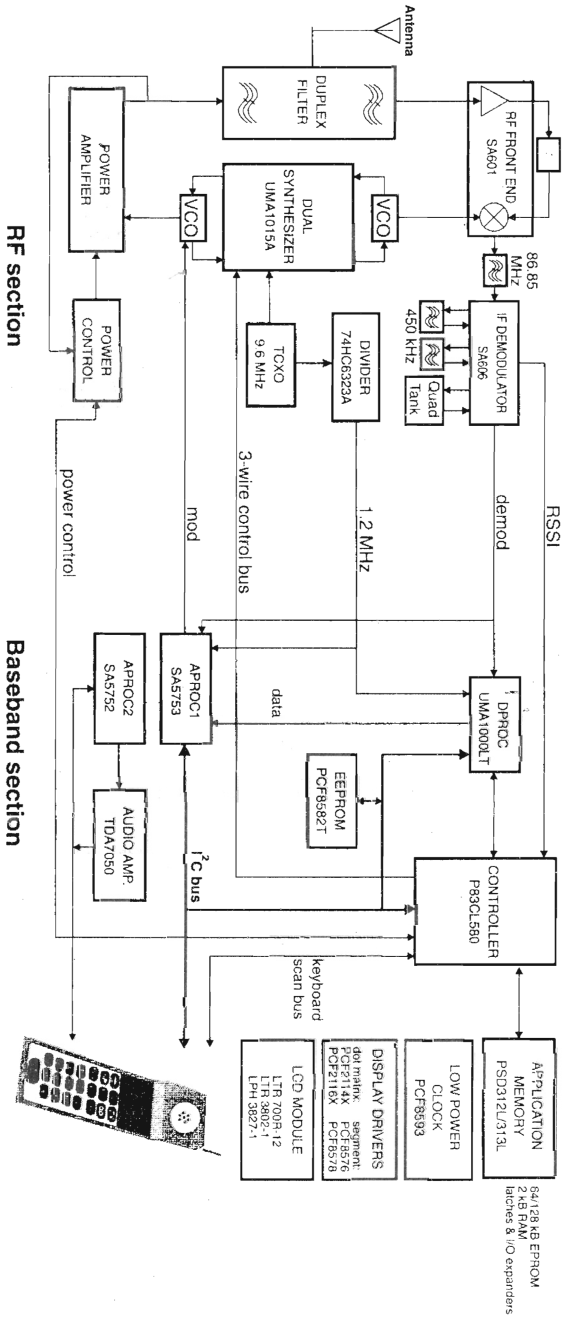
A demonstration software package is available (OM4752), based on the PL/M51 language. Together with the hardware evaluation kits, customers can use this software to evaluate AMPS/(E)TACS protocol and operation. The software controls the transmit, receive and man-machine interface (MMI) portions of the system.

Soon to be available is our protocol software running under a real-time operating system. With its real-time kernel, the software is event-driven, enabling the system controller to power down quickly when idle. As this protocol software is being developed with our module-set for official approval (CTIA/FCC/BABT), you'll be able to purchase a "qualified" software package. The software, supplied as object code, will have standardized MMI and hardware-platform interfaces. This enables easy customization of the MMI and hardware using the "C" language.

The Philips Semiconductors AMPS/(E)TACS/CDPD chipset consists of:

		IC-17 Page
SA601	Low voltage LNA and mixer - 1GHz	51
SA606	Low-voltage high performance mixer FM IF system	522
UMA1015M	Low-power dual frequency synthesizer for radio communications	907
SA5752	Audio processor - companding, VOX and amplifier section	1077
SA5753	Audio processor - filter and control section	1087
UMA1000LT	Data processor for cellular radio (DPROC)	1296
P83CL580	8-Bit Microcontroller	IC-20
TDA7050	Audio amplifier	

AMPS/(E)TACS/CDPD Analog Cellular



IS-54/TDMA Digital Cellular

North American Digital Cellular (NADC) IS-54/TDMA RF Transceiver Chipset

IS-54 (D-AMPS; TDMA) AND IS-95 (CDMA)

Designed to address the problem of using existing channels more efficiently, IS-54 employs the same 30 kHz channel spacing and frequency bands (824-849 and 869-894 MHz) as the current North American analog cellular standard: AMPS. By using TDMA instead of FDMA, IS-54 increases the number of users from 1 to 3 per channel (up to 10 with enhanced TDMA). The IS-54 specification states that the digital handset and system must also support the analog AMPS system. Although it's early days for IS-54, forecasts indicate there will be over 4 million users in three years time. Experience from the low power AMPS chip-set, together with customer inputs, were combined to produce a 4-chip solution for an IS-54 RF/IF section.

IS-95 is another digital standard that uses the same frequency bands as AMPS and supports AMPS operation. This standard uses CDMA, employing spread-spectrum technology and a special coding scheme. This standard is at a very early stage but promises a threefold increase in user capacity over IS-54.

IS-54 transceiver chip-set

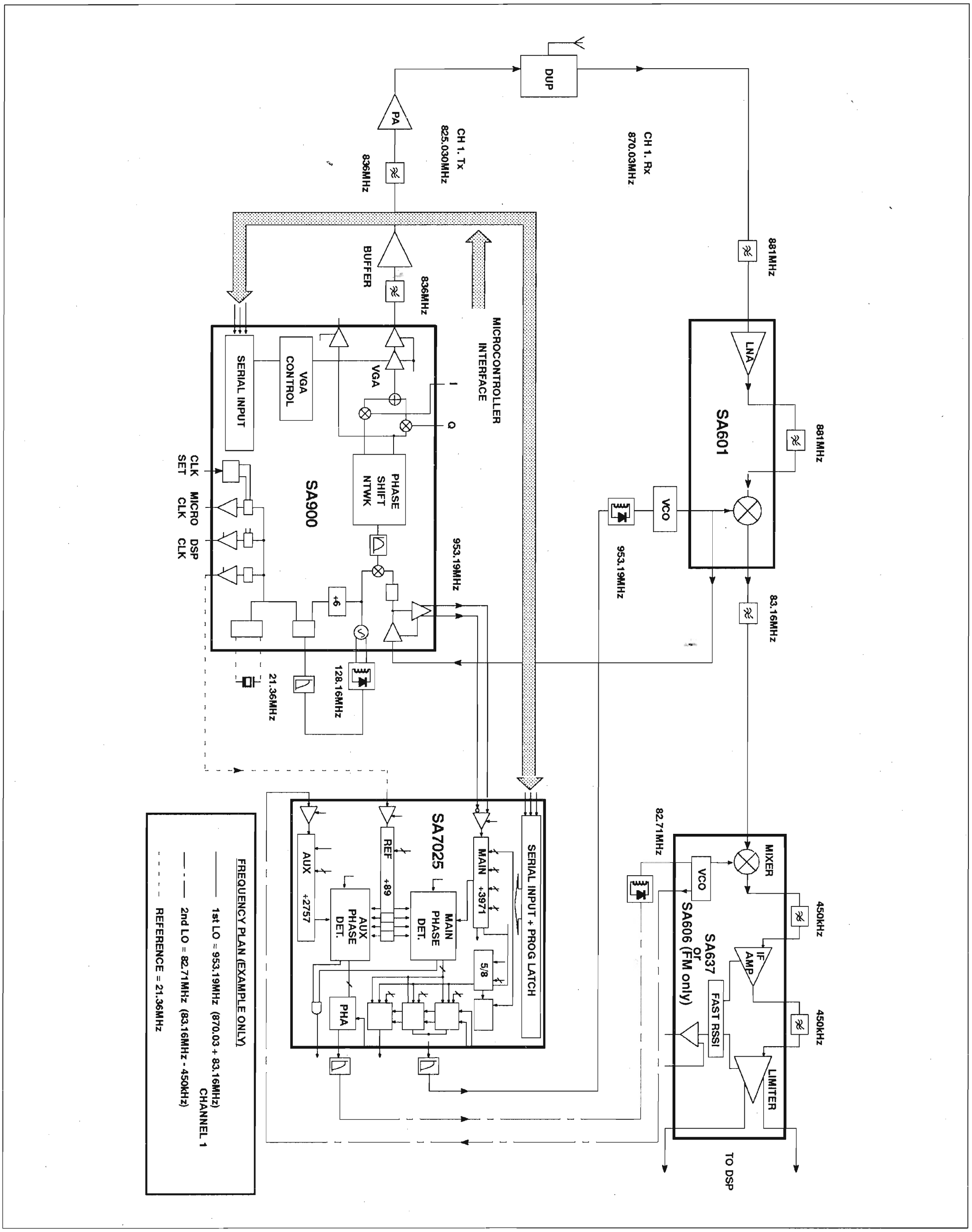
To compete with existing analog standards, a low power, highly integrated solution is a must for any digital standard to succeed. Our new chip-set for IS-54 meets these criteria. The chip-set combines all of the necessary RF and IF functions into four integrated devices: the SA601 RF front end, the SA7025 dual frequency synthesizer, the SA900 I/Q transmit modulator and the SA637 digital IF receiver *or* SA606 FM IF receiver + external I/Q demodulator. These devices were designed as a system and therefore have interface levels which are matched, eliminating the need for additional buffers and interface devices. There is also a common high speed serial interface bus, making addressing the devices simpler. Additionally the frequency plan was designed to eliminate the need for an additional synthesizer and VCO loop. All of these features dramatically reduces the cost and size while improving the performance of the overall system.

Although this is not the only IS-54 solution, our 4-chip configuration is the most integrated and easy to use chip-set available today. For example, the SA900 provides I/Q modulators, the phase shifter, the VGA, a filter, control logic, clock distribution and more in a single IC. The need for two RF synthesizers was eliminated by closely coupling the SA7025 and the SA900 so it is possible to use the main synthesizer to simultaneously generate receive and transmit signals. The integration and connectivity of the chip-set promote significant cost reduction. In addition this integrated solution reduces the time to a final product by simplifying the design effort. The result is a smaller, cost effective, low-power phone that is ultimately more attractive to the end users.

Moving to a digital standard not only provides for increase in capacity, but offers the advantages of service integration. With the use of a digital modulation, other services such as data and fax can also be handled more easily over this system.

The Philips Semiconductors IS-54 TDMA RF transceiver chipset consists of the following ICs:		**IC-17 Page**
SA601	Low voltage LNA and mixer - 1GHz	51
SA606	Low voltage high performance mixer FM/IF system	522
SA637	Low-voltage digital IF receiver	666
SA7025	Low-voltage 1GHz fractional-N synthesizer	756
SA900	I/Q transmit modulator	1005

IS-54/TDMA Digital Cellular



GSM/DCS1800 Digital Cellular

GSM (Global System for Mobile Communications)/DCS1800 Digital Cellular Chipset

GSM/DCS1800 (PCN)

As one of the IPR (intellectual property rights) holders of the Global System for Mobile communications (GSM), Philips Semiconductors was involved in GSM-specific integration at an early stage. In 1992 Philips produced the world's first single-chip baseband signal processor for GSM. This early start, combined with our knowledge in wireless personal communications, has enabled us to provide complete solutions to meet all your needs for the GSM (900 MHz) digital standard , and its PCN derivative DCS1800 (1800 MHz).

Our GSM/DCS1800 portfolio comprises complete, low-power solutions for manufacturers of handsets and modules. These solutions include total support (from system design to software for all GSM "layers"), and cover all functions from loudspeaker & microphone to antenna. All Philips Semiconductors' solutions comply with the general specifications of the GSM digital cellular network.

1st Generation GSM chip-set

Our first generation chip-set uses 5V technology and has built-in power management to increase standby and talk-time. It performs all functions required for GSM phones and comes with complete hardware/software support. A fully operational demo-kit is available for system evaluation.

The RF transceiver performs all up-/down-modulation of the baseband and RF frequencies, respectively. It comprises: the PCA5075 (power amplifier controller), UAA2071 (RF transmitter), UAA2072M (RF receiver), UMA1018 (frequency synthesizer), NE602A (IF receiver) and the TDA8780 (logarithmic amplifier).

The single-chip baseband interface (BBI; PCD5071) performs all AD/DA conversions of the baseband (IF) frequency and the GMSK modulation/demodulation.

All GSM baseband signal-processing algorithms are handled in the PCF5081 single-chip RISC processor. The DSP communicates via three interfaces: a serial interface through the BBI to the RF section, a serial speech interface to the audio Codec and a parallel interface to our 68000-based system controller. Signal processing is implemented in software using application-specific hardware to speed up execution of the program modules.

The system controller (P90CL301) and TDMA timer (PCF5076) perform all the GSM layer 1 to layer 3 tasks and provide time-critical hardware signals. The smartcard interface (TDA8005) controls the display, keyboard and smartcard (SIM - Subscriber Identity Module).

Other components of the chip-set comprise a program ROM and data RAM for the system controller, and a proprietary 14-bit audio Codec (ARCOFI).

2nd generation GSM/DCS1800 chip-set

With samples available in early 1995, this 3 V chip-set uses low-power, low-voltage technology, is highly integrated and is suitable for GSM and DCS1800 (PCN) systems. This 8-chip solution is the next milestone on the road to smaller digital phones. Key features include ICs fabricated in 0.5mm CMOS technology for the baseband and QUBiC (BiCMOS) technology for the RF part. The ICs are encapsulated in small TQFP packages.

In the RF section, three new ICs complement the existing PCA5075: the SA1620 RF transceiver, the SA1638 IF transceiver and the UMA1019 RF synthesizer. The new chip-set has been developed with future systems in mind. Only minor changes are required to support DCS1800/PCS1900 or dual-mode and multi-mode handsets (e.g. GSM/DCS or GSM/DCS/DECT). The chip set supports high IF frequencies and allows simple, low-cost filters to be used for image-rejection.

The baseband and audio interface (PCD5072) is a new single-chip interface between the IF transceiver, the microphone & earpiece and the baseband processor. It integrates an audio Codec and auxiliary AD/DA converters for AGC, AFC and power management.

The new baseband DSP (PCF5083) includes the TDMA timer. Like the earlier PCF5081, an on-chip ROM contains firmware program modules to perform all necessary processing algorithms. Special attention has now been given to equalization to improve performance in hilly areas and fast-moving vehicles.

GSM/DCS1800 Digital Cellular

Philips Semiconductors offers two complete GSM chipsets for mobile telephones and base-stations that consist of:

IC-17 Page

1st Generation Chipset for GSM:

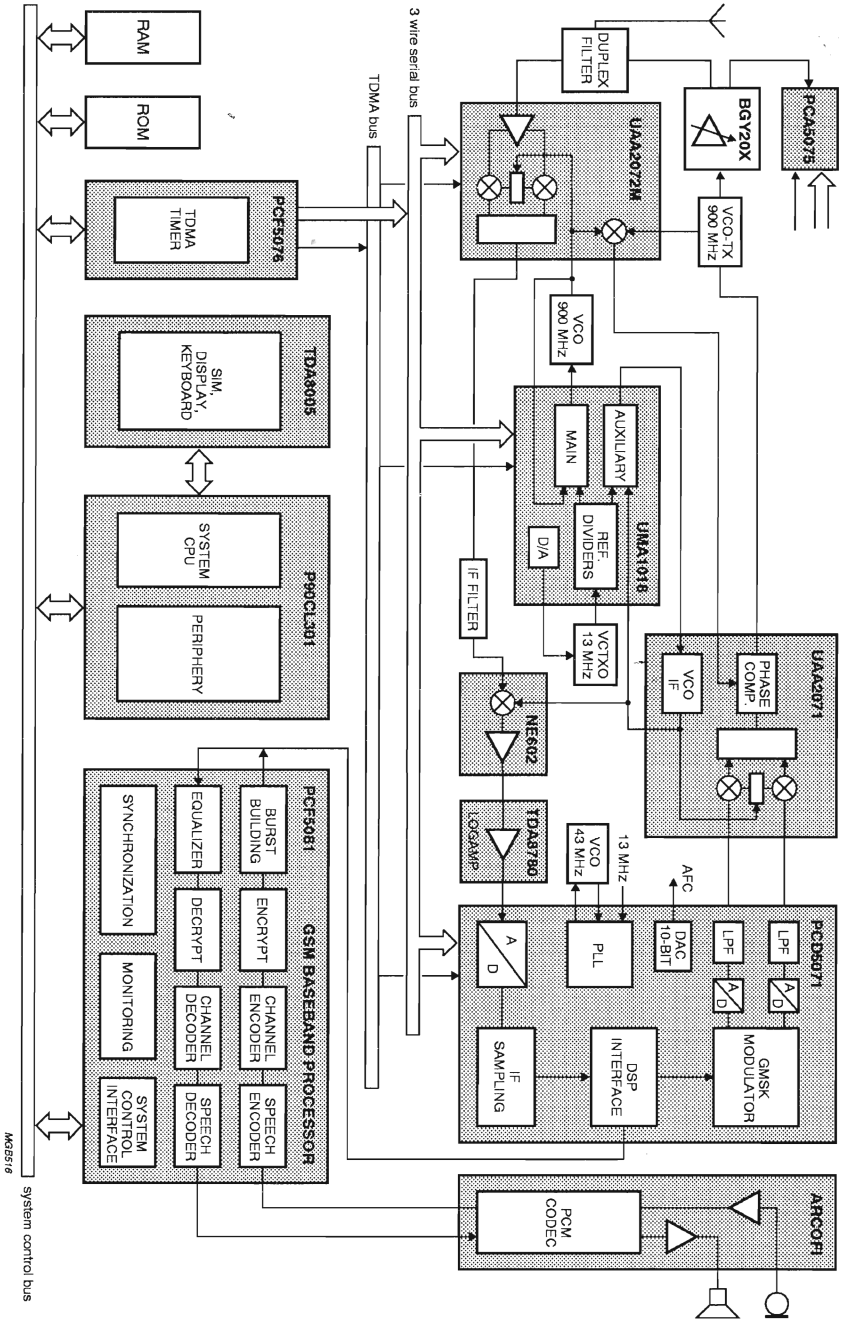
NE/SA602A	Double-balanced mixer and oscillator	62
UAA2072M	Image reject GSM front-end	137
TDA8780M	True logarithmic amplifier	409
UMA1018M	Low-voltage dual frequency synthesizer for radio telephones	1071
PCA5075	Power amplifier controller for GSM systems	1115
PCD5071	GSM baseband interface	1205
PCF5081/PCF5082	GSM baseband processors for digital mobile cellular radio	1252
UAA2071	GSM transmit modulator	IC03
TDA8005	SIM interface	IC12
PCF5076	TDMA timer	
P90CL301	Low-voltage microcontroller	

2nd Generation Chipset for GSM/DCS1800:

SA1620	Low-voltage GSM RF transceiver	102
SA1638	Low-voltage GSM IF transceiver	694
UMA1019M	Low-voltage frequency synthesizer for radio telephones	957
PCA5075	Power amplifier controller for GSM systems	1115
TDA8005	SIM interface	IC12
P90CL301	Low-voltage microcontroller	
PCD5072	GSM baseband interface	
PCF5083	GSM baseband processor	

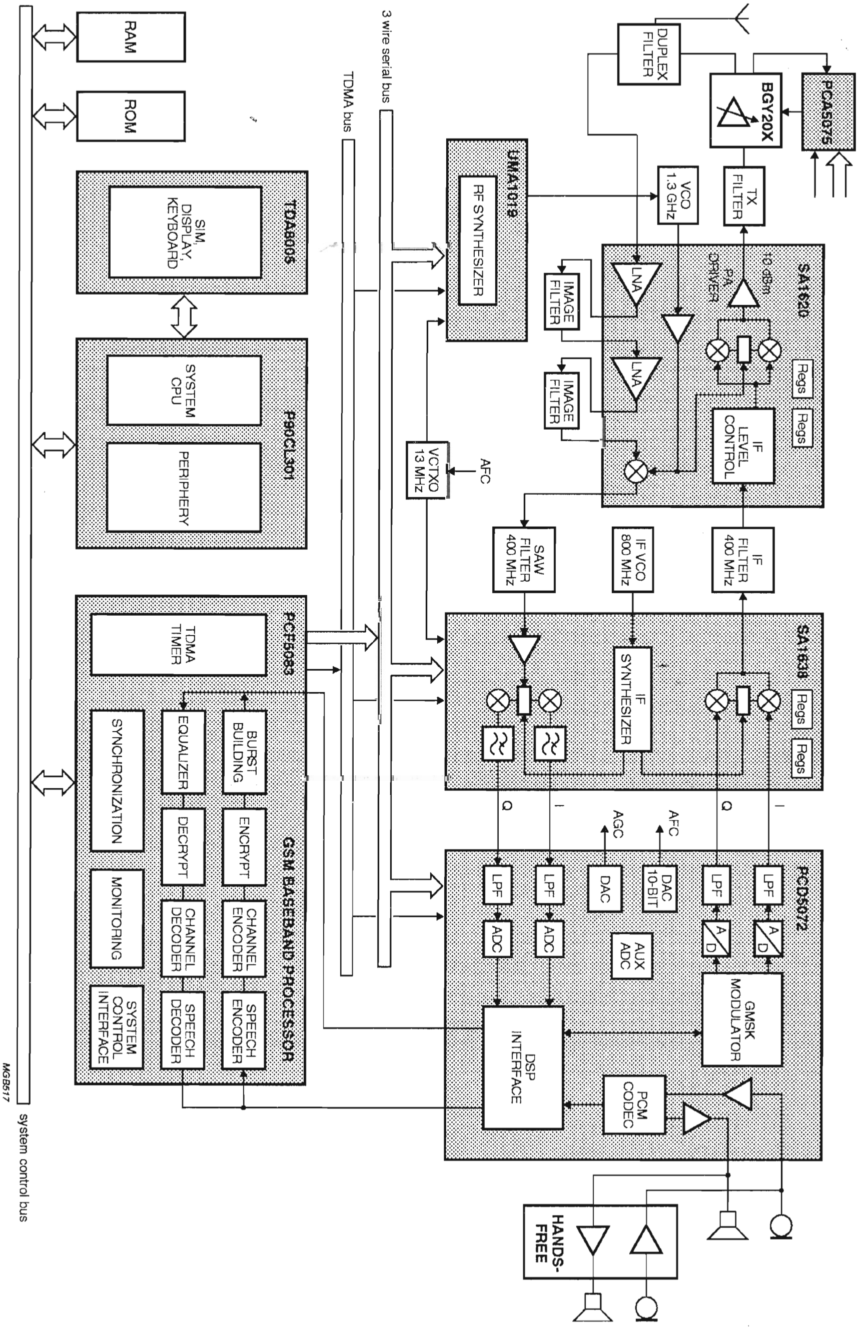
GSM/DCS1800 Digital Cellular

1st Generation Chipset for GSM



GSM/DCS1800 Digital Cellular

2nd Generation Chipset for GSM/DCS1800



CT0 Analog Cordless

CT0 Analog Cordless Chipset

CT0

This low-frequency analog cordless standard is established in many countries at various frequencies around 50MHz, including:

- France (26/41 MHz)
- Australia (30/39 MHz)
- The Netherlands & Spain (31/40 MHz)
- China, S. Korea, Taiwan, USA, Latin America (46/49 MHz)
- China (48/74 MHz).

As this market continues to grow (in terms of countries and increasing user density), our complete module/chip-set system approach to CT0 offers a low-cost solution with a number of advantages over competitors:

- It is an auto-scan, multiple-channel access (MCA) system: the base station and handset(s) automatically detect and select a free channel for incoming and outgoing calls
- 8 of the most commonly used CT0 frequency tables are incorporated in the standard chip-set, consequently software changes are not required
- One base-station unit can operate up to eight handsets.

System design is based on an advanced communication protocol using MSK (minimum shift keying) at 1200bps. This means high spectral efficiency and low-energy harmonics. Moreover, communication between base unit and handset features:

- A 20-bit security code (factory or user programmable)
- 2-way paging and 2-way intercom
- Call transfer between base unit & handset OR handset & handset
- Noise reduction for high audio performance
- DTMF/pulse dialling, or mixed-mode dialling.

The base-station unit offers a full-function speaker phone with keypad for use without handset, and a last number redial memory of 32 digits. It also includes a repertory dial memory (10 numbers of 24 digits, or 10 numbers of 16 digits + 3 emergency 28-digit numbers) and a music-on-hold facility.

The handset design incorporates an advanced power-saving algorithm to achieve a *12-day standby time.* With the same number memory facilities as the base station, it also includes a low-battery warning, an out-of-range warning and a back-light for night use.

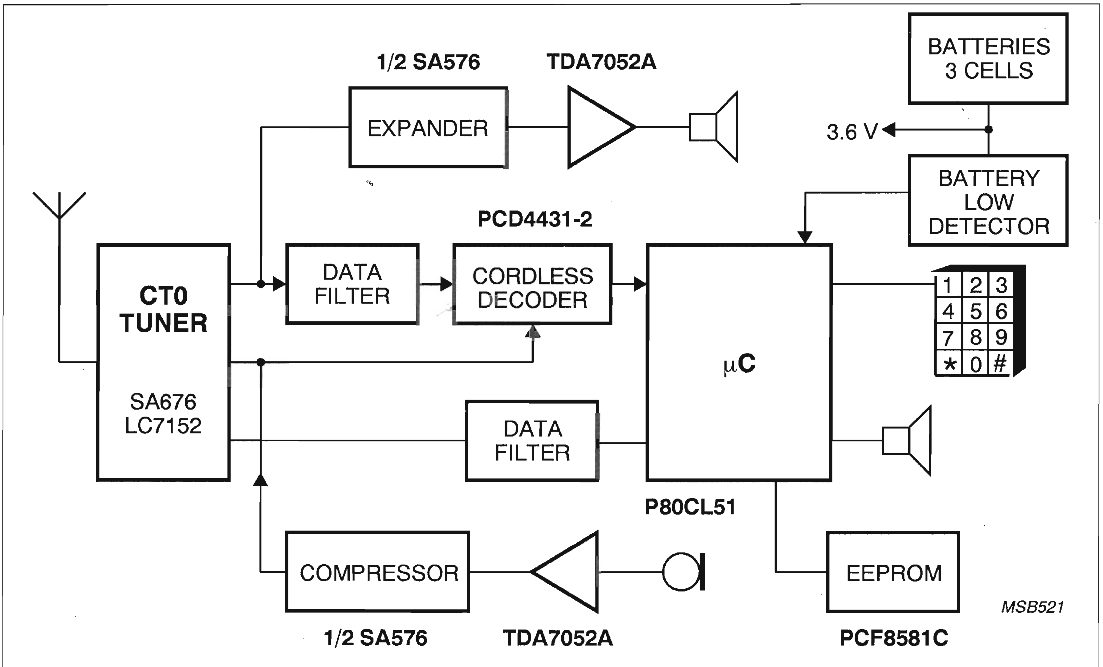
Evaluation kit

Demo/evaluation boards are available to cover all CT0 frequencies (type OM4760-X; X = country version).

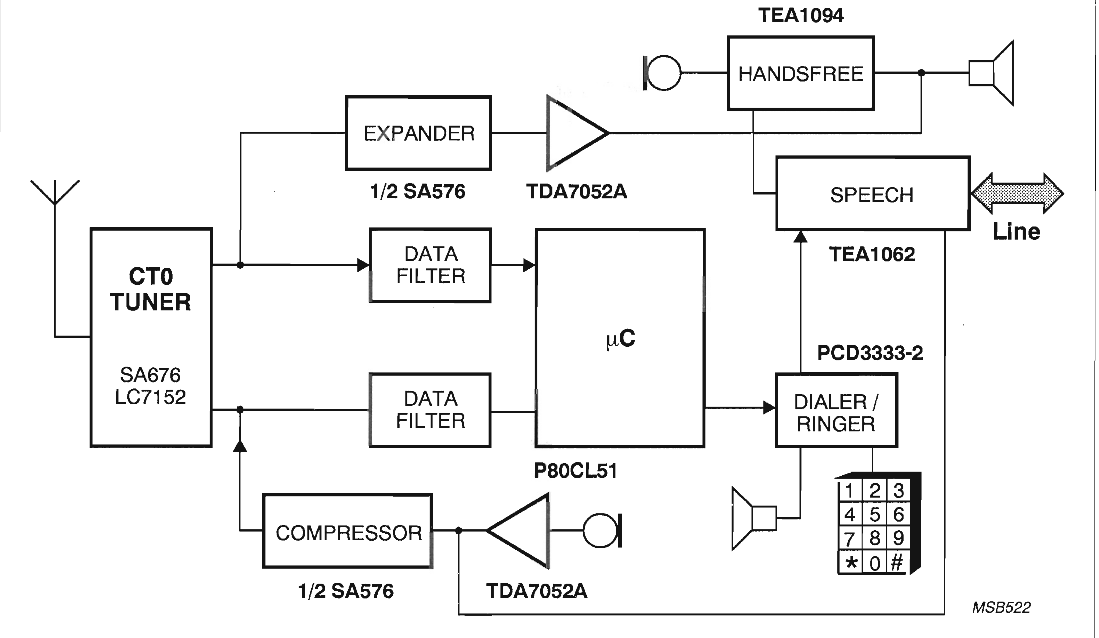
The Philips Semiconductors CTO chipset consists of the following ICs:

		IC-17 Page
TDA7052A/AT	1-Watt low voltage audio power amp with DC volume control	391
SA676	Low-voltage mixer FM IF system	685
NE/SA576	Low power compandor	1371
PCD4431-2	Cordless Decoder (handset)	IC-20
PCD3333-2	Cordless Decoder (basestation)	IC-20
TEA1094	Handsfree Speaker Phone Amplifier (basestation)	IC-20
TEA1062/ TEA1062A	Speech and Line Interface (basestation)	IC-20
P80CL51	Microcontroller	IC-20

CT0 Analog Cordless



CT0 Auto-scan Handset Solution



CT0 Base-station Solution

CT1/CT1+ Analog Cordless

CT1/CT1+ Analog Cordless Chipset

CT1/CT1+

CT1 and CT1+ have been chosen as the analog cordless standard by PTTs in several European countries. Their choice was based on the CT1/CT1+ multi-channel capability and 900MHz frequency. The high-frequency used and smaller market for this standard has made CT1/CT1+ sets inherently more expensive than CT0. However, as CT0 now features a multi-channel capability, consumer pressure is forcing CT1/CT1+ price-reductions. A low-voltage, auto-scan MCA solution for CT1/CT1+ offers a highly competitive package:

- A full solution for CT1 and CT1+ with software/hardware modifications available on request, and help in obtaining PTT approval
- One base-station can operate up to six handsets
- Advanced communication protocol
- 21-bit security code (factory or user programmable)
- 2-way paging and 2-way intercom
- Call transfer between base unit & handset OR handset & handset
- Noise reduction for high audio performance
- DTMF/pulse dialling, or mixed-mode dialling
- Programmable country settings, for all European countries.

The base-station unit offers a full-function speaker phone with keypad for use without handset, and a last number redial memory of 23 digits. It also includes a repertory dial memory (10 numbers of 23 digits), a music-on-hold facility and a fast battery charger (< 4 hrs).

The handset features the same number-memory facilities as the base-station unit, out-of-range warning and low battery warning. Battery management assures a standby time of more than 24 hours, with the handset supporting fixed or replaceable batteries.

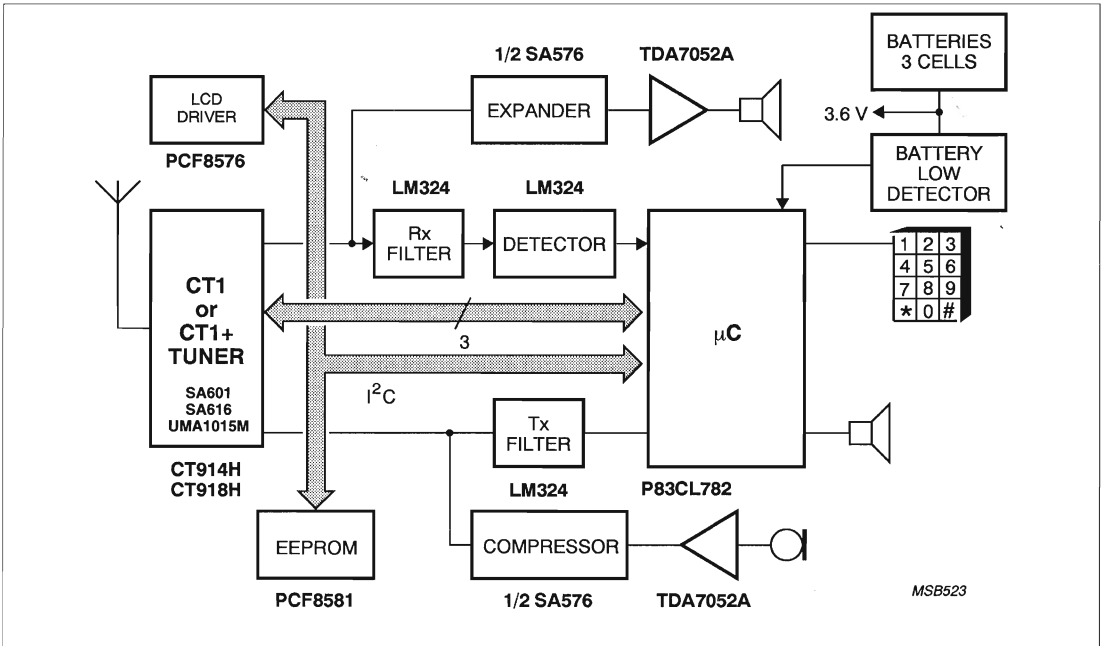
For CT1/CT1+, Philips also provide production-line testing software and service-engineer maintenance software.

Evaluation kits

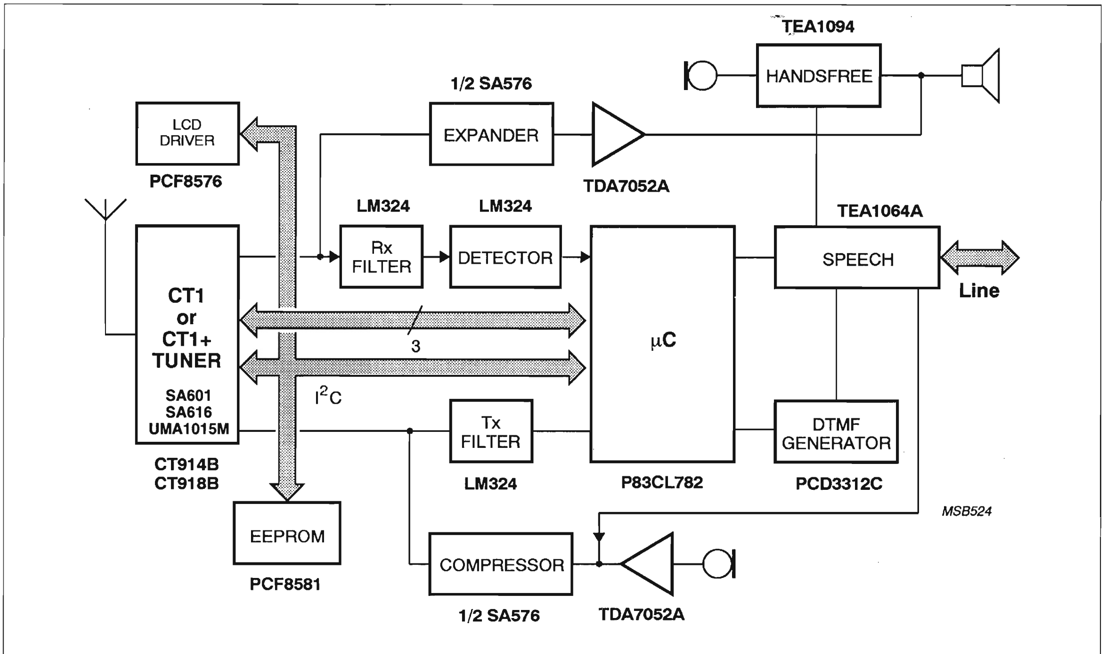
Demo/evaluation boards are available: type OM4743 for CT1 and type OM4744 for CT1+.

The Philips Semiconductors CT1/CT1+ chipset consists of:		**IC-17 Page**
SA601	Low voltage LNA and mixer — 1GHz	51
TDA7052A/AT	1-Watt low voltage audio power amp with DC volume control	391
SA616	Low voltage high performance mixer FM/IF system	538
UMA1015M	Low power dual frequency synthesizer for radio communications	907
NE/SA576	Low power compandor	1371
PCD3312	DTMF generator	IC14
P83CL782	Low voltage microcontroller	IC20
TEA1064AT	Speech and Line Interface (base-station)	IC20
TEA1094	Handsfree Speaker Phone Amplifier (base-station)	IC20

CT1/CT1+ Analog Cordless



CT1/CT1+ Handset Solution



CT1/CT1+ Base-station Solution

DECT Digital Cordless

DECT (Digital European Cordless Telephone) Chipset

DECT

The Philips Semiconductors chip-set for Digital European Cordless Telecommunication (DECT) is intended for use in a variety of wireless office and residential communications products. The chip-set is comprised of low-power ICs which provide a complete solution for both baseband and RF.

Our DECT products are supported by a complete evaluation kit, and exclusive software support via our partner Silicon & Software Systems Ltd. The services of our worldwide application laboratories are also available to help with optimum design-in.

DECT office-communication chip-set

The Philips Semiconductors low-voltage DECT PCD504X Burst-Mode Controller (BMC) forms the heart of the baseband section in base-stations and handsets. It communicates with the:

- The RF transceiver incorporates a double superheterodyne receiver that is composed of the UMA1020 2 GHz double frequency synthesizer and SA639 FM IF. Our next front-end product, the UAA2067, will include the LNA, VCOs and preamplifier. In the near future, the front-end and zero-IF ICs will become available. This will revolutionize the RF section by making SAW filters obsolete, reducing external components and making the receiver design easier.
- The speech interface to our ADPCM CODEC (PCD5032) for encoding/decoding (G721) is in compliance with CCITT recommendations. Philips Semiconductors advanced bitstream technology is used to achieve the A/D & D/A conversion. The serial DSP interface can be connected to a DSP with echo control algorithms.
- The microcontroller interface is suited to one of the Philips Semiconductors low-voltage microcontrollers: the P80CL782 (8051-core), the P83CLXXX (8051-core), the P90CL301 (68K-core) and in the near future, the 16-bit P87C51XA (80C51XA core) microcontrollers. These execute the upper layer software of the DECT protocol.

Domestic and small-business systems

For this rapidly growing market, samples of a new IC family will be available by the end of 1994: the PCD509X series. A PCD509X combines the ADPCM, BCM and microcontroller in a single IC, hence its name, the “ABC chip”. The RF interface will be upwardly compatible with the PCD504X family.

Evaluation kit supports design-in

Philips Semiconductors offers a kit (OM4756) which can be used to evaluate the DECT chip-set and as a prototype development tool. It includes an operating manual, a complete base-station and a complete rechargeable-battery-powered remote unit (hand-held). The latter comprises a baseband section built around the PCD5041 BMC, a keyboard, an LCD, an RF section and a handset.

The software on the DECT chip-set is supplied exclusively for Philips Semiconductors. It provides basic or enhanced functionality for the base-station and the remote unit. Our partner, S3, provides three different software packages: an object code license for a software package including the basic functions for a feature phone, an enhanced GAP compatible software package and, last but not least, custom-designed software.

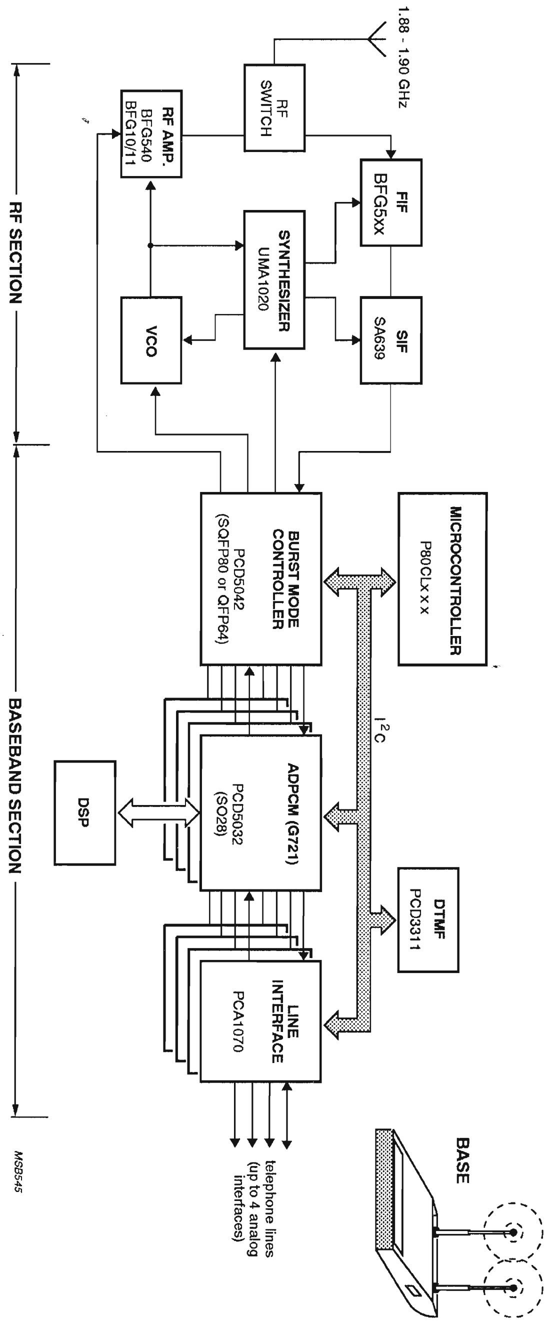
DECT Digital Cordless

Philips Semiconductors offers a DECT chipset for handsets and basestations that consists of:

		IC-17 Page
SA639	Low voltage mixer FM IF system with filter amplifier and data switch	677
UMA1020M	Low-voltage dual frequency synthesizer for radio telephones	980
PCD5032	ADPCM (G721) codec for digital cordless telephone	1165
PCD3311	DTMF Generator (basestation)	IC03
PCA1070	Line Interface (basestation)	IC03
PCD5041	DECT burst mode controller (handset)	IC03
BFG540/10/11	RF Power Amplifier	IC10
P80CLxxx	Low voltage microcontroller	IC20a
PCD5042	DECT burst mode controller (base-station)	

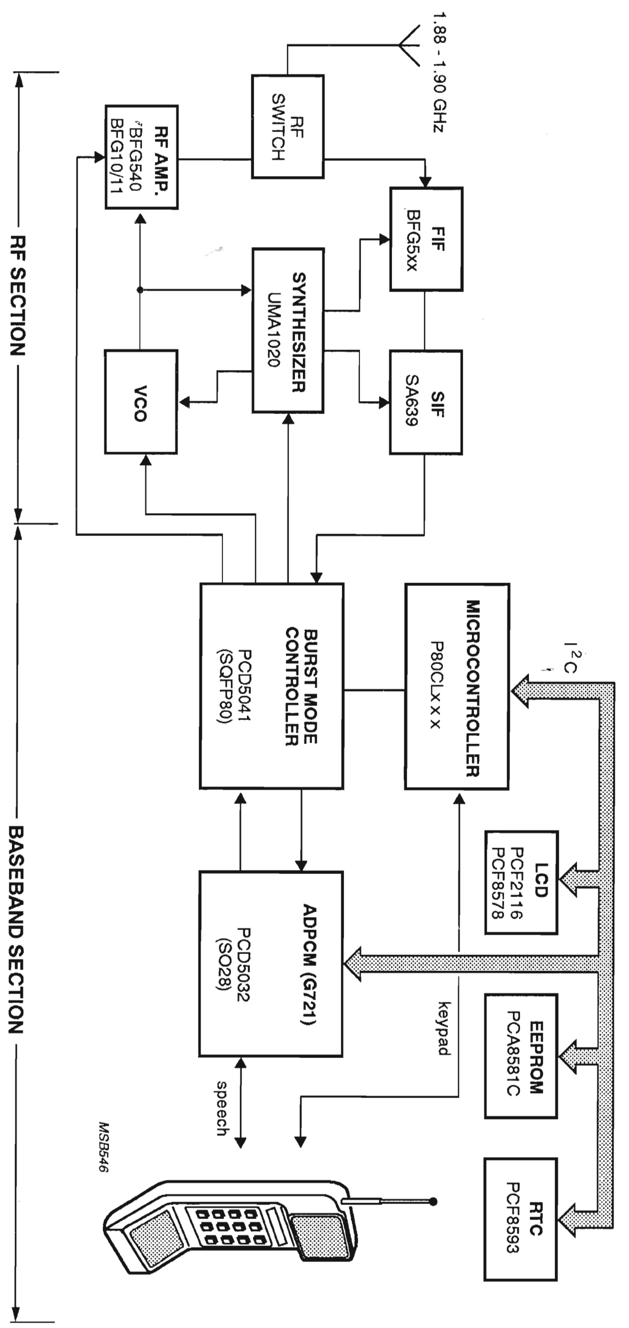
DECT Digital Cordless

DECT Base-station with a Double Superheterodyne RF Receiver



DECT Digital Cordless

DECT Handset with a Double Superheterodyne RF Receiver



PAGERS

POCSAG

Because the pager market is characterized by customization, Philips Semiconductors do not offer a turnkey solution. However, Philips Semiconductors does provide two advanced chips for all the key functions of beep-only, numeric and alphanumeric pagers:

- The UAA2080 advanced pager receiver
- The PCF5001 POCSAG paging decoder.

Philips Semiconductors also provide application support on how to build complete pagers (the only extra components required are a microcontroller, memory, LCD module and real-time clock), and offer unrivalled application support, including evaluation kits.

UAA2080 advanced pager receiver

This is a high-performance low-power radio receiver circuit primarily intended for VHF and UHF (25 - 512MHz) wide-area (country-wide) digital pagers. With a high level of integration, this is currently the only chip available for use in very thin pagers (e.g., wrist-watch or credit card types). Employing direct FM non-return-to-zero (NRZ) frequency shift keying (FSK), the receiver is based on the direct conversion principle (zero IF). Operating up to 2400 baud, the UAA2080 is unique in its size, power consumption and performance advantages. Key features include:

- High integration level
- Wide frequency range
- Low power consumption
- High sensitivity
- High dynamic range
- Interfaces directly with the PCA5000A, PCF5001 and PCD5003 POCSAG decoders
- QFP32, SO28 package or naked chip.

The next generation UAA2082 will have two additional features: the low-battery detect voltage will be reduced from 2.05V to 1.1V; the internal oscillator will be disconnected when using direct injection from a frequency synthesizer, to further reduce current consumption.

PCF5001 POCSAG paging decoder

This is a fully integrated low-power decoder and pager controller. It decodes the CCIR radio paging Code No.1 at 512 and 1200 bits/s data rates and includes a digital input filter for high call success rates. Key features include:

- On-chip EEPROM storage
- Wide supply voltage range (1.5 - 6V)
- Very low supply current (60 mA with 76.8kHz crystal)
- Data rates up to 2400 bits/s possible
- Supports 4 user addresses (Receiver Identity Codes) in 2 independent frames
- Drives an LED, a magnetic or piezo ceramic beeper directly and offers optional vibrator type alerting
- Silent call storage (up to 8 calls).
- QFP32, SO28 package or naked chip.

PCF5003 new POCSAG paging decoder

The new PCD5003 is a very low power decoder and pager controller. It supports data rates of 512, 1200 and 2400 bps using a single 76.8kHz crystal. Its on chip EEPROM is programmable with a minimum supply of 2.5V. Key features are:

- Low operating current (50mA ON; 25mA OFF)
- 2-bit random and (optional) 4-bit burst address error correction
- Up to 6 user addresses (RICs), in 6 (max) different frames
- Standard POCSAG synchronization word, plus up to 4 user-programmable synchronization words

Pagers

- Received data inversion (optional)
- Synthesizer set-up and control interface (3-line serial)
- Separate power control or Receiver and RF oscillator for battery economy
- On-chip SRAM buffer for message data
- Direct and I^2C-bus control of operating status (ON/OFF)
- Wake-up interrupt for microcontroller, programmable polarity
- Built-in data filter and bit clock recovery

Evaluation kits

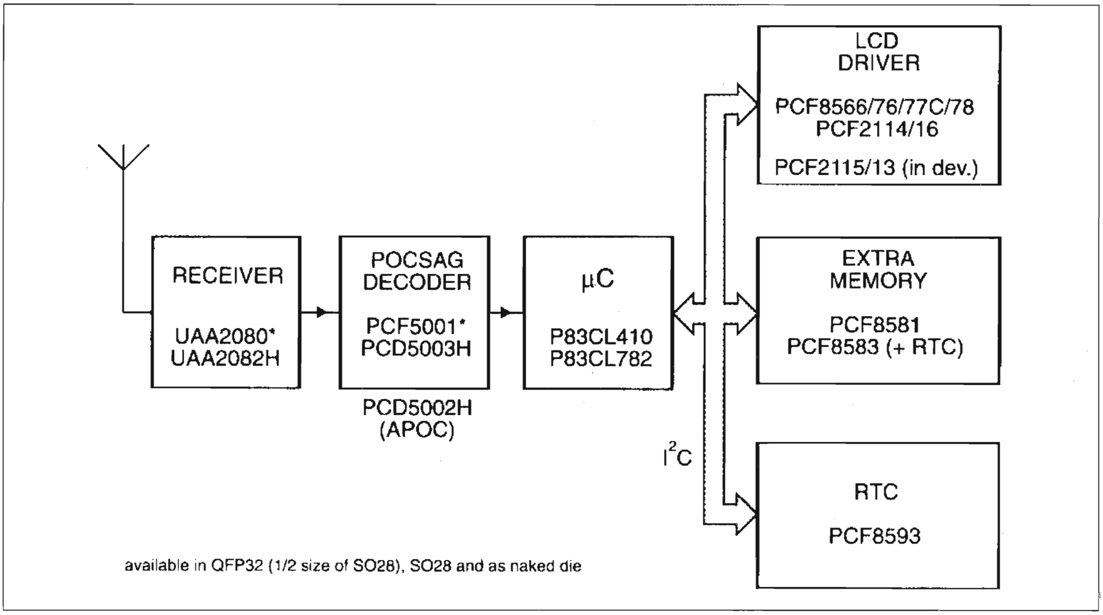
For the UAA2080 receiver, one may choose from four evaluation/demo boards:

- OM4745 for 173MHz
- OM4746 for 288MHz
- OM4747 for 470MHz
- OM4748 - frequency open.

For the PCF5001, Philips Semiconductors offers the OM4706 decoder evaluation/demo board and the OM4718 test program board. The latter allows monitoring of the decoder output from either a signal into the receiver, or a signal directly into the decoder.

Philips Semiconductors offers the following pager ICs:

		IC-17 Page
UAA2080T	Advanced pager receiver	171
UAA2082	Advanced pager receiver	209
PCD5003	Advanced POCSAG paging decoder	1128
PCF5001	POCSAG paging decoder	1218
P83CL410/782	Low voltage microcontroller	IC20



available in QFP32 (1/2 size of SO28), SO28 and as naked die

Section 10
Package Outlines

RF/Wireless Communications

INDEX

SOT97-1	8-Pin (300 mil) Plastic Dual In-Line Package	1419
0404B	8-Pin (300 mils wide) Plastic Dual In-Line (N) Package	1420
0174C	8-Pin (157 mils wide) Plastic SO (Small Outline) Dual In-Line (D) Package	1421
SOT110-1	9-Pin Plastic SIL (Single In-Line) Medium Power Package With Fin	1422
0405B	14-PIn (300 mils wide) Plastic Dual In-Line (N) Package	1423
0175D	14-Pin (157 mils wide) Plastic SO (Small Outline) Dual In-Line (D) Package	1424
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SOT38-1	16-Pin (300mil) Plastic Dual In-Line Package	1427
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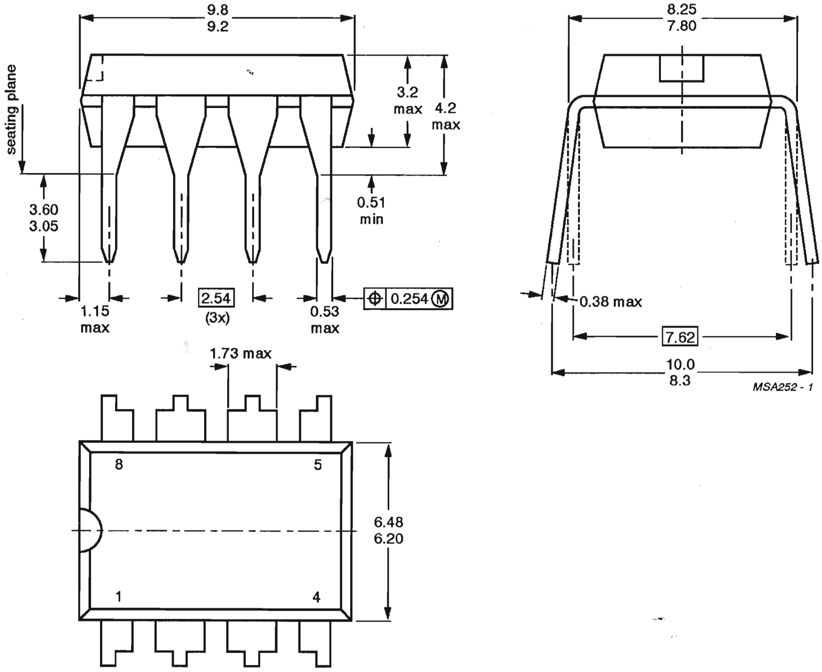
SOT109-1	16-Pin (3.9mm) Plastic SO (Small Outline) Package	1429
SOT162-1	16-Pin Plastic SO (Small Outline) Package; Large Body	1430
SOT102	18-pin Plastic Dual In-Line (N/P) Package With Internal Heat Spreader	1431
0408B	20-Pin (300 mils wide) Plastic Dual In-Line (N) Package	1432
SOT163-1	20-Pin (Large Body) Plastic SO (Small Outline) Package	1433
0172D	20-Pin (300 mils wide) Plastic SOL (Small Outline Large) Dual In-Line (D) Package	1434
1563–	20-Pin Plastic (170 mils wide) SSOP (Shrink Small Outline Package)	1435
SOT266-1	20-Pin (4.4mm) Plastic SSOP (Shrink Small Outline Package	1436
0412A	24-Pin (600 mils wide) Plastic Dual In-Line (N) Package	1437
0173D	24-Pin (300 mils wide) Plastic SOL (Small Outline Large) Dual In-Line (D) Package	1438
SOT355-1	24-Pin (Medium Body) Plastic TSSOP (Thin Shrink Small Outline) Package	1439
0413B	28-pin (600 mils wide) Plastic Dual In-Line (N) Package	1440
SOT117-1	28-Pin (600 mil) Plastic Dual In-Line Package With Internal Heat Spreader	1441
SOT136-1	28-Pin (7.5mm) Plastic Small Outline Package	1442
0006C	28-Pin (300 mils wide) Plastic SOL (Small Outline Large) Dual In-Line (D) Package	1443
SOT358-1	32-Pin (7x7x1.4 mm) Plastic TQFP (Thin Quad Flat Package)	1444
SOT287-1	32-Pin (7.5mm) Plastic SO (Small Outline) Package	1445
SOT307B	44-Pin Plastic QFP (Quad Flat Pack)	1446
1706B	48-Pin Plastic Thin Quad Flat Pack (B) Package	1447
SOT208A	64-Lead Plastic QFP (Quad Flat Package)	1448

Package outlines

SOT97-1 8-Pin (300 mil) Plastic Dual In-Line Package



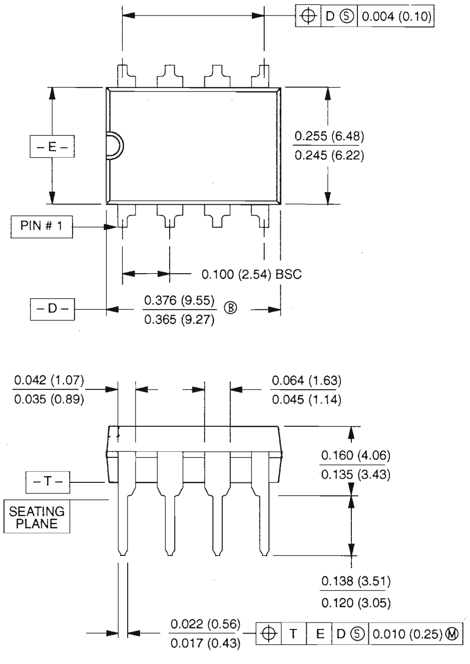
Dimensions in mm.

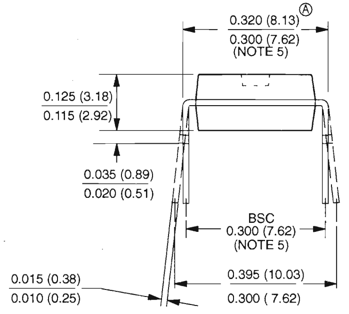
Package outlines

0404B 8-Pin (300 mils wide) Plastic Dual In-Line (N) Package

NOTES

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AB for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 8 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #8 when viewed from the top.

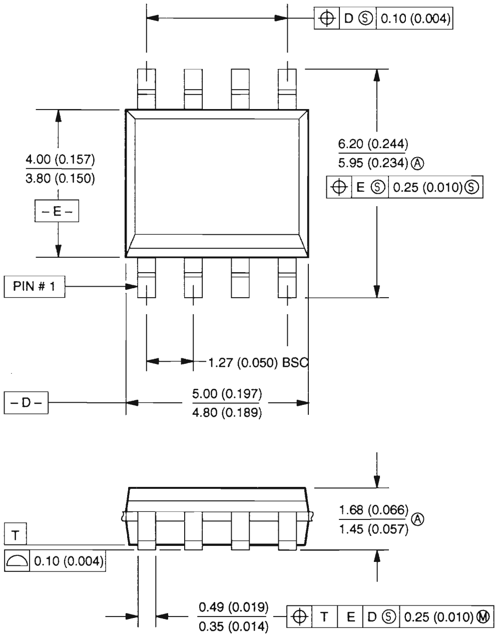




853–0404B 07236

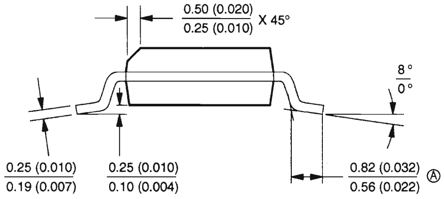
Package outlines

0174C 8-Pin (157 mils wide) Plastic SO (Small Outline) Dual In-Line (D) Package



NOTES

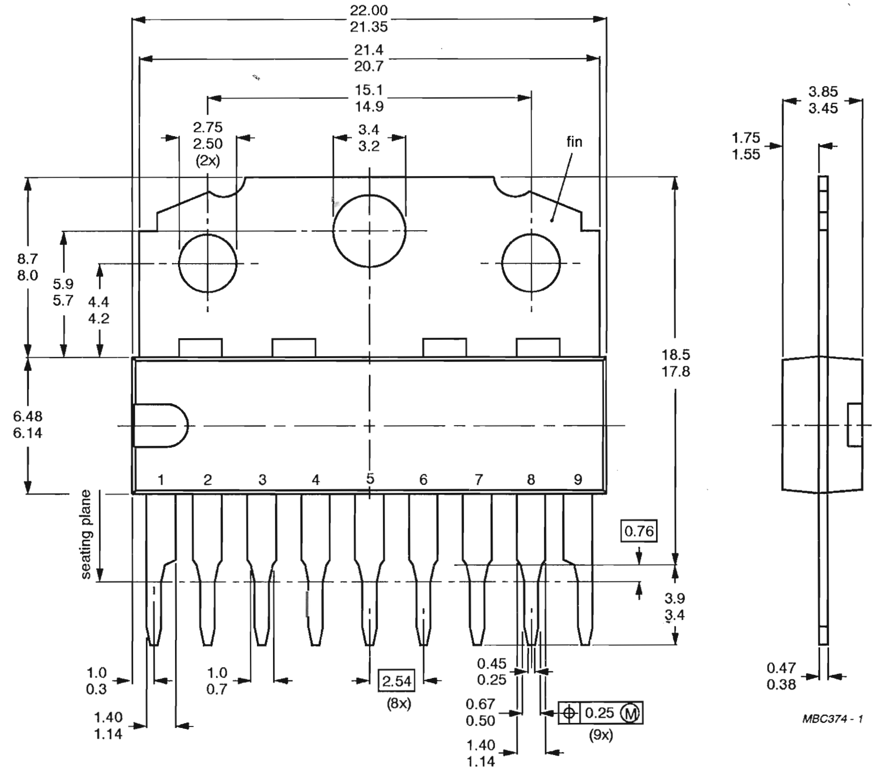
1. Package dimensions conform to JEDEC Specification MS-012-AA for standard Small Outline (SO) package, 8 leads, 3.75mm (0.150") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "D" and "E" are reference datums on the molded body and do not include mold flash/protrusions. Mold flash/protrusions at "D" shall not exceed 0.15mm (0.006") per side. Inter-lead flash/protrusions at "E" shall not exceed 0.25mm (0.010") per side.
5. The lead width above the seating plane shall not exceed a maximum value of 0.61mm (0.024").
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #8 when viewed from top.
7. Signetics ordering code for a product packages in a plastic Small Outline (SO) package is the suffix D after the product number.



853–0174C 04697

Package outlines

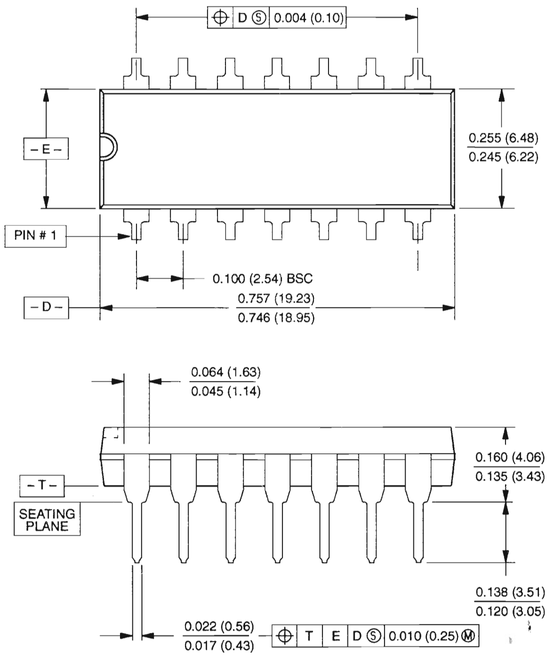
SOT110-1 9-Pin Plastic SIL (Single In-Line) Medium Power Package With Fin



Dimensions in mm.

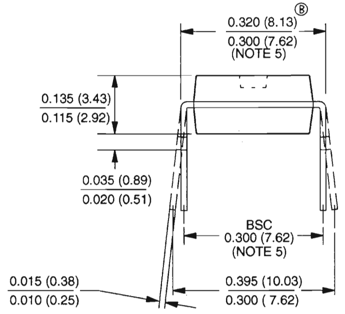
Package outlines

0405B 14-PIn (300 mils wide) Plastic Dual In-Line (N) Package



NOTES

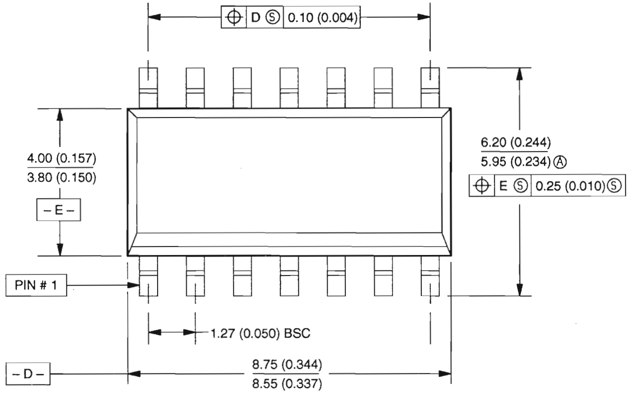
1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AC for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 14 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #14 when viewed from the top.

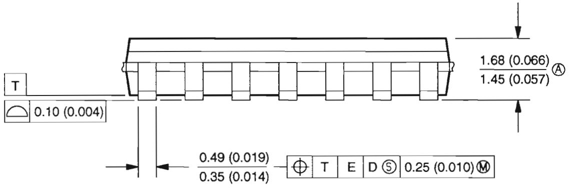


853–0405B 02880

Package outlines

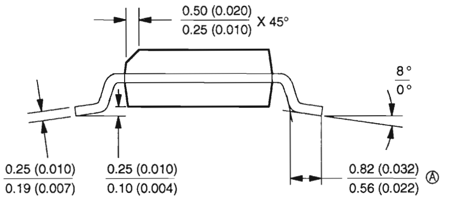
0175D 14-Pin (157 mils wide) Plastic SO (Small Outline) Dual In-Line (D) Package





NOTES

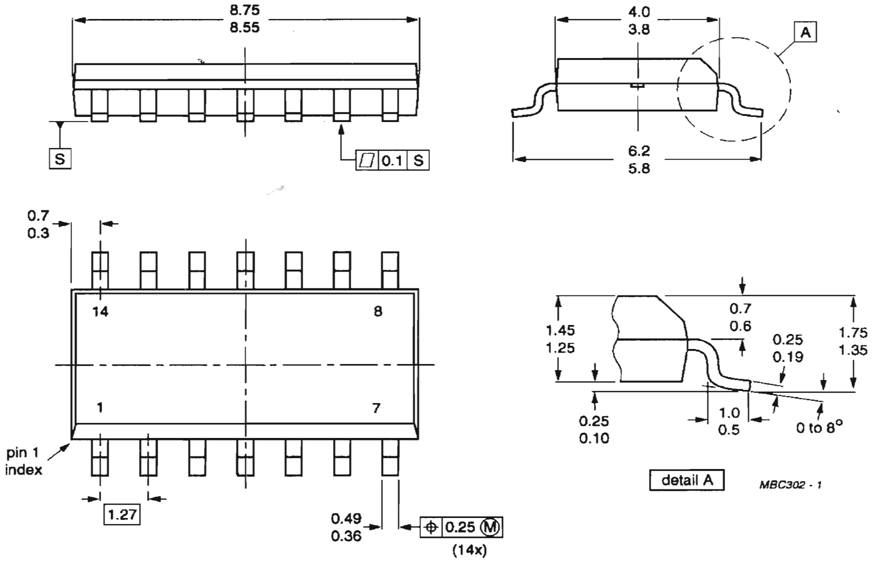
1. Package dimensions conform to JEDEC Specification MS-012-AB for standard Small Outline (SO) package, 14 leads, 3.75mm (0.150") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "D" and "E" are reference datums on the molded body and do not include mold flash/protrusions. Mold flash/protrusions at "D" shall not exceed 0.15mm (0.006") per side. Inter-lead flash/protrusions at "E" shall not exceed 0.25mm (0.010") per side.
5. The lead width above the seating plane shall not exceed a maximum value of 0.61mm (0.024").
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #14 when viewed from the top.
7. Signetics ordering code for a product packages in a plastic Small Outline (SO) package is the suffix D after the product number.



853–0175D 04697

Package outlines

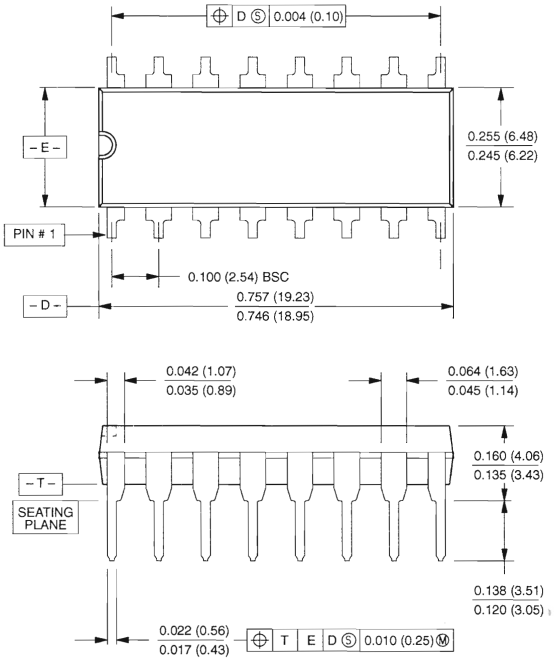
SOT108-1 14-Pin (3.9mm) Plastic SO (Small Outline) Package



Dimensions in mm.

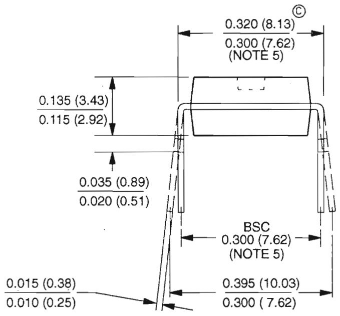
Package outlines

SOT38Z/0406C 16-Pin (300 mils wide) Plastic Dual In-Line (N) Package



NOTES

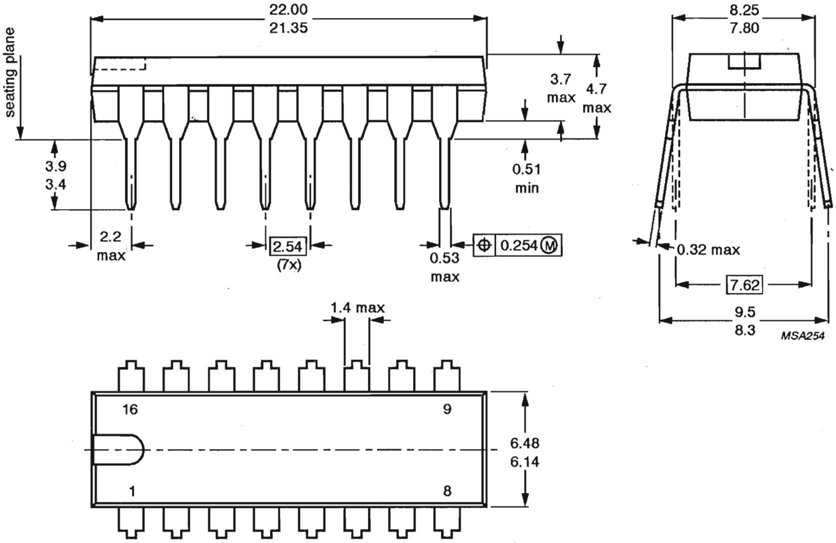
1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AA for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 16 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. “T”, “D”, and “E” are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #16 when viewed from the top.



853–0406C 02880

Package outlines

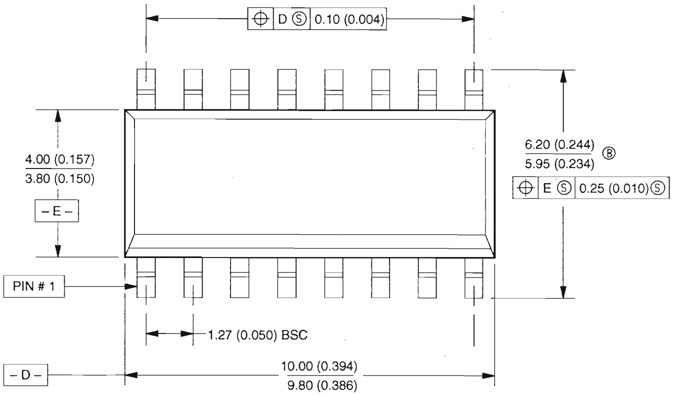
SOT38-1 16-Pin (300mil) Plastic Dual In-Line Package

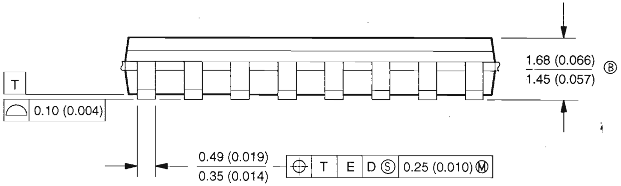


Dimensions in mm.

Package outlines

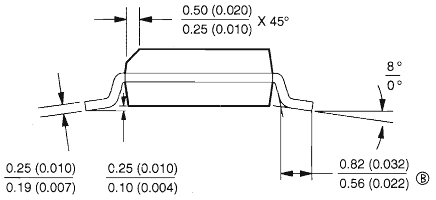
0005D 16-Pin (157 mils wide) Plastic SO (Small Outline) Dual In-Line (D) Package





NOTES

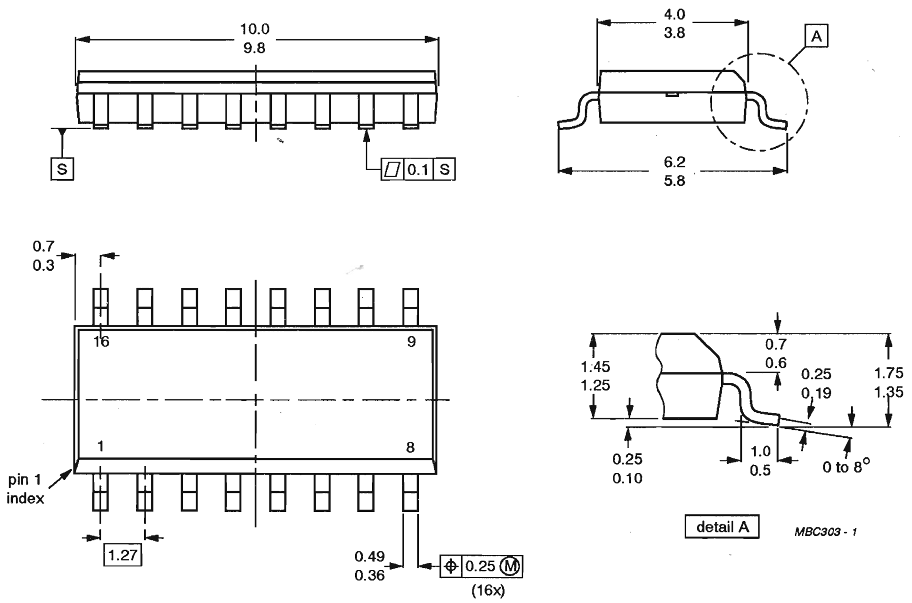
1. Package dimensions conform to JEDEC Specification MS-012-AC for standard Small Outline (SO) package, 16 leads, 3.75mm (0.150") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "D" and "E" are reference datums on the molded body and do not include mold flash/protrusions. Mold flash/protrusions at "D" shall not exceed 0.15mm (0.006") per side. Inter-lead flash/protrusions at "E" shall not exceed 0.25mm (0.010") per side.
5. The lead width above the seating plane shall not exceed a maximum value of 0.61mm (0.024").
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #16 when viewed from top.
7. Signetics ordering code for a product packages in a plastic Small Outline (SO) package is the suffix D after the product number.



853–0005D 04697

Package outlines

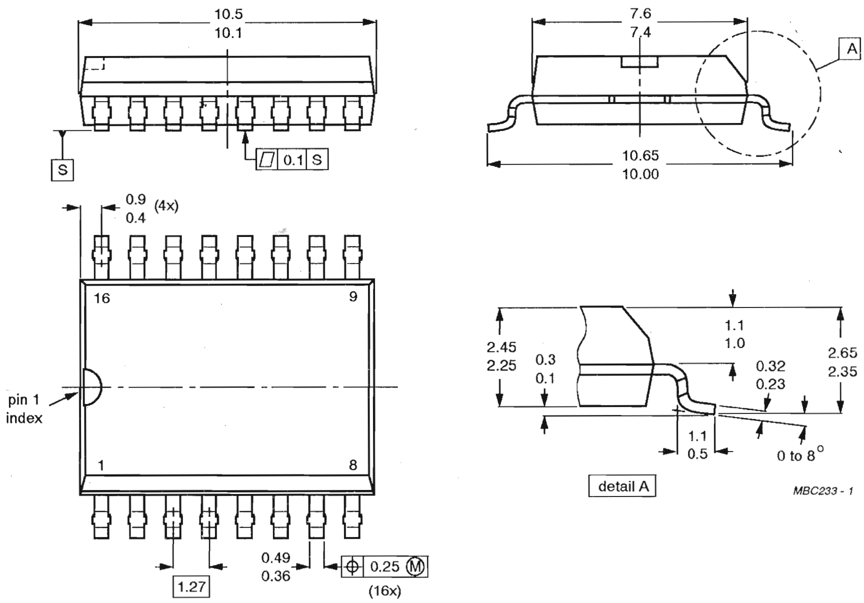
SOT109-1 16-Pin (3.9mm) Plastic SO (Small Outline) Package



Dimensions in mm.

Package outlines

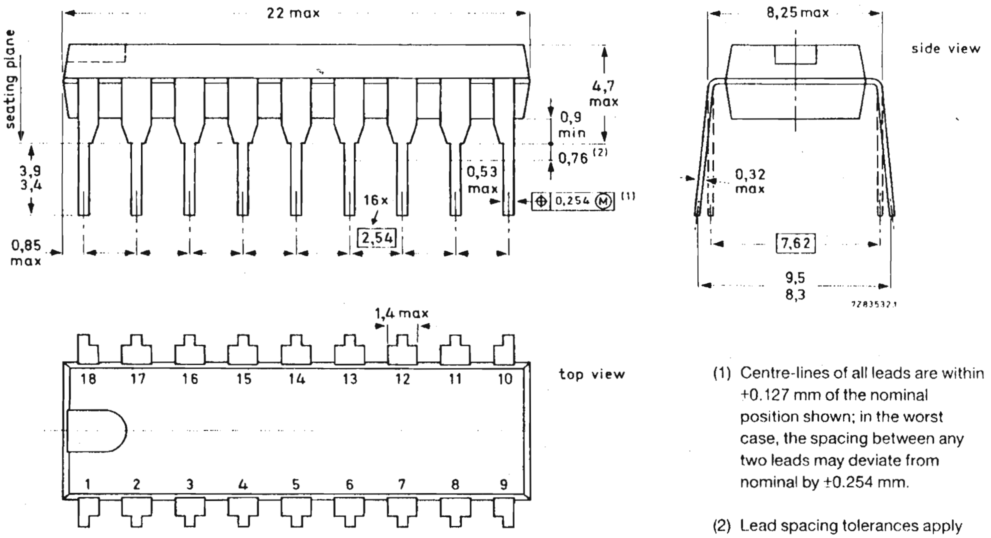
SOT162-1 16-Pin Plastic SO (Small Outline) Package; Large Body



Dimensions in mm.

Package outlines

SOT102 18-pin Plastic Dual In-Line (N/P) Package With Internal Heat Spreader



(1) Centre-lines of all leads are within ±0.127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0.254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

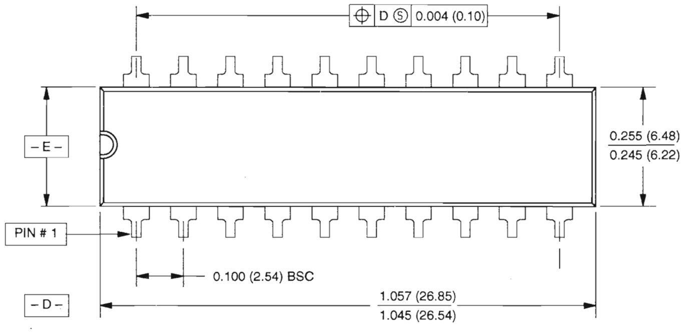
(3) Dimensions in mm.

SOT 102

7Z83532.1

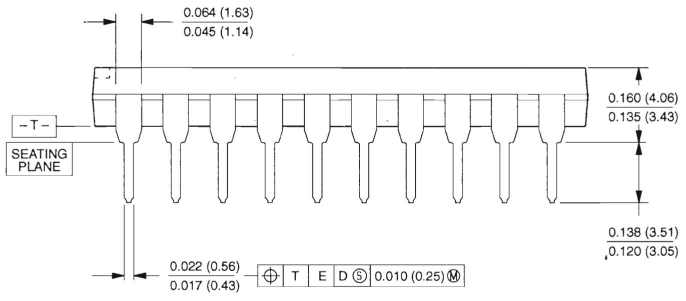
Package outlines

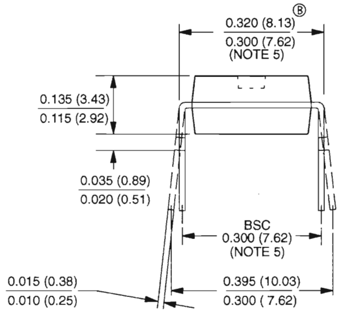
0408B 20-Pin (300 mils wide) Plastic Dual In-Line (N) Package



NOTES

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AE for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 20 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. “T”, “D”, and “E” are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #20 when viewed from the top.

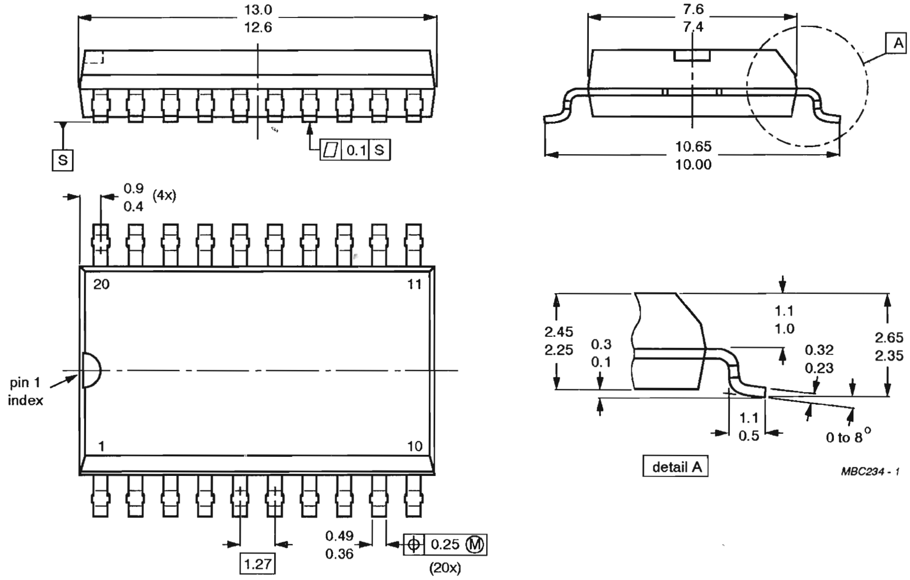




853–0408B 02880

Package outlines

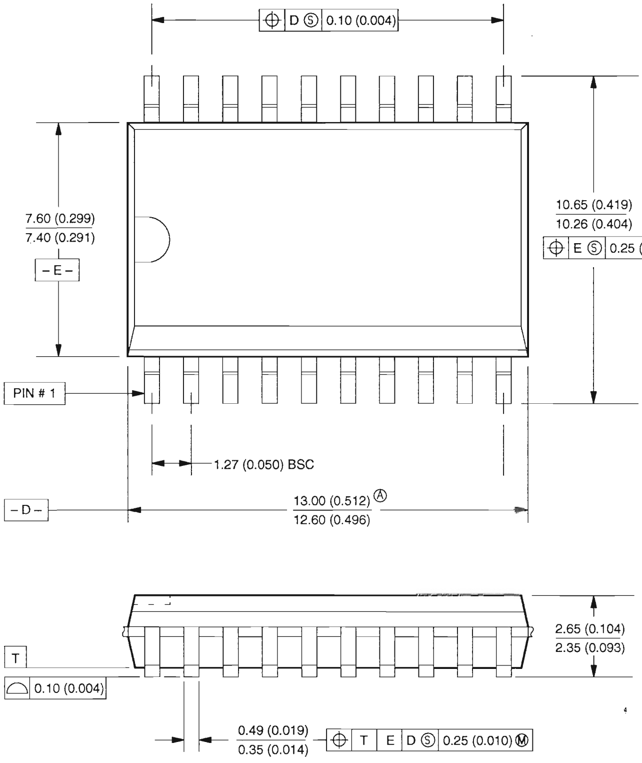
SOT163-1 20-Pin (Large Body) Plastic SO (Small Outline) Package



Dimensions in mm.

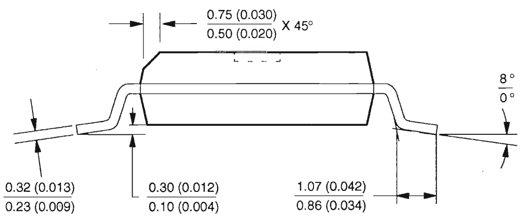
Package outlines

0172D 20-Pin (300 mils wide) Plastic SOL (Small Outline Large) Dual In-Line (D) Package



NOTES

1. Package dimensions conform to JEDEC Specification MS-013-AC for standard Small Outline (SO) package, 20 leads, 7.50mm (0.300") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "D" and "E" are reference datums on the molded body and do not include mold flash/protrusions. Mold flash/protrusions at "D" shall not exceed 0.15mm (0.006") per side. Inter-lead flash/protrusions at "E" shall not exceed 0.25mm (0.010") per side.
5. The lead width above the seating plane shall not exceed a maximum value of 0.61mm (0.024").
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #20 when viewed from top.
7. Signetics ordering code for a product packaged in a plastic Small Outline (SO) package is the suffix D after the product number.



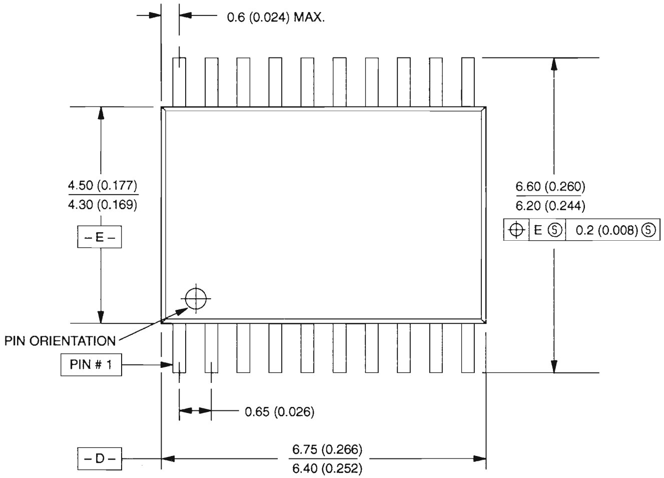
853–0172D 04697

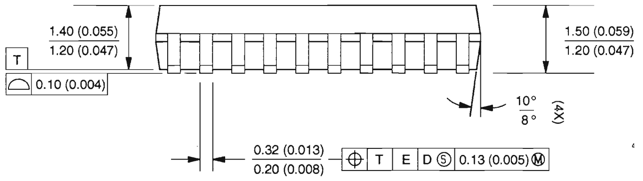
Package outlines

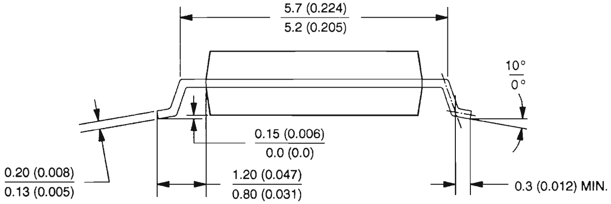
1563– 20-Pin Plastic (170 mils wide) SSOP (Shrink Small Outline Package)

NOTES

1. Package dimensions conform to Philips Envelope Specification SOT-266/EIAJ TYPE I for Shrink Small Outline Package (SSOP), 20 leads, 4.3mm (0.170 inch) body width (Issue April 1990).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. “T”, “D”, and “E” are reference datums on the molded body.
4. Pin numbers start with Pin #1 and continue counterclockwise to Pin #20 when viewed from top.
5. Signetics ordering code for a product packaged in a plastic Shrink Small Outline Package (SSOP) is the suffix D after the product number.



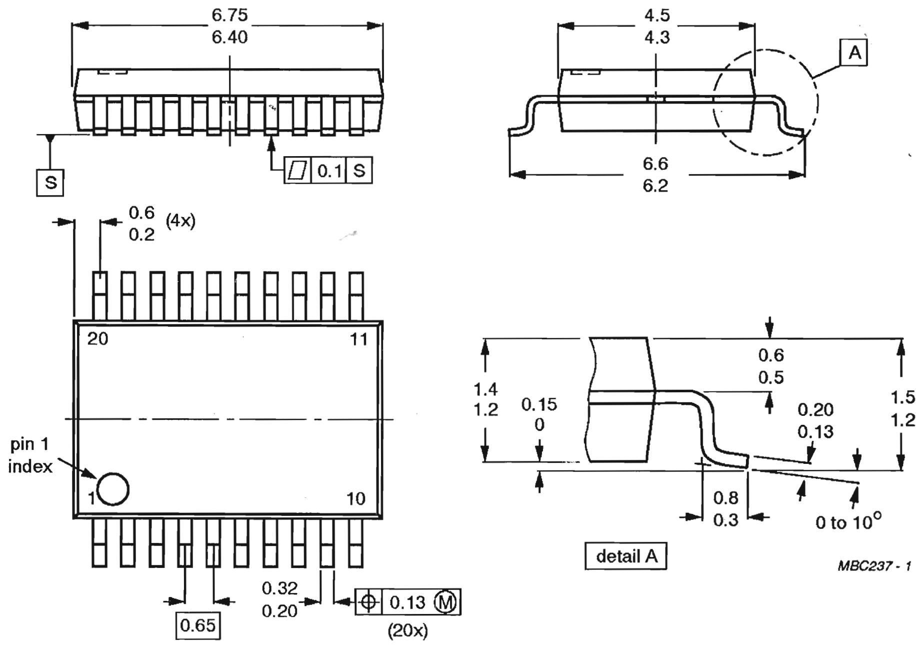




853–1563 03360

Package outlines

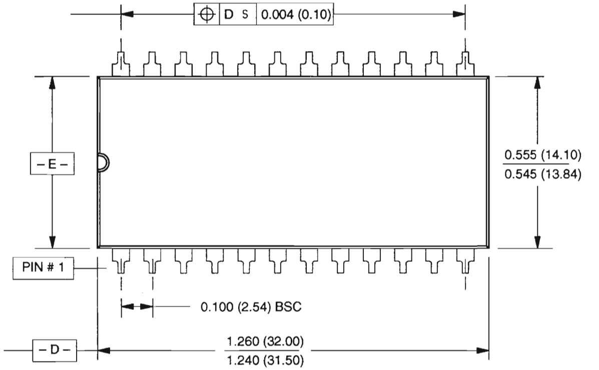
SOT266-1 **20-Pin (4.4mm) Plastic SSOP (Shrink Small Outline Package**



Dimensions in mm.

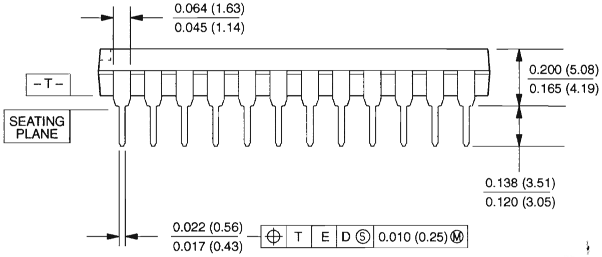
Package outlines

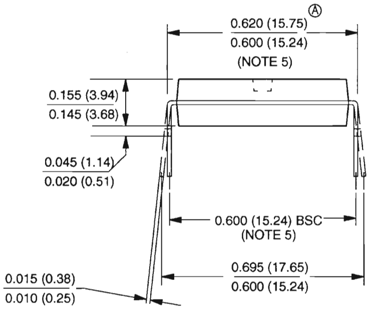
0412A 24-Pin (600 mils wide) Plastic Dual In-Line (N) Package



NOTES:

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-011-AA for standard Dual In-Line (DIP) package 0.600 inch row spacing (plastic) 24 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #24 when viewed from the top.

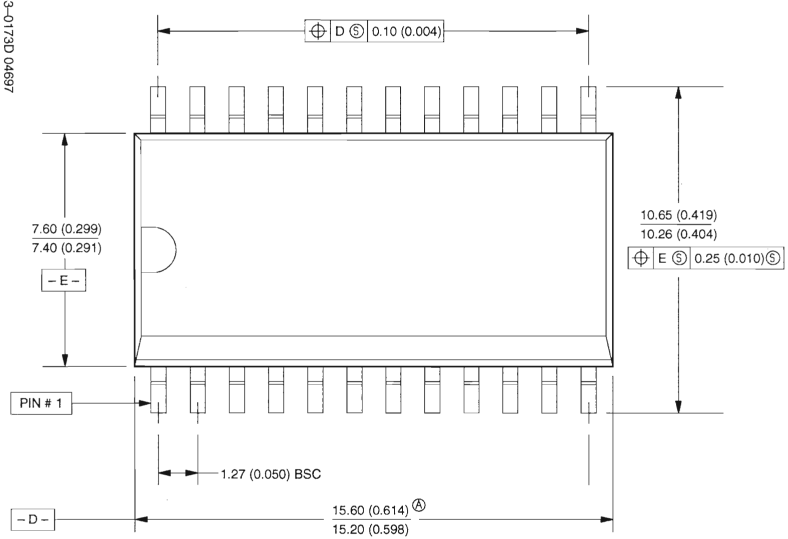




853–0412A 02880

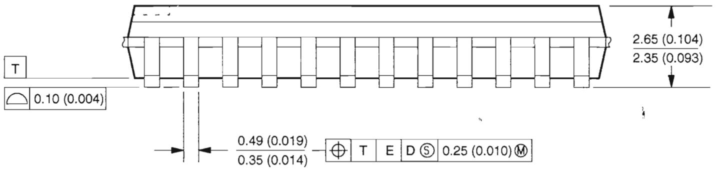
Package outlines

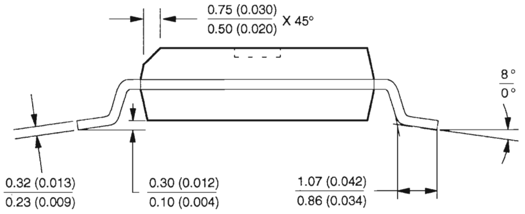
0173D 24-Pin (300 mils wide) Plastic SOL (Small Outline Large) Dual In-Line (D) Package



NOTES

1. Package dimensions conform to JEDEC Specification MS-013-AD for standard Small Outline (SO) package, 24 leads, 7.50mm (0.300”) body width (Issue A. June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. “D” and “E” are reference datums on the molded body and do not include mold flash/protrusions. Mold flash/protrusions at “D” shall not exceed 0.15mm (0.006”) per side. Inter-lead flash/protrusions at “E” shall not exceed 0.25mm (0.010”) per side.
5. The lead width above the seating plane shall not exceed a maximum value of 0.61mm (0.024”).
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #24 when viewed from top.
7. Signetics ordering code for a product packaged in a plastic Small Outline (SO) package is the suffix D after the product number.

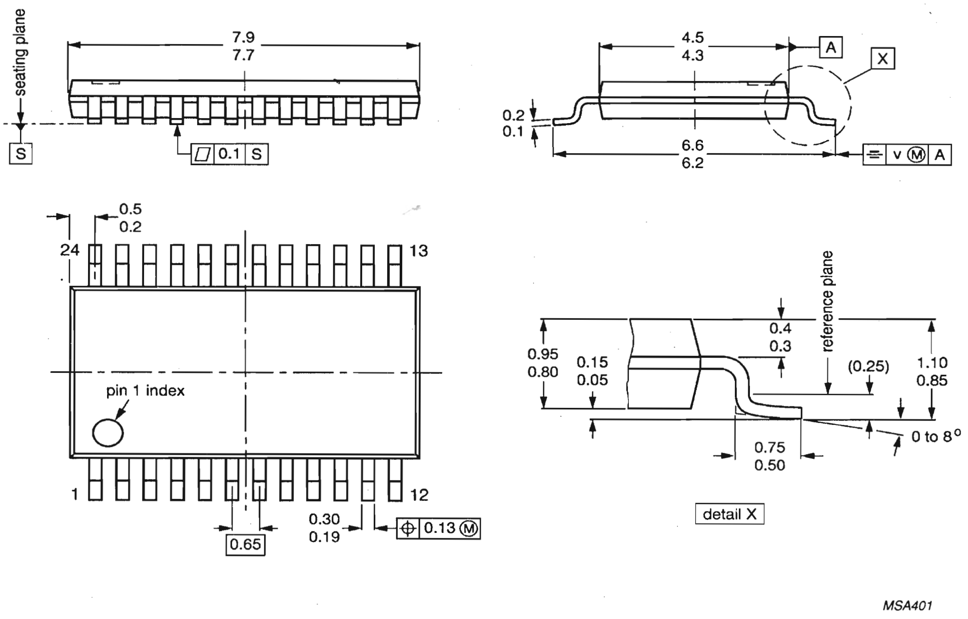




853–0173D 04697

Package outlines

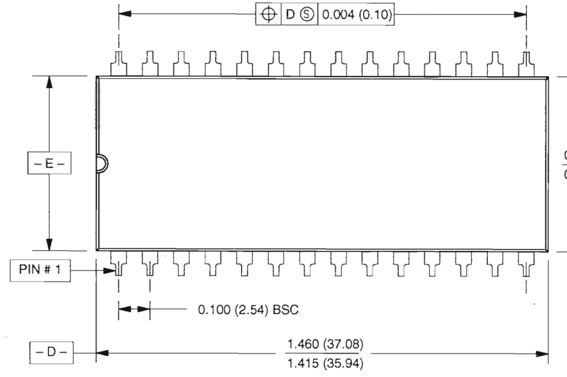
SOT355-1 24-Pin (Medium Body) Plastic TSSOP (Thin Shrink Small Outline) Package



Dimensions in mm.

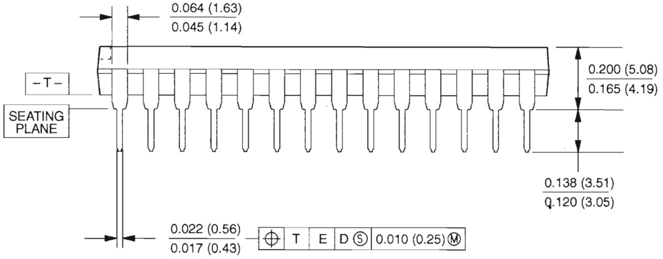
Package outlines

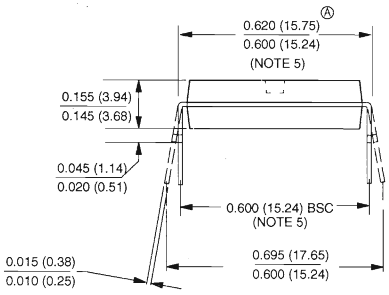
0413B 28-pin (600 mils wide) Plastic Dual In-Line (N) Package



NOTES:

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-011-AB for standard Dual In-Line (DIP) package 0.600 inch row spacing (plastic) 28 leads (Issue B, 7/84).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. “T”, “D”, and “E” are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #28 when viewed from the top.

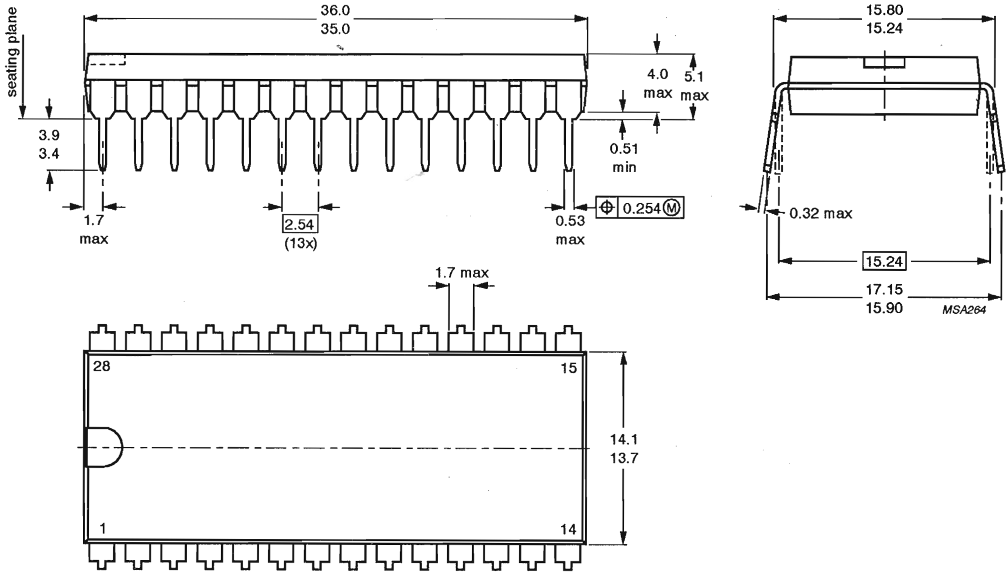




853-0413B 01988

Package outlines

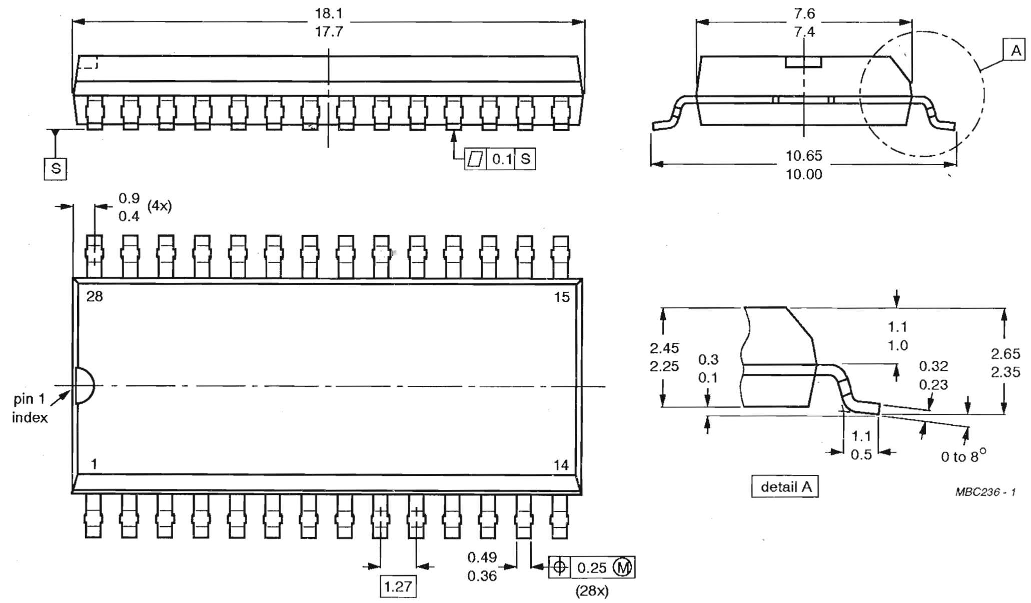
SOT117-1 28-Pin (600 mil) Plastic Dual In-Line Package With Internal Heat Spreader



Dimensions in mm.

Package outlines

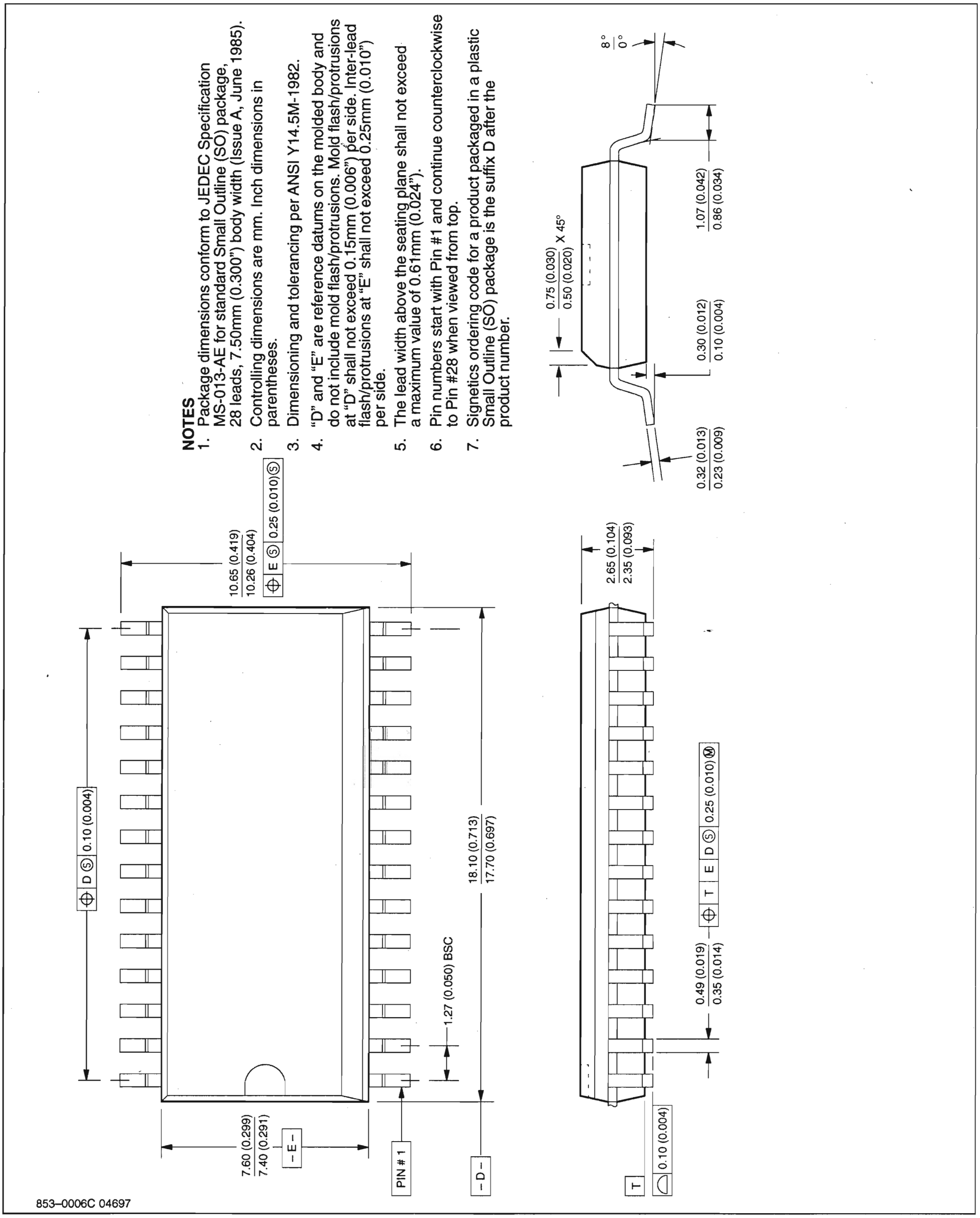
SOT136-1 28-Pin (7.5mm) Plastic Small Outline Package



Dimensions in mm.

Package outlines

0006C 28-Pin (300 mils wide) Plastic SOL (Small Outline Large) Dual In-Line (D) Package

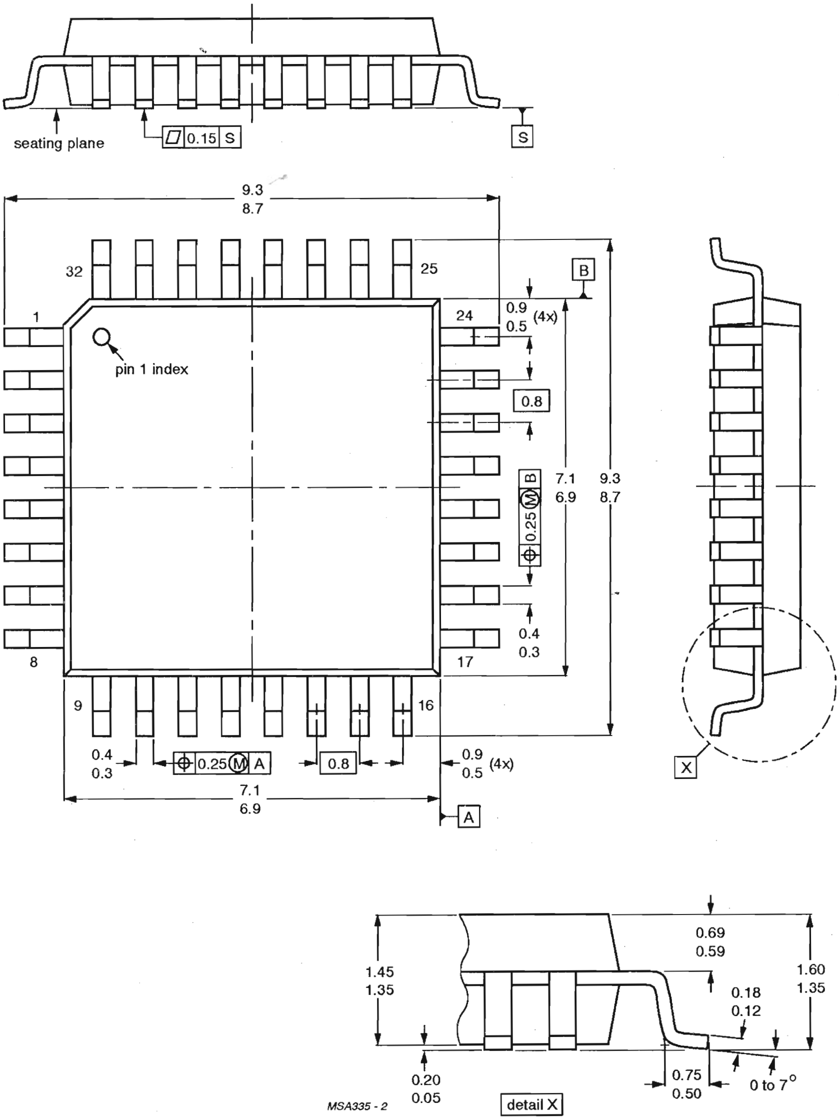


NOTES

1. Package dimensions conform to JEDEC Specification MS-013-AE for standard Small Outline (SO) package, 28 leads, 7.50mm (0.300") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "D" and "E" are reference datums on the molded body and do not include mold flash/protrusions. Mold flash/protrusions at "D" shall not exceed 0.15mm (0.006") per side. Inter-lead flash/protrusions at "E" shall not exceed 0.25mm (0.010") per side.
5. The lead width above the seating plane shall not exceed a maximum value of 0.61mm (0.024").
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #28 when viewed from top.
7. Signetics ordering code for a product packaged in a plastic Small Outline (SO) package is the suffix D after the product number.

Package outlines

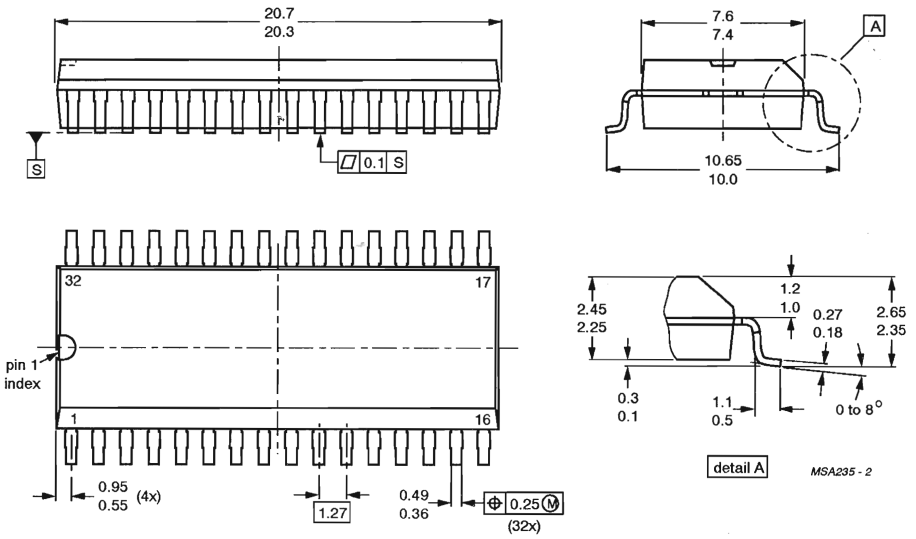
SOT358-1 32-Pin (7x7x1.4 mm) Plastic TQFP (Thin Quad Flat Package)



Dimensions in mm.

Package outlines

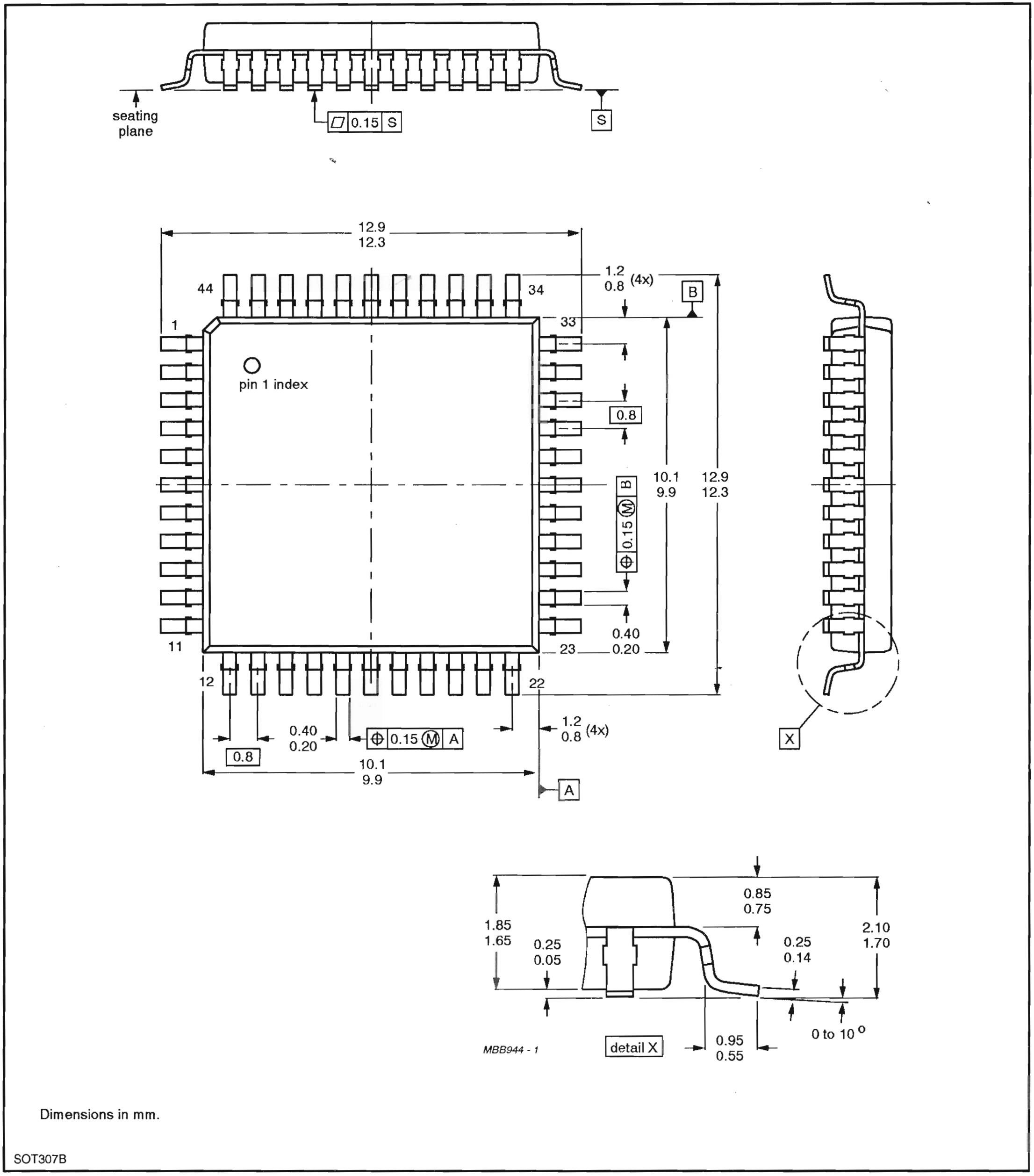
SOT287-1 32-Pin (7.5mm) Plastic SO (Small Outline) Package



Dimensions in mm.

Package outlines

SOT307B 44-Pin Plastic QFP (Quad Flat Pack)



Dimensions in mm.

SOT307B

Package outlines

1706B 48-Pin Plastic Thin Quad Flat Pack (B) Package

NOTES:

1. Package dimensions conform to JEDEC registration MO-136-BE-1992. (This is equivalent to Philips Euro. SQFP48 outline, SOT313-1.)
2. Controlling dimensions: millimeters. Dimensions in inches are shown in parentheses.
3. Dimension and tolerancing per ANSI Y14.5M-1982.

△4 Datum plane "H" is located at the mold parting line and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.

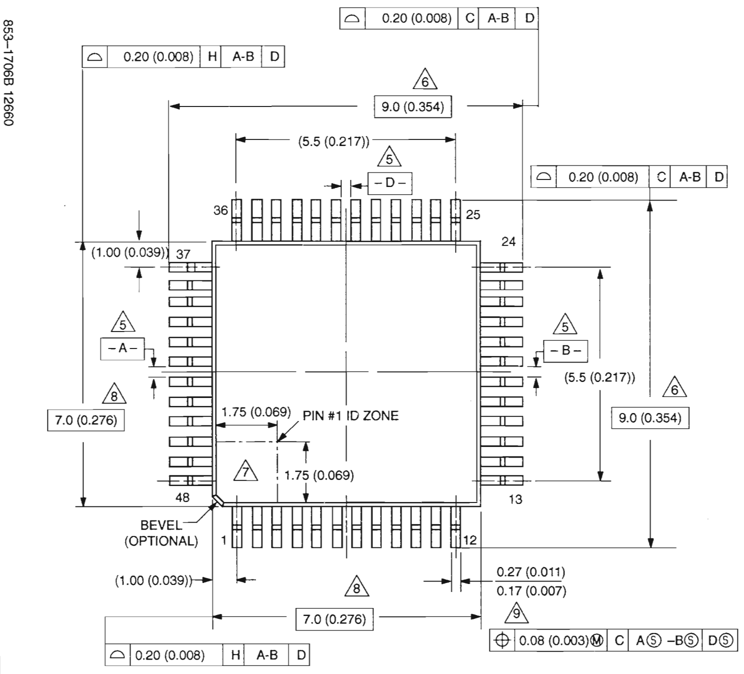
△5 Datums "A-B" and "D" to be determined at datum plane "H".

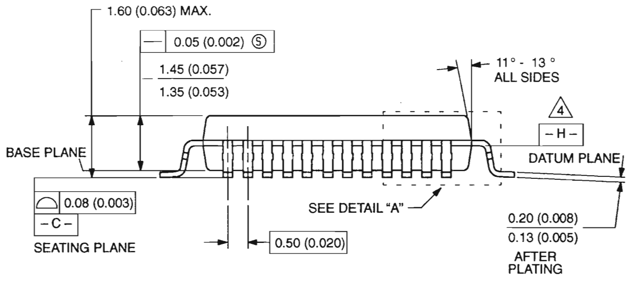
△6 To be determined at seating plane "C".

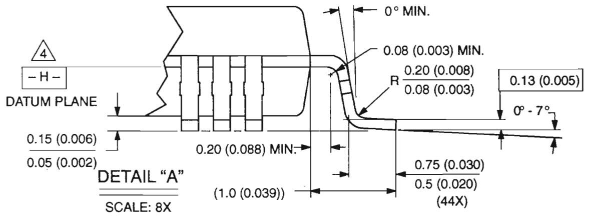
△7 Details of Pin 1 identifier are optional but must be located within the zone indicated.

△8 Package body dimensions do not include mold protrusion. Allowable protrusion is 0.25mm per side, but it includes mold mismatch.

△9 Lead width does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm / 0.003" total in excess of this dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.



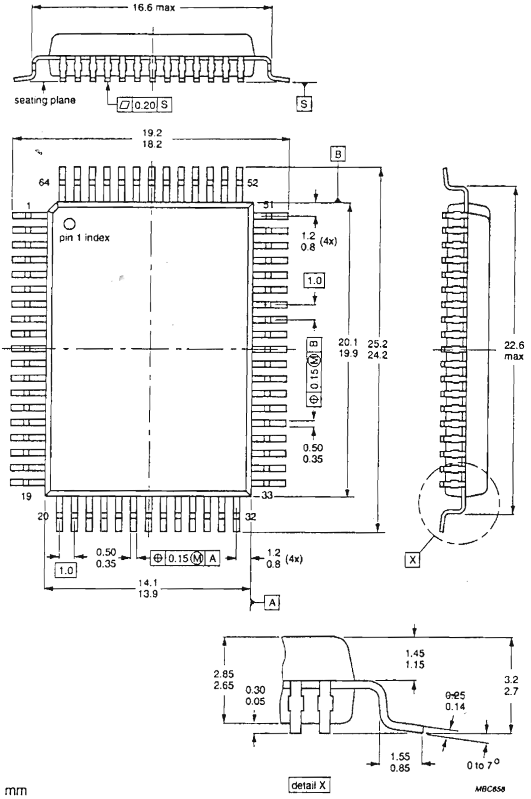




853–1706B 12660

Package outlines

SOT208A 64-Lead Plastic QFP (Quad Flat Package)



Dimensions in mm

Data handbook system

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